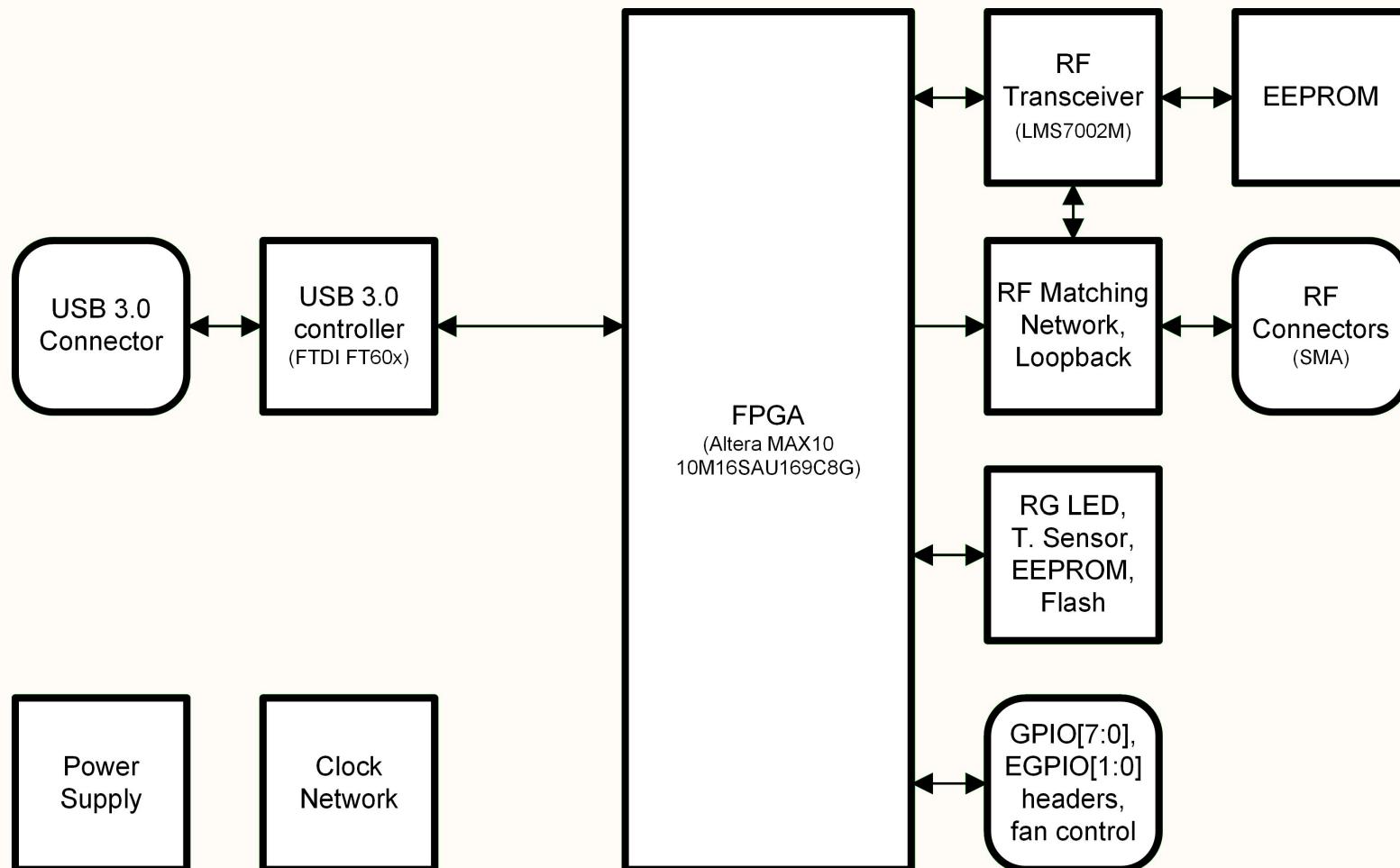


## Block diagram



Project name: **LimeSDR\_Mini\_Iv0.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.0**

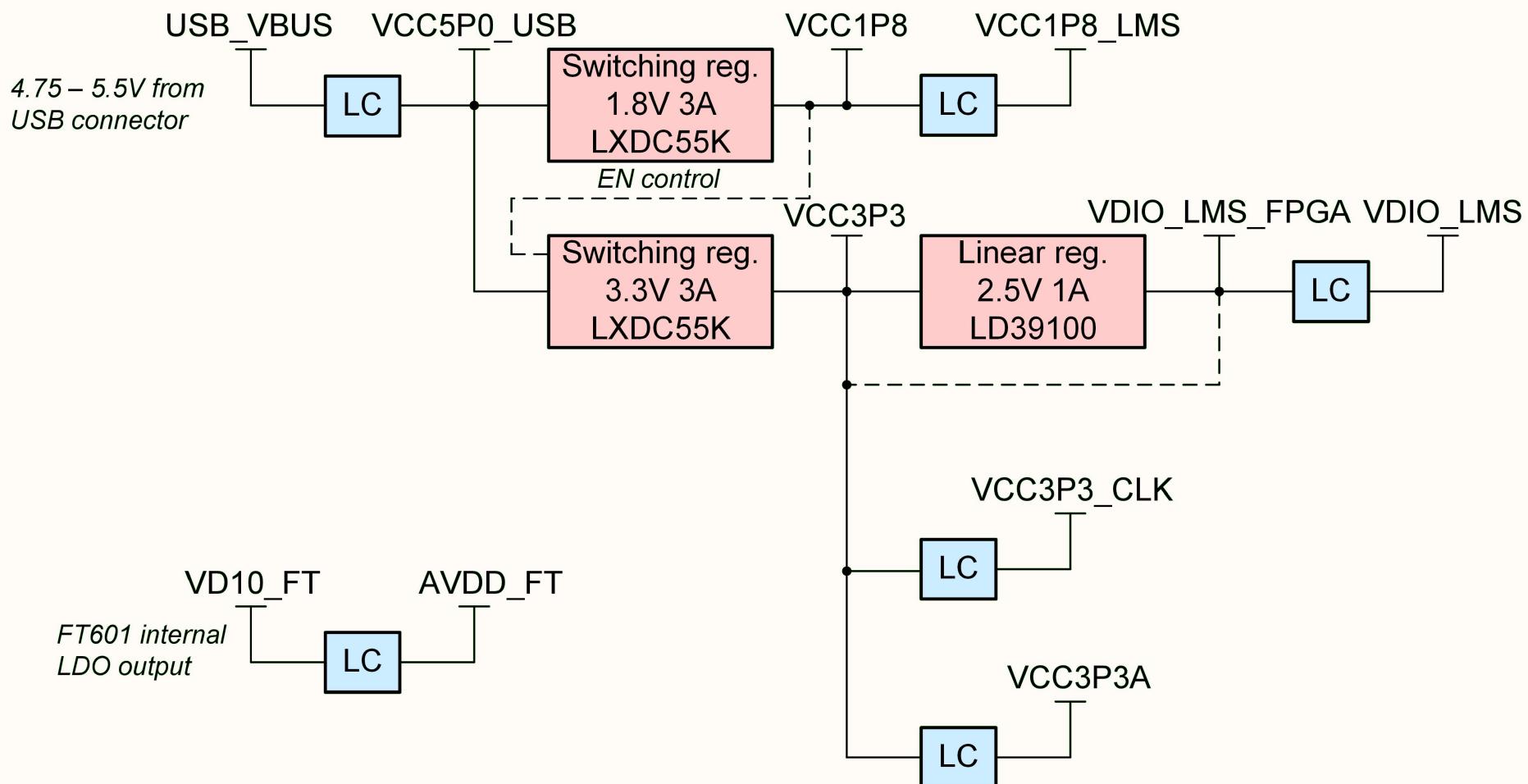
Date: **2017-09-22** Time: **12:16:54** Sheet **1** of **9**

File: **01\_BlockDiagram.SchDoc**

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Surrey  
United Kingdom



## Power diagram



Project name: **LimeSDR\_Mini\_Iv0.PrjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.0**

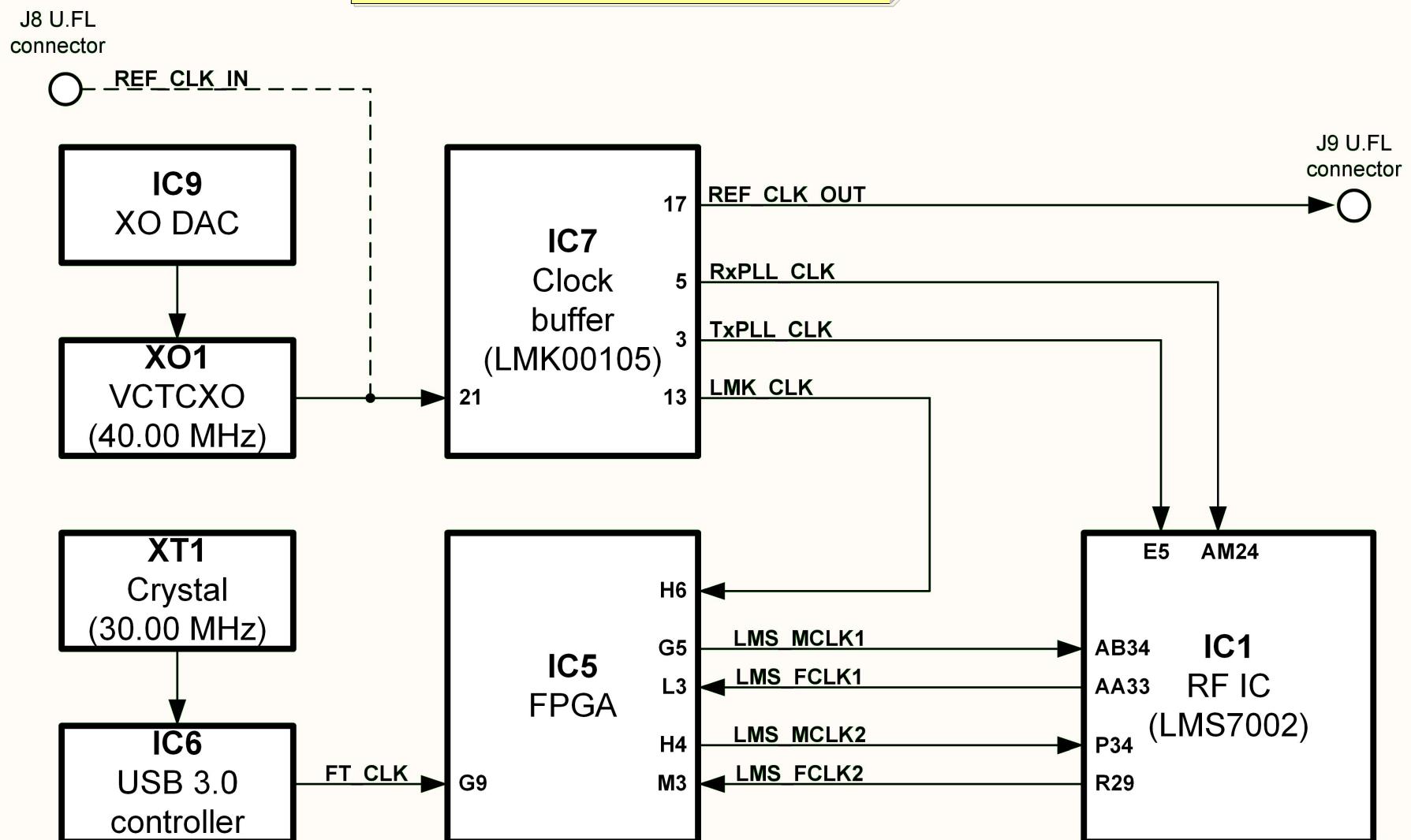
Date: **2017-09-22** Time: **12:16:56** Sheet **2** of **9**

File: **02\_PowerDiagram.SchDoc**

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United Kingdom



## Clock diagram

Project name: *LimeSDR\_Mini\_Iv0.PrbPcb*Title: *Clock diagram*Size: **A4** Revision: **v1.0**

Date: 2017-09-22 Time: 12:17:00 Sheet 3 of 9

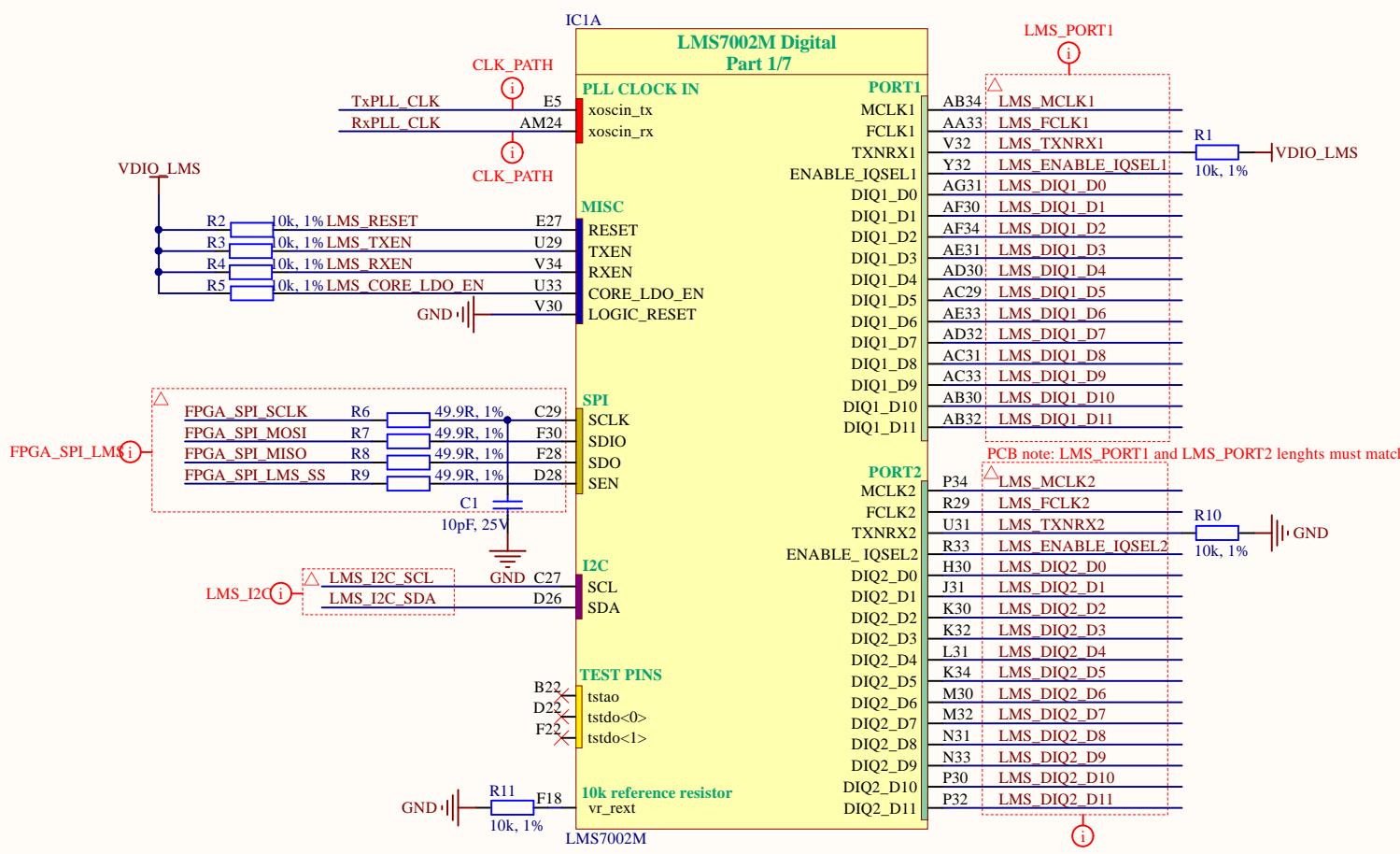
File: 03\_ClockDiagram.SchDoc

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NF elements on sheet: -  
Number of NF elements on sheet: 0

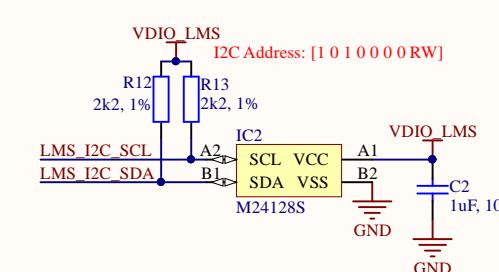
## LMS7002M misc



## Baseband external IO

Local fiducial LMS Top  
FL1

## LMS EEPROM



Project name: **LimeSDR\_Mini\_1v0.PrbPcb**

Title: **LMS7002M misc**

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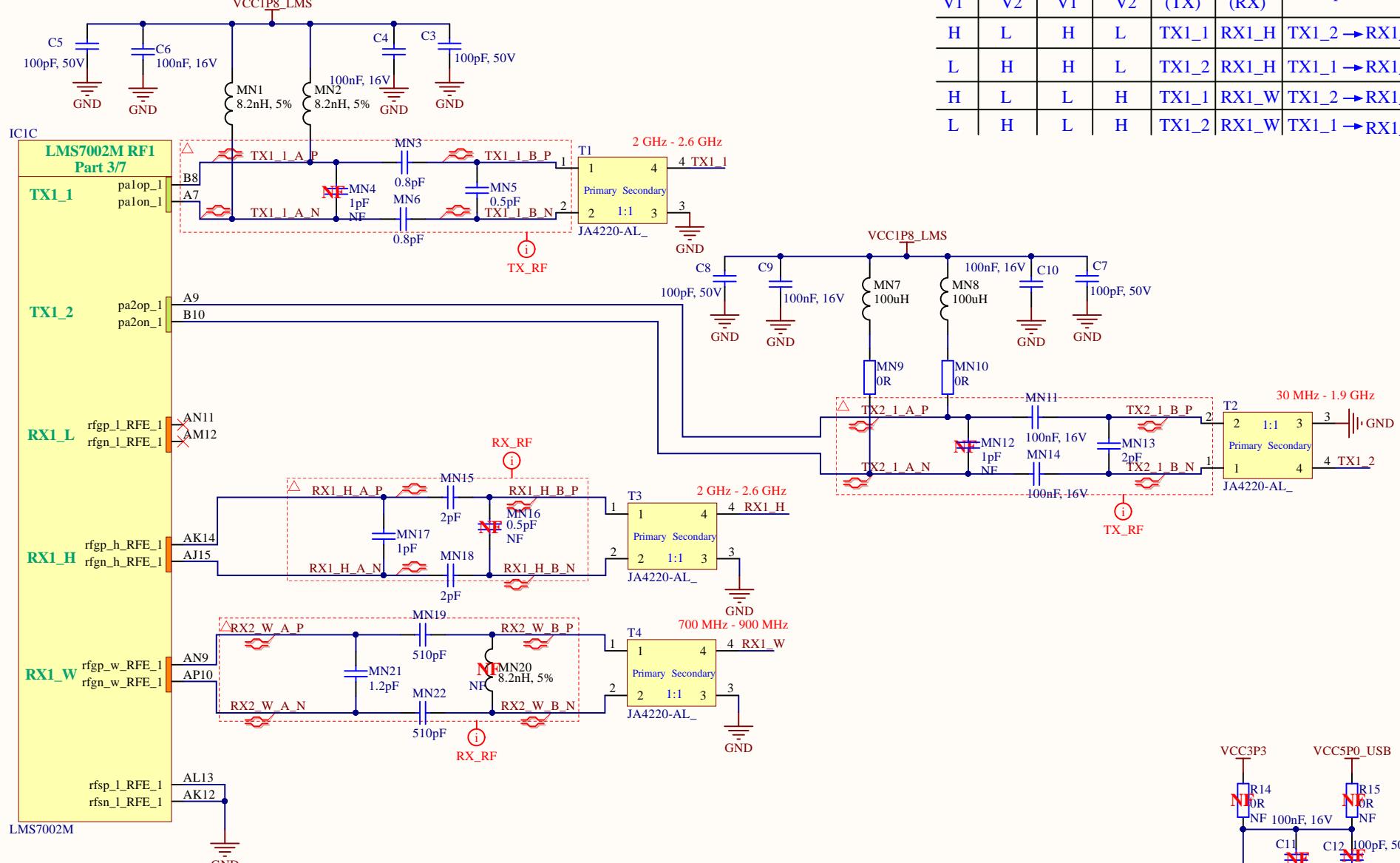
Size: **A3** Revision: **v1.0**

Date: **2017-09-22** Time: **12:17:02** Sheet**4** of **9**

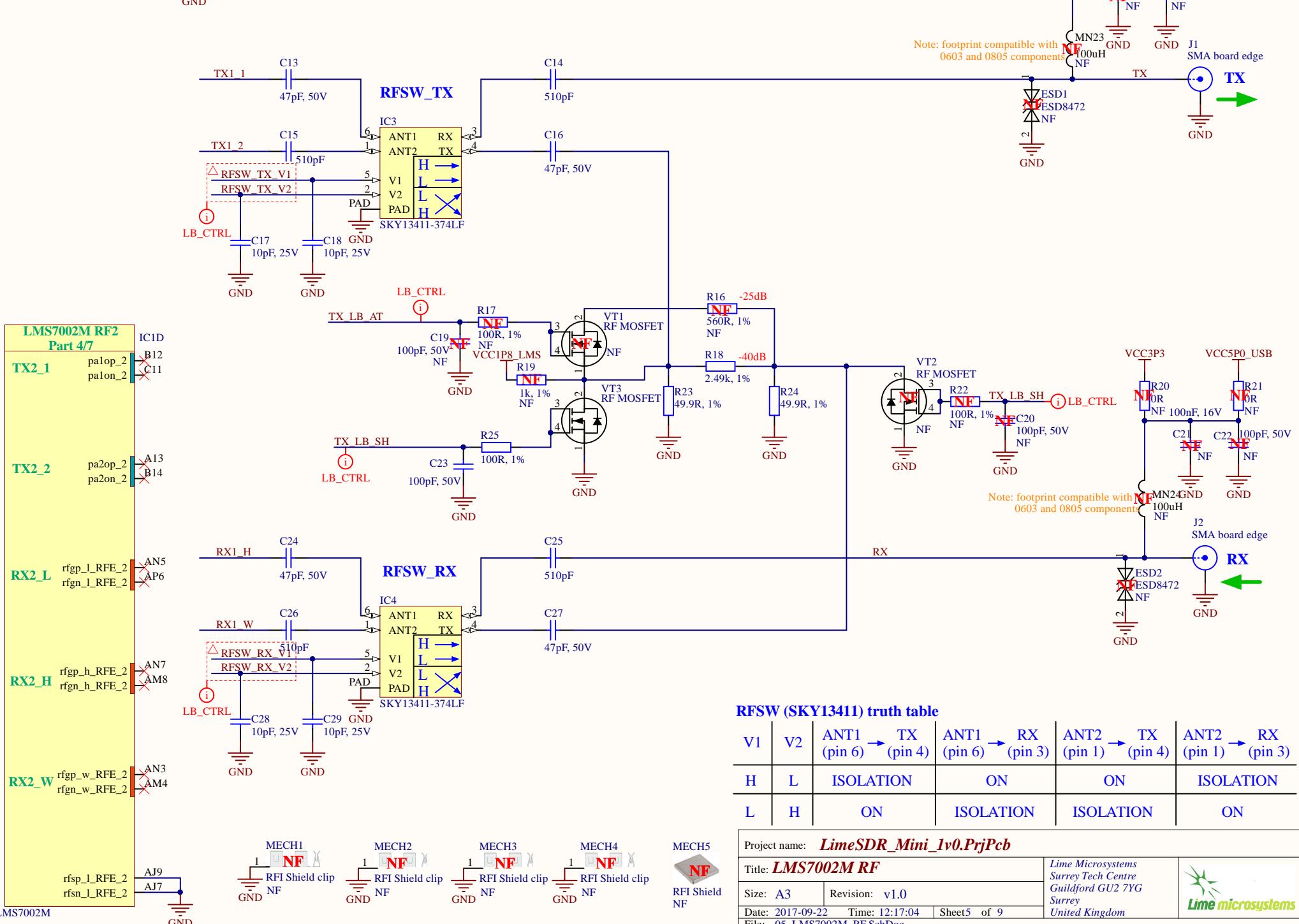
File: **04\_LMS7002M\_Misc.SchDoc**

# LMS7002M RF circuits

## LMS RF Channel 1

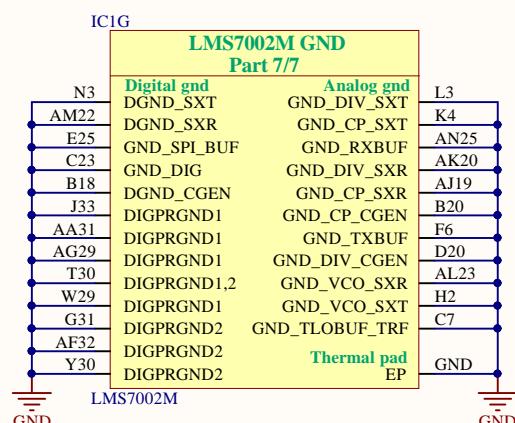
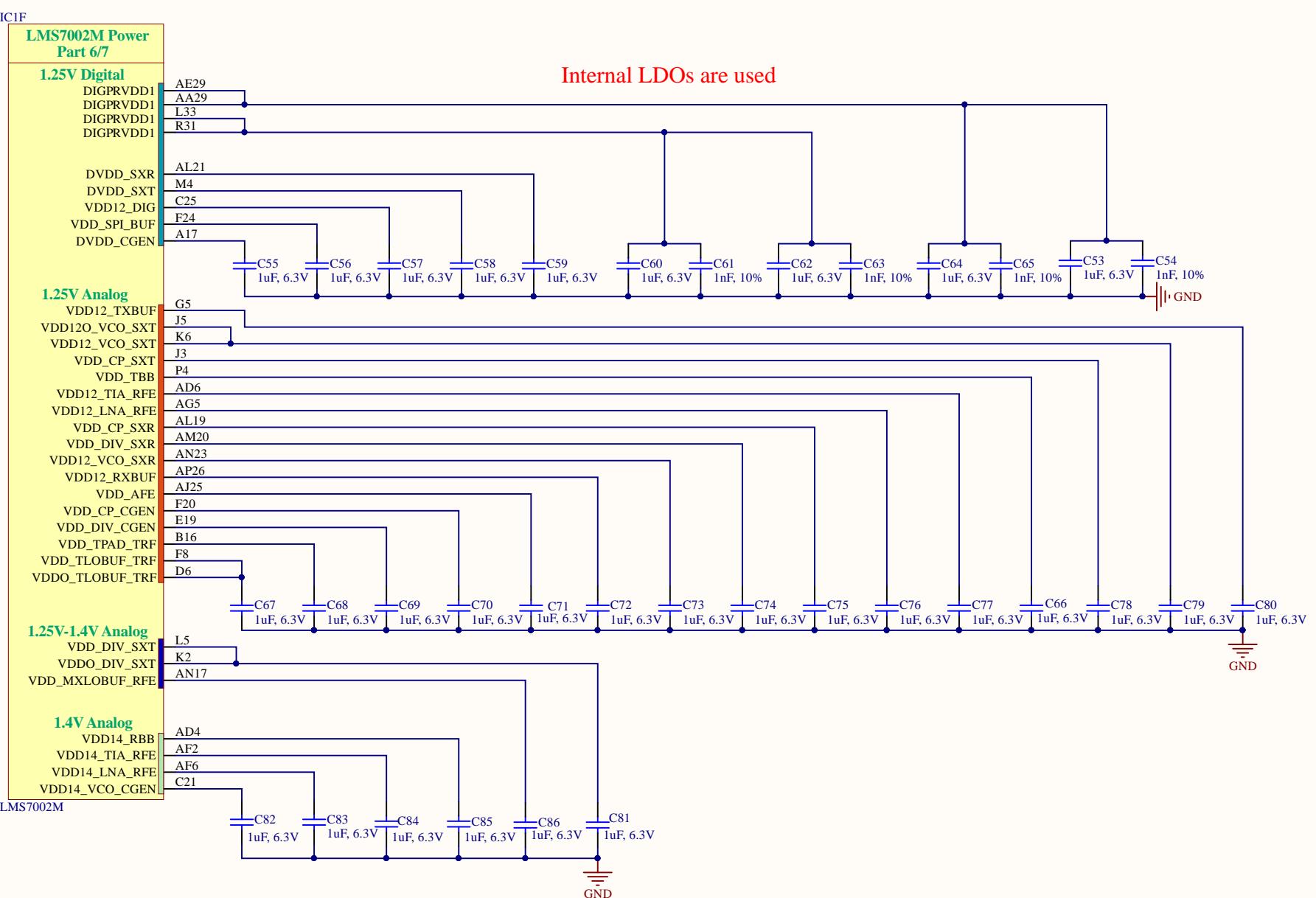
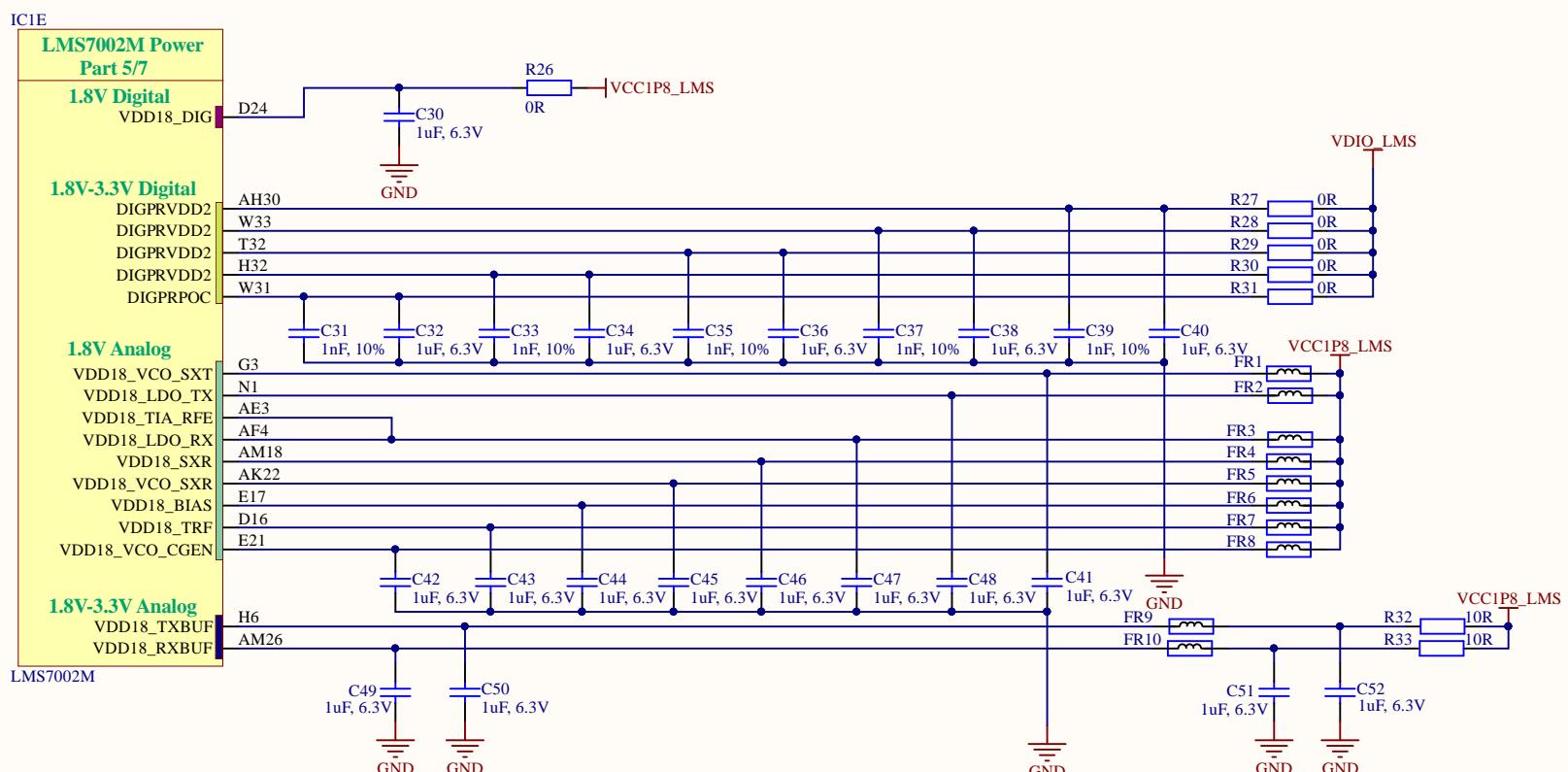


| RF truth table |    |         |    |         |         |
|----------------|----|---------|----|---------|---------|
| RFSW_TX        |    | RFSW_RX |    | J1 (TX) | J2 (RX) |
| V1             | V2 | V1      | V2 | (TX)    |         |
| H              | L  | H       | L  | TX1_1   | RX1_H   |
| L              | H  | H       | L  | TX1_2   | RX1_H   |
| H              | L  | L       | H  | TX1_1   | RX1_W   |
| L              | H  | L       | H  | TX1_2   | RX1_W   |
| Loopback       |    |         |    |         |         |
| TX1_2 → RX1_W  |    |         |    |         |         |
| TX1_1 → RX1_W  |    |         |    |         |         |
| TX1_1 → RX1_H  |    |         |    |         |         |
| TX1_2 → RX1_H  |    |         |    |         |         |



# LMS7002M power supply circuit

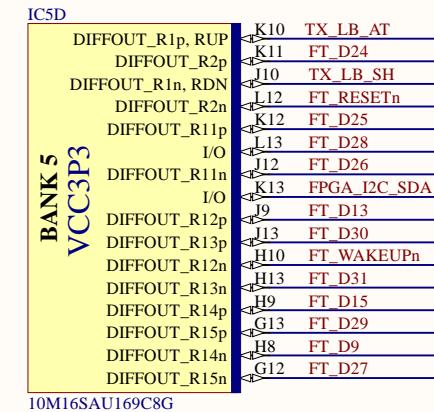
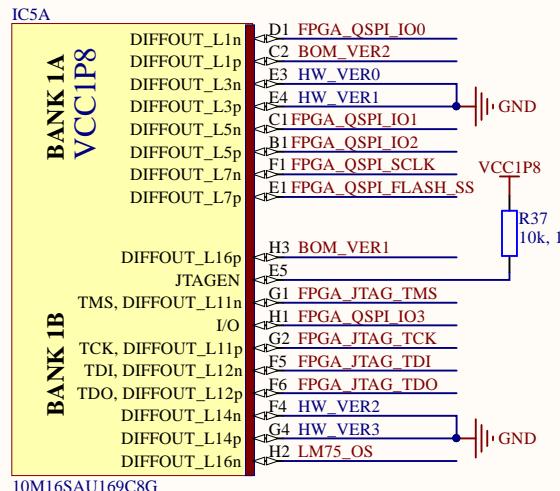
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Number of NF elements on sheet: 0



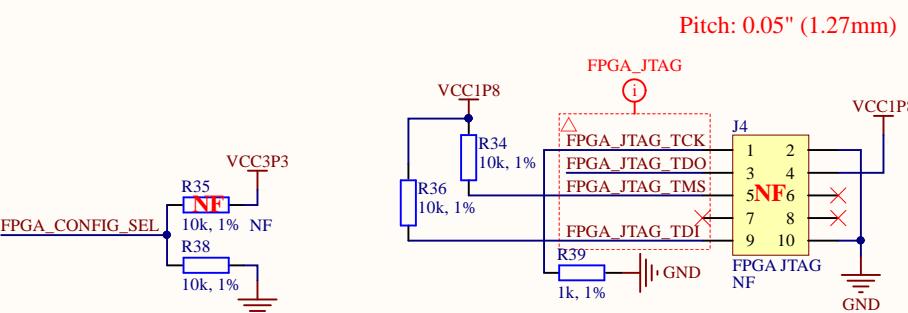
NF elements on sheet: R35, J3, J4, J5, J6, R41  
Number of NF elements on sheet: 6

FPGA

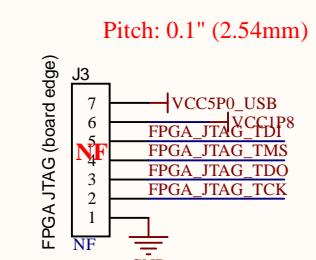
## FPGA Banks



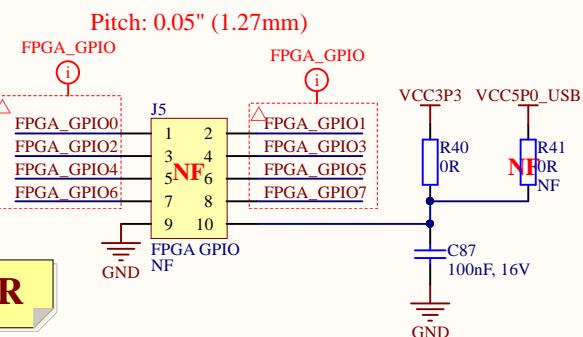
FPGA JTAG



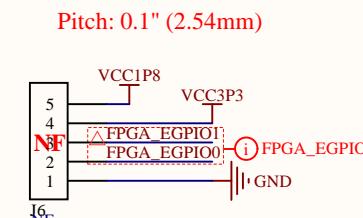
FPGA JTAG (edge)



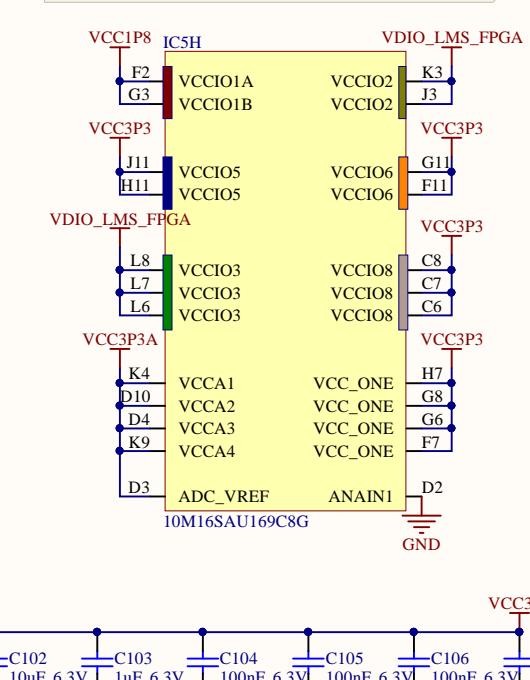
FPGA GPIO



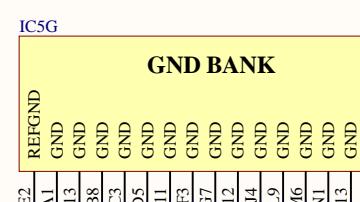
## FPGA GPIO (edge)



FPGA Power



GND BANK



Date: 2017-09-22 Time: 12:17:07 Sheet 1 of 9 United Kingdom  
File: 07\_FPGA.SchDoc

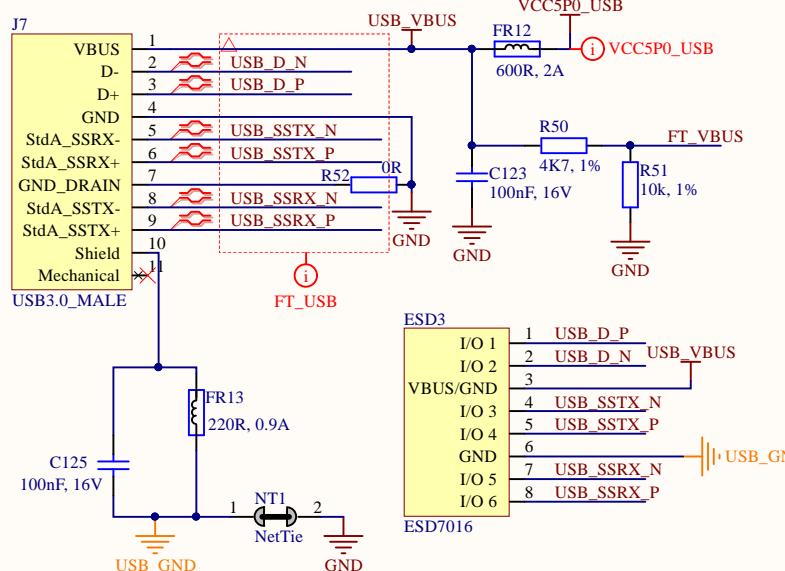
6



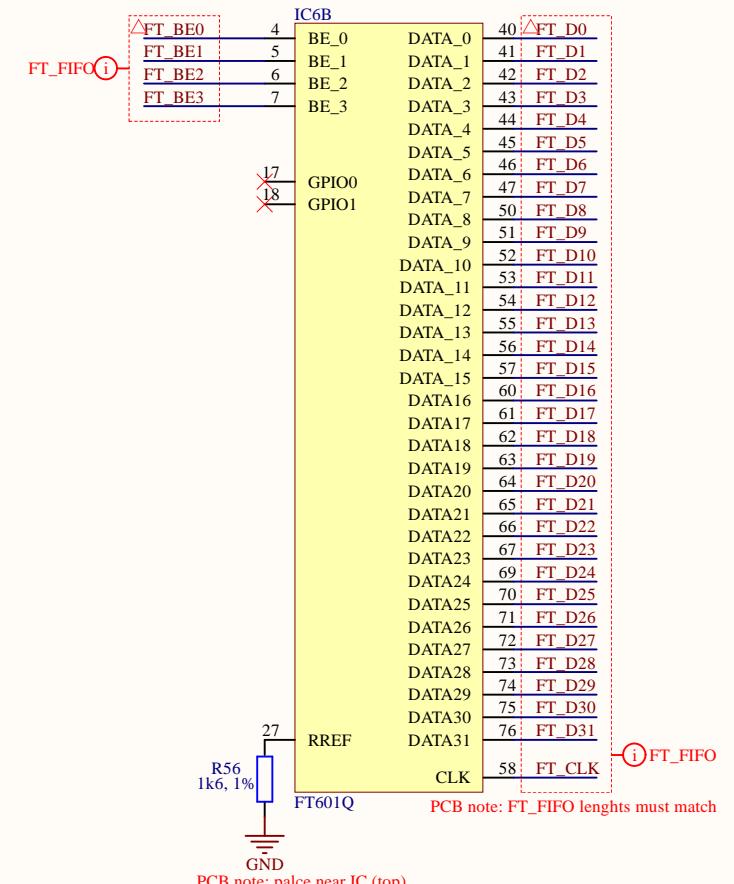
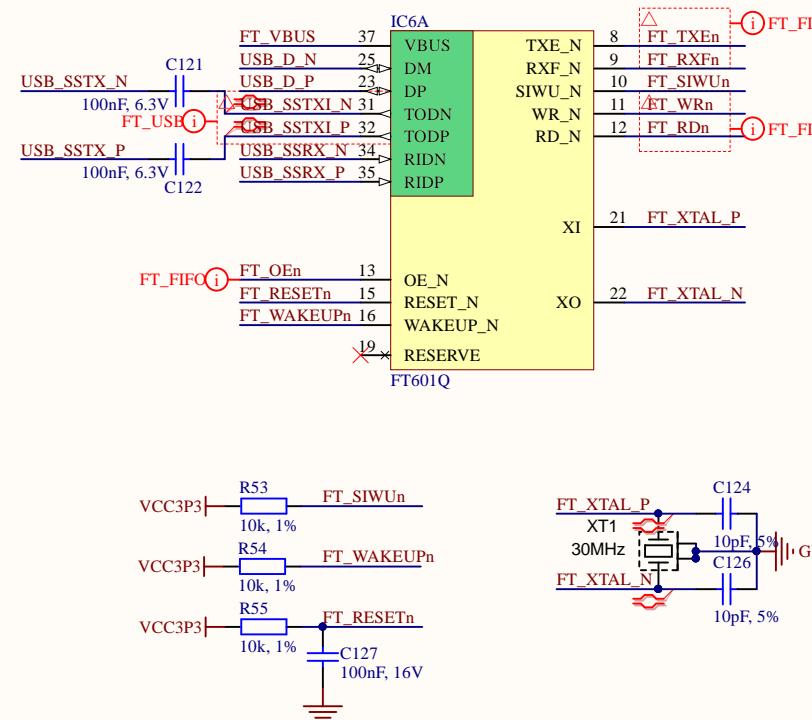
NF elements on sheet: MECH6, MECH7, MECH8, MECH9, MECH10  
Number of NF elements on sheet: 5

FTDI (USB3) core

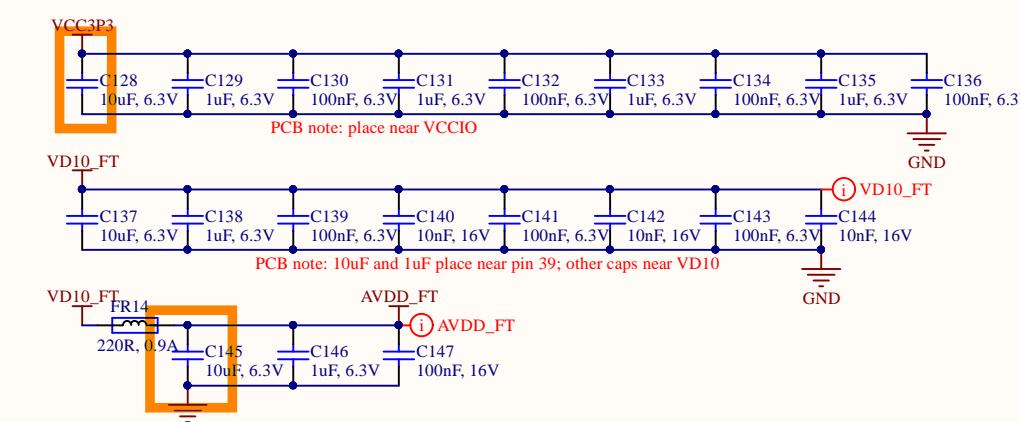
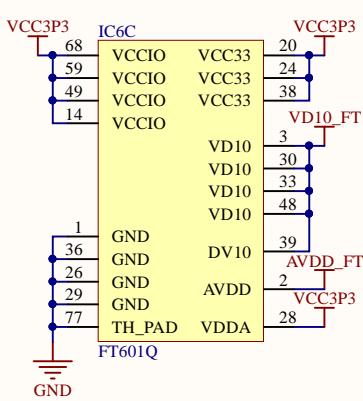
## USB3.0 plug and



## FTDI digital interfaces



FTDI Power



Project name: LimeSDR Mini Lv0 PriPch

Title: *USB3.0 device*

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Guildford GU2 7YG  
Surrey  
United Kingdom*



GND  
Schematic note: marked 10uF caps not crucial and can be removed to reduce BOM price

