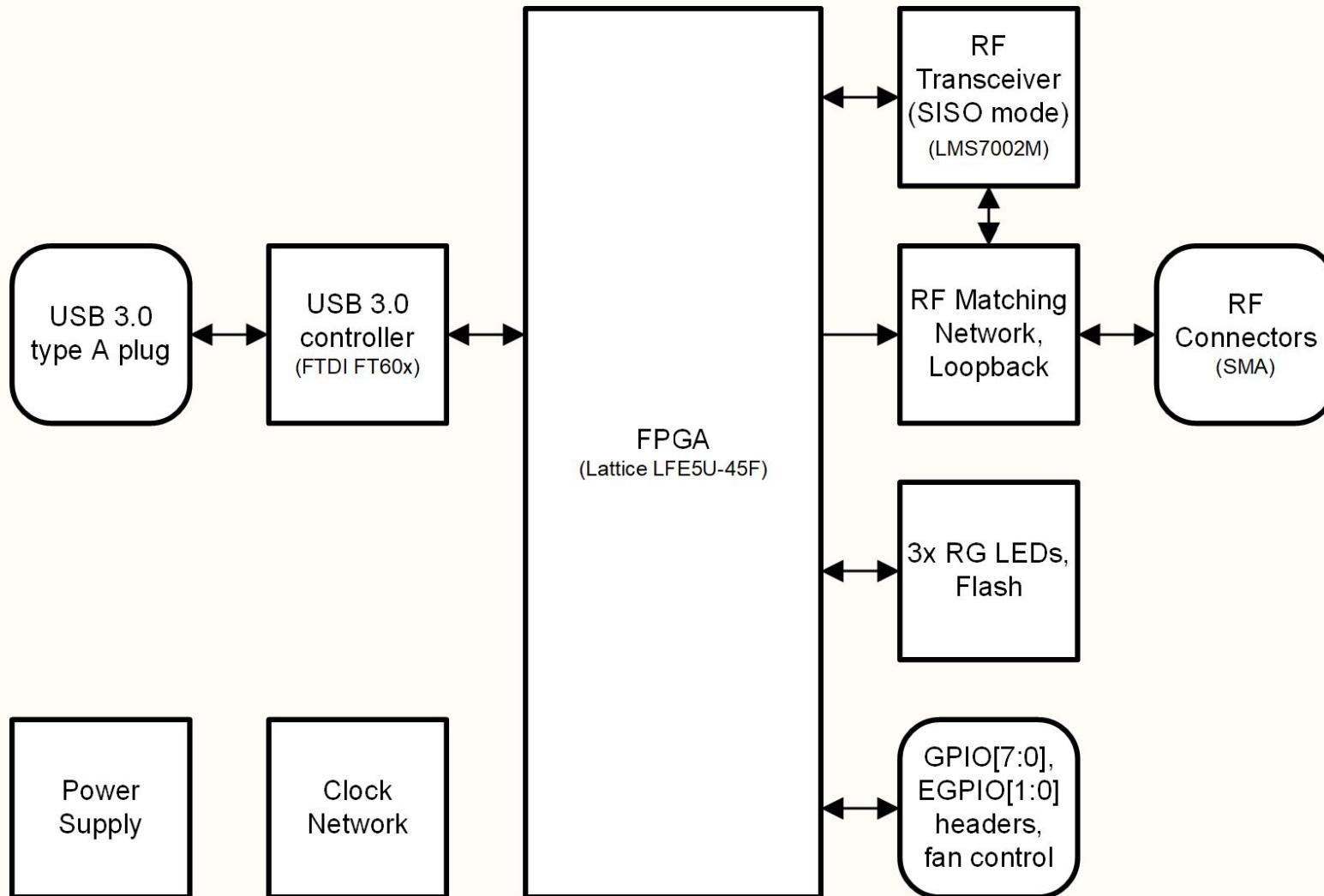


Block diagram



Project name: **LimeSDR_Mini_2v0.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v2.0**

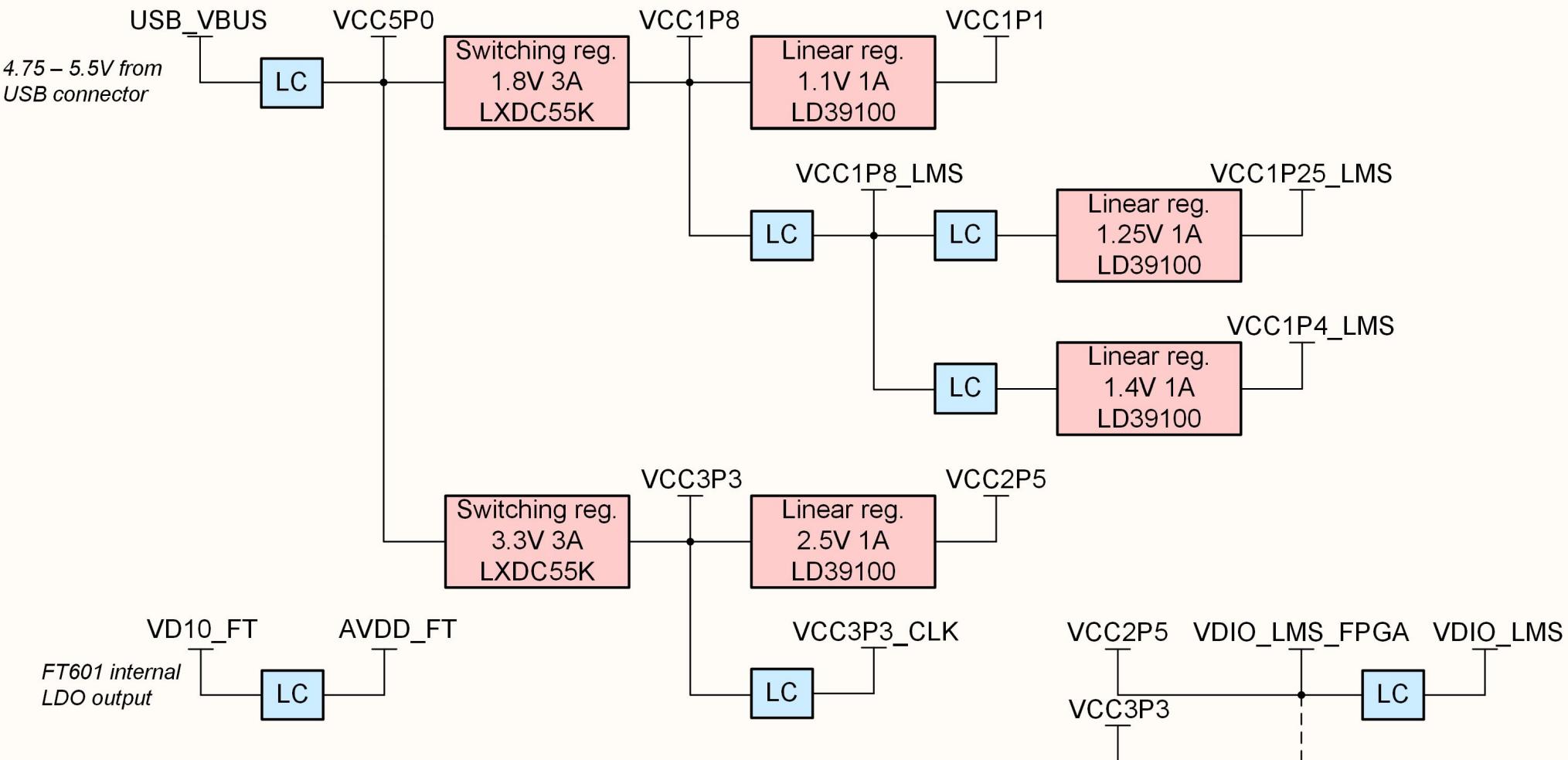
Date: **2021-12-01** Time: **10:49:25** Sheet **1** of **10**

File: **01_Block_Diagram.SchDoc**

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United Kingdom



Power diagram



Project name: **LimeSDR_Mini_2v0.PrjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v2.0**

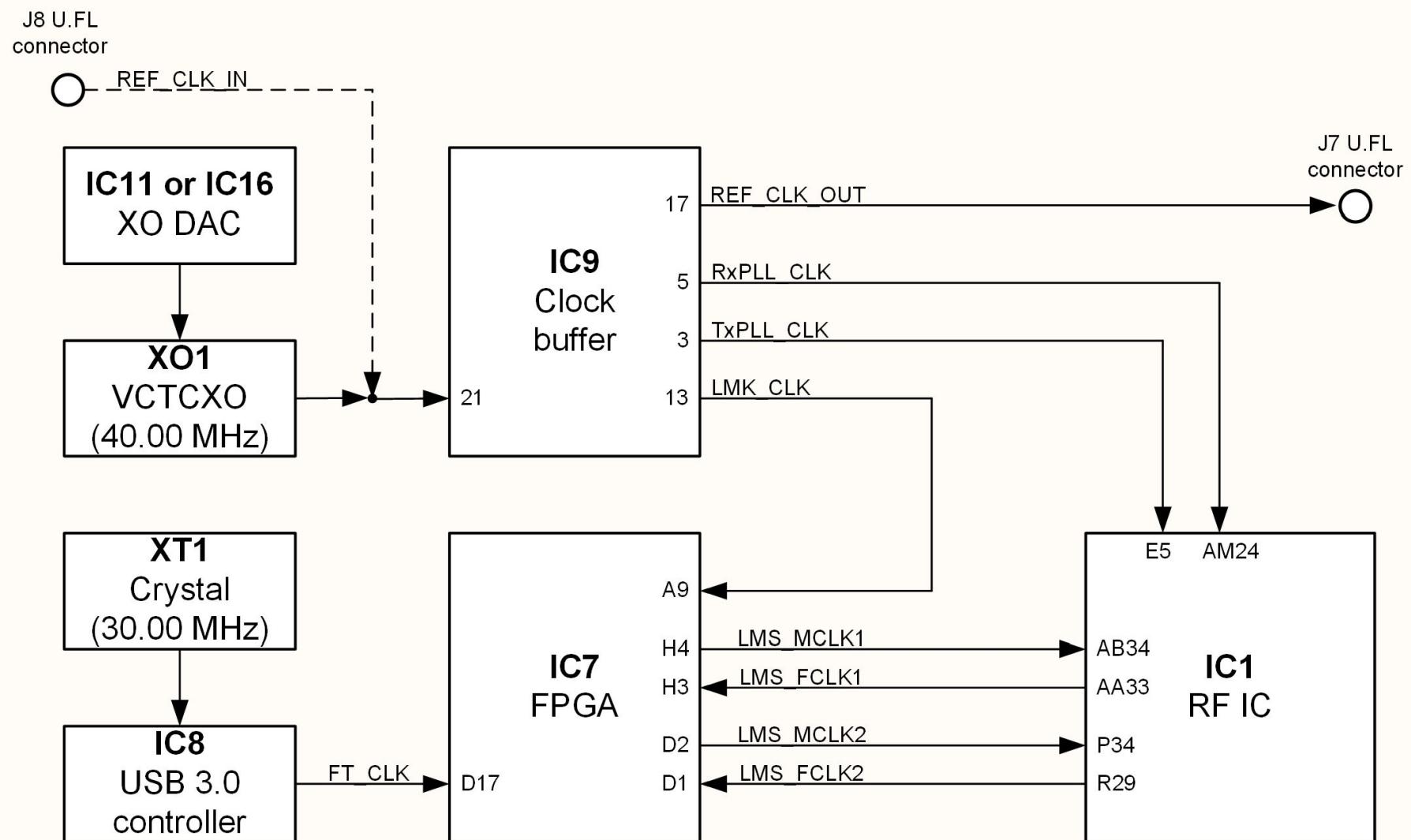
Date: **2021-12-01** Time: **10:49:26** Sheet**2** of **10**

File: **02_Power_Diagram.SchDoc**

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Clock diagram



Project name: *LimeSDR_Mini_2v0.PrbPcb*

Title: *Clock diagram*

Size: *A4* Revision: *v2.0*

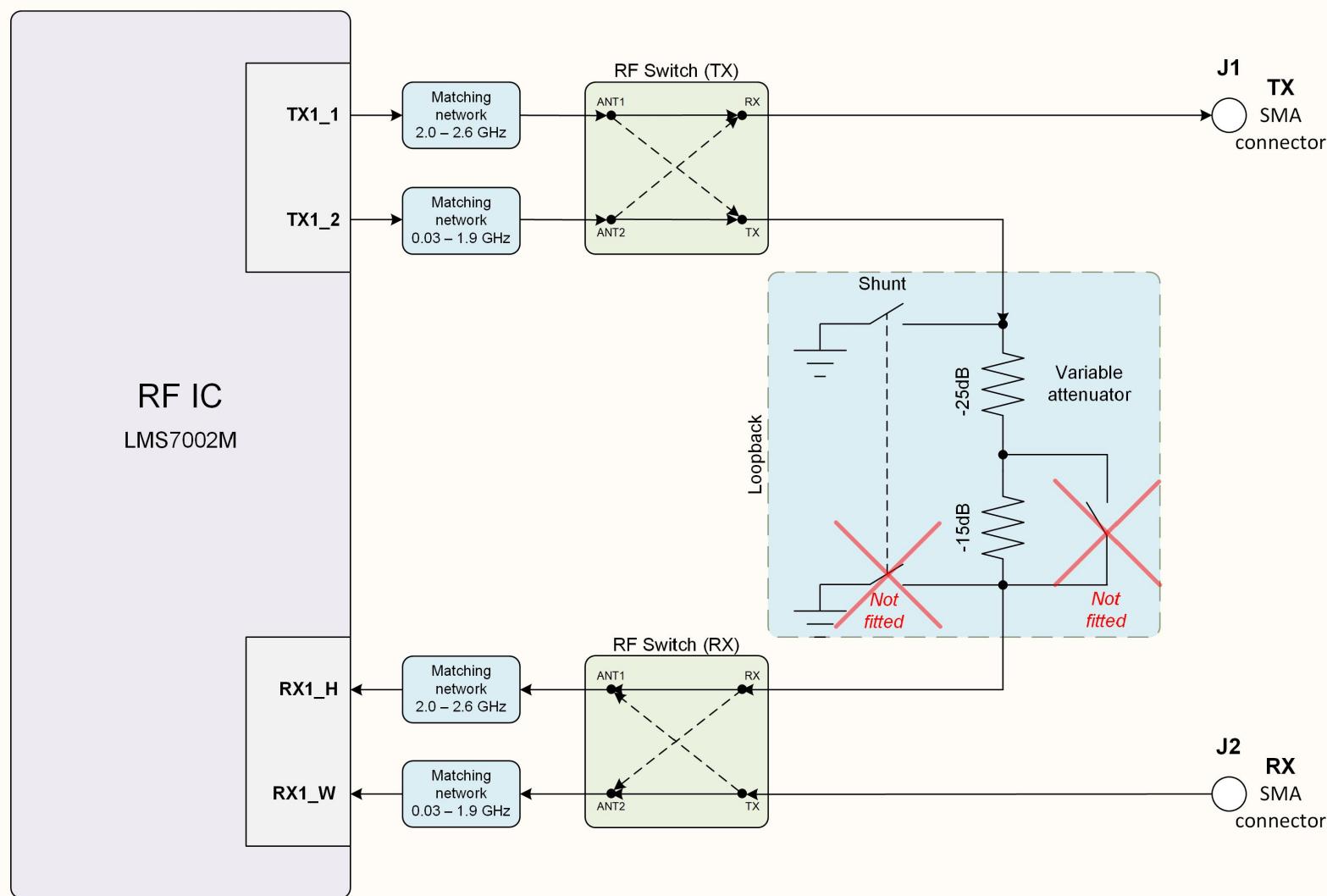
Date: *2021-12-01* Time: *10:49:29* Sheet *3* of *10*

File: *03_Clock_Diagram.SchDoc*

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RF diagram



Project name: **LimeSDR_Mini_2v0.PrbPcb**

Title: **RF diagram**

Size: **A4** Revision: **v2.0**

Date: **2021-12-01** Time: **10:49:31** Sheet **4** of **10**

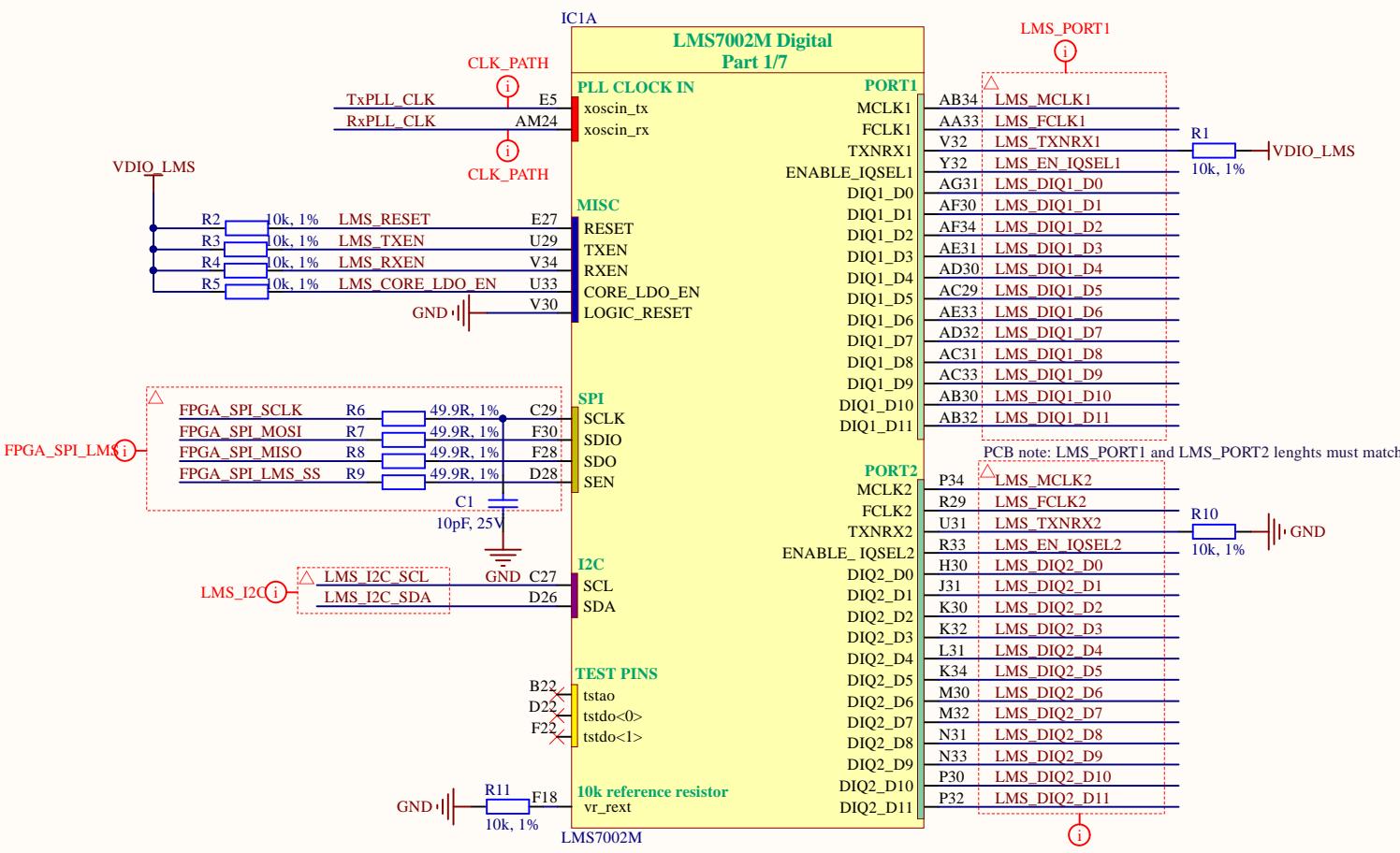
File: **04_RF_Diagram.SchDoc**

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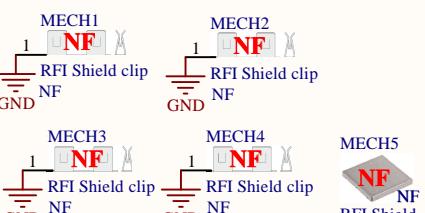
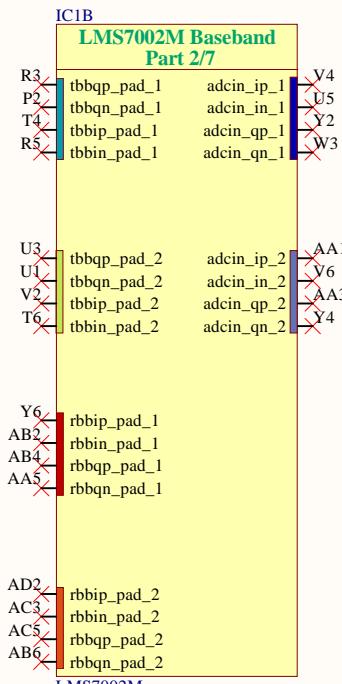


NF elements on sheet: IC2, MECH1-MECH11, FAN1
Number of NF elements on sheet: 13

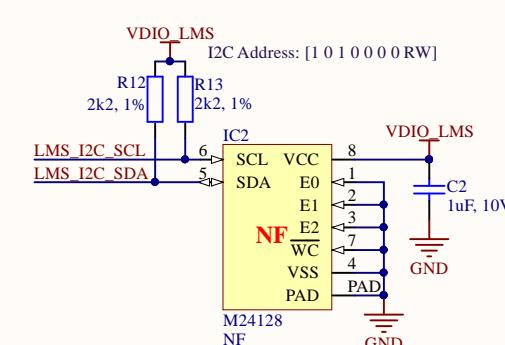
LMS7002M misc



Baseband external IO



LMS EEPROM



Local fiducial LMS Top
FL1

Project name: LimeSDR_Mini_2v0.PrjPcb

Title: LMS7002M misc

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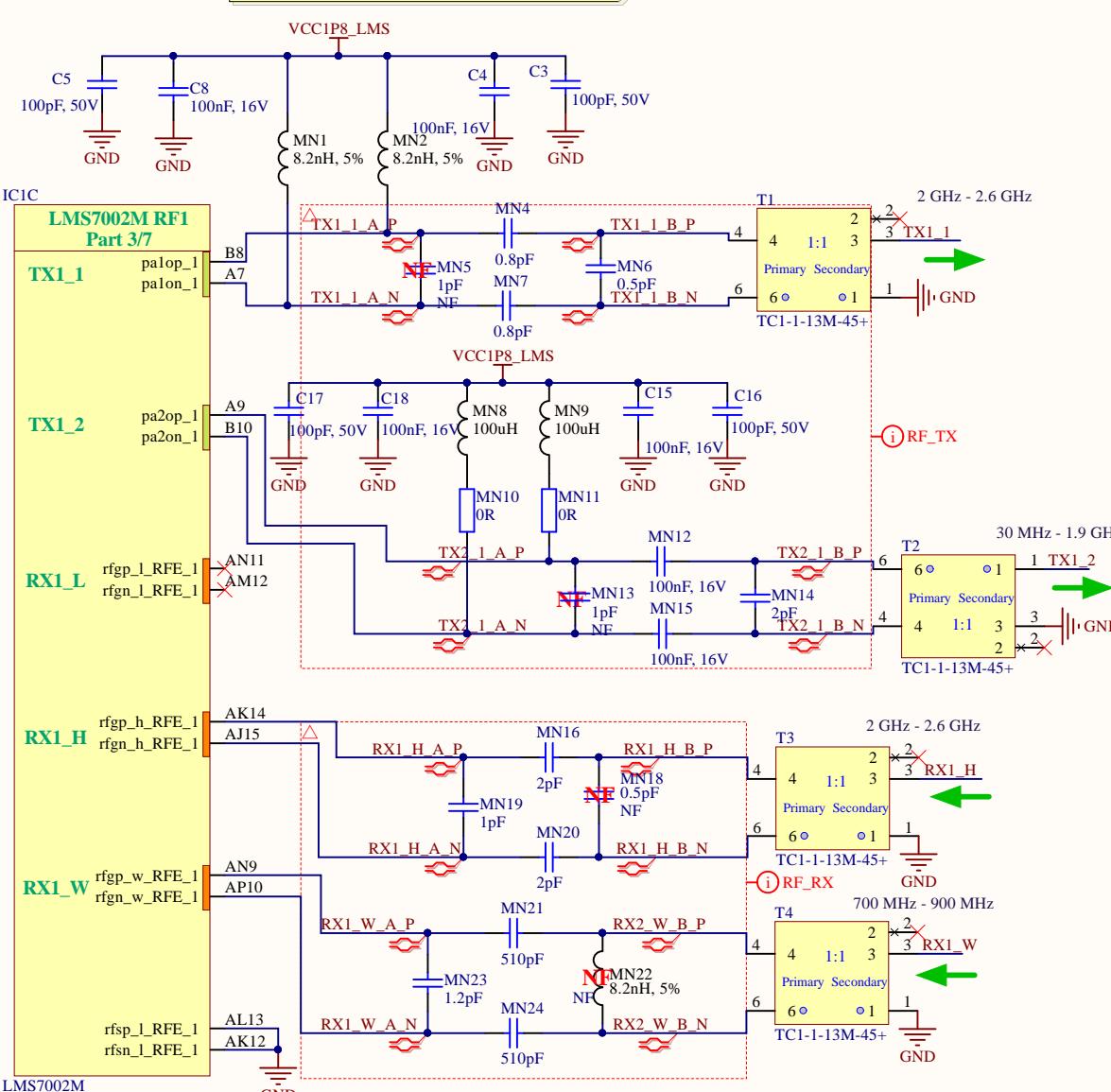
Size: A3 Revision: v2.0

Date: 2021-12-01 Time: 10:49:33 Sheet 5 of 10

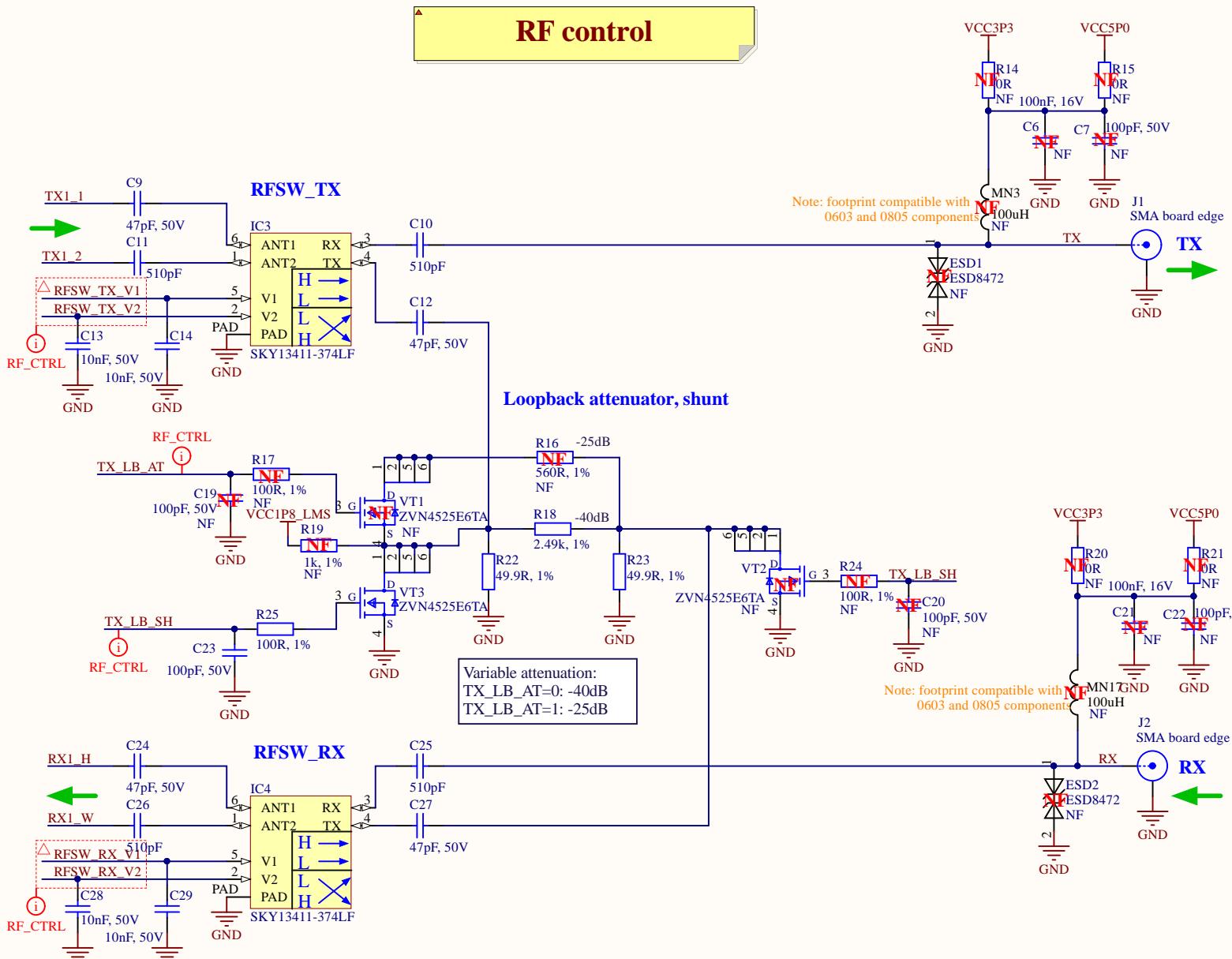
File: 05_LMS7002M_Misc.SchDoc

LMS7002M RF circuits

LMS RF Channel 1

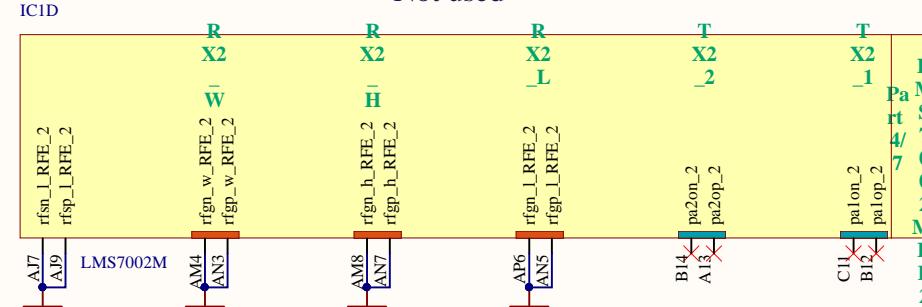


RF control



JMS RF Channel 2

Not used

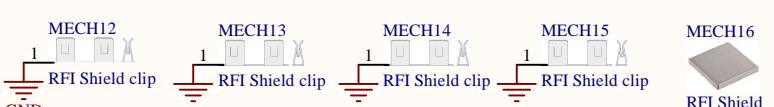


RF truth table

RF truth table				J1 (TX)	J2 (RX)	Loopback
RFSW_TX	RFSW_RX	V1	V2	V1	V2	
H	L	H	L	TX1_1	RX1_H	TX1_2 → RX1_W
L	H	H	L	TX1_2	RX1_H	TX1_1 → RX1_W
H	L	L	H	TX1_1	RX1_W	TX1_2 → RX1_H
L	H	L	H	TX1_2	RX1_W	TX1_1 → RX1_H

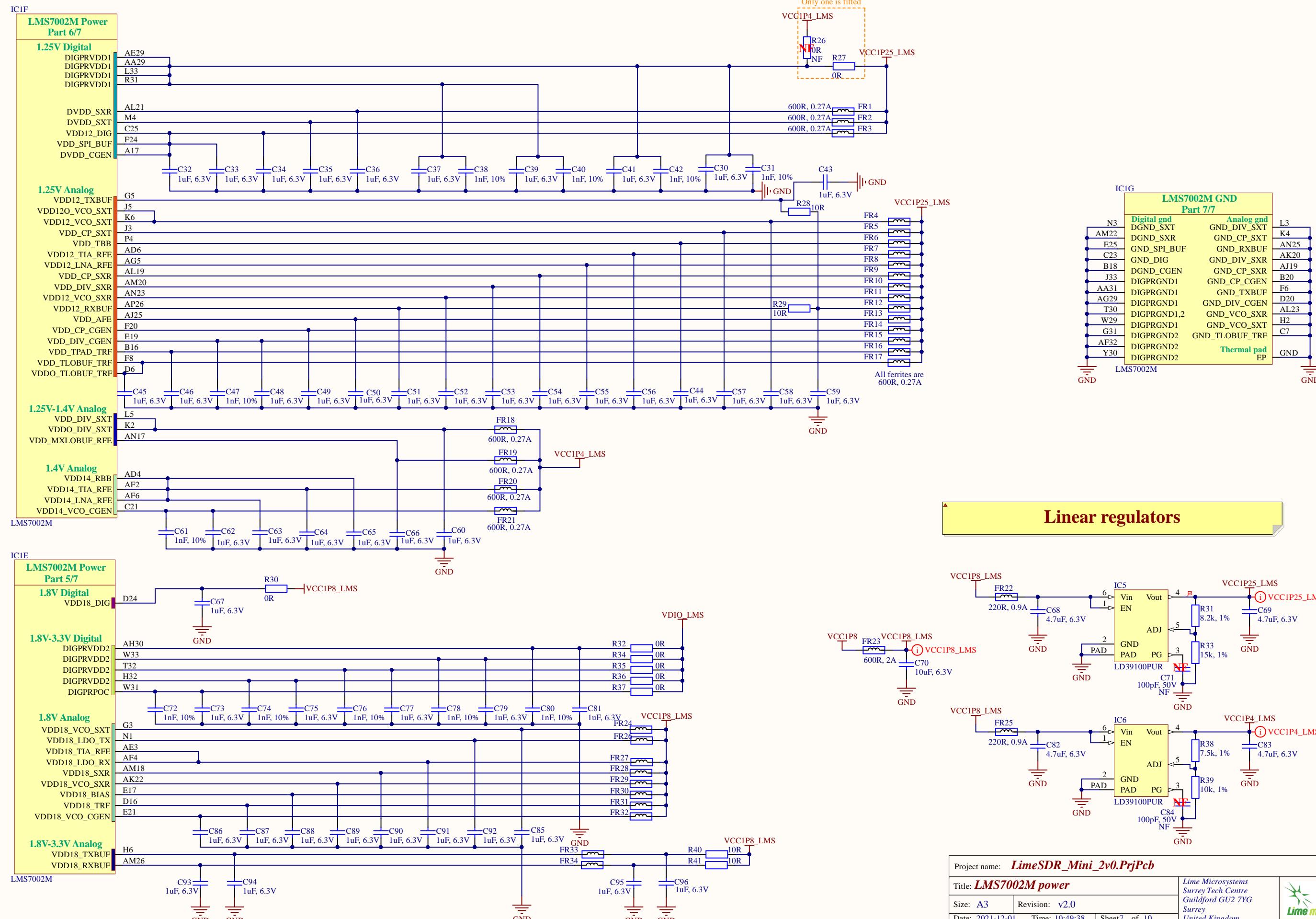
RFSW (SKY13411) truth table

LED A (SPLIT RX) STATE TABLE					
V1	V2	ANT1 (pin 6) → TX (pin 4)	ANT1 (pin 6) → RX (pin 3)	ANT2 (pin 1) → TX (pin 4)	ANT2 (pin 1) → RX (pin 3)
H	L	ISOLATION	ON	ON	ISOLATION
L	H	ON	ISOLATION	ISOLATION	ON



NF elements on sheet: R26, C71, C84
Number of NF elements on sheet: 3

LMS7002M power supply circuit



Project name: LimeSDR_Mini_2v0.PrbPcb

Title: LMS7002M power

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Size: A3 Revision: v2.0

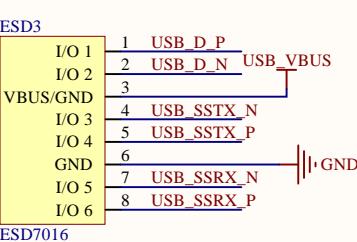
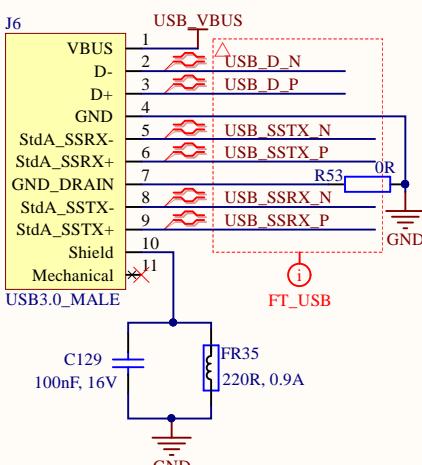
Date: 2021-12-01 Time: 10:49:38 Sheet 7 of 10

File: 07_LMS7002M_Power.SchDoc

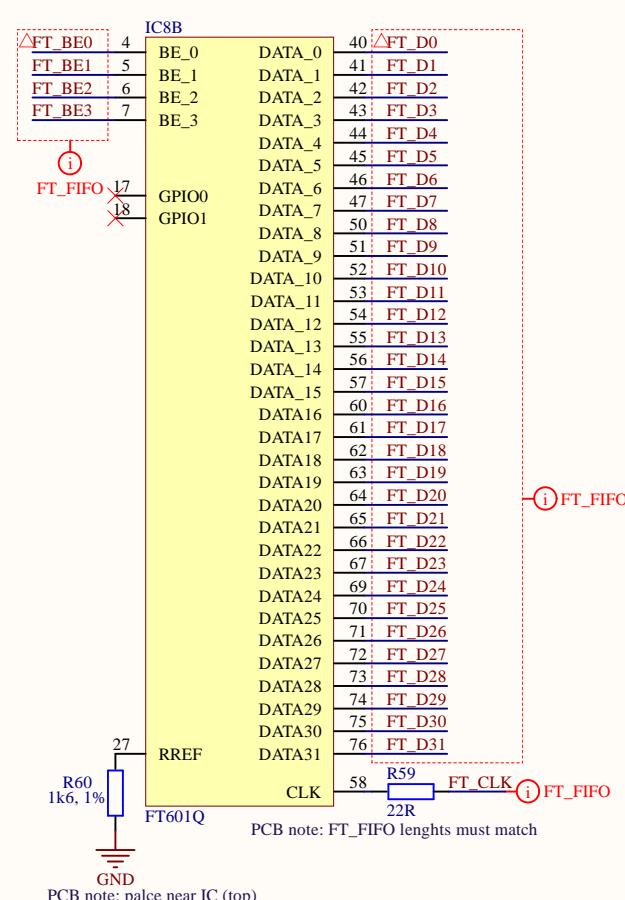
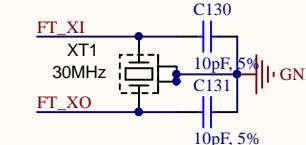
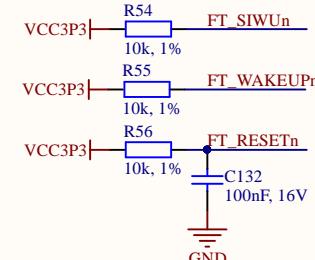
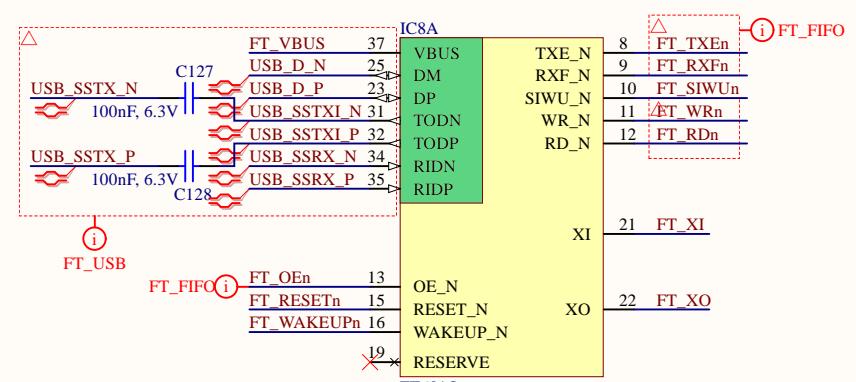
NF elements on sheet: MECH18-MECH21
Number of NF elements on sheet: 5

USB 3.0 to FIFO interface

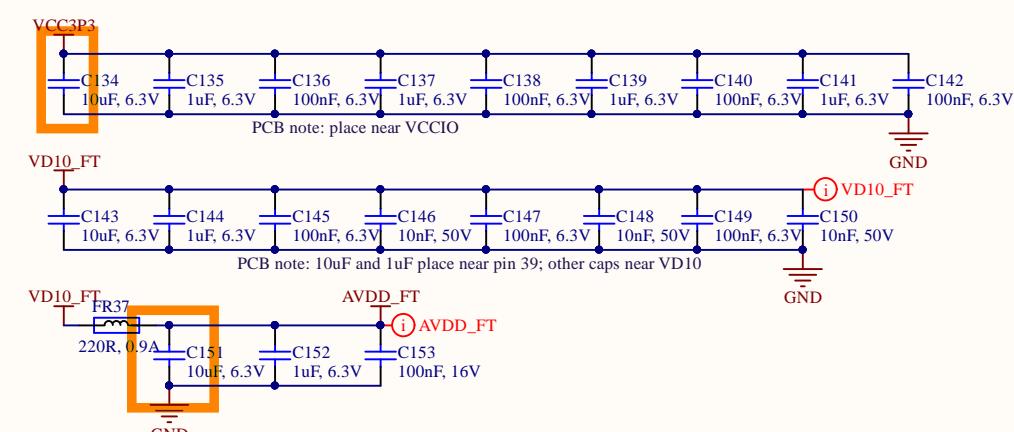
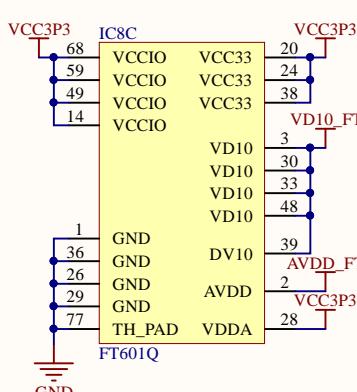
USB 3.0 type A plug and ESD



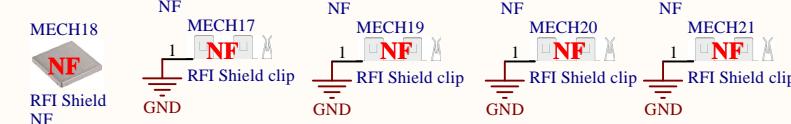
FTDI digital interface



FTDI Power



Schematic note: marked 10uF caps not crucial and can be removed to reduce BOM price



Project name: LimeSDR_Mini_2v0.PrjPcb

Title: USB3.0 device

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Size: A3 Revision: v2.0

Date: 2021-12-01 Time: 10:49:42 Sheet 9 of 10

File: 09_USB3_0_FIFO.SchDoc

