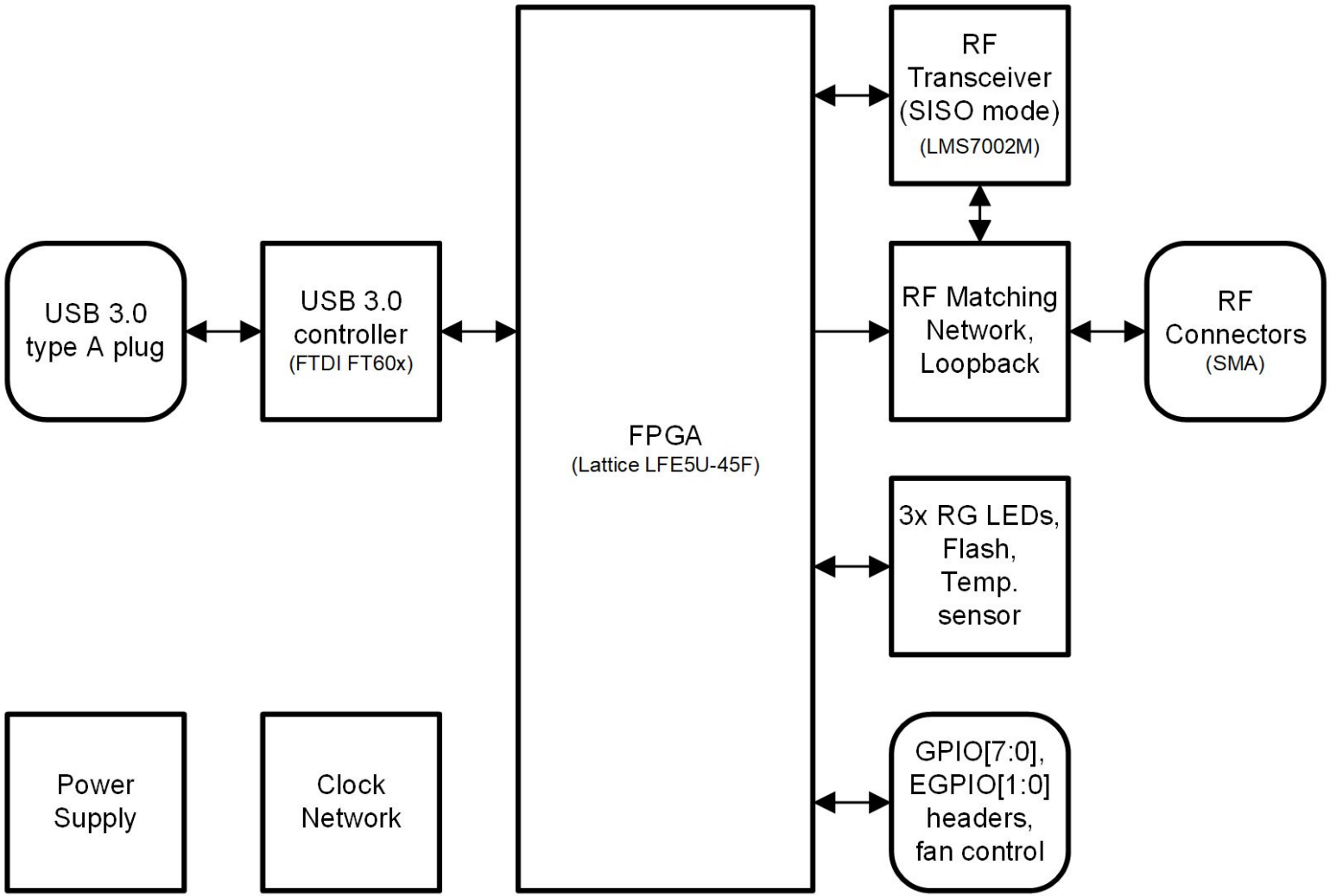
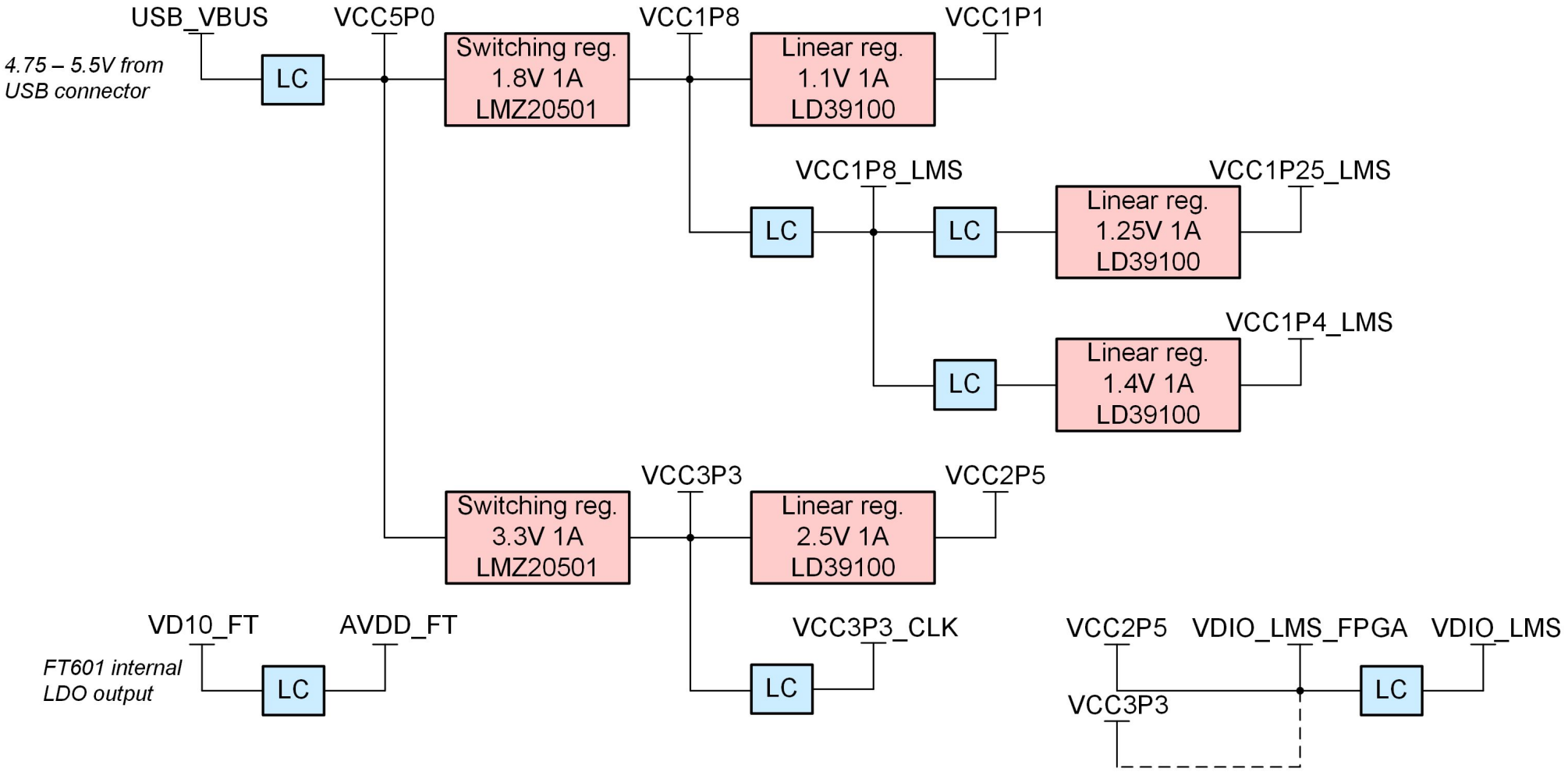
Block diagram



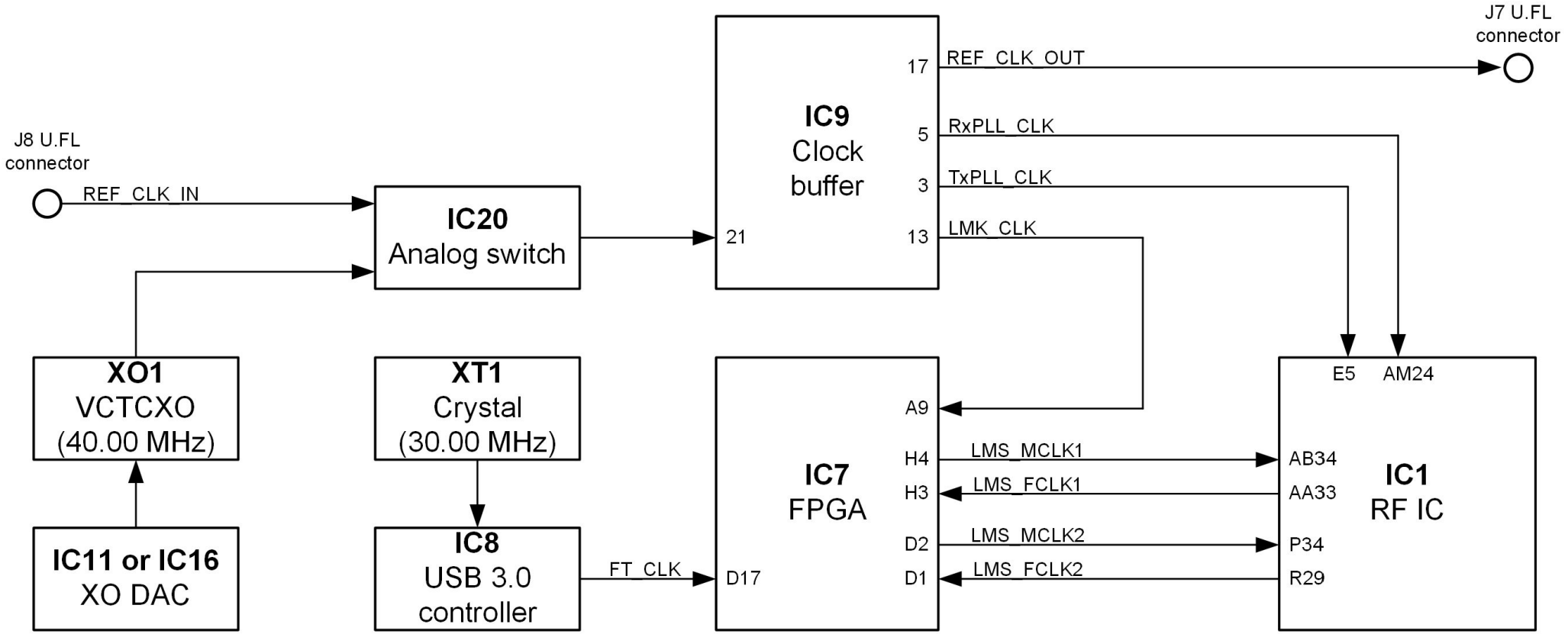
Project name: *LimeSDR-Mini_2v4.PrjPcb*			
Title: ***Block diagram***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*	Lime microsystems
Size: A4	Revision: v2.4		
Date: 2023-04-24 Time: 16:06:30	Sheet1 of 10		
File: 01_Block_Diagram.SchDoc			

Power diagram



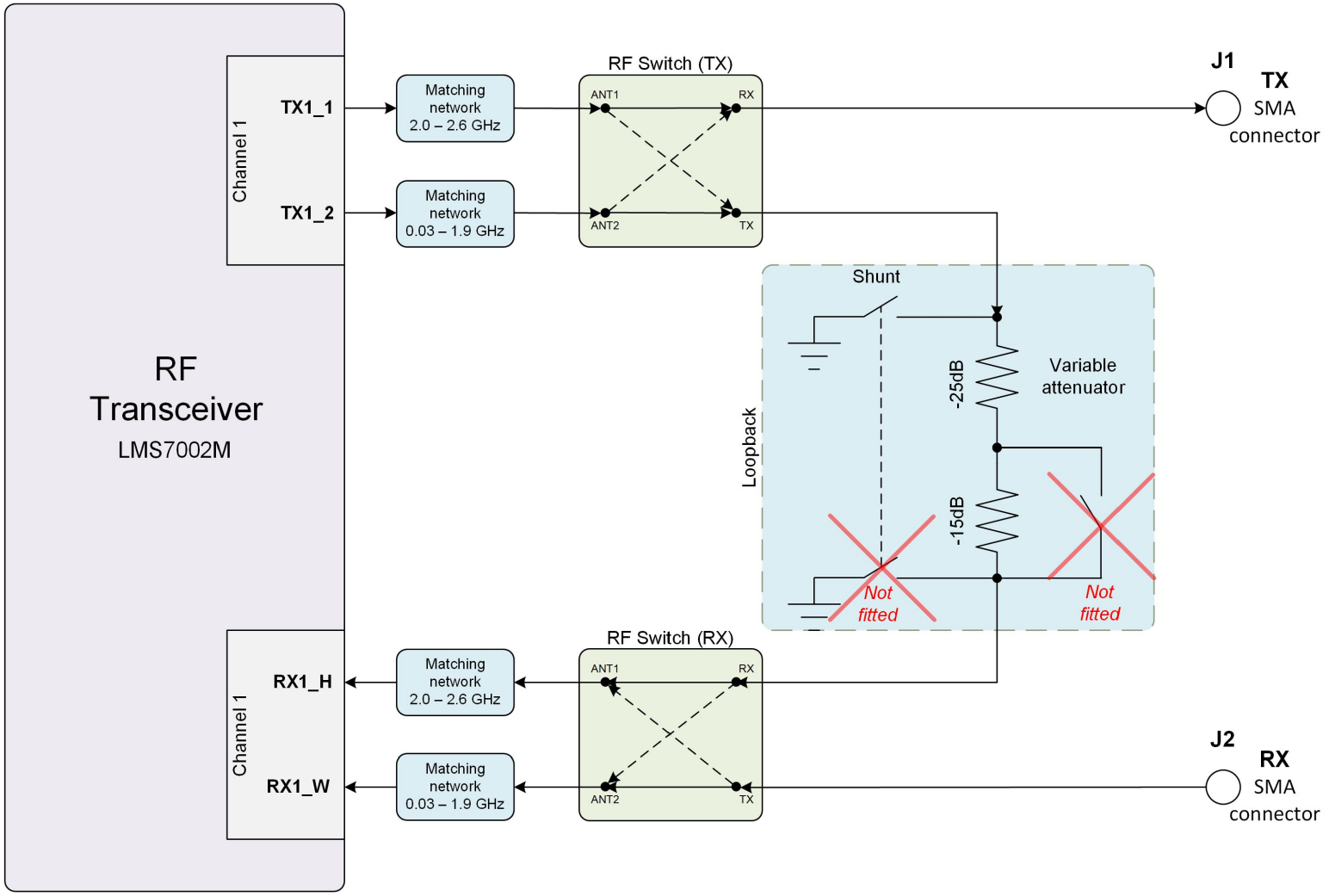
Project name: *LimeSDR-Mini_2v4.PrjPcb*			
Title: ***Power diagram***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*	Lime microsystems
Size: A4	Revision: v2.4		
Date: 2023-04-24 Time: 16:06:30	Sheet2 of 10		
File: 02_Power_Diagram.SchDoc			

Clock diagram



Project name: *LimeSDR-Mini_2v4.PrjPcb*			
Title: *Clock diagram*			*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A4	Revision: v2.4		
Date: 2023-04-24	Time: 16:06:30	Sheet 3 of 10	
File: 03_Clock_Diagram.SchDoc			

RF diagram

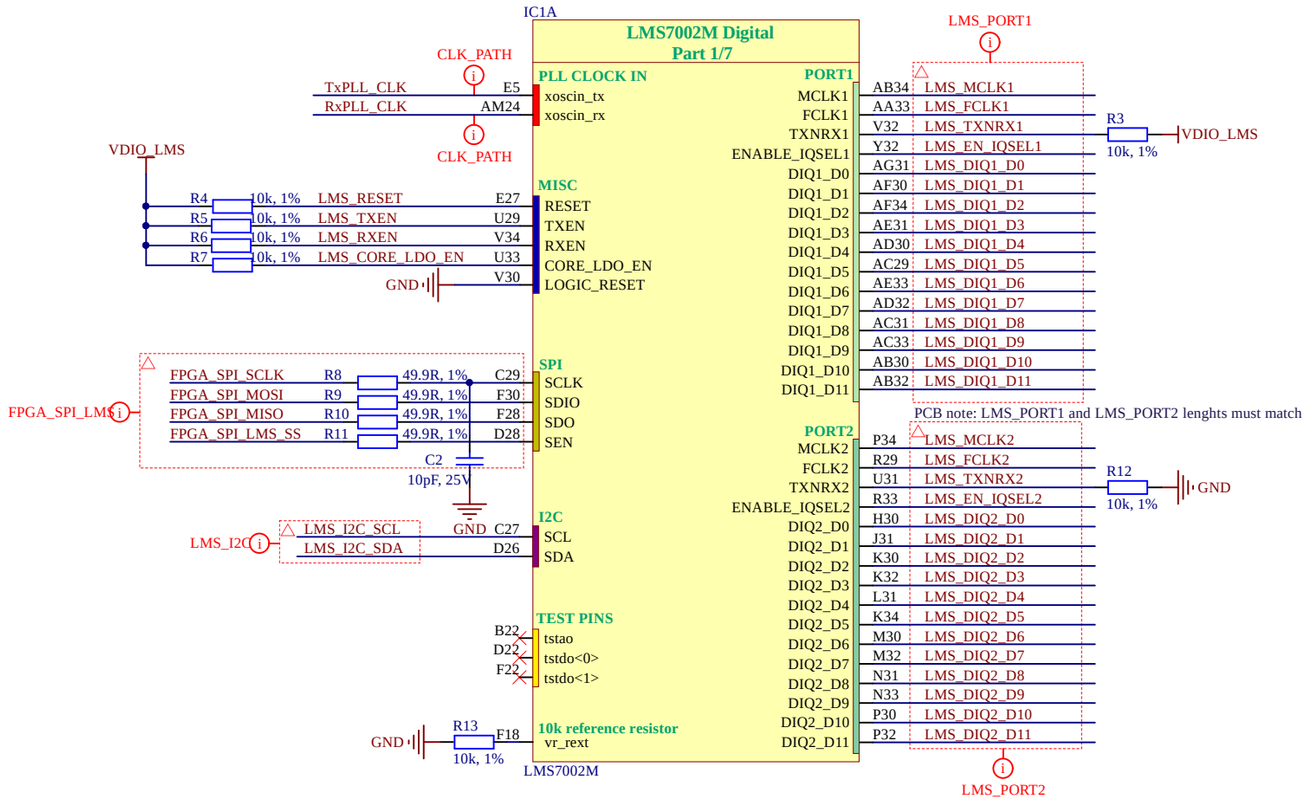


Project name: *LimeSDR-Mini_2v4.PrjPcb*			
Title: *RF diagram*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*	Lime microsystems
Size: A4	Revision: v2.4		
Date: 2023-04-24 Time: 16:06:30	Sheet 4 of 10		
File: 04_RF_Diagram.SchDoc			

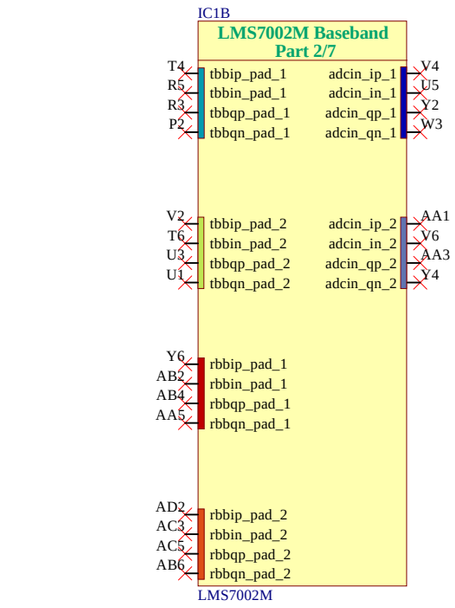
NF elements on sheet: IC2, MECH1-MECH5, MECH11-MECH15, MEHC16-MECH21, FAN1
Number of NF elements on sheet: 18

LMS7002M misc

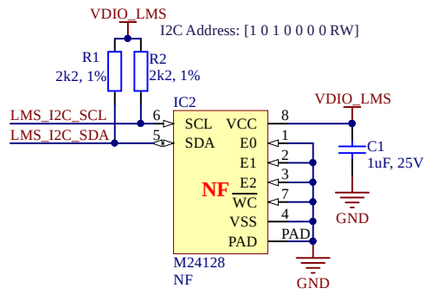
LMS7002M digital circuit



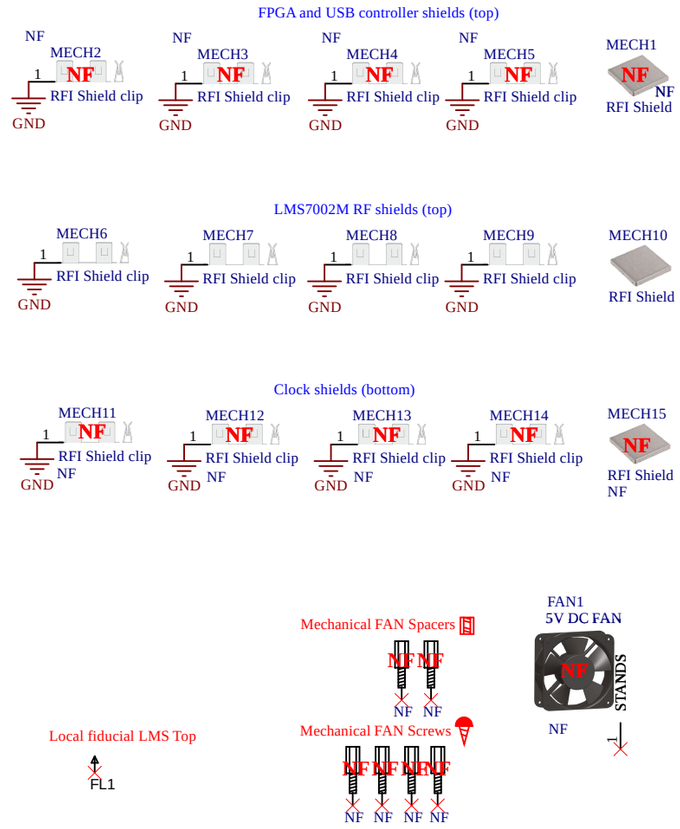
Baseband external IO



LMS EEPROM



Mechanical components

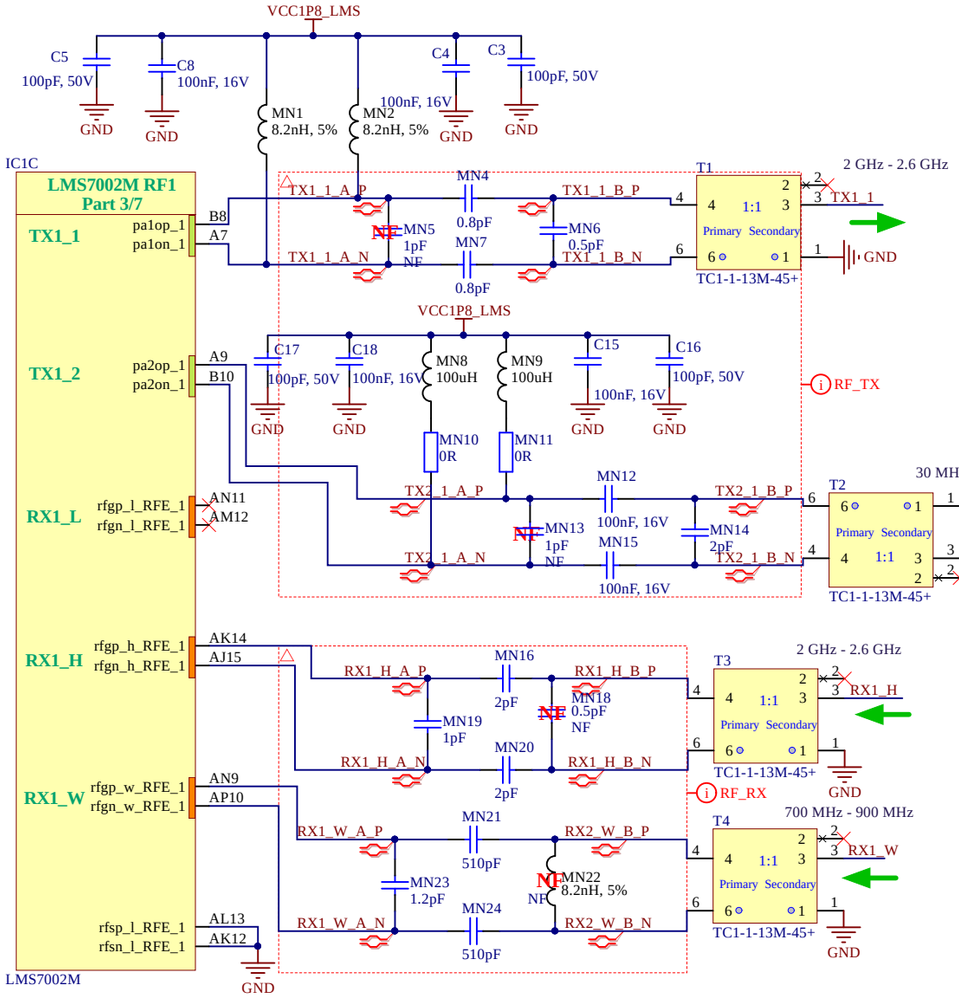


Project name: *LimeSDR-Mini_2v4.PrjPcb*			
Title: *LMS7002M misc*			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v2.4		
Date: 2023-04-24	Time: 16:06:30	Sheet 5 of 10	
File: 05_LMS7002M_Misc.SchDoc			

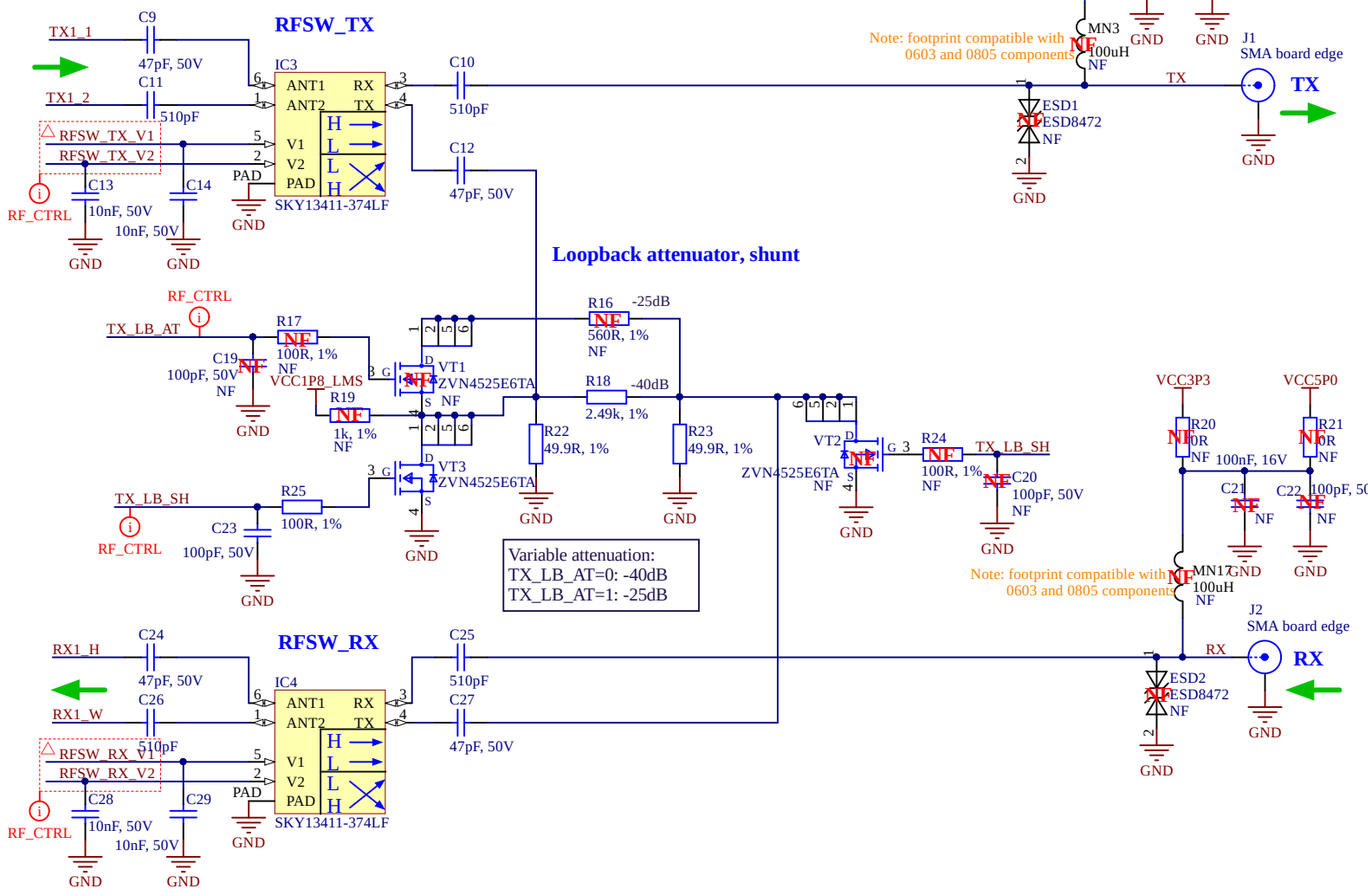
NF elements on sheet: R14, R15, C6, C7, MN3, ESD1, MN5, C19, R17, R19, VT1, R16, VT2, R24, C20, MN13, R20, R21, C21, C22, MN17, ESD2, MN18, MN22
Number of NF elements on sheet: 24

LMS7002M RF circuits

LMS RF Channel 1

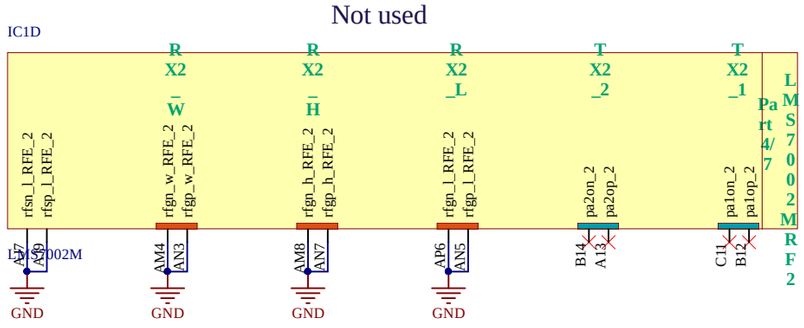


RF control



LMS RF Channel 2

Not used



RF truth table

RFSW_TX		RFSW_RX		J1	J2	Loopback
V1	V2	V1	V2	(TX)	(RX)	
H	L	H	L	TX1_1	RX1_H	TX1_2 → RX1_W
L	H	H	L	TX1_2	RX1_H	TX1_1 → RX1_W
H	L	L	H	TX1_1	RX1_W	TX1_2 → RX1_H
L	H	L	H	TX1_2	RX1_W	TX1_1 → RX1_H

RFSW (SKY13411) truth table

V1	V2	ANT1 (pin 6) → TX (pin 4)	ANT1 (pin 6) → RX (pin 3)	ANT2 (pin 1) → TX (pin 4)	ANT2 (pin 1) → RX (pin 3)
H	L	ISOLATION	ON	ON	ISOLATION
L	H	ON	ISOLATION	ISOLATION	ON

Project name:	LimeSDR-Mini_2v4.PrjPcb
Title:	LMS7002M RF
Size:	A3
Revision:	v2.4
Date:	2023-04-24
Time:	16:06:31
Sheet	6 of 10
File:	06_LMS7002M_RF.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

NF elements on sheet: R26, C71, C84
Number of NF elements on sheet: 3

LMS7002M power supply circuit

IC1F
LMS7002M Power Part 6/7
1.25V Digital
DIGPRVDD1 AE29
DIGPRVDD1 AA29
DIGPRVDD1 L33
DIGPRVDD1 R31
DVDD_SXR AL21
DVDD_SXT M4
VDD12_DIG C25
VDD_SPI_BUF F24
DVDD_CGEN A17
1.25V Analog
VDD12_TXBUF G5
VDD12O_VCO_SXT J5
VDD12_VCO_SXT K6
VDD_CP_SXT J3
VDD_TBB P4
VDD12_TIA_RFE AD6
VDD12_LNA_RFE AG5
VDD_CP_SXR AL19
VDD_DIV_SXR AM20
VDD12_VCO_SXR AN23
VDD12_RXBUF AP26
VDD_AFE AJ25
VDD_CP_CGEN F20
VDD_DIV_CGEN E19
VDD_TPAD_TRF B16
VDD_TLOBUF_TRF F8
VDDO_TLOBUF_TRF D6
1.25V-1.4V Analog
VDD_DIV_SXT L5
VDDO_DIV_SXT K2
VDD_MXLOBUF_RFE AN17
1.4V Analog
VDD14_RBB AD4
VDD14_TIA_RFE AF2
VDD14_LNA_RFE AF6
VDD14_VCO_CGEN C21
LMS7002M

Only one is fitted
VCC1P4_LMS
R26 0R NF
R27 0R
VCC1P25_LMS
600R, 0.27A FR1
600R, 0.27A FR2
600R, 0.27A FR3
C32 1uF, 6.3V
C33 1uF, 6.3V
C34 1uF, 6.3V
C35 1uF, 6.3V
C36 1uF, 6.3V
C37 1uF, 6.3V
C38 1nF, 10%
C39 1uF, 6.3V
C40 1nF, 10%
C41 1uF, 6.3V
C42 1nF, 10%
C30 1uF, 6.3V
C31 1nF, 10%
GND
C43 1uF, 6.3V
GND
R28 10R
VCC1P25_LMS
FR4
FR5
FR6
FR7
FR8
FR9
FR10
FR11
FR12
R29 10R
FR13
FR14
FR15
FR16
FR17
All ferrites are 600R, 0.27A
C45 1uF, 6.3V
C46 1uF, 6.3V
C47 1nF, 10%
C48 1uF, 6.3V
C49 1uF, 6.3V
C50 1uF, 6.3V
C51 1uF, 6.3V
C52 1uF, 6.3V
C53 1uF, 6.3V
C54 1uF, 6.3V
C55 1uF, 6.3V
C56 1uF, 6.3V
C44 1uF, 6.3V
C57 1uF, 6.3V
C58 1uF, 6.3V
C59 1uF, 6.3V
GND
FR18 600R, 0.27A
FR19 600R, 0.27A
VCC1P4_LMS
FR20 600R, 0.27A
FR21 600R, 0.27A
C61 1nF, 10%
C62 1uF, 6.3V
C63 1uF, 6.3V
C64 1uF, 6.3V
C65 1uF, 6.3V
C66 1uF, 6.3V
C60 1uF, 6.3V
GND

IC1G
LMS7002M GND Part 7/7
Digital gnd
N3 DGND_SXT
AM22 DGND_SXR
E25 GND_SPI_BUF
C23 GND_DIG
B18 DGND_CGEN
J33 DIGPRGND1
AA31 DIGPRGND1
AG29 DIGPRGND1
T30 DIGPRGND1,2
W29 DIGPRGND1
G31 DIGPRGND2
AF32 DIGPRGND2
Y30 DIGPRGND2
Analog gnd
L3 GND_DIV_SXT
K4 GND_CP_SXT
AN25 GND_RXBUF
AK20 GND_DIV_SXR
AJ19 GND_CP_SXR
B20 GND_CP_CGEN
F6 GND_TXBUF
D20 GND_DIV_CGEN
AL23 GND_VCO_SXR
H2 GND_VCO_SXT
C7 GND_TLOBUF_TRF
Thermal pad
EP GND
GND
LMS7002M
GND

IC1E
LMS7002M Power Part 5/7
1.8V Digital
VDD18_DIG D24
R30 0R
VCC1P8_LMS
C67 1uF, 6.3V
GND
1.8V-3.3V Digital
DIGPRVDD2 AH30
DIGPRVDD2 W33
DIGPRVDD2 T32
DIGPRVDD2 H32
DIGPRPOC W31
VDIO_LMS
R32 0R
R34 0R
R35 0R
R36 0R
R37 0R
C72 1nF, 10%
C73 1uF, 6.3V
C74 1nF, 10%
C75 1uF, 6.3V
C76 1nF, 10%
C77 1uF, 6.3V
C78 1nF, 10%
C79 1uF, 6.3V
C80 1nF, 10%
C81 1uF, 6.3V
1.8V Analog
VDD18_VCO_SXT G3
VDD18_LDO_TX N1
VDD18_TIA_RFE AE3
VDD18_LDO_RX AF4
VDD18_SXR AM18
VDD18_VCO_SXR AK22
VDD18_BIAS E17
VDD18_TRF D16
VDD18_VCO_CGEN E21
VCC1P8_LMS
FR24
FR26
FR27
FR28
FR29
FR30
FR31
FR32
C86 1uF, 6.3V
C87 1uF, 6.3V
C88 1uF, 6.3V
C89 1uF, 6.3V
C90 1uF, 6.3V
C91 1uF, 6.3V
C92 1uF, 6.3V
C85 1uF, 6.3V
GND
1.8V-3.3V Analog
VDD18_TXBUF H6
VDD18_RXBUF AM26
FR33
FR34
R40 10R
R41 10R
VCC1P8_LMS
C93 1uF, 6.3V
C94 1uF, 6.3V
C95 1uF, 6.3V
C96 1uF, 6.3V
GND
GND
GND
GND
LMS7002M

Linear regulators

VCC1P8_LMS
FR22 220R, 0.9A
C68 4.7uF, 6.3V
GND
IC5
Vin Vout
EN
ADJ
GND
PAD PG
LD39100PUR
VCC1P25_LMS
R31 8.2k, 1%
R33 15k, 1%
C69 4.7uF, 6.3V
GND
C71 100pF, 50V NF
GND
VCC1P8
FR23 600R, 2A
VCC1P8_LMS
C70 10uF, 6.3V
GND
VCC1P8_LMS
FR25 220R, 0.9A
C82 4.7uF, 6.3V
GND
IC6
Vin Vout
EN
ADJ
GND
PAD PG
LD39100PUR
VCC1P4_LMS
R38 7.5k, 1%
R39 10k, 1%
C83 4.7uF, 6.3V
GND
C84 100pF, 50V NF
GND

Project name:	*LimeSDR-Mini_2v4.PrjPcb*		
Title:	*LMS7002M power*		
Size:	A3	Revision:	v2.4
Date:	2023-04-24	Time: 16:06:31	Sheet7 of 10
File:	07_LMS7002M_Power.SchDoc		

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Surrey Tech Centre
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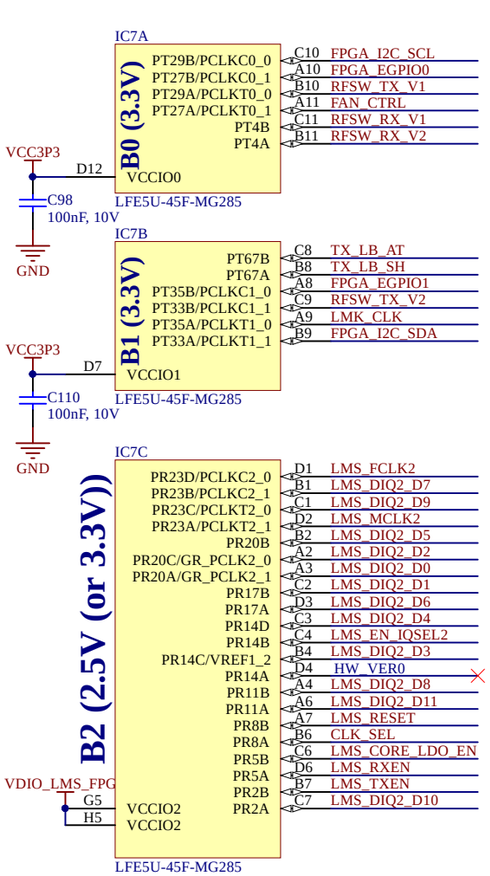
Surrey
United Kingdom

NF elements on sheet: J3, R43, J4, J5
Number of NF elements on sheet: 4

FPGA

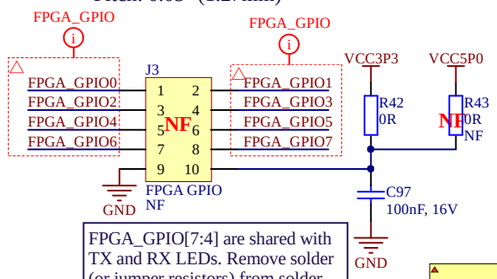
FPGA Banks

By default LFE5U-45F-xxMG285 is fitted and the schematic symbol represents LFE5U-25F pins. LFE5U-45F and LFE5U-85F parts are footprint and pin compatible with LFE5U-25F with small nuances. For example VCCIO0 bank C10 pin has different function:
LFE5U-25F: C10 pin is PT29B/PCLKC0_0
LFE5U-45F: C10 pin is PT38B/PCLKC0_0
LFE5U-85F: C10 pin is PT65B/PCLKC0_0
Therefore if a different to the default FPGA is used, one should look up the proper function note for each pin.
All power and fixed-function pins are the same for LFE5U-25F, LFE5U-45F, LFE5U-85F parts.



FPGA GPIO

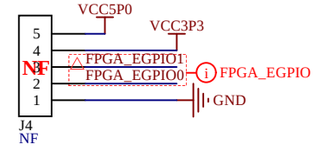
Pitch: 0.05" (1.27mm)



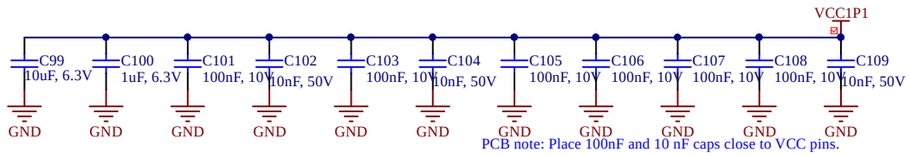
FPGA_GPIO[7:4] are shared with TX and RX LEDs. Remove solder (or jumper resistors) from solder bridges to disconnect LEDs from GPIOs lines.

FPGA GPIO (edge)

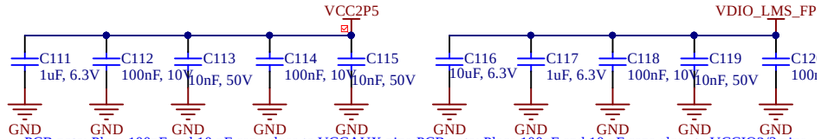
Pitch: 0.1" (2.54mm)



Decoupling

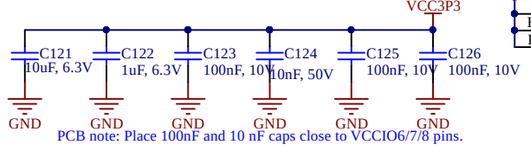


PCB note: Place 100nF and 10 nF caps close to VCC pins.

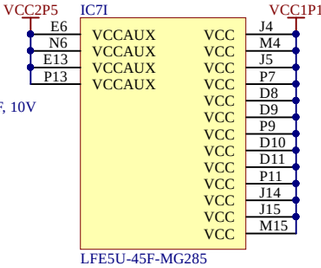


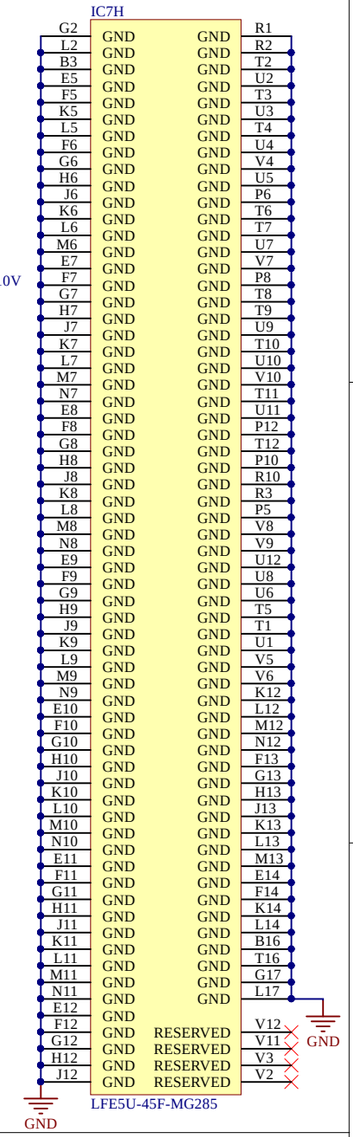
PCB note: Place 100nF and 10 nF caps close to VCCAUX pins.

PCB note: Place 100nF and 10 nF caps close to VCCIO2/3 pins.



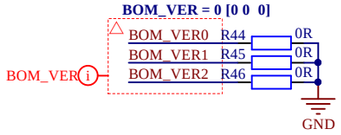
PCB note: Place 100nF and 10 nF caps close to VCCIO6/7/8 pins.





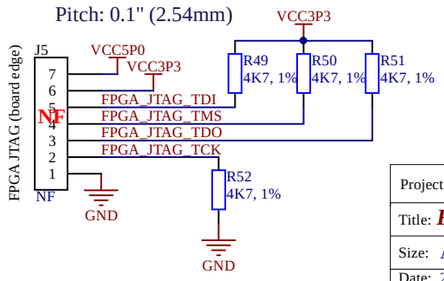
HW_VER & BOM_VER

HW_VER = 7 [0 1 1 1]
BOM_VER = 0 [0 0 0]



FPGA JTAG (edge)

Pitch: 0.1" (2.54mm)



Project name:	*LimeSDR-Mini_2v4.PrjPcb*		
Title:	*FPGA*		
Size: A3	Revision: v2.4		
Date: 2023-04-24	Time: 16:06:32	Sheet 8 of 10	
File: 08_FPGA.SchDoc			

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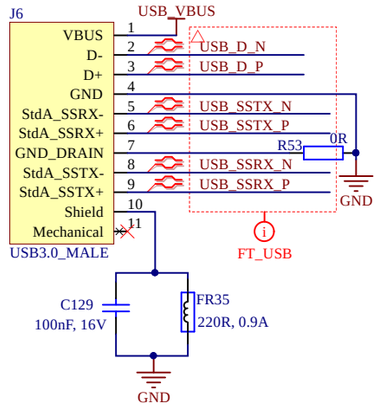
Surrey
United Kingdom

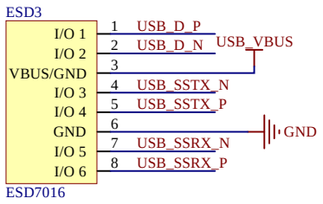
Lime microsystems

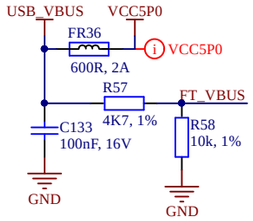
NF elements on sheet: -
Number of NF elements on sheet: 0

USB 3.0 to FIFO interface

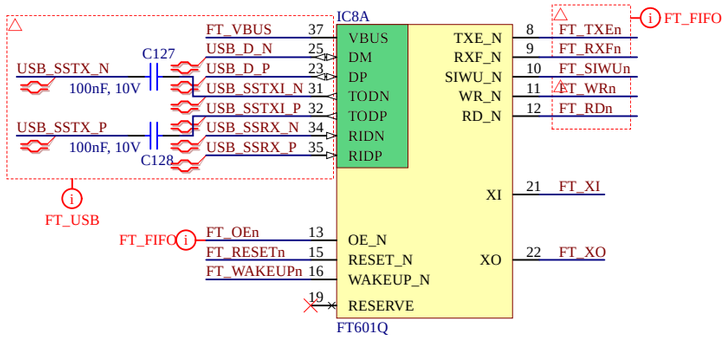
USB 3.0 type A plug and ESD

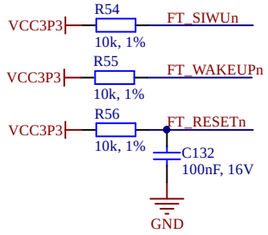


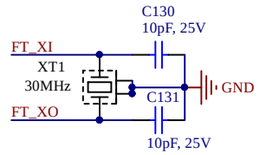


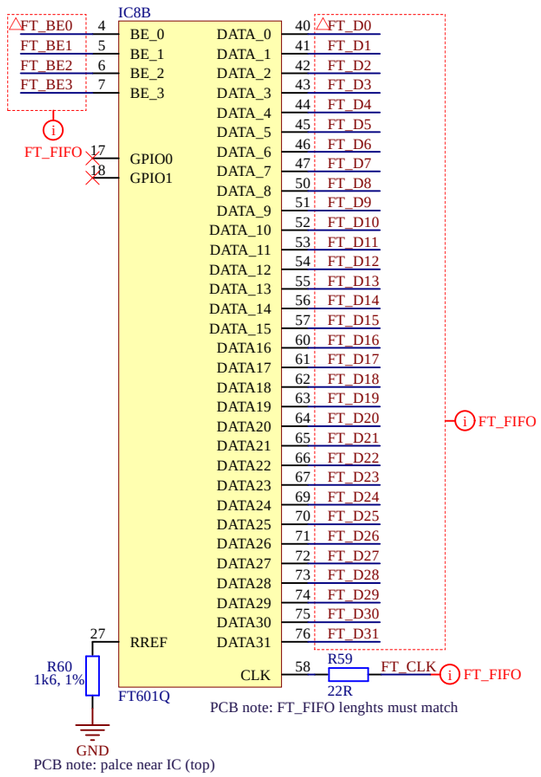


FTDI digital interface

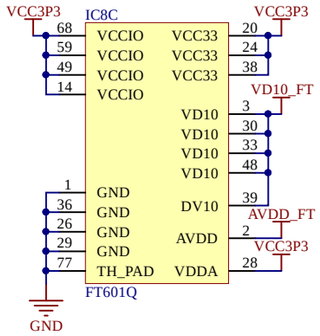


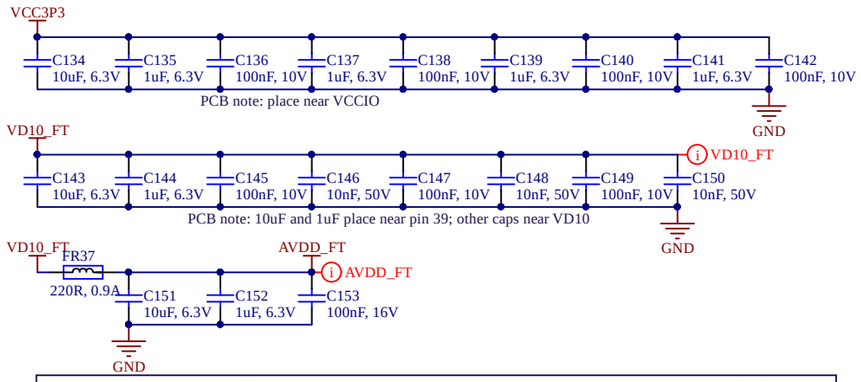






FTDI Power





Schematic note: marked 10uF caps (C134, C143, C151) not crucial and can be removed to reduce BOM price

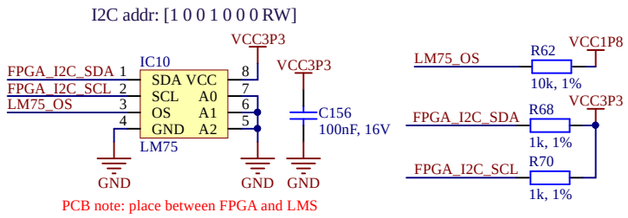
Project name: *LimeSDR-Mini_2v4.PrjPcb*			
Title: *USB3.0 device*			*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surray* *United Kingdom*
Size: A3	Revision: v2.4		
Date: 2023-04-24	Time: 16:06:32	Sheet9 of 10	
File: 09_USB3_0_FIFO.SchDoc			

NF elements on sheet:C157, C158, C160, R71, IC12, C174, FR42, R76, C180, R78, R81, R83, C183, IC16, C184, IC17, R63, R66, R102, C186, R93, C194, C192, R96, J9, R100, R101
Number of NF elements on sheet: 27
Number of NF elements on all sheets: 76

Misc

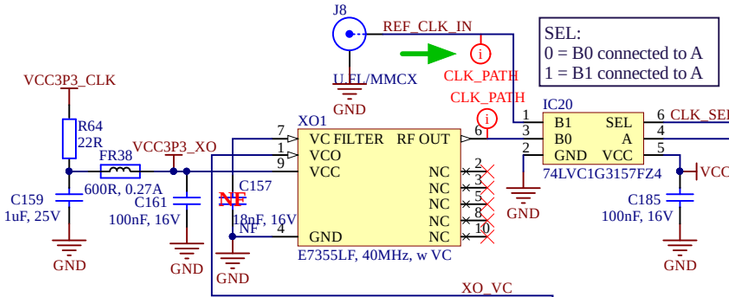
I2C Temperature sensor

I2C addr: [1 0 0 1 0 0 0 RW]

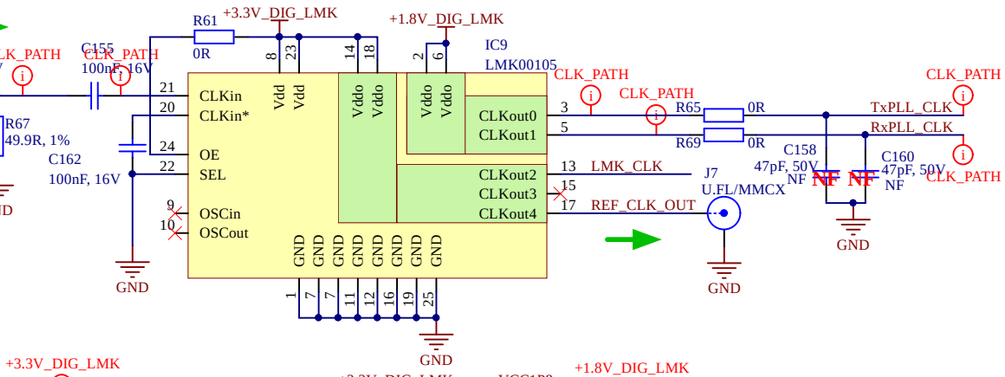


PCB note: place between FPGA and LMS

(VC)TCXO and REF CLK

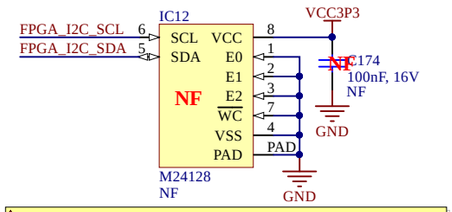


Clock buffer

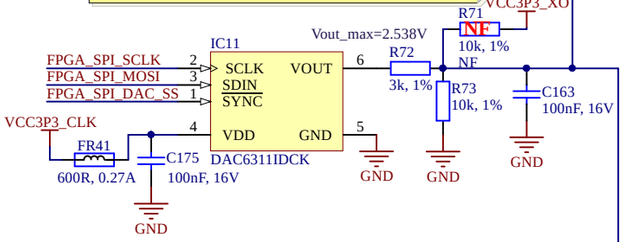


I2C EEPROM

I2C Address: [1 0 1 0 0 0 0 RW]

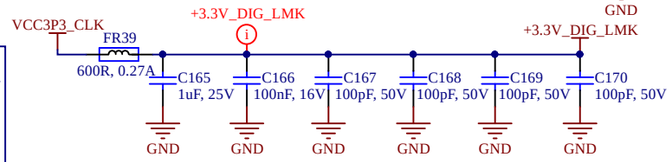


XO DAC (10 bit)

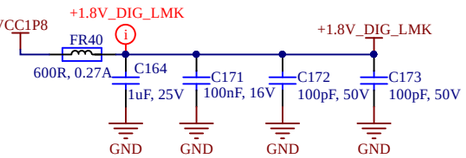


IC10 alternatives: DAC5311IDCK (8 bit) or DAC5311IDCK (12 bit). Compatible FPGA GW must be used.

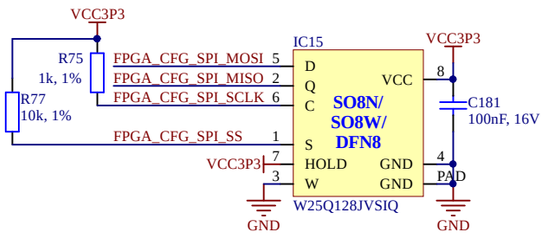
PCB note: Place 100pF close to each Vdd and Vddo pins.



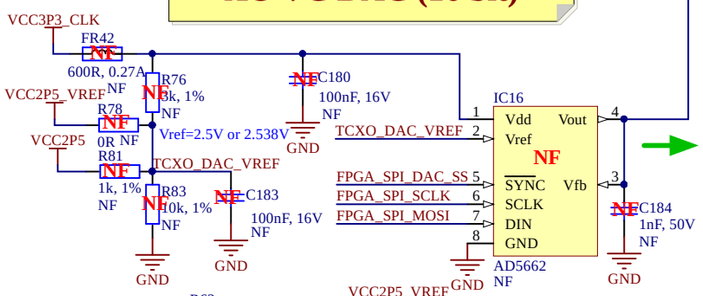
PCB note: Place 100pF close to each Vddo pins.



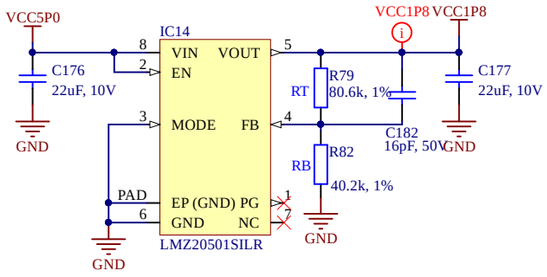
FPGA configuration Flash



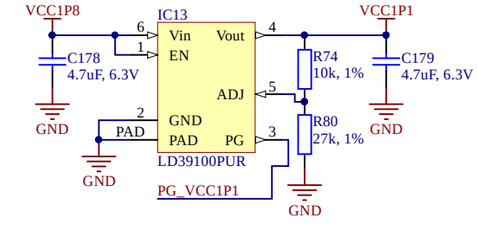
XO VC DAC (16 bit)



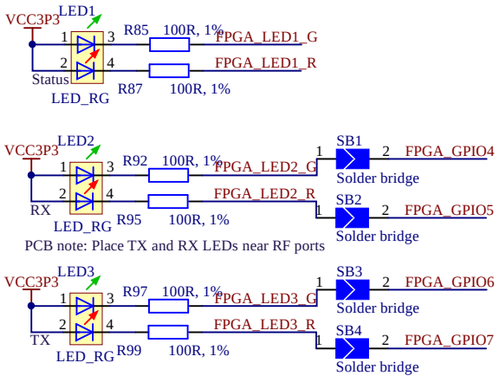
Switching regulators



Linear regulators



FPGA LEDs (Red/Green)

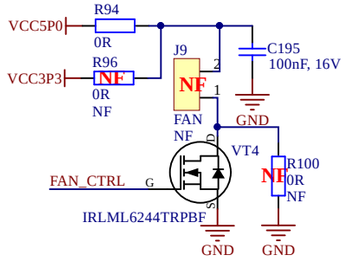


PCB note: Place TX and RX LEDs near RF ports

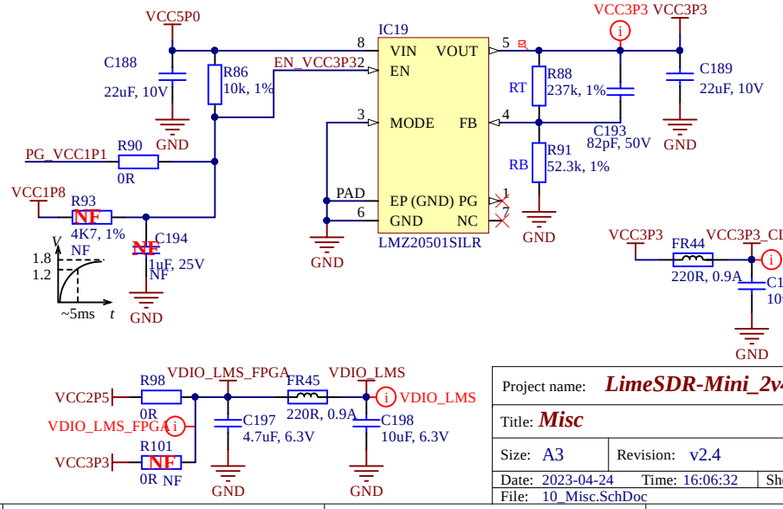
FPGA_GPIO[7:4] are shared with TX and RX LEDs. Remove solder (jumper resistors) from solder bridges to disconnect LEDs from GPIOs lines.

Possible to use fixed and adjustable shunt voltage references. Fit proper resistors accordingly.

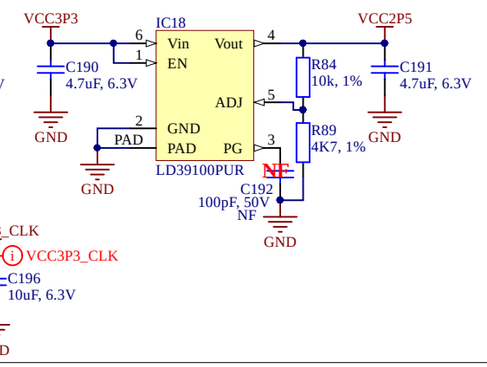
FAN control



Switching regulators



Linear regulators



Project name:	LimeSDR-Mini_2v4.PrjPcb
Title:	Misc
Size:	A3
Revision:	v2.4
Date:	2023-04-24
Time:	16:06:32
Sheet	10 of 10
File:	10_Misc.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

Lime microsystems