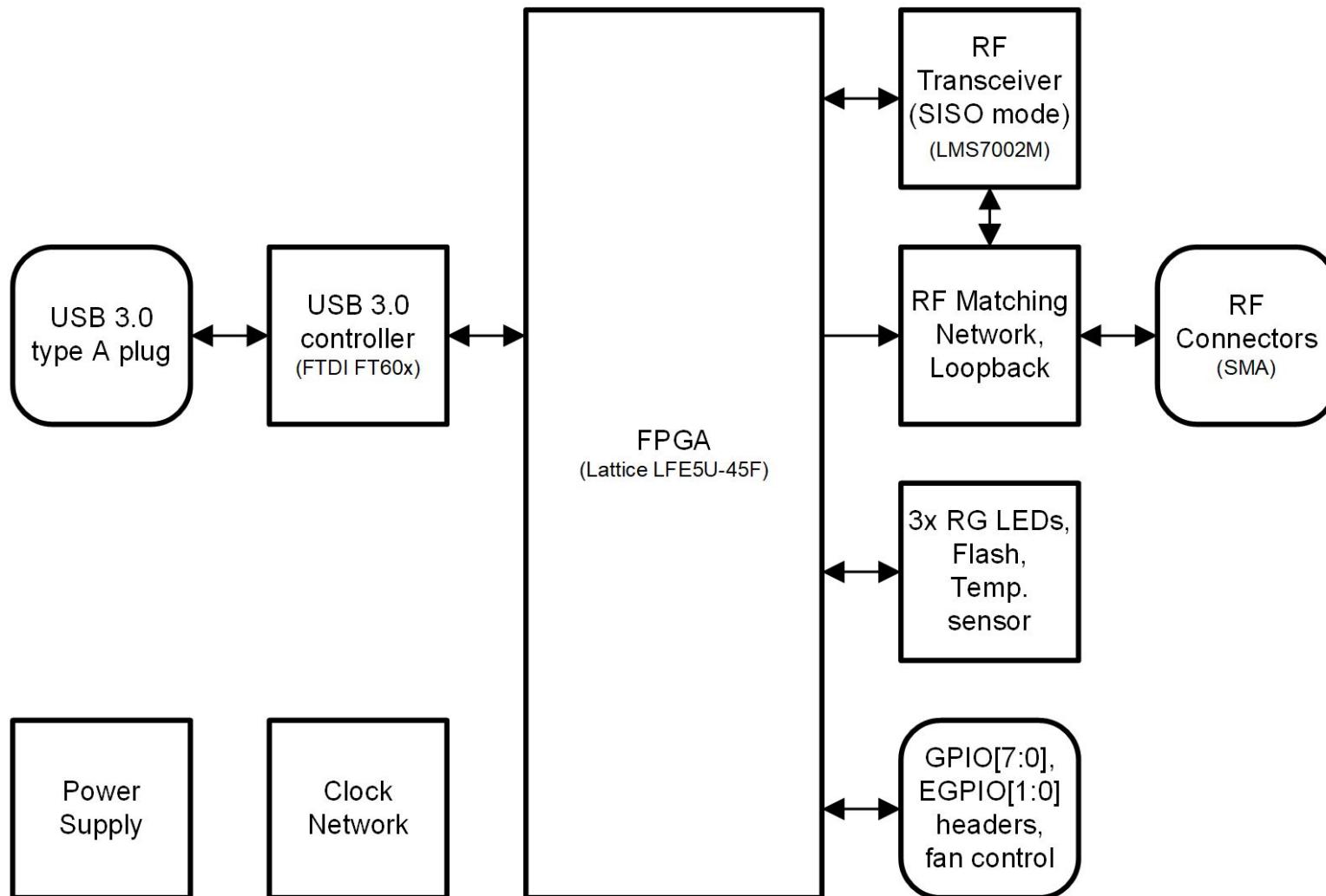


## Block diagram



Project name: **LimeSDR-Mini\_2v2.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v2.2**

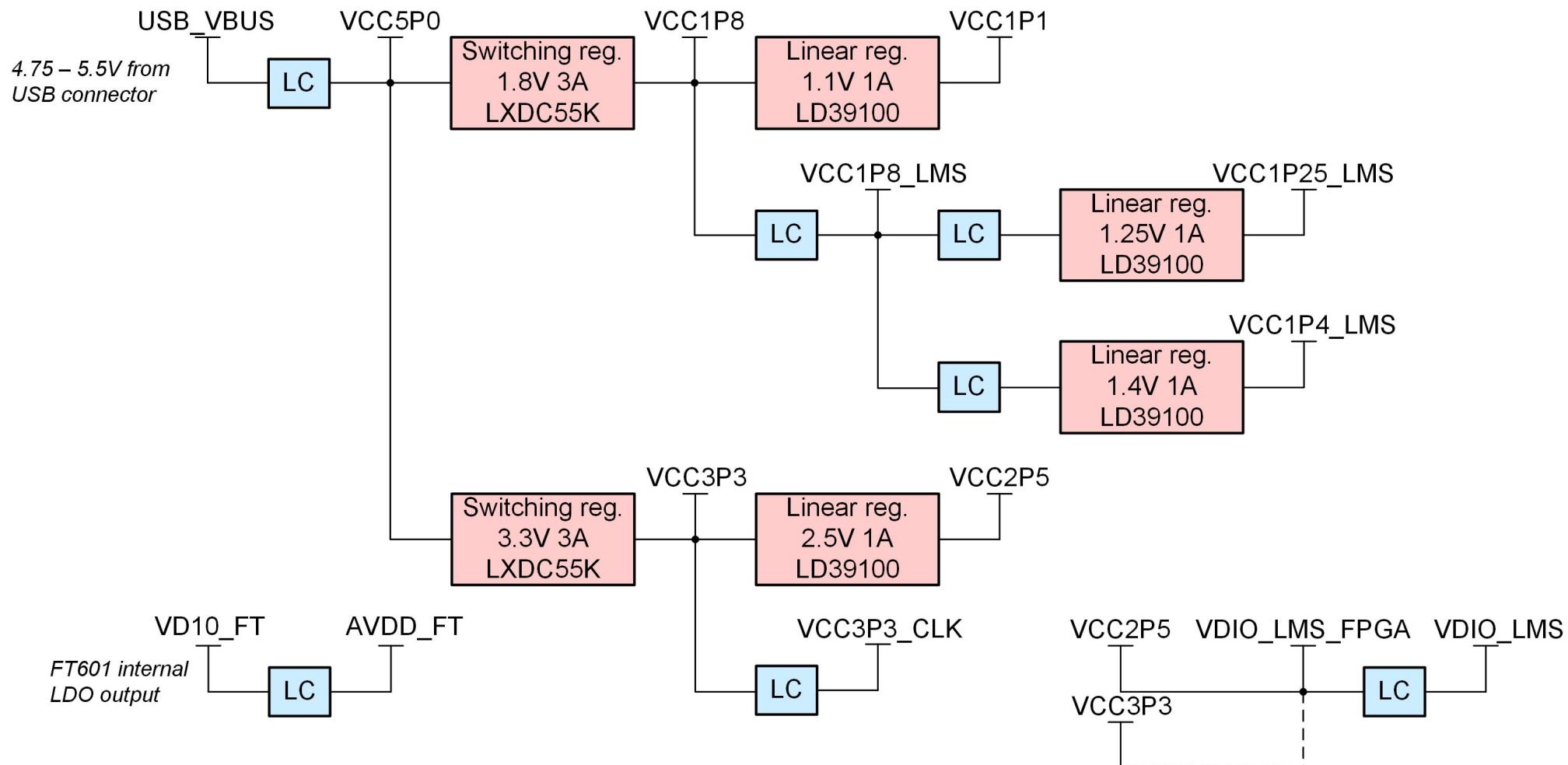
Date: **2022-11-15** Time: **12:52:51** Sheet **1** of **10**

File: **01\_Block\_Diagram.SchDoc**

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Surrey  
United Kingdom



## Power diagram



Project name: **LimeSDR-Mini\_2v2.Pcb**

Title: **Power diagram**

Size: **A4** Revision: **v2.2**

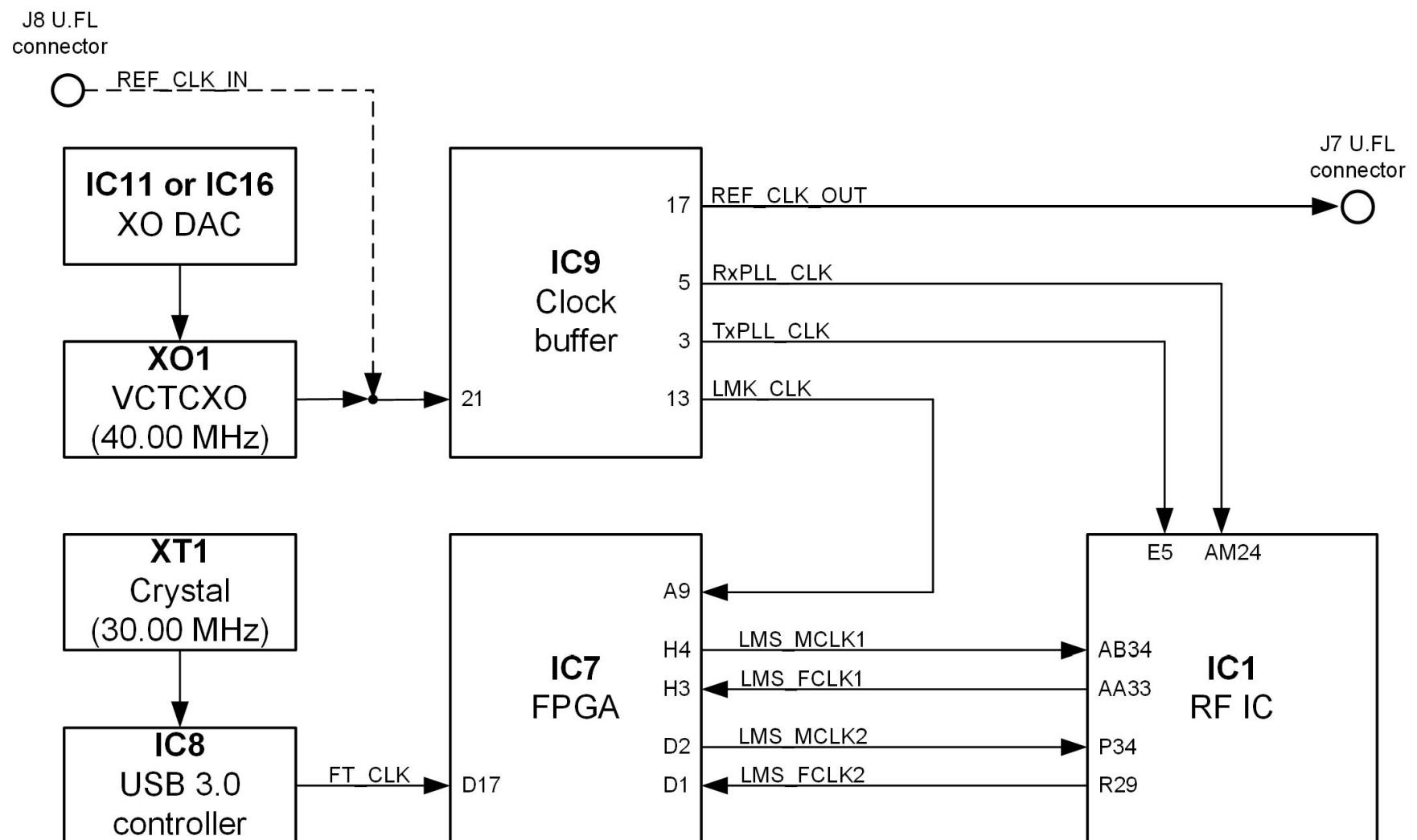
Date: **2022-11-15** Time: **12:52:53** Sheet **2** of **10**

File: **02\_Power\_Diagram.SchDoc**

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Surrey  
United Kingdom



## Clock diagram

Project name: *LimeSDR-Mini\_2v2.PrbPcb*Title: *Clock diagram*Size: **A4** Revision: **v2.2**

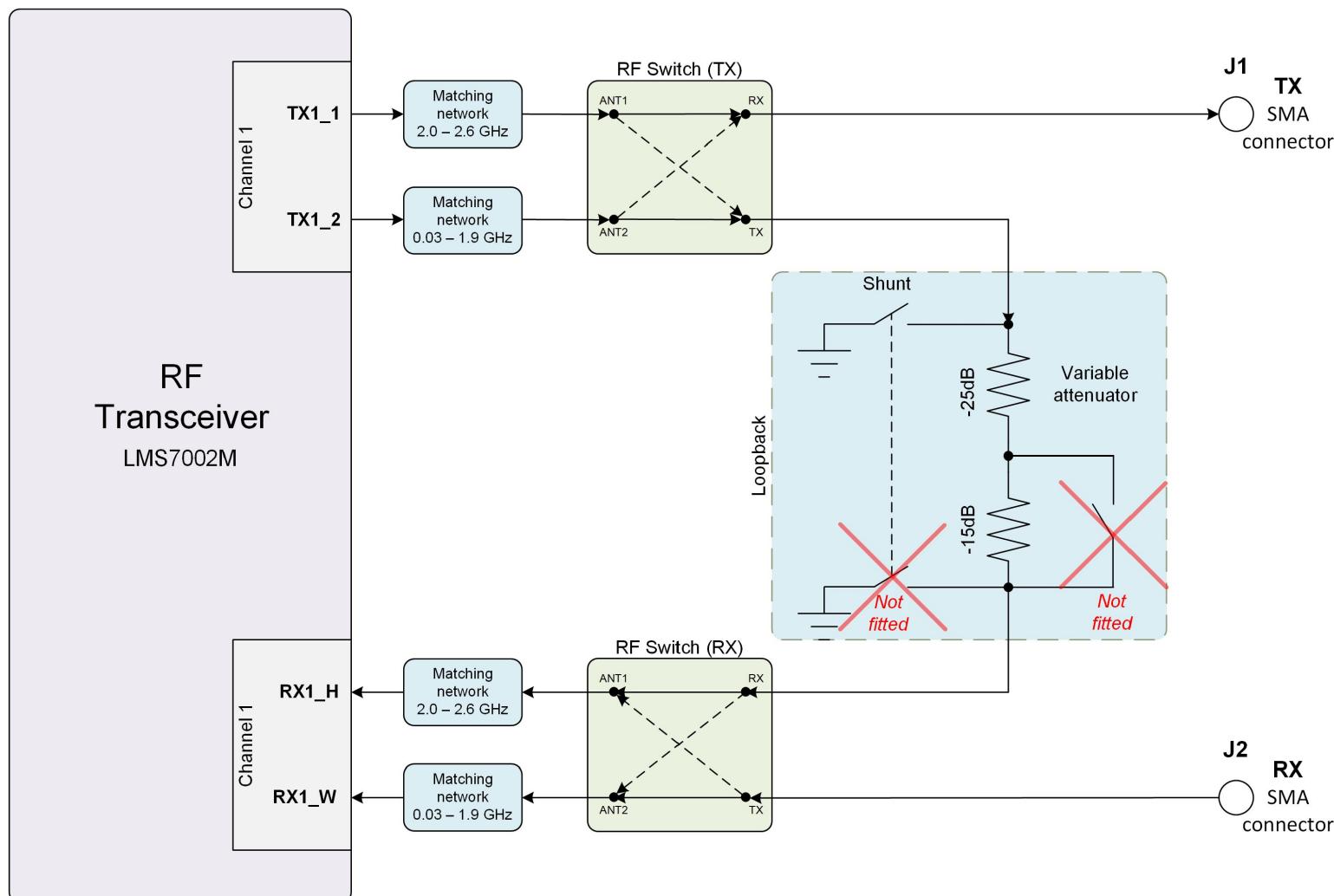
Date: 2022-11-15 Time: 12:52:55 Sheet 3 of 10

File: 03\_Clock\_Diagram.SchDoc

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United Kingdom



## RF diagram



Project name: **LimeSDR-Mini\_2v2.PrjPcb**

Title: **RF diagram**

Size: **A4** Revision: **v2.2**

Date: **2022-11-15** Time: **12:52:58** Sheet **4** of **10**

File: **04\_RF\_Diagram.SchDoc**

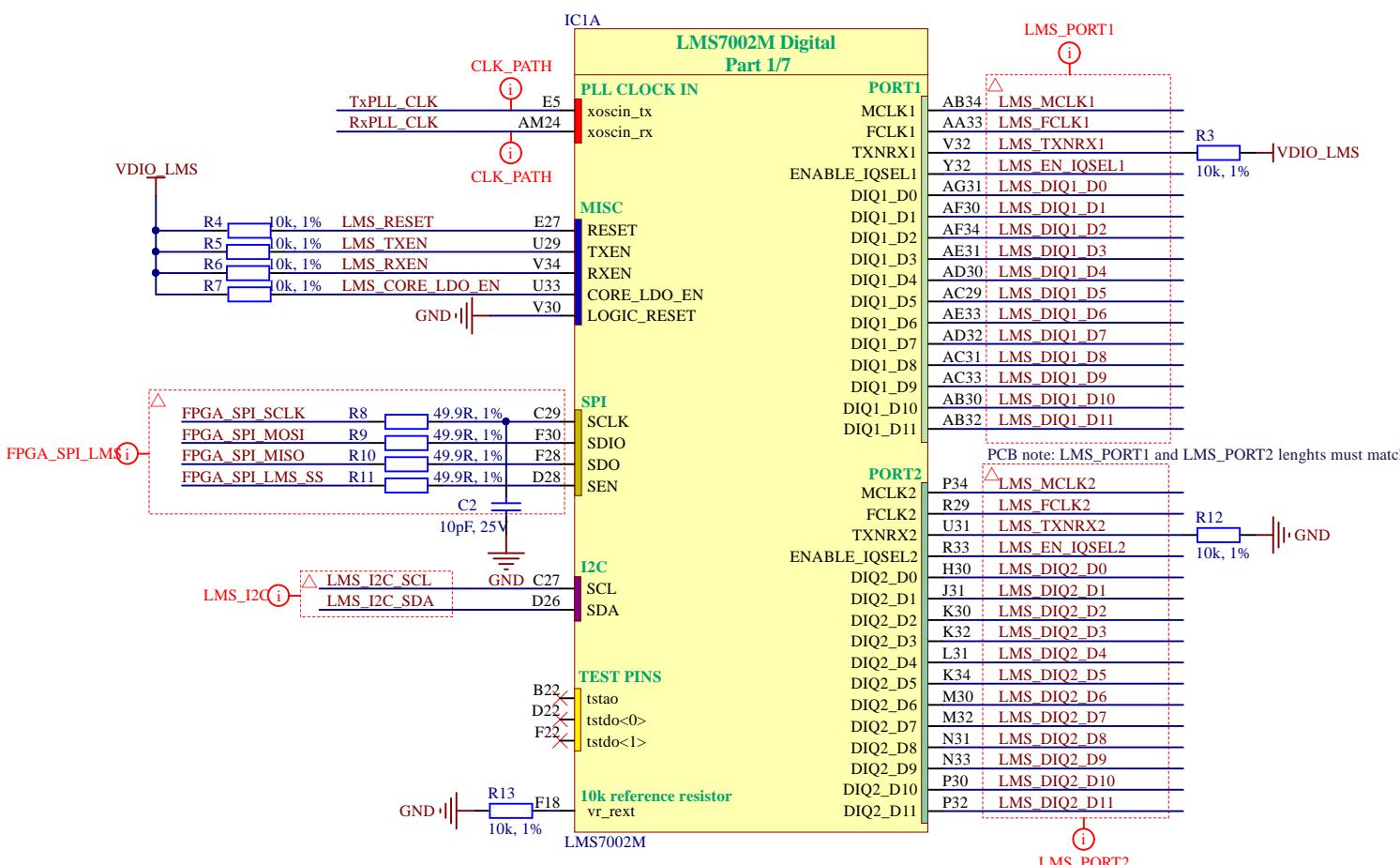
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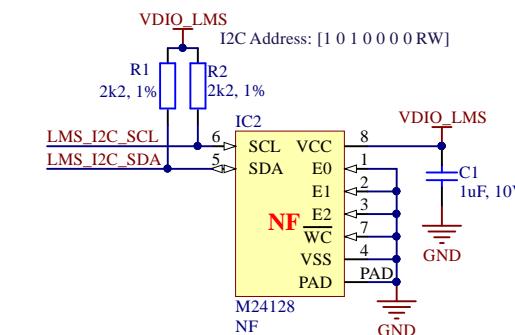
NF elements on sheet: IC2, MECH1-MECH5, MECH11-MECH15, MEHC16-MECH21, FAN1  
Number of NF elements on sheet: 18

## LMS7002M misc

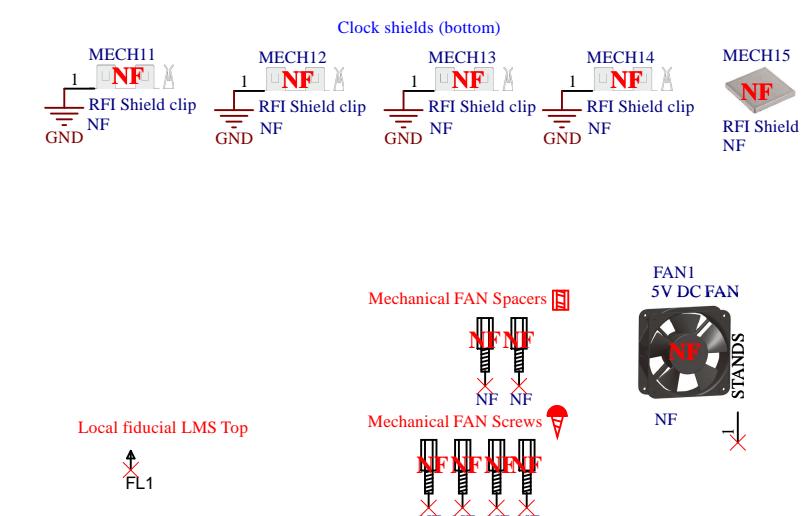
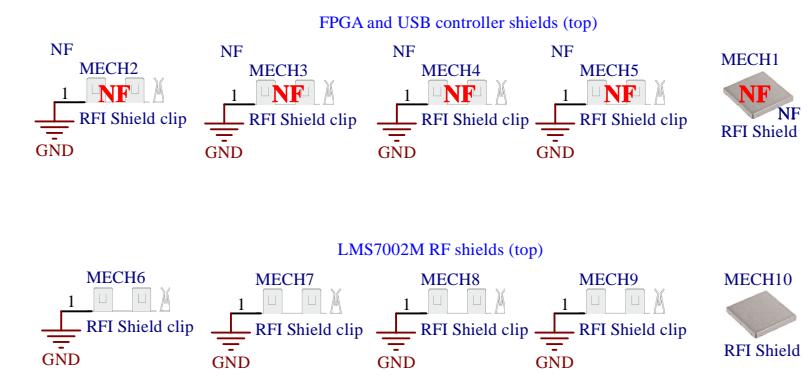
### LMS7002M digital circuit



### LMS EEPROM



### Mechanical components



Project name: LimeSDR-Mini\_2v2.PjrPcb

Title: LMS7002M misc

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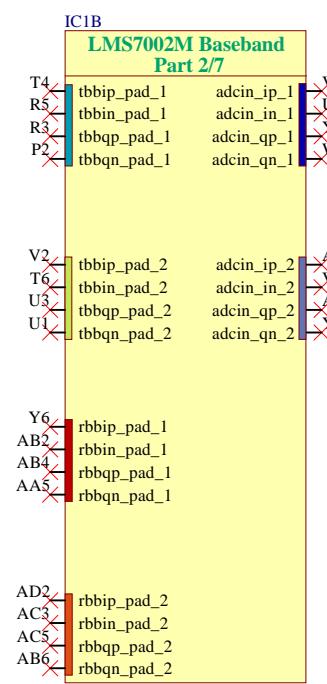


Size: A3 Revision: v2.2

Date: 2022-11-15 Time: 12:53:01 Sheet 5 of 10

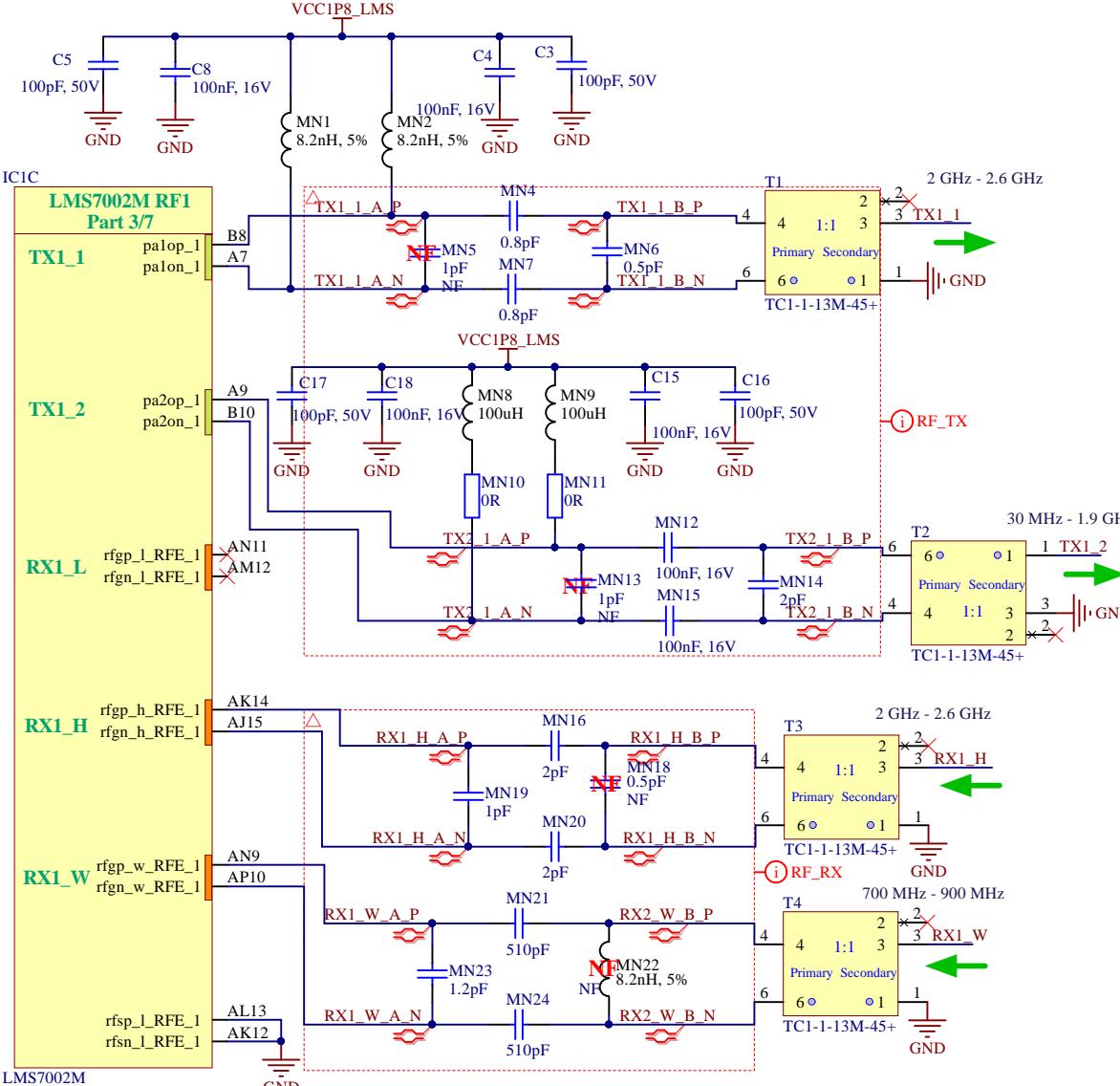
File: 05\_LMS7002M\_Misc.SchDoc

### Baseband external IO

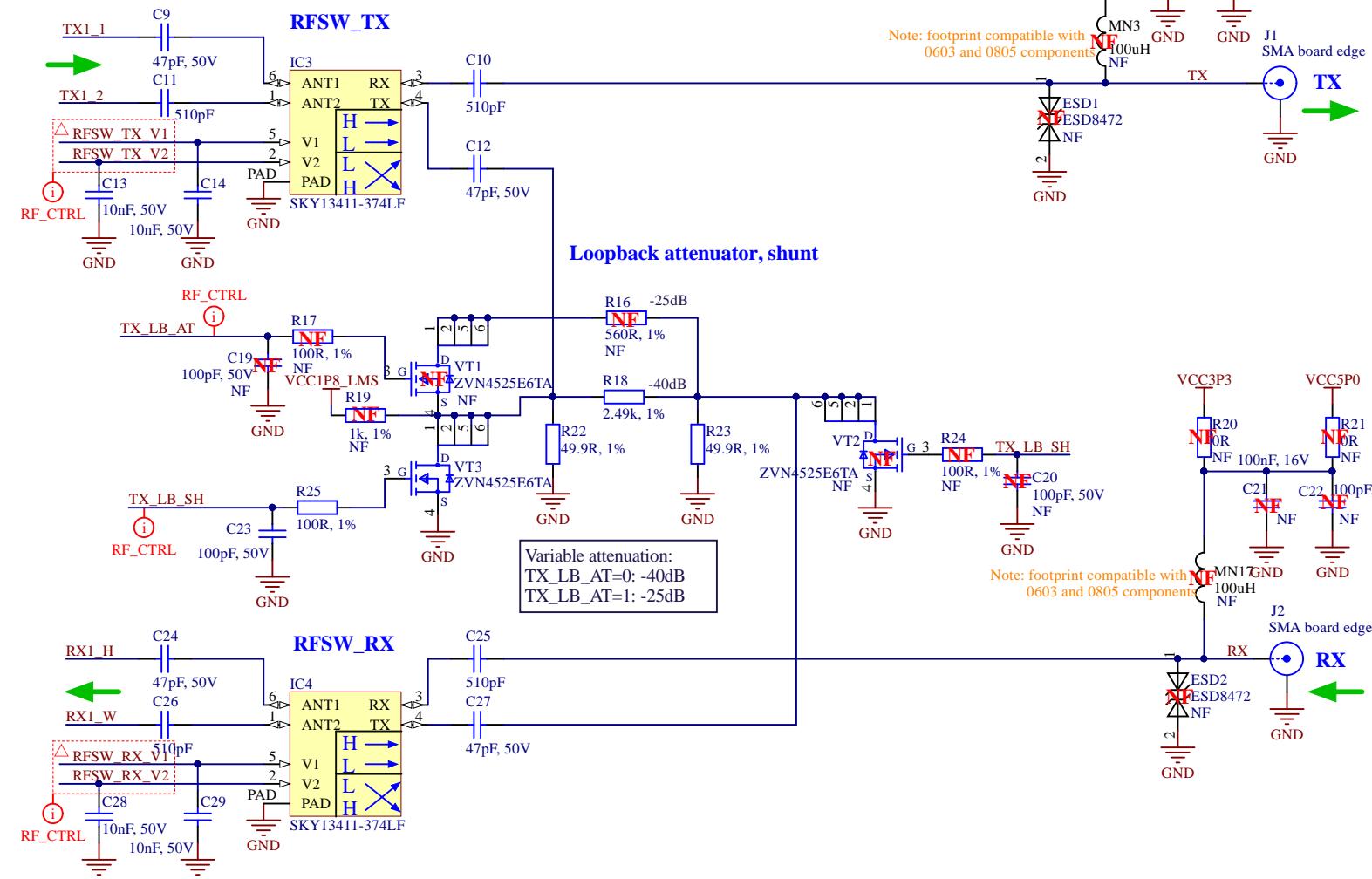


## LMS7002M RF circuits

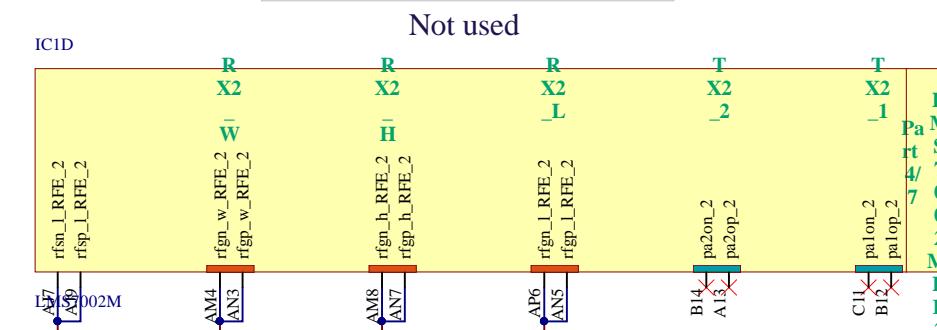
### LMS RF Channel 1



### RF control



### LMS RF Channel 2



### RF truth table

RFSW_TX	RFSW_RX	J1 (TX)	J2 (RX)	Loopback
V1 H	V2 L	H	L	TX1_1 → RX1_H
V1 L	V2 H	L	H	TX1_2 → RX1_H
V1 H	V2 L	H	H	TX1_1 → RX1_W
V1 L	V2 H	L	H	TX1_2 → RX1_H

### RFSW (SKY13411) truth table

V1	V2	ANT1 (pin 6) → TX (pin 4)	ANT1 (pin 6) → RX (pin 3)	ANT2 (pin 1) → TX (pin 4)	ANT2 (pin 1) → RX (pin 3)
H	L	ISOLATION	ON	ON	ISOLATION
L	H	ON	ISOLATION	ISOLATION	ON

Project name: LimeSDR-Mini\_2v2.PnjPcb

Title: LMS7002M RF

Size: A3 Revision: v2.2

Date: 2022-11-15 Time: 12:53:04 Sheet 6 of 10

File: 06\_LMS7002M\_RF.SchDoc

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# LMS7002M power supply circuit

NF elements on sheet: R26, C71, C84  
Number of NF elements on sheet: 3

IC1F

## LMS7002M Power Part 6/7

### 1.25V Digital

DIGPRVDD1  
DIGPRVDD1  
DIGPRVDD1  
DIGPRVDD1

DVDD\_SXR  
DVDD\_SXT  
VDD12\_DIG  
VDD\_SPI\_BUF  
DVDD\_CGEN

### 1.25V Analog

VDD12\_TXBUF  
VDD12O\_VCO\_SXT  
VDD12\_VCO\_SXT  
VDD\_CP\_SXT  
VDD\_TBB  
VDD12\_TIA\_RFE  
VDD12\_LNA\_RFE  
VDD\_CP\_SXR  
VDD\_DIV\_SXR  
VDD12\_VCO\_SXR  
VDD12\_RXBUF  
VDD\_AFE  
VDD\_CP\_CGEN  
VDD\_DIV\_CGEN  
VDD\_TPAD\_TRF  
VDD\_TLOBUF\_TRF  
VDDO\_TLOBUF\_TRF

### 1.25V-1.4V Analog

VDD\_DIV\_SXT  
VDDO\_DIV\_SXT  
VDD\_MXLOBUF\_RFE

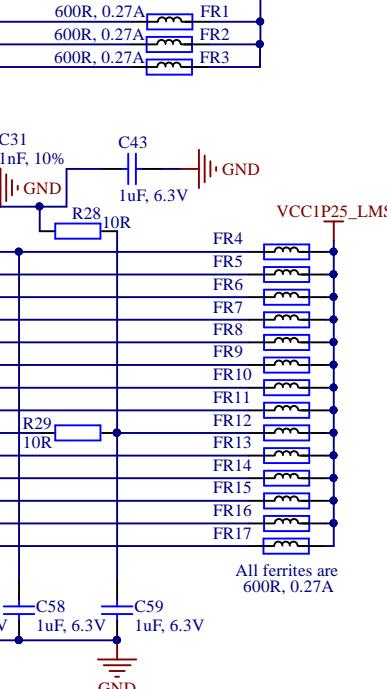
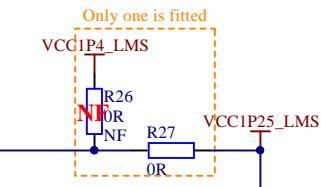
### 1.4V Analog

VDD14\_RBB  
VDD14\_TIA\_RFE  
VDD14\_LNA\_RFE  
VDD14\_VCO\_CGEN

LMS7002M

A

A



All ferrites are 600R, 0.27A

IC1E

## LMS7002M Power Part 5/7

### 1.8V Digital

VDD18\_DIG

### 1.8V-3.3V Digital

DIGPRVDD2  
DIGPRVDD2  
DIGPRVDD2  
DIGPRVDD2  
DIGPRPOC

### 1.8V Analog

VDD18\_VCO\_SXT  
VDD18\_LDO\_TX  
VDD18\_TIA\_RFE  
VDD18\_LDO\_RX  
VDD18\_SXR  
VDD18\_VCO\_SXR  
VDD18\_BIAS  
VDD18\_TRF  
VDD18\_VCO\_CGEN

LMS7002M

D

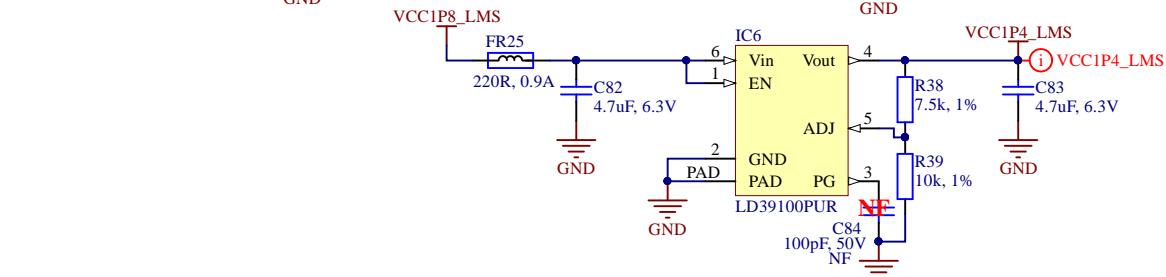
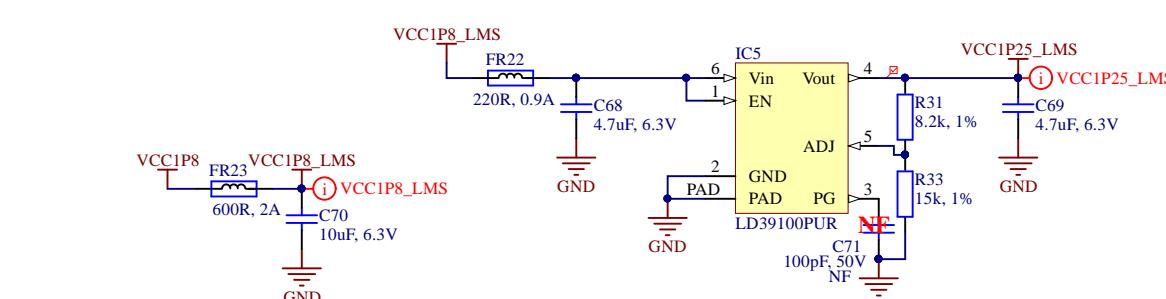
D

### 1.8V-3.3V Analog

VDD18\_TXBUF  
VDD18\_RXBUF

LMS7002M

C93 1uF, 6.3V  
C94 1uF, 6.3V



Project name: LimeSDR-Mini\_2v2.PnjPcb

Title: LMS7002M power

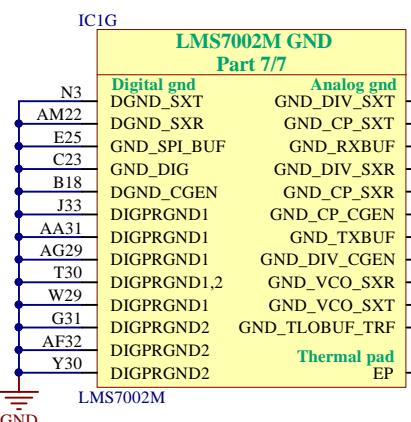
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United Kingdom



Size: A3 Revision: v2.2

Date: 2022-11-15 Time: 12:53:07 Sheet 7 of 10

File: 07\_LMS7002M\_Power.SchDoc

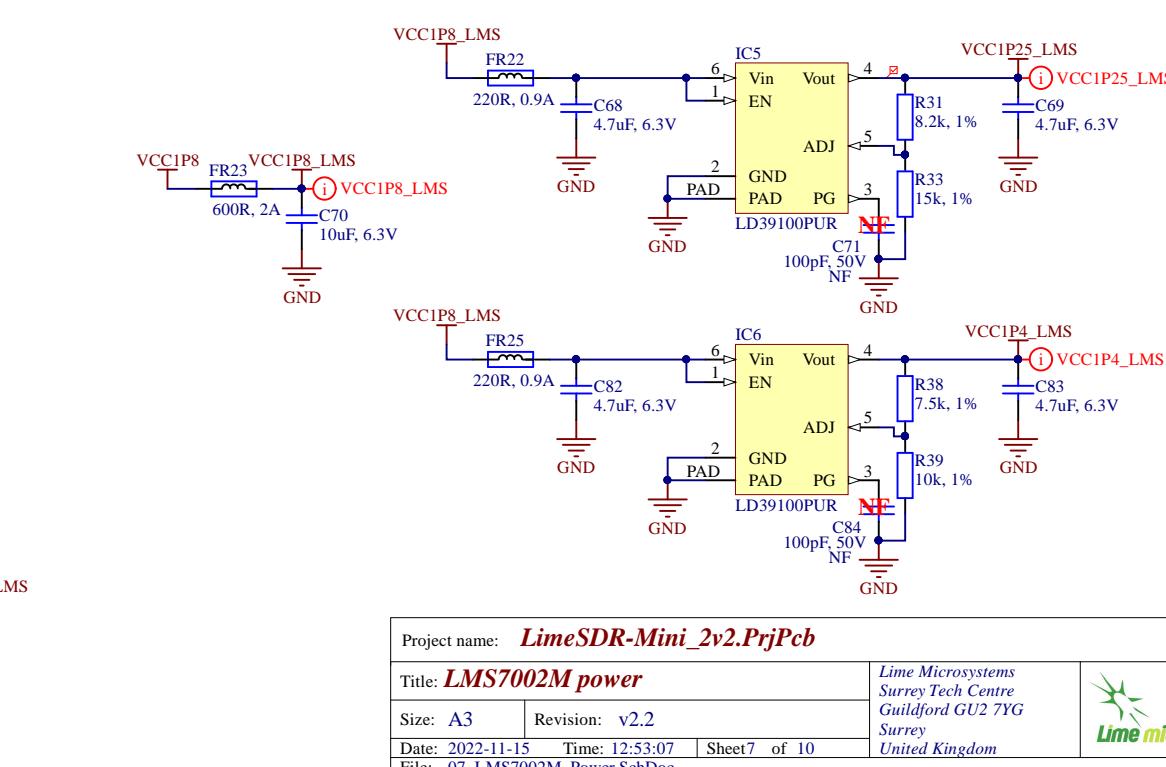


LMS7002M

GND GND

EP EP

# Linear regulators



1

2

3

4

5

6

7

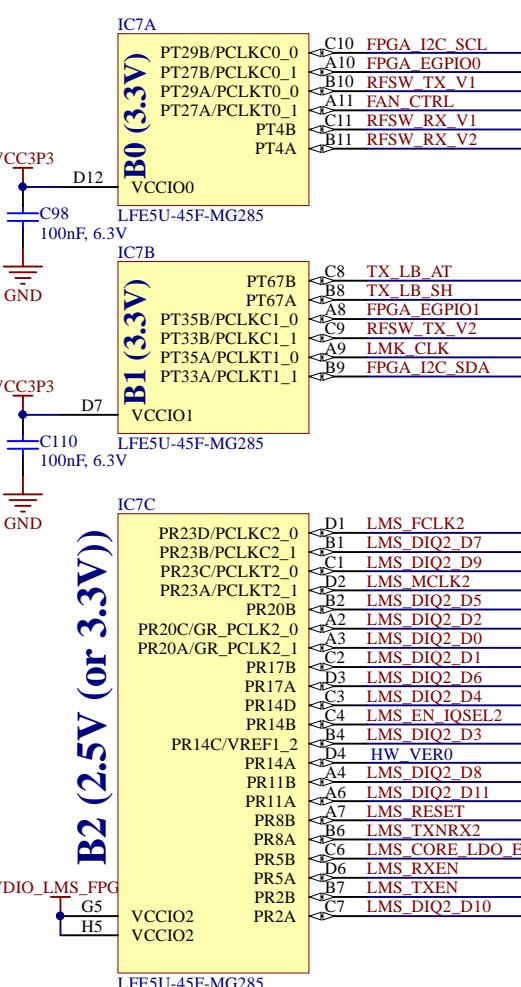
8

## FPGA Banks

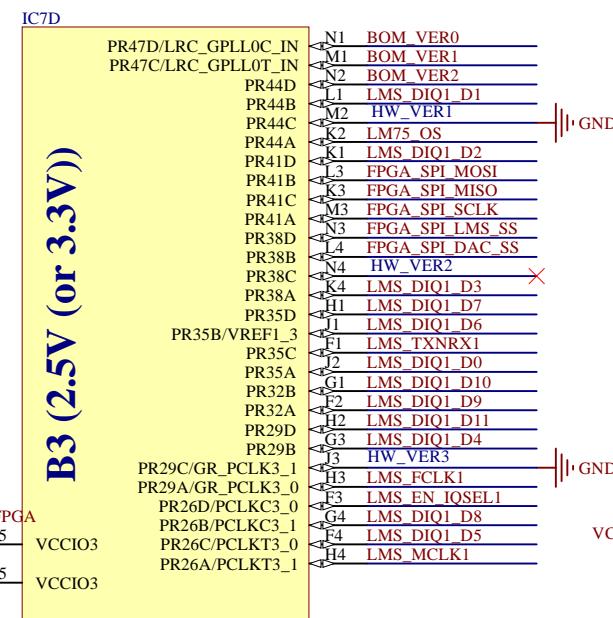
By default LFE5U-45F-xxMG285 is fitted and the schematic symbol represents LFE5U-25F pins. LFE5U-45F and LFE5U-85F parts are footprint and pin compatible with LFE5U-25F with small nuances. For example VCCIO0 bank C10 pin has different function:

LFE5U-25F: C10 pin is PT29B/PCLKC0\_0  
LFE5U-45F: C10 pin is PT38B/PCLKC0\_0  
LFE5U-85F: C10 pin is PT65B/PCLKC0\_0

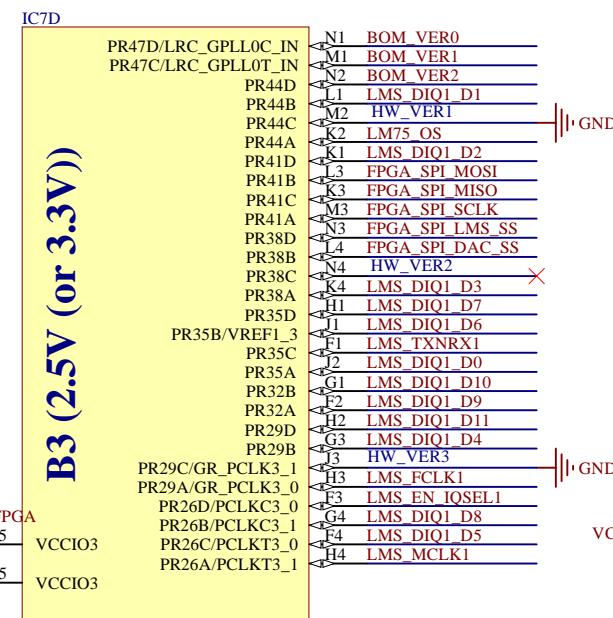
Therefore if a different to the default FPGA is used, one should look up the proper function note for each pin.  
All power and fixed-function pins are the same for LFE5U-25F, LFE5U-45F, LFE5U-85F parts.



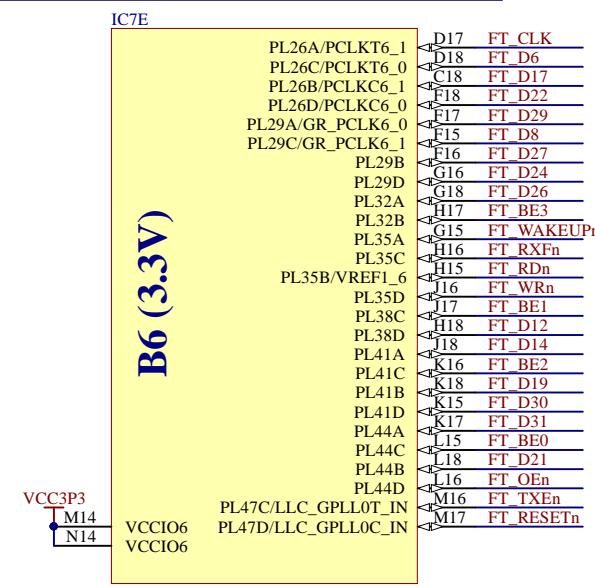
## B2 (2.5V (or 3.3V))



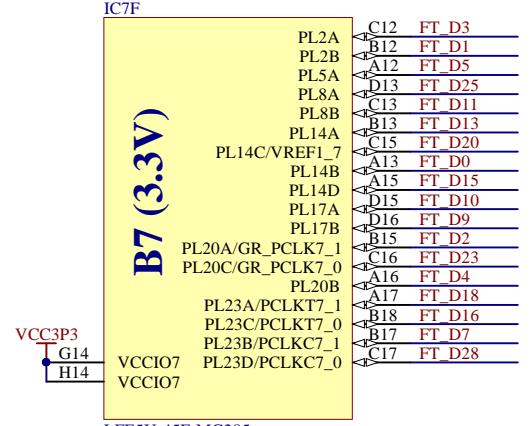
## B3 (2.5V (or 3.3V))



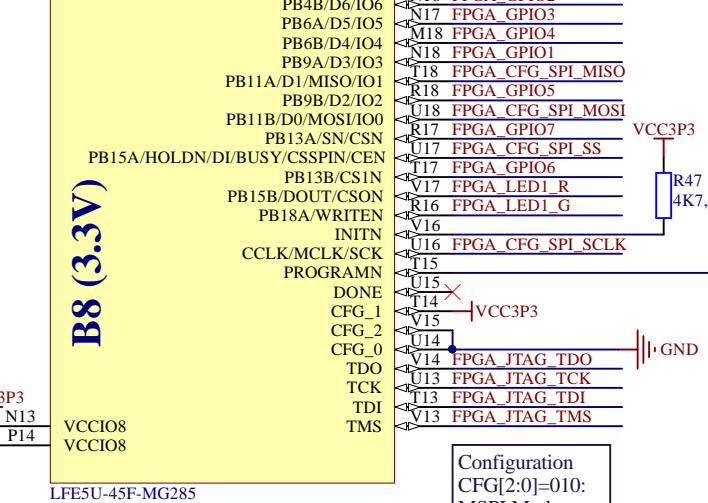
## FPGA



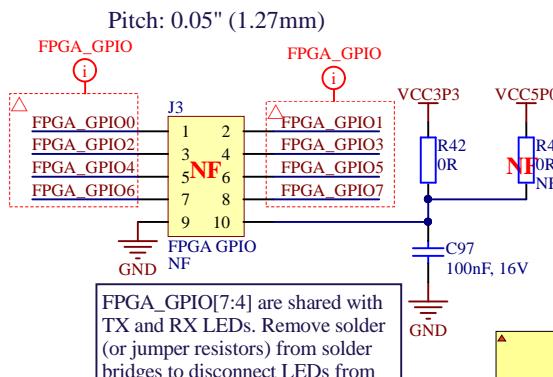
## B7 (3.3V)



## B8 (3.3V)

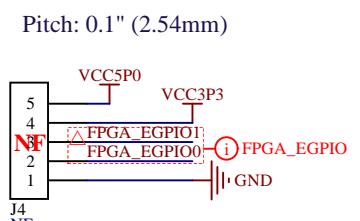


## FPGA GPIO

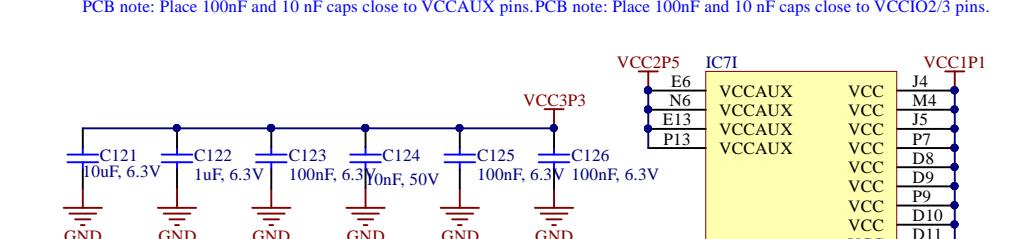
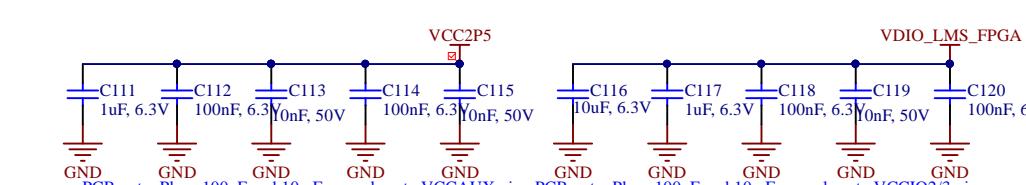
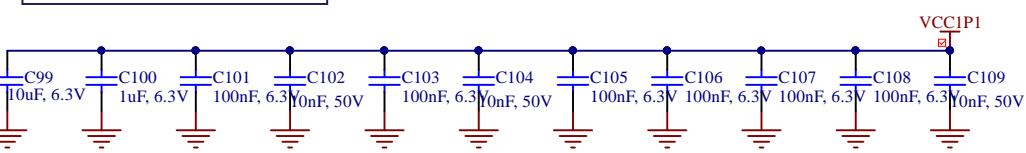


FPGA\_GPIO[7:4] are shared with TX and RX LEDs. Remove solder (or jumper resistors) from solder bridges to disconnect LEDs from GPIOs lines.

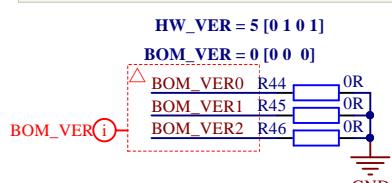
## FPGA GPIO (edge)



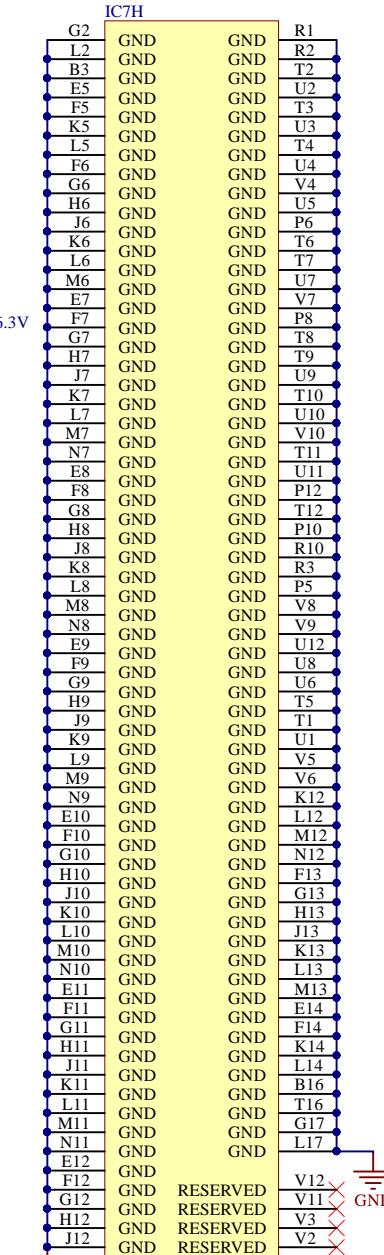
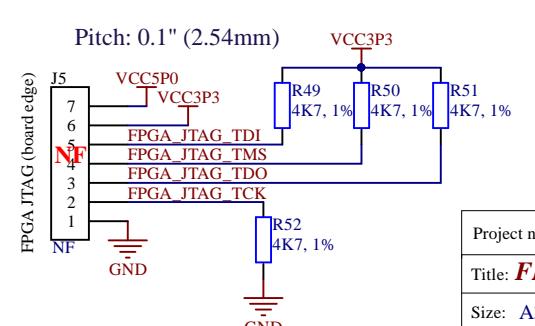
## Decoupling



## HW\_VER & BOM\_VER



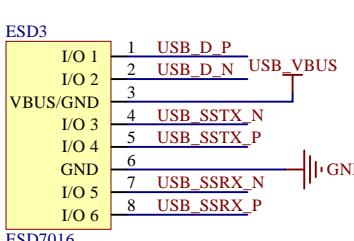
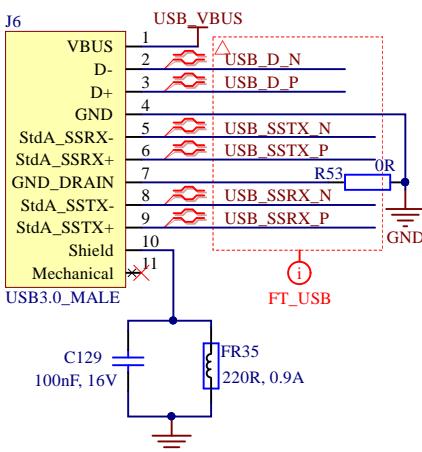
## FPGA JTAG (edge)



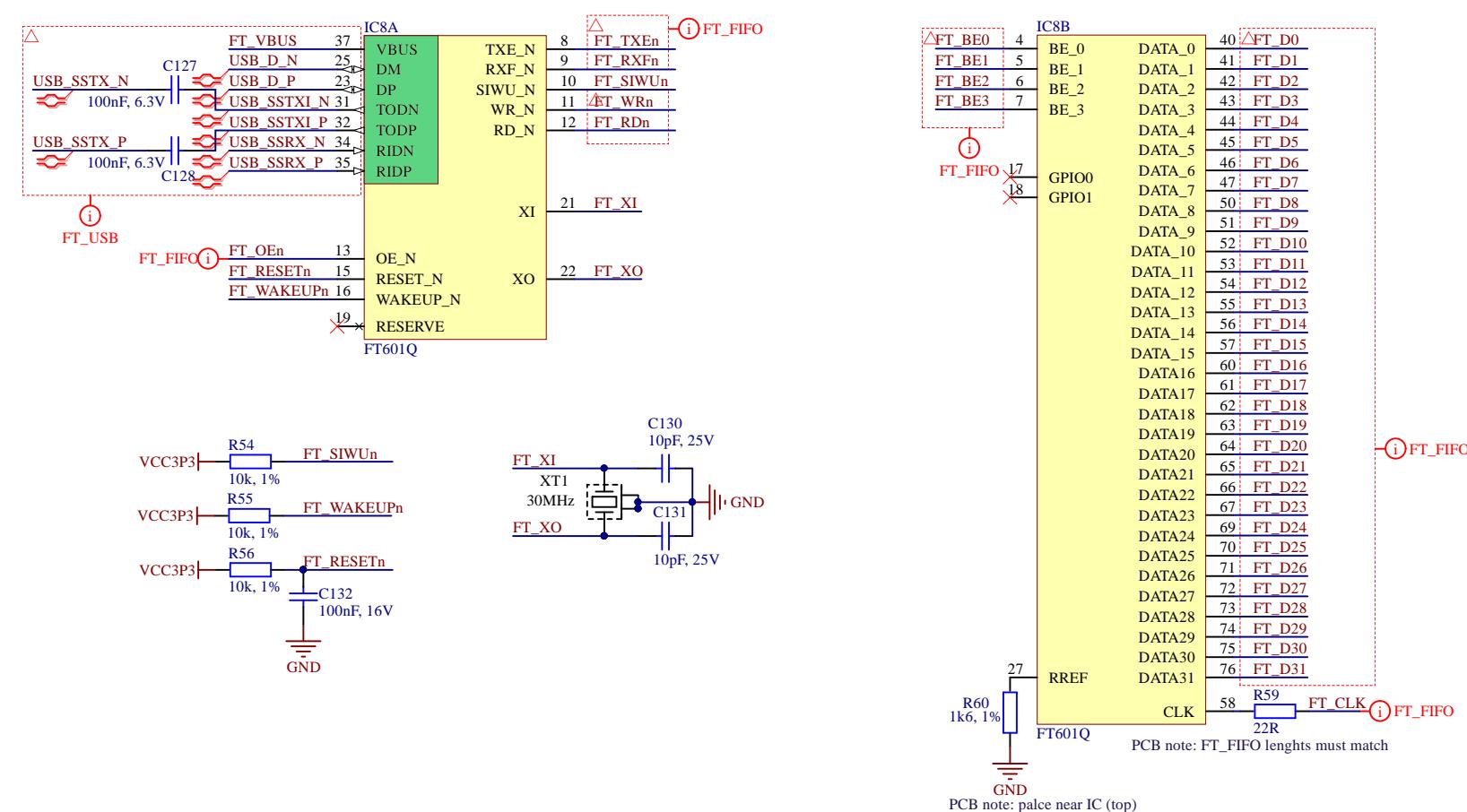
NF elements on sheet: -  
Number of NF elements on sheet: 0

## USB 3.0 to FIFO interface

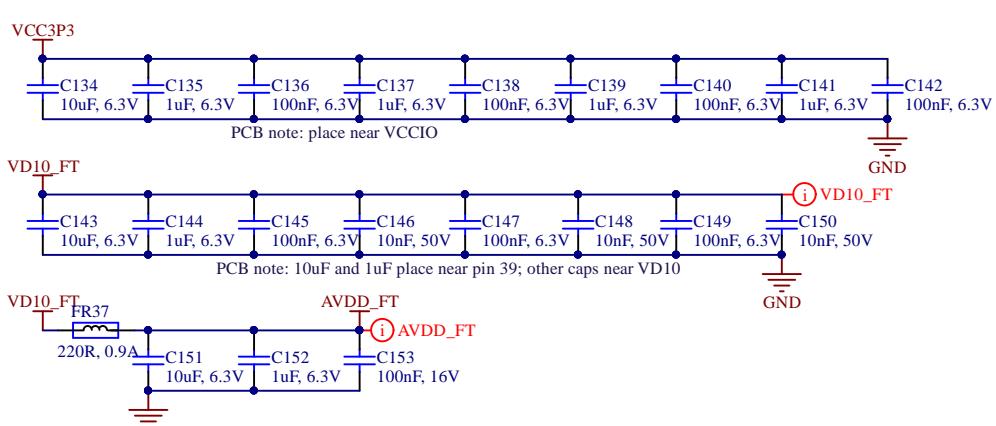
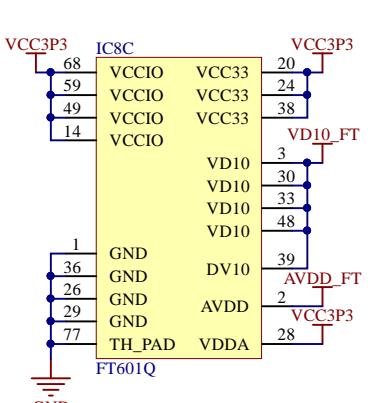
### USB 3.0 type A plug and ESD



### FTDI digital interface



### FTDI Power



Project name: <b>LimeSDR-Mini_2v2.PnjPcb</b>	
Title: <b>USB3.0 device</b>	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: <b>A3</b>	Revision: <b>v2.2</b>
Date: <b>2022-11-15</b>	Time: <b>12:53:14</b>
File: <b>09_USB3_0_FIFO.SchDoc</b>	Sheet <b>9</b> of <b>10</b>

