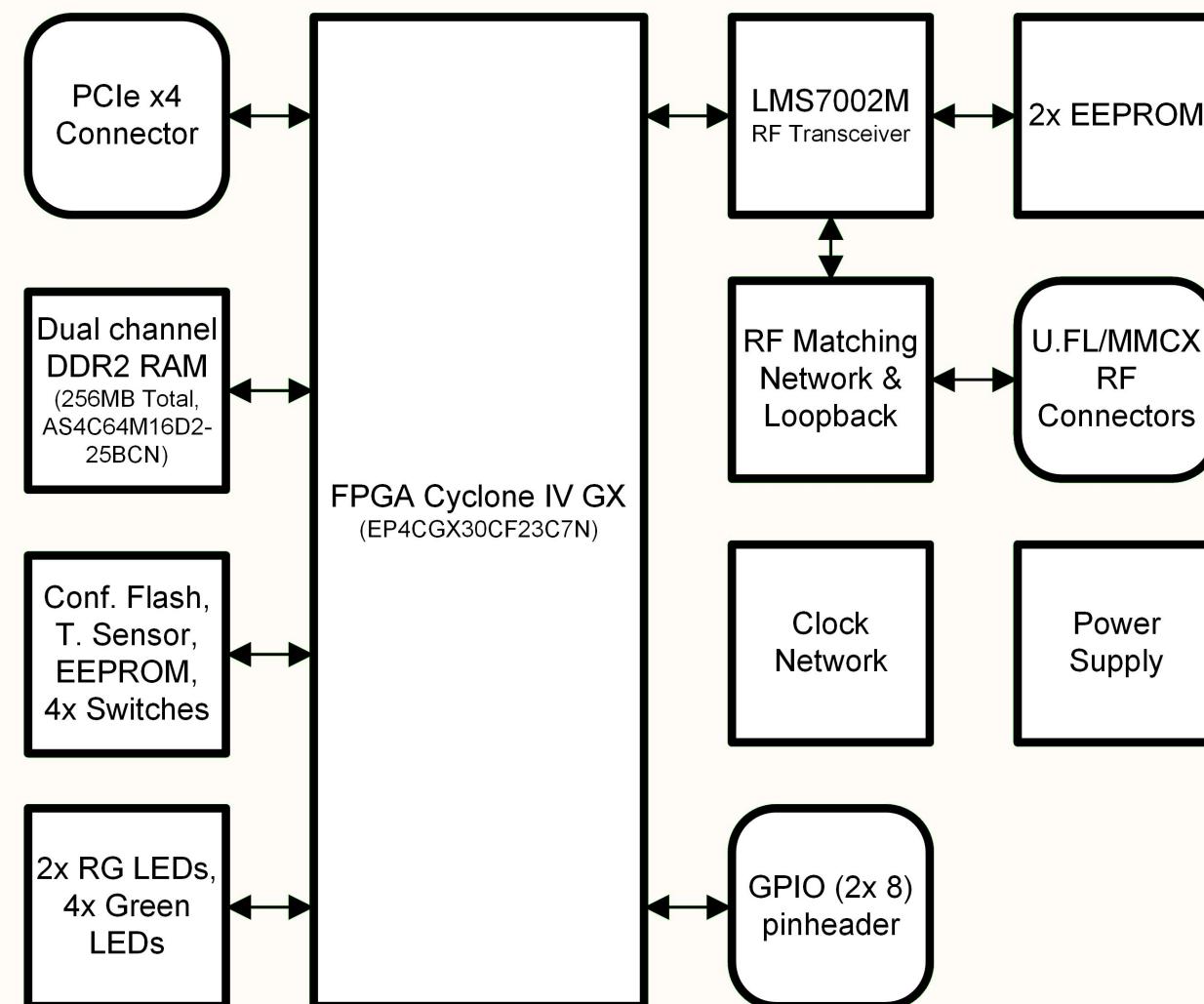


## Block diagram



Project name: **LimeSDR-PCIe\_Inv2.PnjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.2**

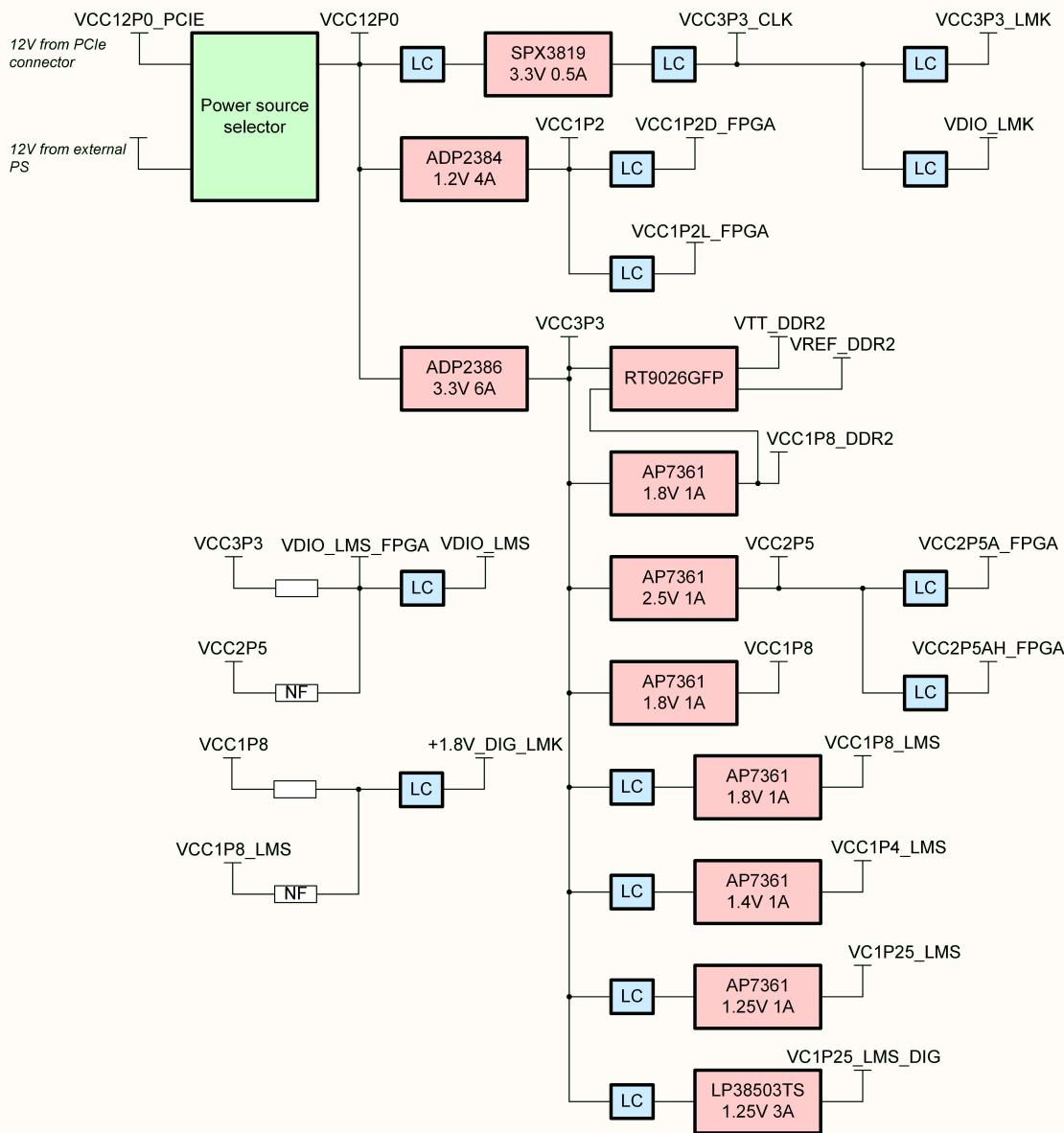
Date: **2017-02-01** Time: **15:49:11** Sheet **1** of **16**

File: **01\_BlockDiagram.SchDoc**

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United Kingdom



## Power diagram



Project name: **LimeSDR-PCIe\_Iv2.PrjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.2**

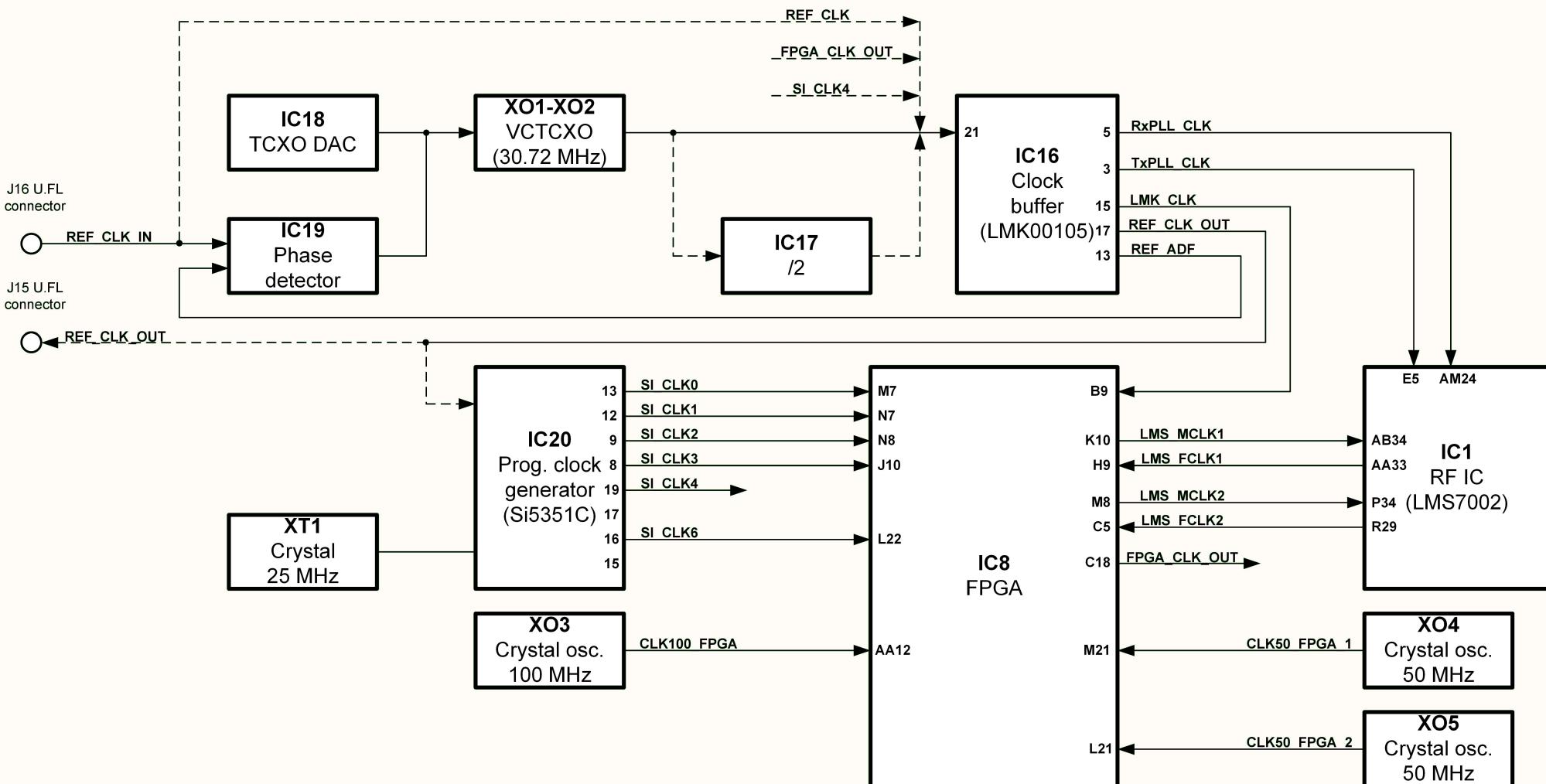
Date: **2017-02-01** Time: **15:49:16** Sheet**2** of **16**

File: **02\_PowerDiagram.SchDoc**

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United Kingdom



## Clock diagram



Project name: *LimeSDR-PCIe\_Rev2.PrjPcb*

Title: *Clock diagram*

Size: *A4* Revision: *v1.2*

Date: 2017-02-01 Time: 15:49:25 Sheet 3 of 16

File: 03\_ClockDiagram.SchDoc

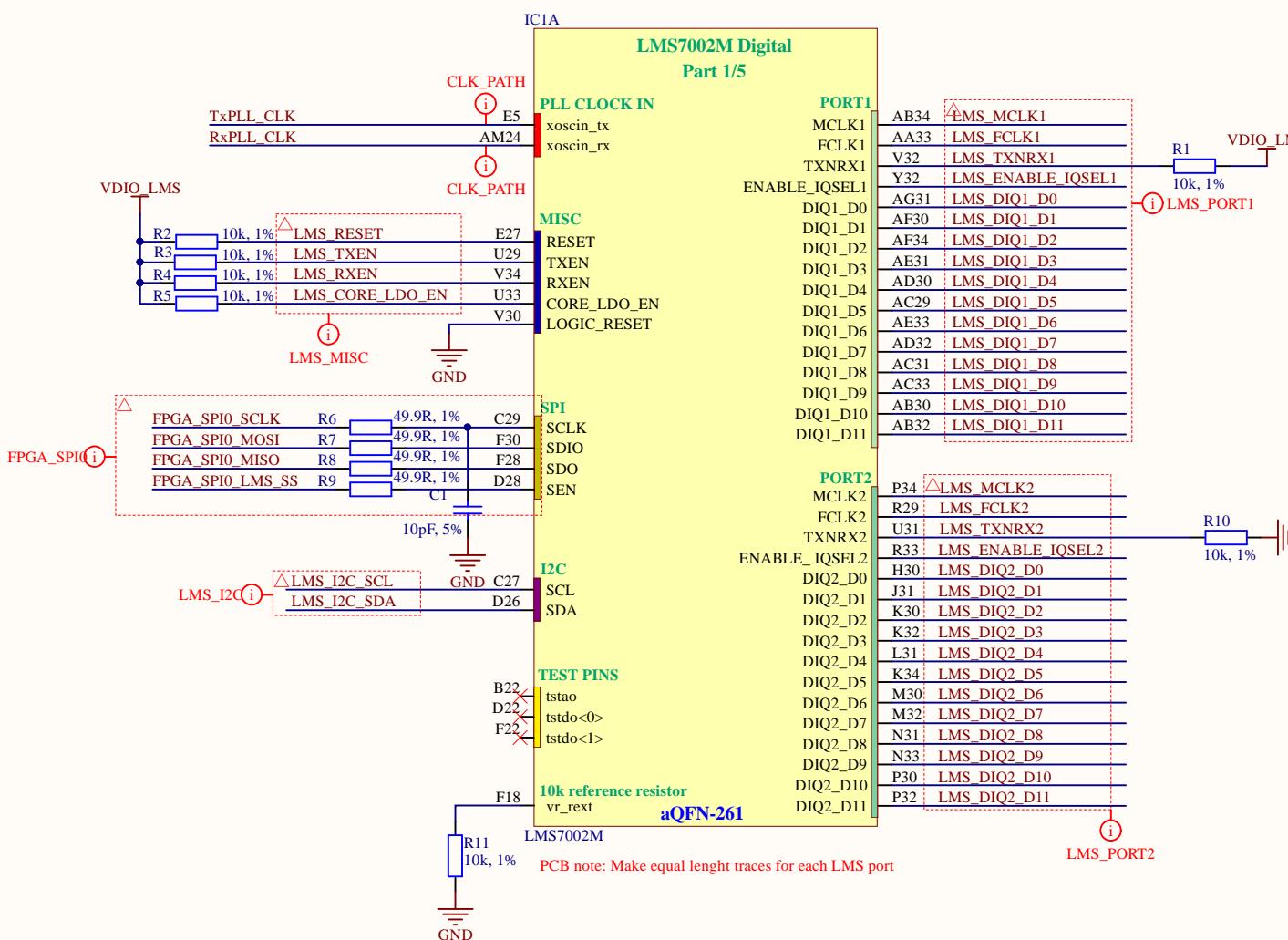
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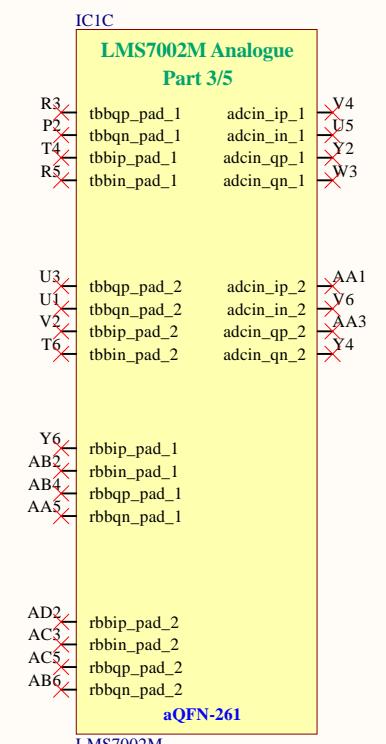
NF elements on sheet: -  
Number of NF elements on sheet: 0

## LMS7002M misc

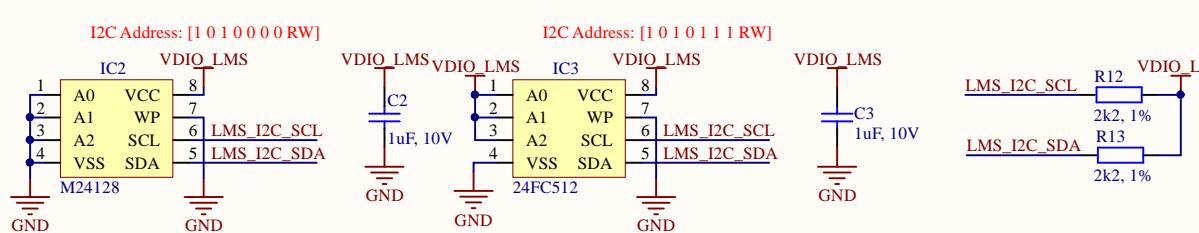
### Digital interfaces



### Baseband external IO



### LMS EEPROMs



Project name: LimeSDR-PCIe\_1v2.PrjPcb

Title: LMS7002M misc

Size: A3 Revision: v1.2

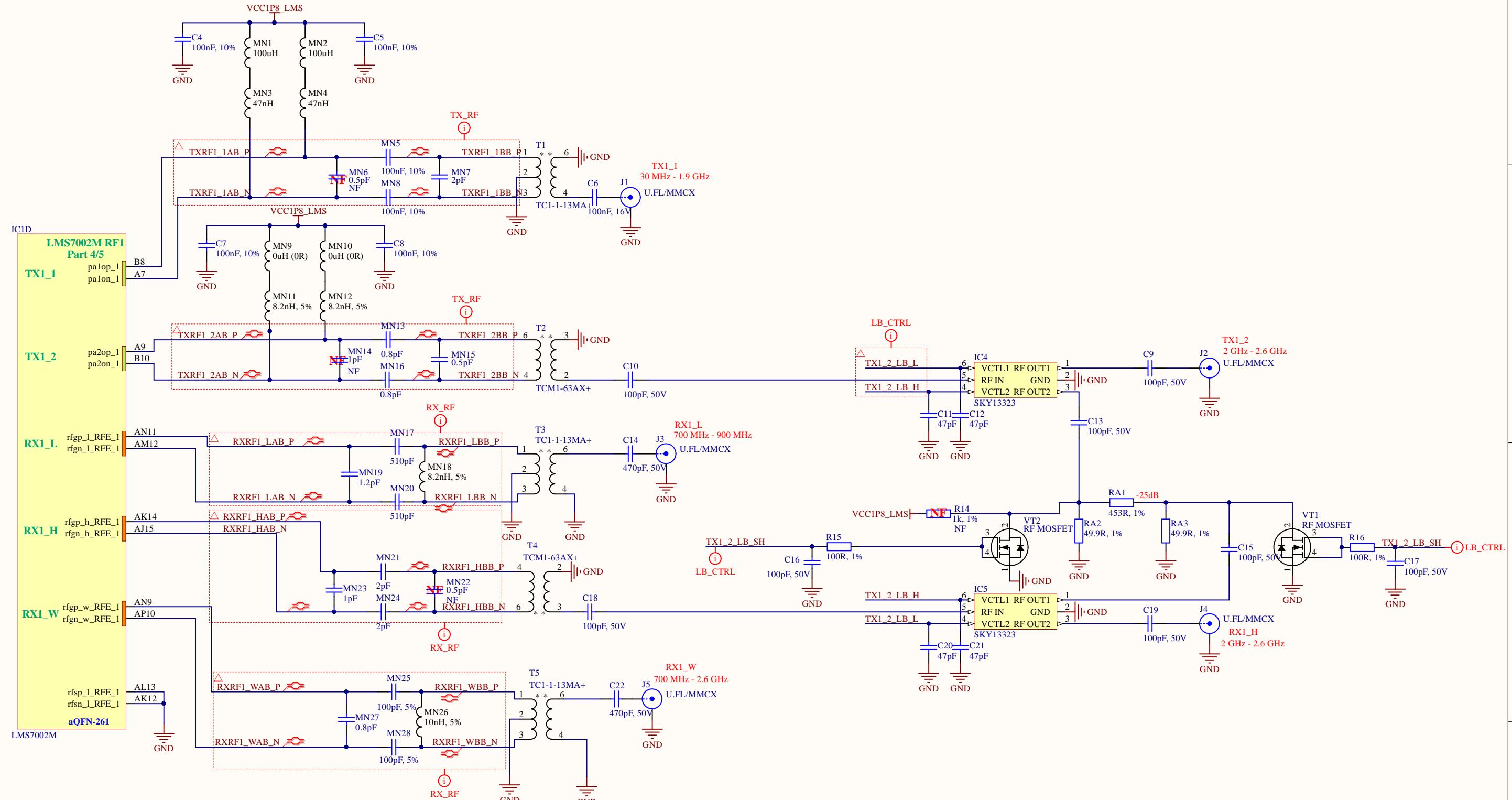
Date: 2017-02-01 Time: 15:49:33 Sheet 4 of 16

File: 04\_LMS7002M\_Misc.SchDoc



NF elements on sheet: MN6, MN14, MN22, R14  
Number of NF elements on sheet: 4

## LMS7002M RF1 circuits



Project name: LimeSDR-PCIe\_1v2.PrbPcb

Title: LMS7002M RF

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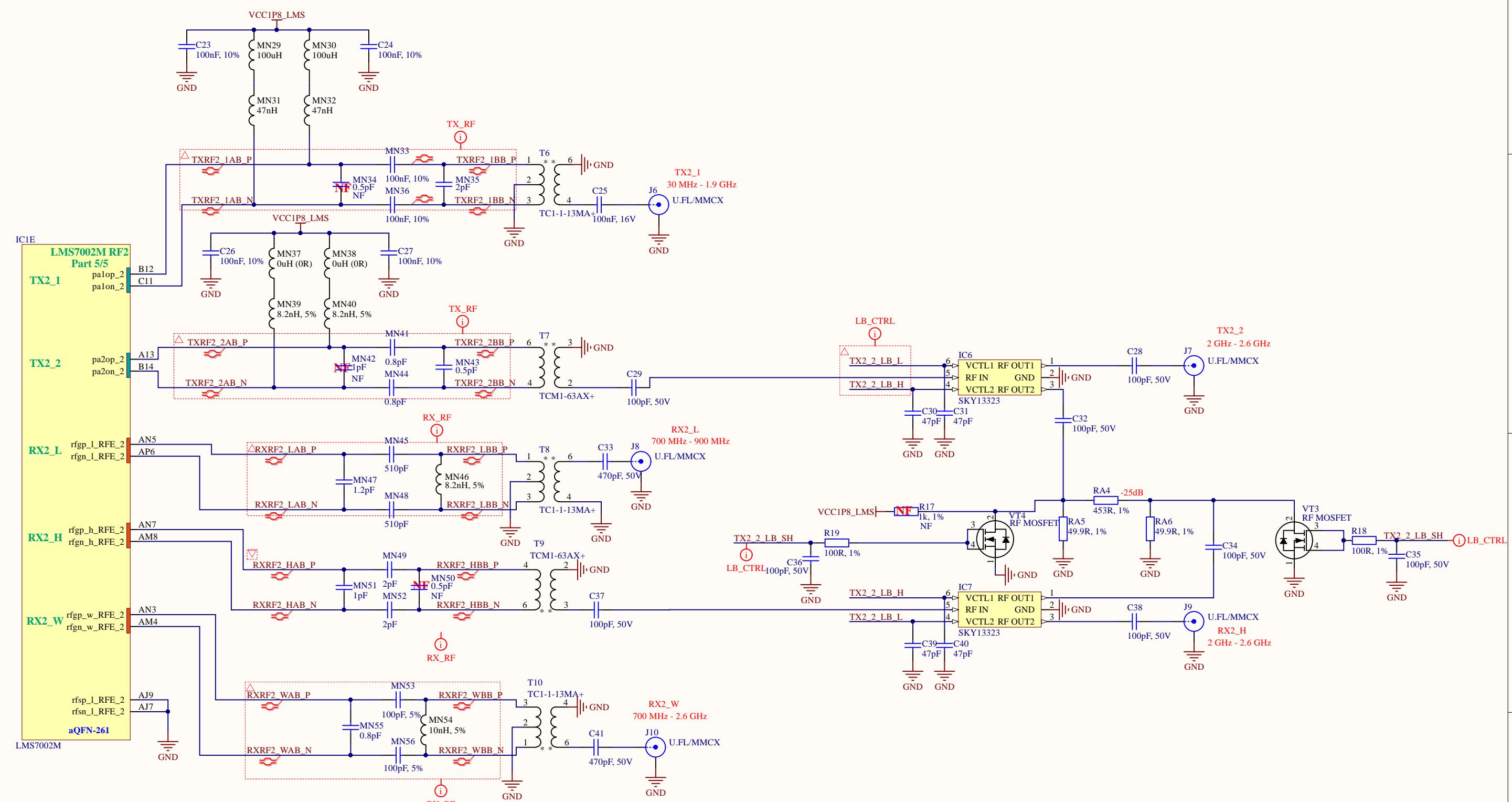
Size: A3 Revision: v1.2

Date: 2017-02-01 Time: 15:49:35 Sheet 5 of 16

File: 05\_LMS7002M\_RF1.SchDoc

NF elements on sheet: MN34, MN42, MN50, R17  
Number of NF elements on sheet: 4

## LMS7002M RF2 circuits



Project name: **LimeSDR-PCIe\_1v2.PnjPcb**

Title: **LMS7002M RF**

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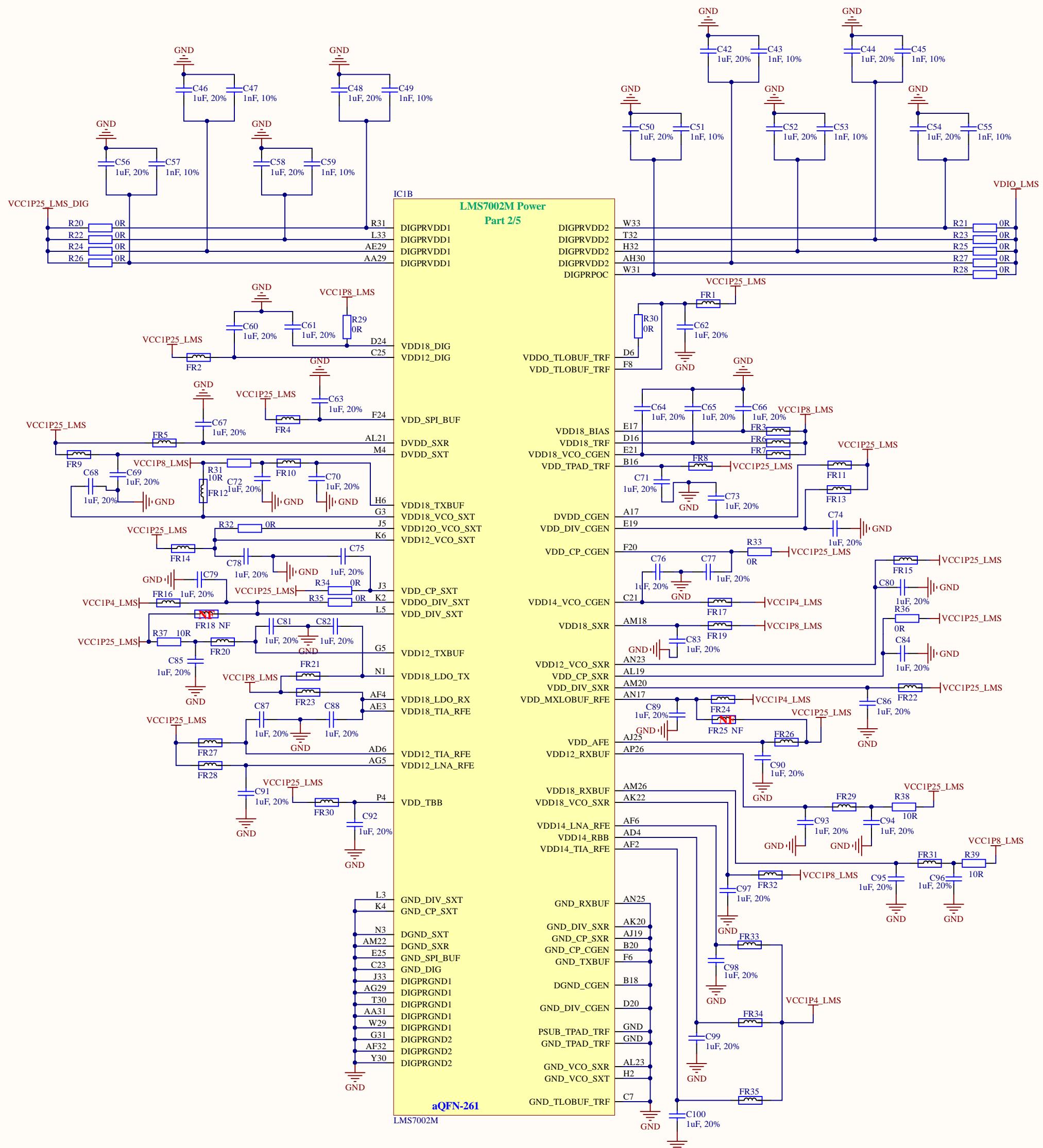
Size: **A3** Revision: **v1.2**

Date: **2017-02-01** Time: **15:49:38** Sheet**6** of **16**

File: **06\_LMS7002M\_RF2.SchDoc**

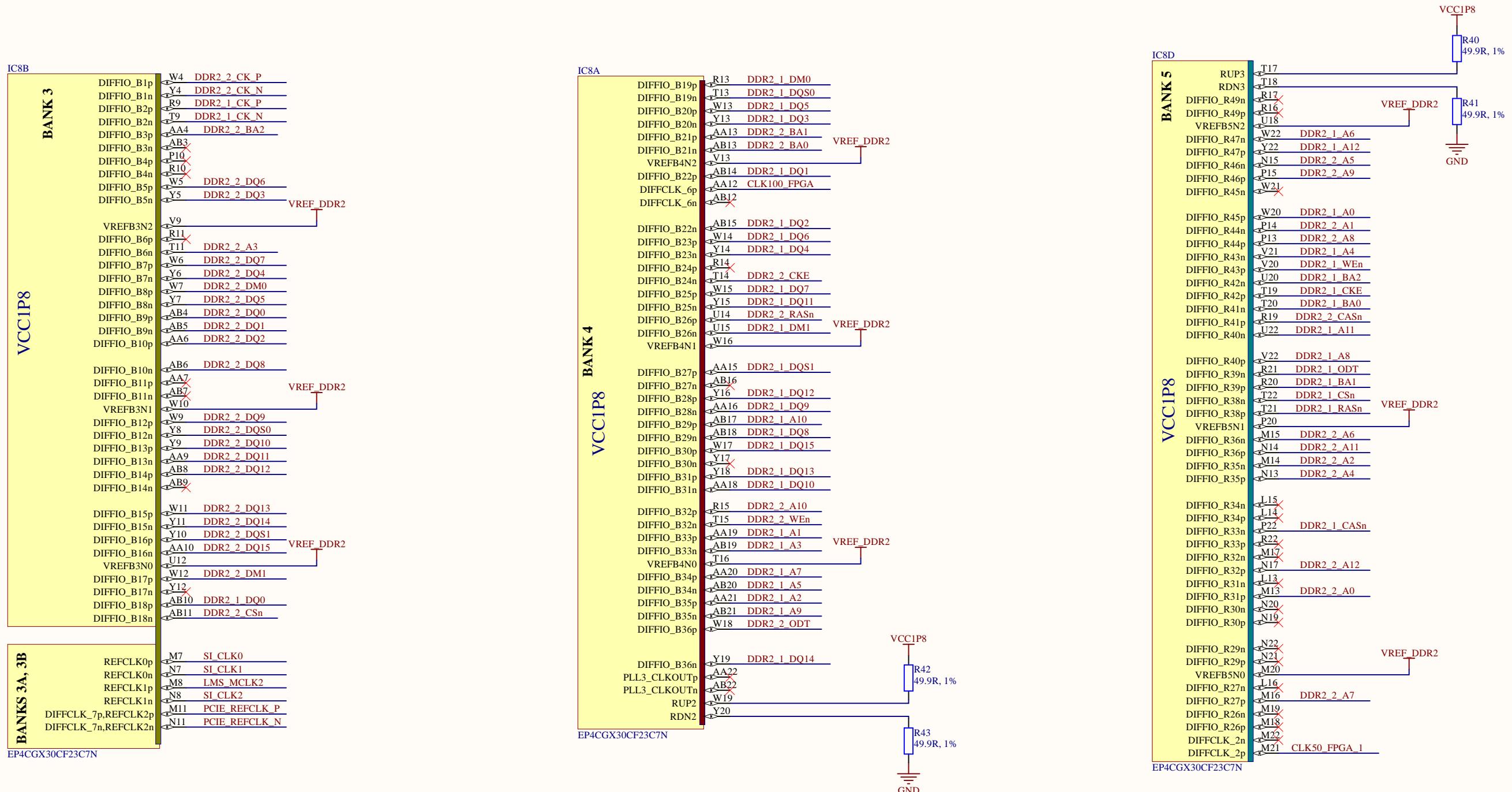
NF elements on sheet: FR18, FR25  
Number of NF elements on sheet: 2

## LMS7002M power supply circuit



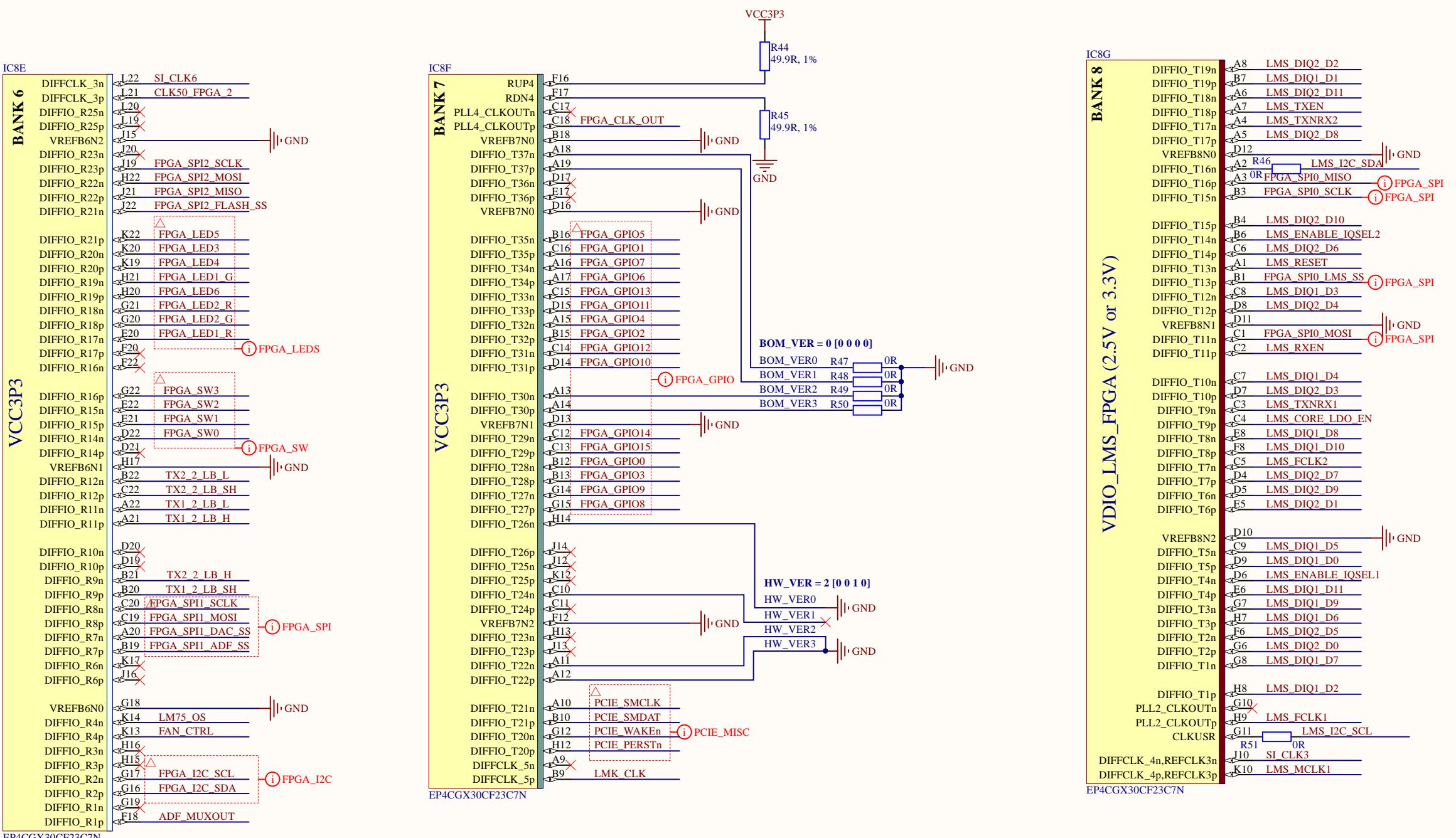
# FPGA banks 3, 4, 5

NF elements on sheet: -  
Number of NF elements on sheet: 0



NF elements on sheet: -  
Number of NF elements on sheet: 0

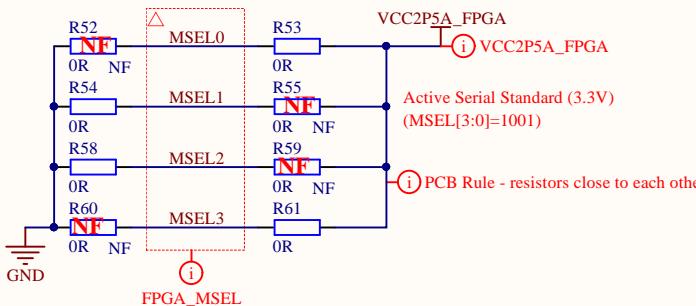
FPGA banks 6, 7, 8



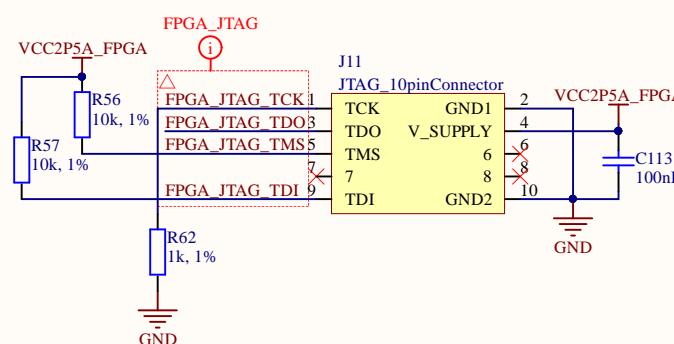
NF elements on sheet: R52, R55, R59, R60, IC9  
Number of NF elements on sheet: 5

## FPGA misc (clocks, config, PCIe)

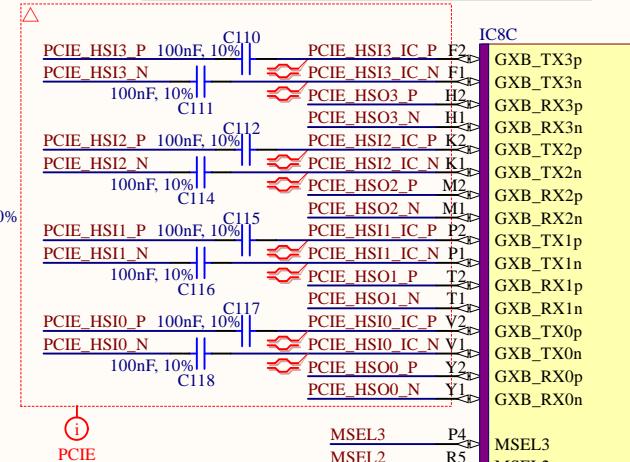
### MSEL config



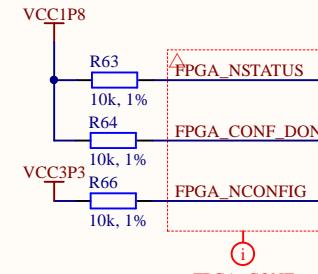
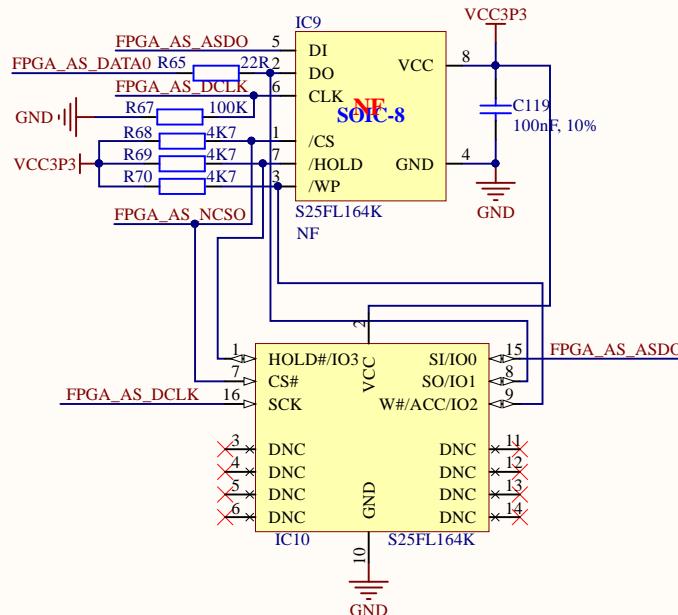
### 10 pin JTAG connector



### FPGA Misc



### FPGA Configuration Flash (AS)



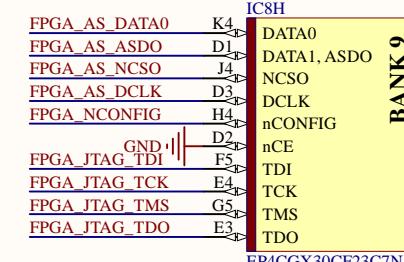
Project name: **LimeSDR-PCIe\_1v2.PrbPcb**

Title: **FPGA misc**

Size: **A4** Revision: **v1.2**

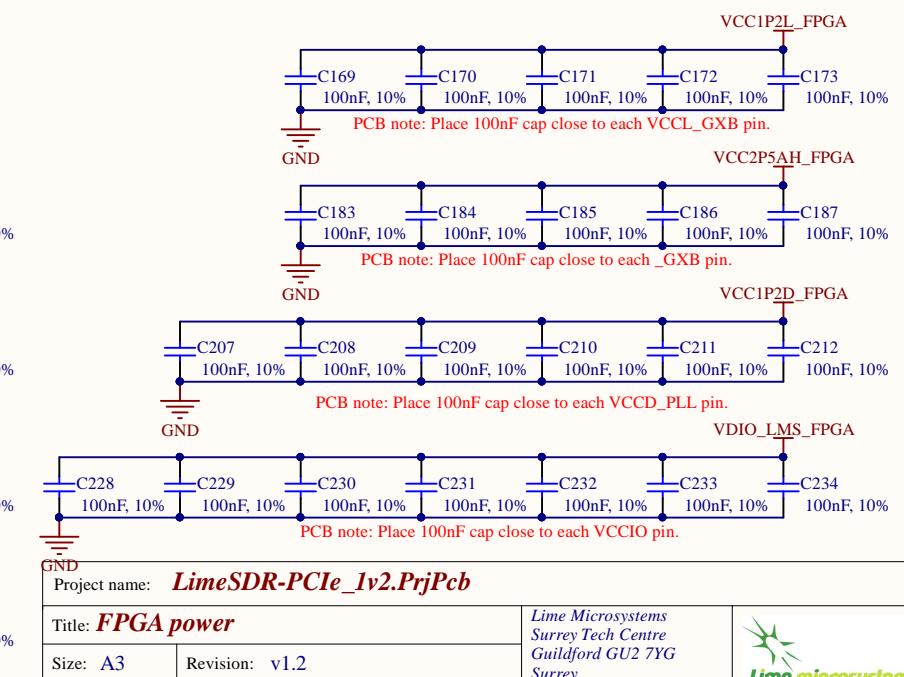
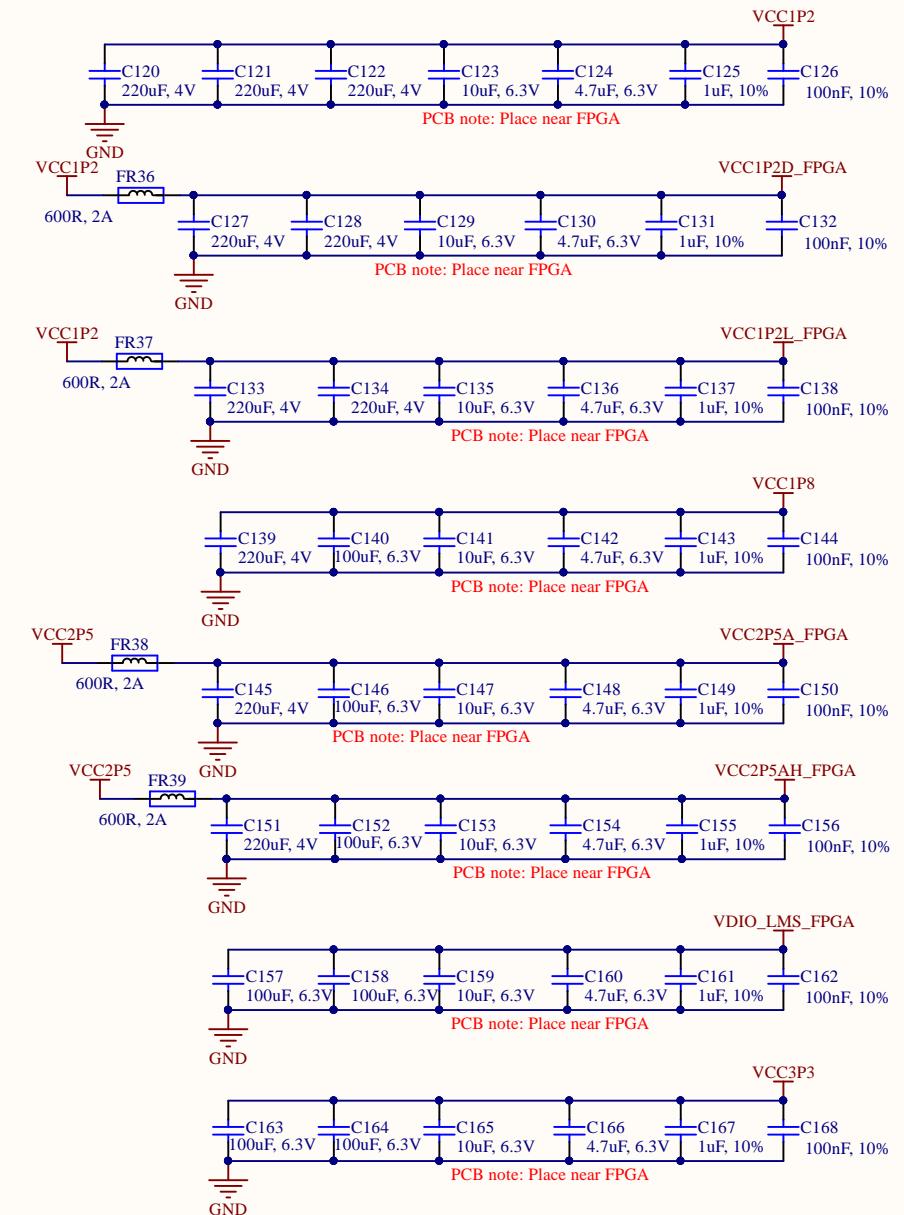
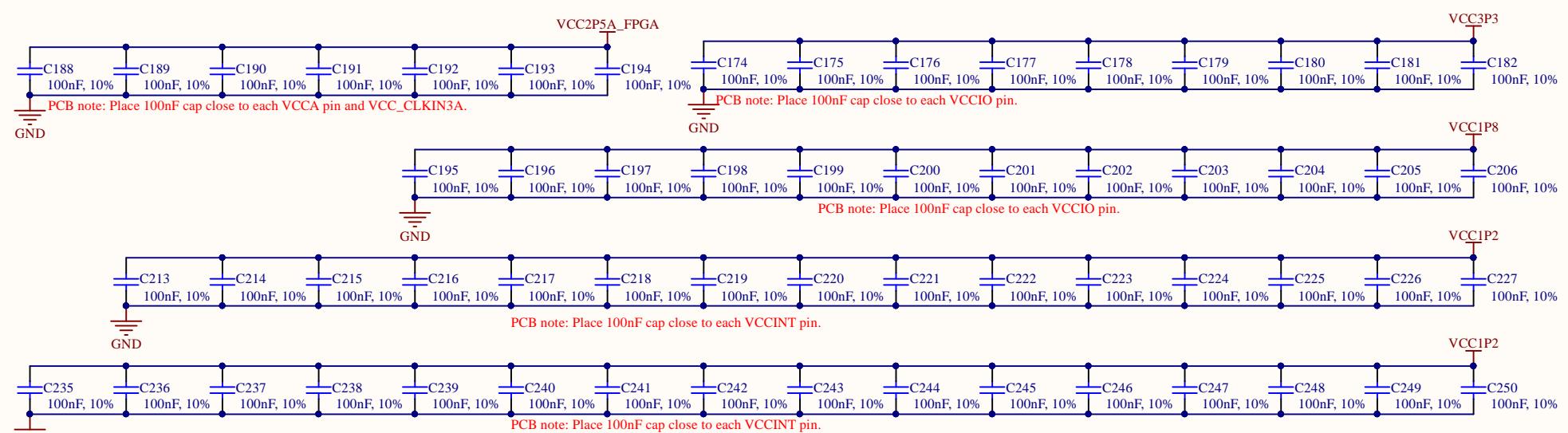
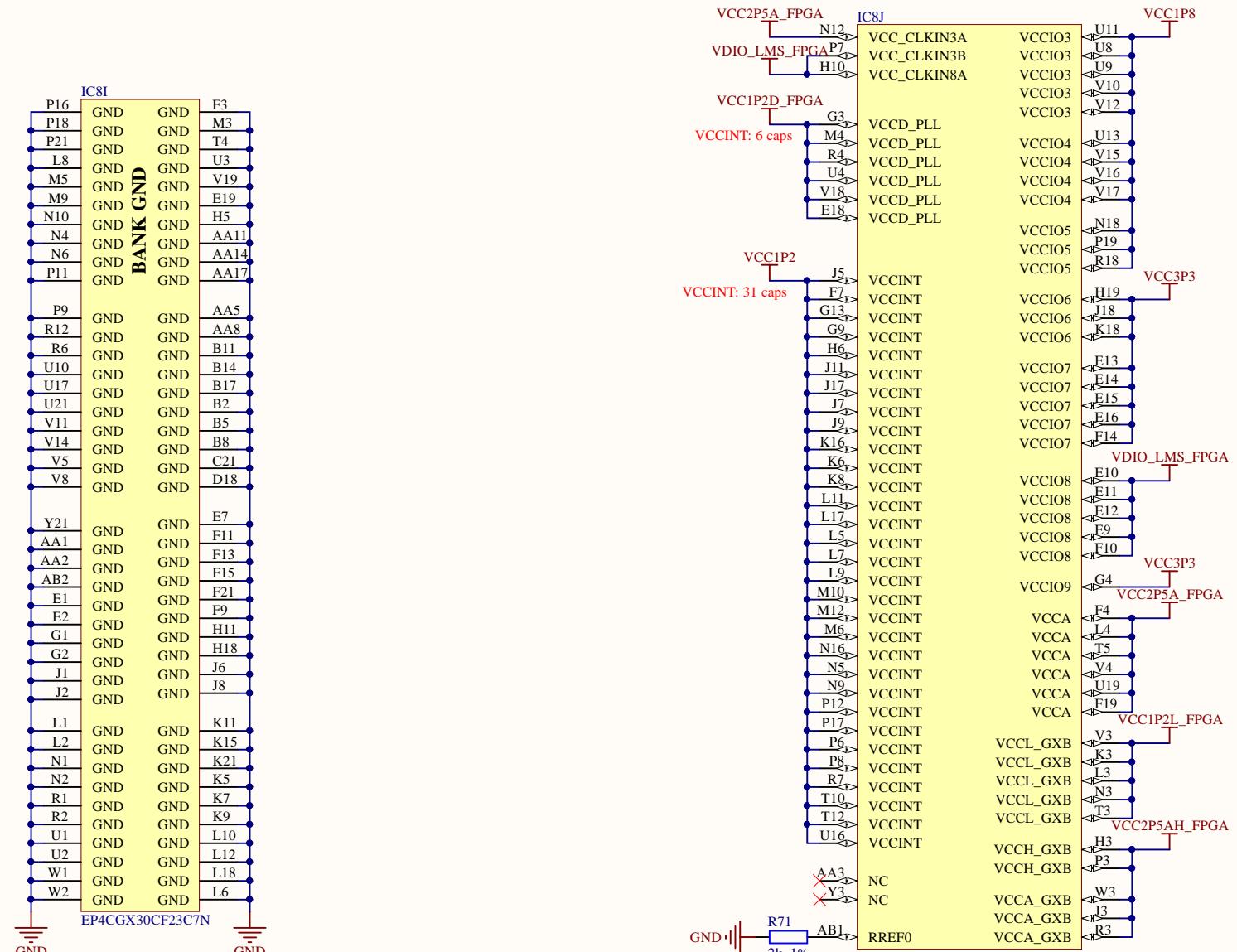
Date: 2017-02-01 Time: 15:49:50 Sheet 10 of 16

File: 10\_FPGA\_msc.SchDoc



NF elements on sheet: -  
Number of NF elements on sheet: 0

# FPGA power



GND Project name: **LimeSDR-PCIe\_1v2.PrjPcb**

Title: *FPGA power*

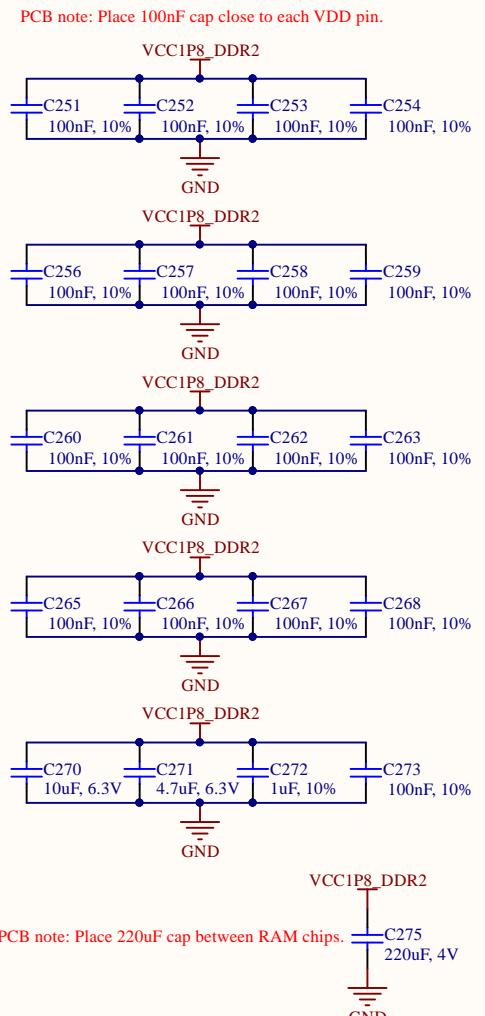
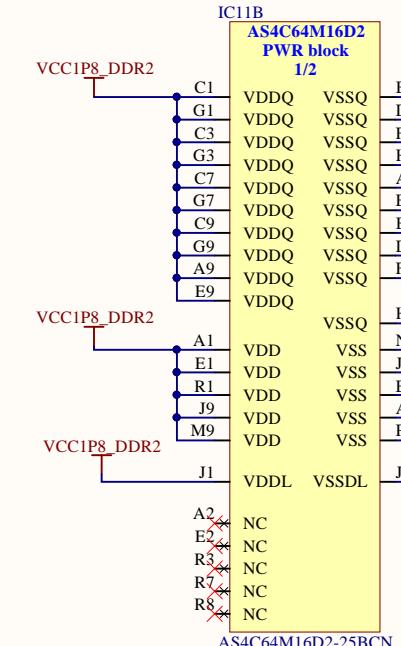
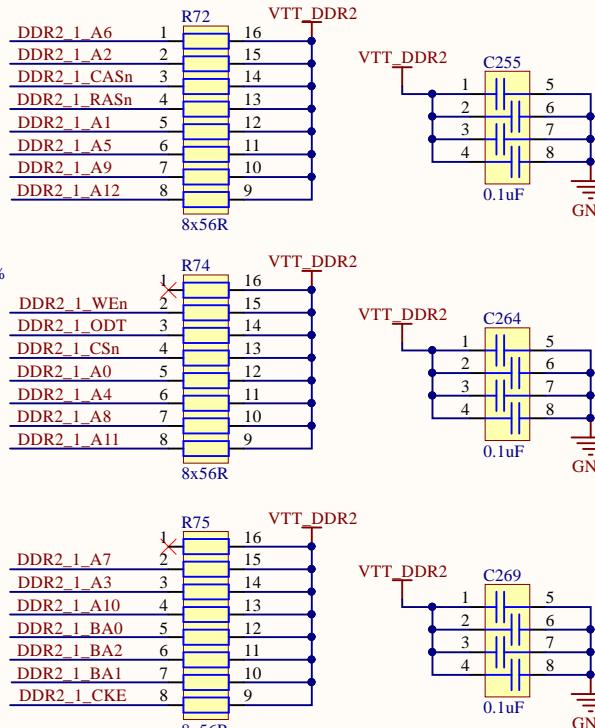
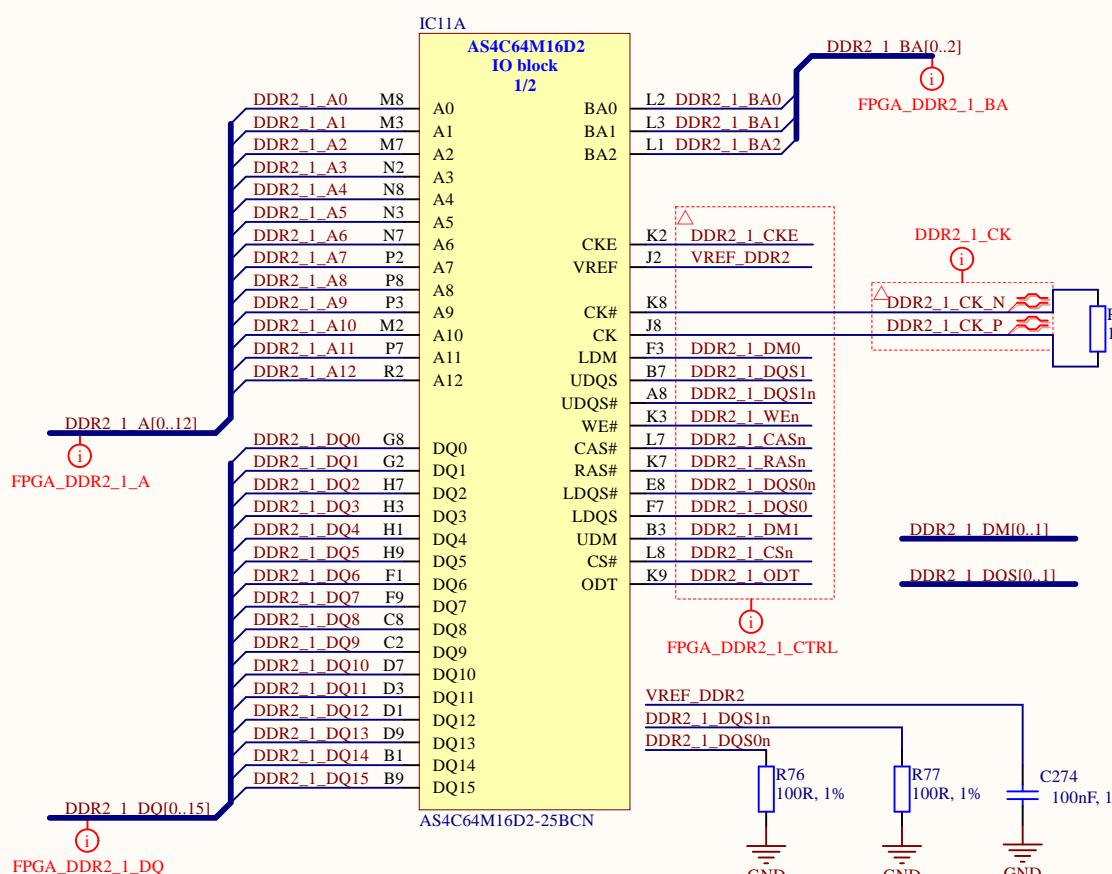
% Size: A3 Revision: v1.2

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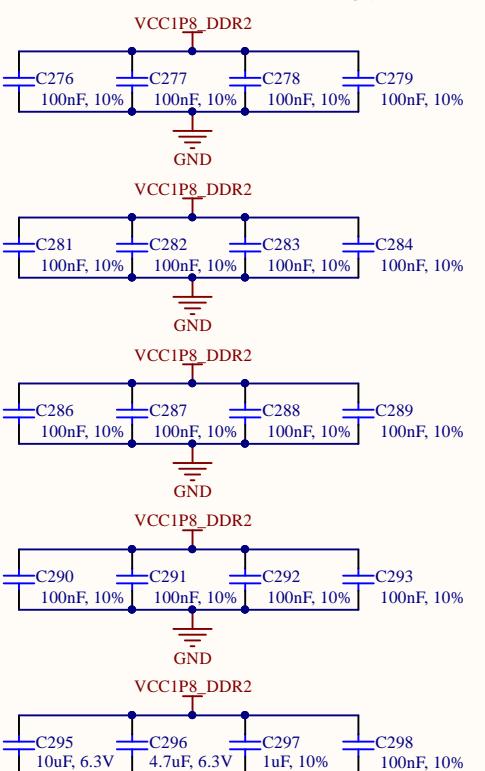
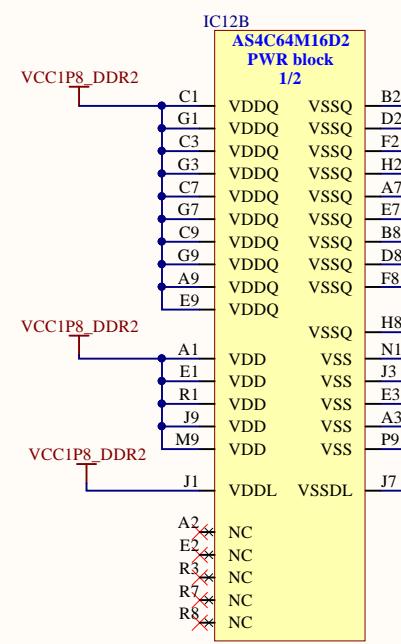
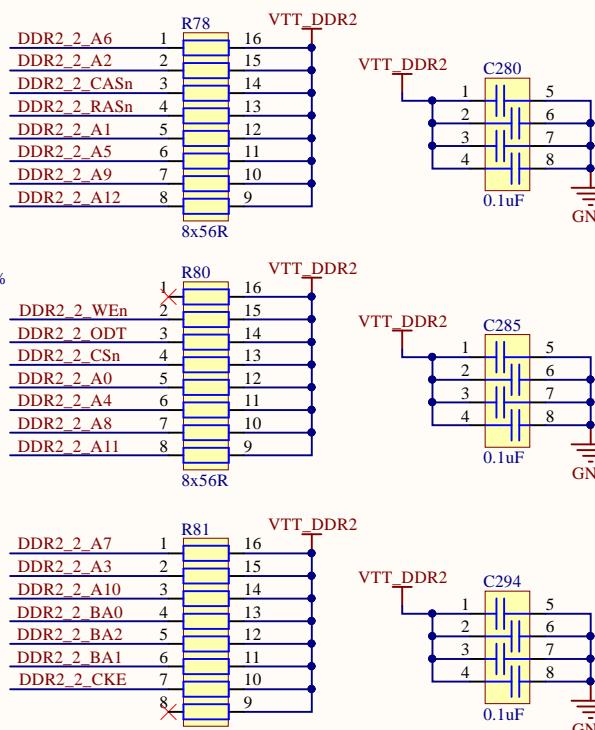
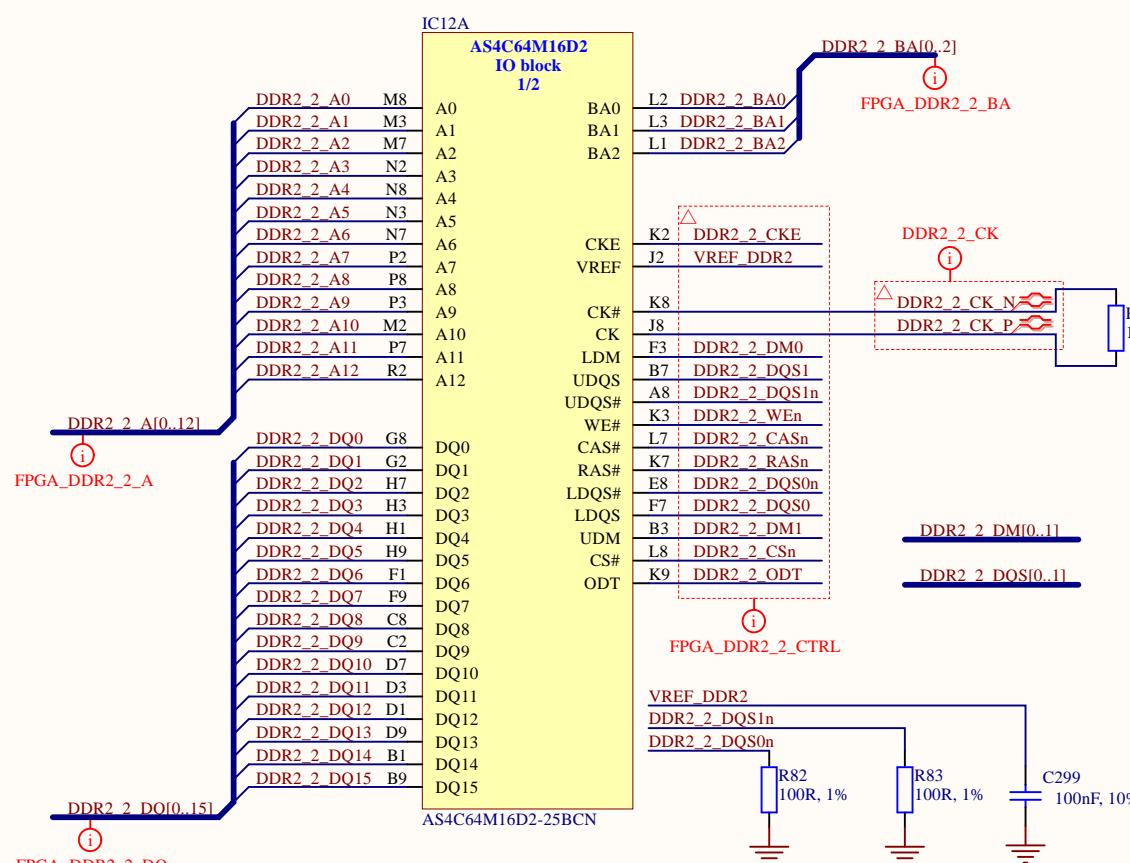


NF elements on sheet: -  
Number of NF elements on sheet: 0

**DDR2\_1 (BOT L)**



**DDR2\_2 (BOT R)**



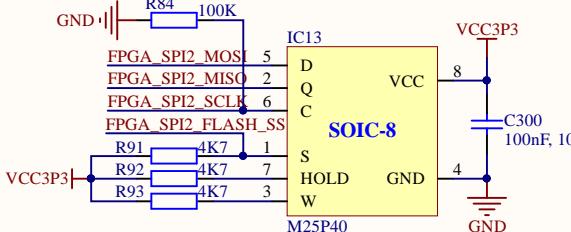
Project name:	<b>LimeSDR-PCIe_1v2.PrjPcb</b>	GND
Title:	<b>DDR2</b>	<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>
Size:	A3	Revision: v1.2
Date:	2017-02-01	Time: 15:49:57
File:	12_DDR2_S1.Dwg	 Lime <b>microsystems</b>

NF elements on sheet: R98, R99, R100, LED1, LED4

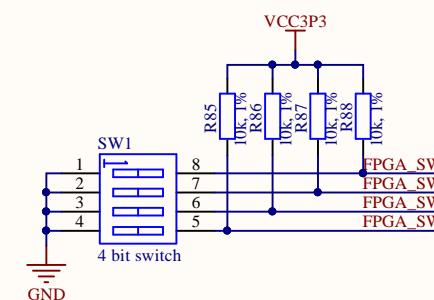
Number of NF elements on sheet: 5

## Peripherals

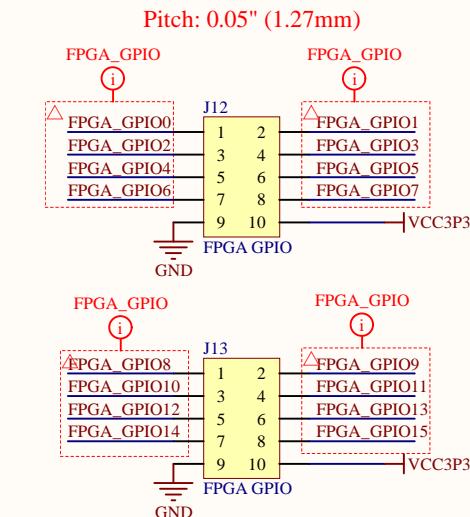
### FPGA Flash



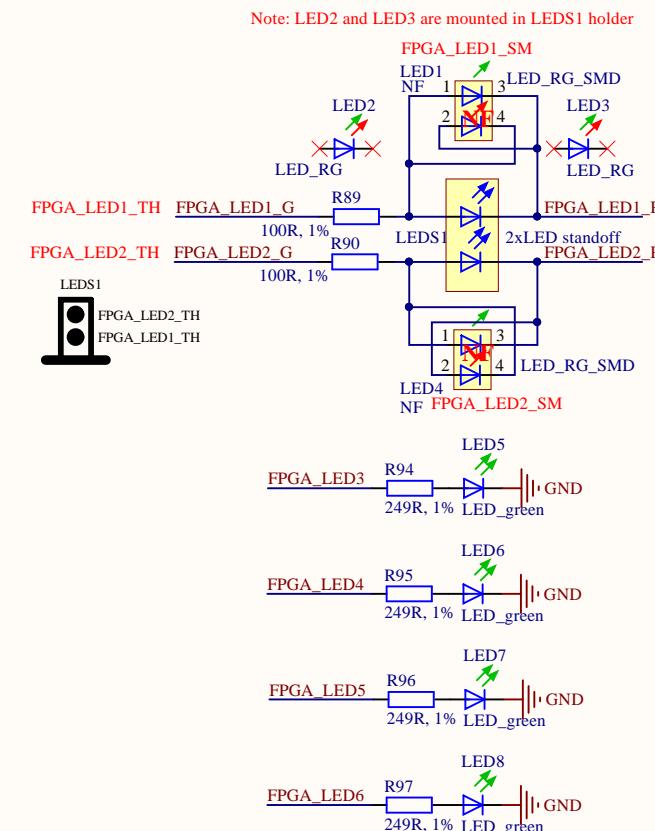
### FPGA SW



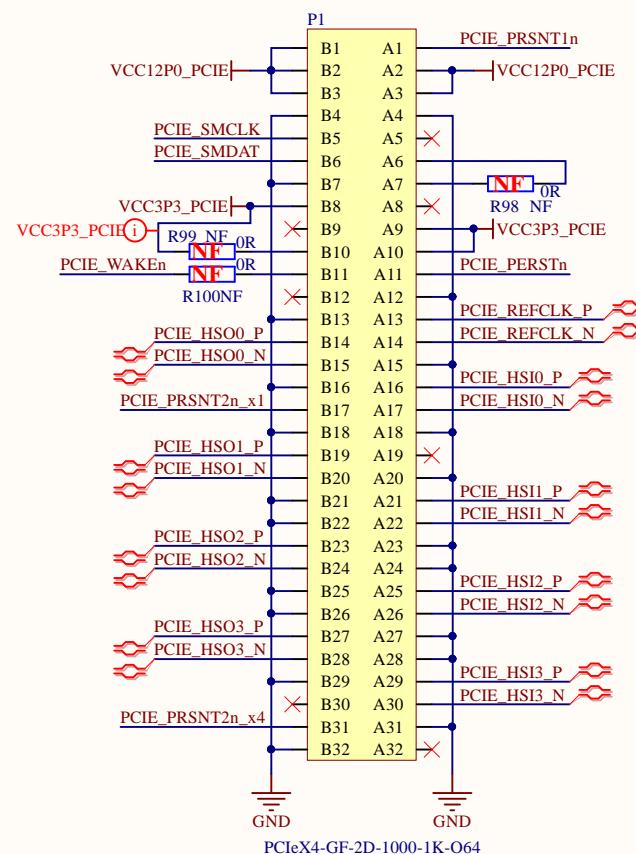
### FPGA GPIO



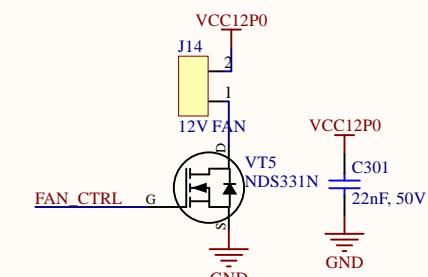
### FPGA LED



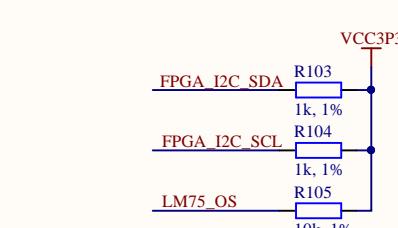
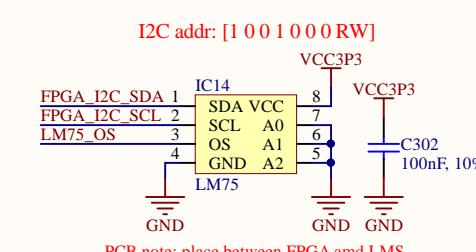
### PCI Express x4



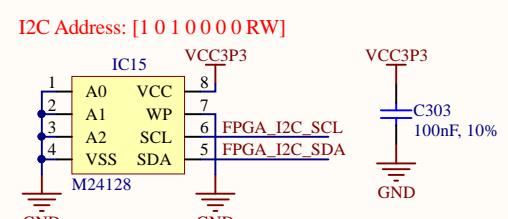
### FAN control



### I2C Temperature sensor



### I2C EEPROM



Project name: LimeSDR-PCIe\_1v2.PrjPcb

Title: Peripherals

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Size: A3 Revision: v1.2

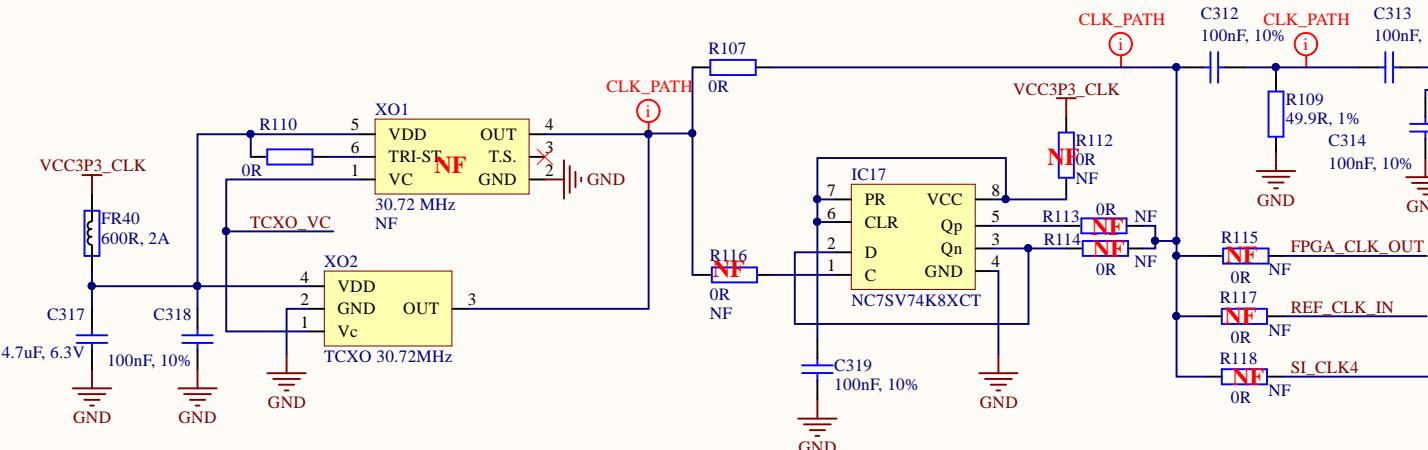
Date: 2017-02-01 Time: 15:50:00 Sheet 13 of 16

File: 13\_Periph.SchDoc

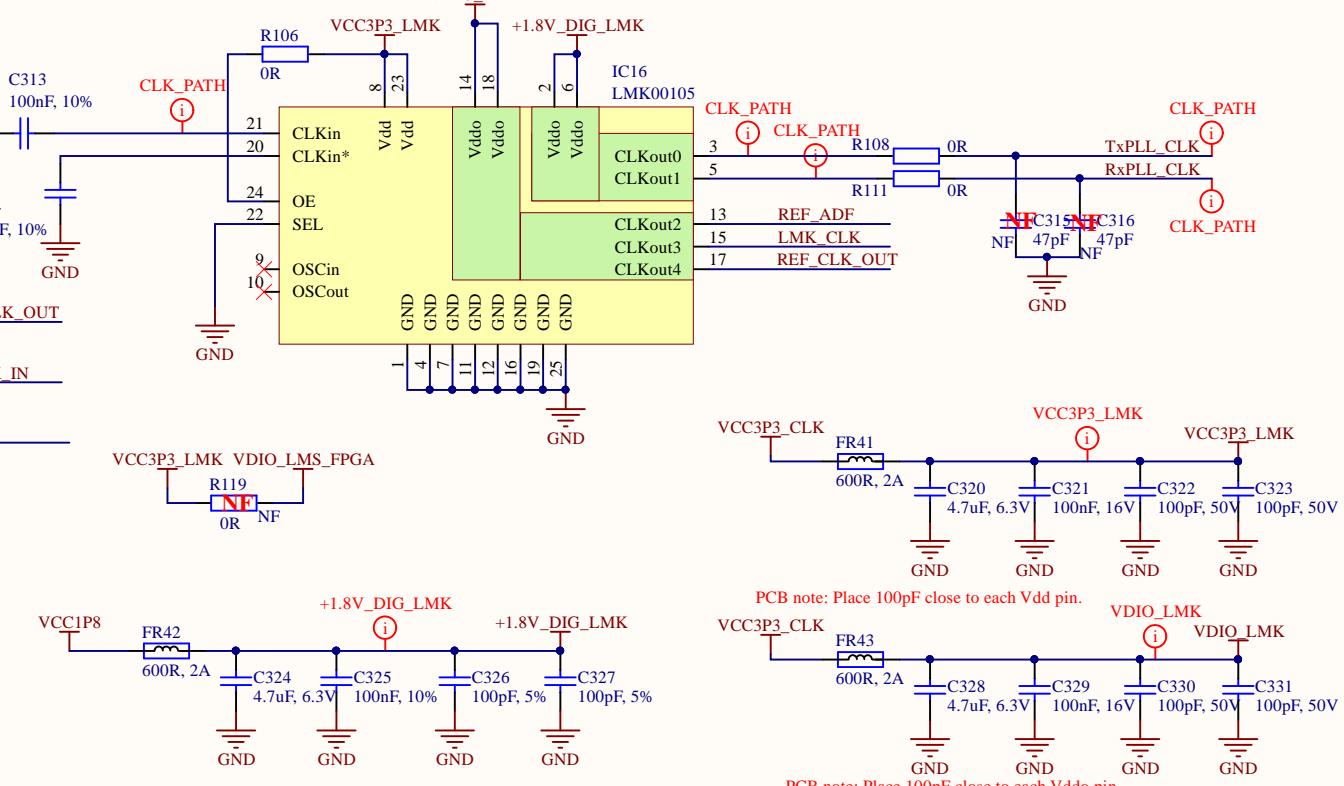
NF elements on sheet: XO1, R112, R113, R114, R115, R116, R117, R118, R119, R121, R125, C315, C316, C332  
Number of NF elements on sheet: 14

## Clock circuits 1

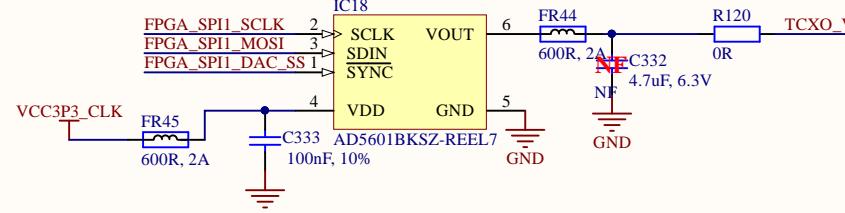
### (VC)TCXO



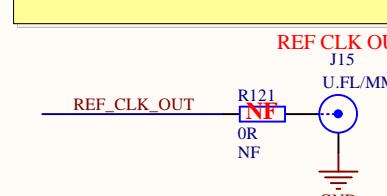
### Clock buffer



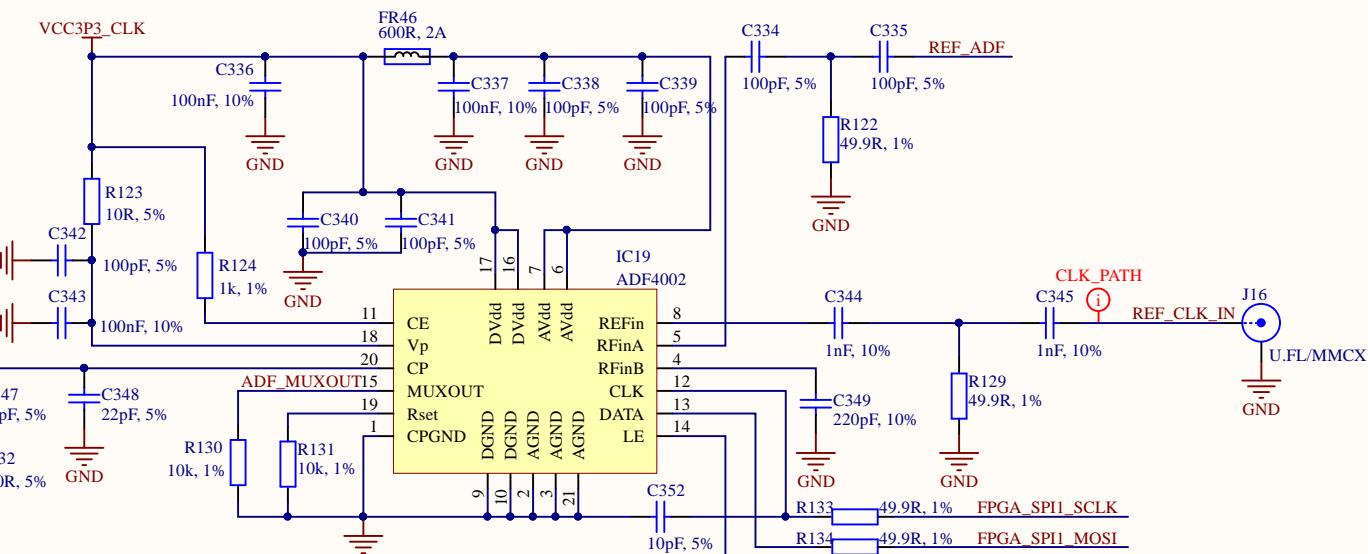
### DAC



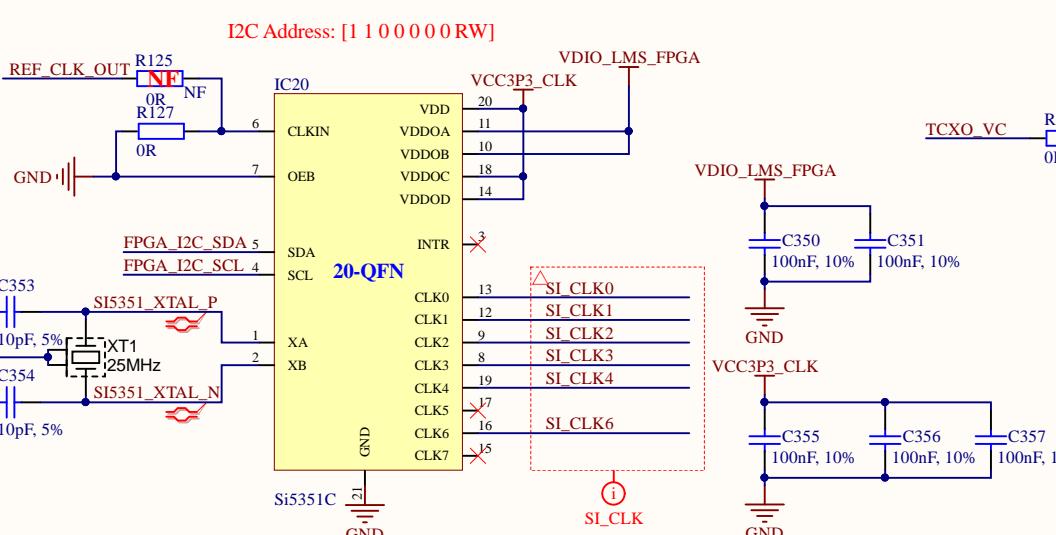
### REF CLK OUT



### Phase Detector



### Clock generator



Project name: LimeSDR-PCIe\_1v2.PrjPcb

Title: Clocks 1

Size: A3 Revision: v1.2

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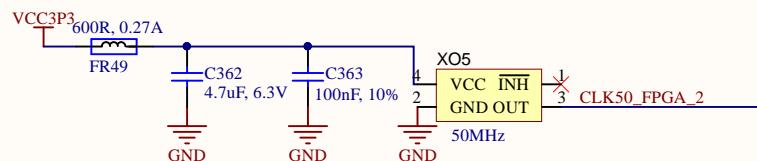
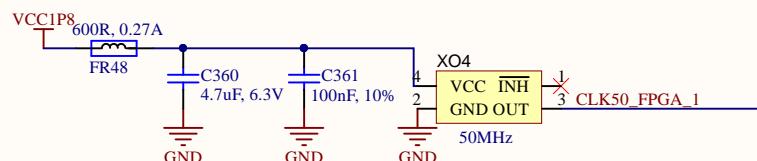
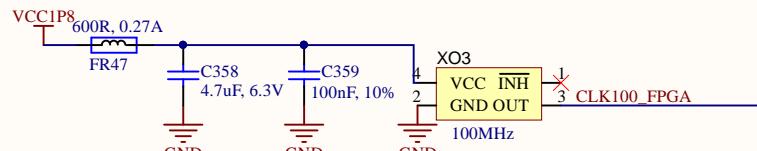
File: 14\_Clocks\_1.SchDoc

NF elements on sheet: -  
Number of NF elements on sheet: 0

## Clock circuits 2

A

### SE Crystal Oscillators



Project name: LimeSDR-PCIe\_1v2.PrjPcb

Title: Clocks 2

Size: A4 Revision: v1.2

Date: 2017-02-01 Time: 15:50:06 Sheet 15 of 16

File: 15\_Clocks\_2.SchDoc

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## Board power circuits

