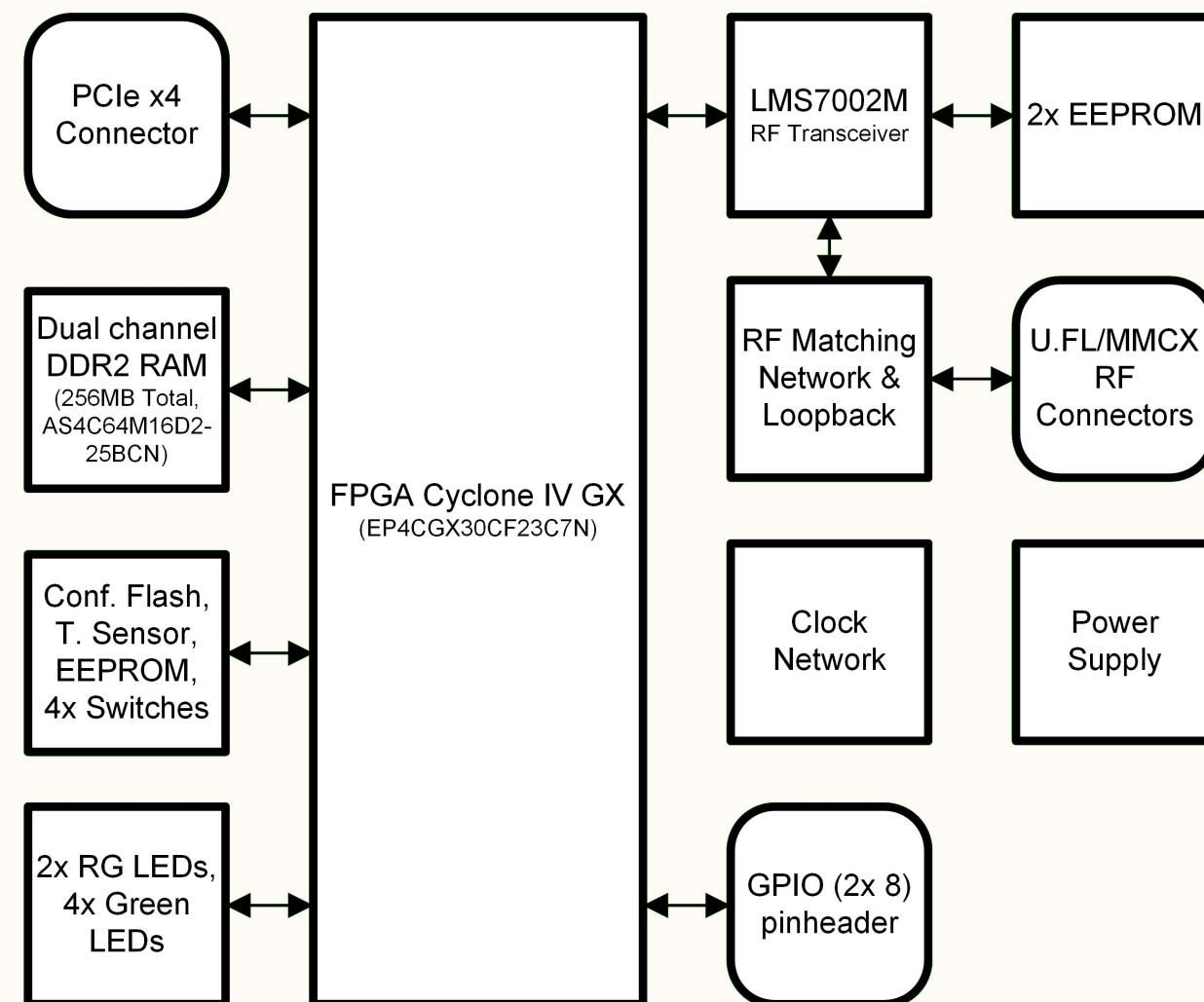


Block diagram



Project name: **LimeSDR-PCIe_Iv3.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.3**

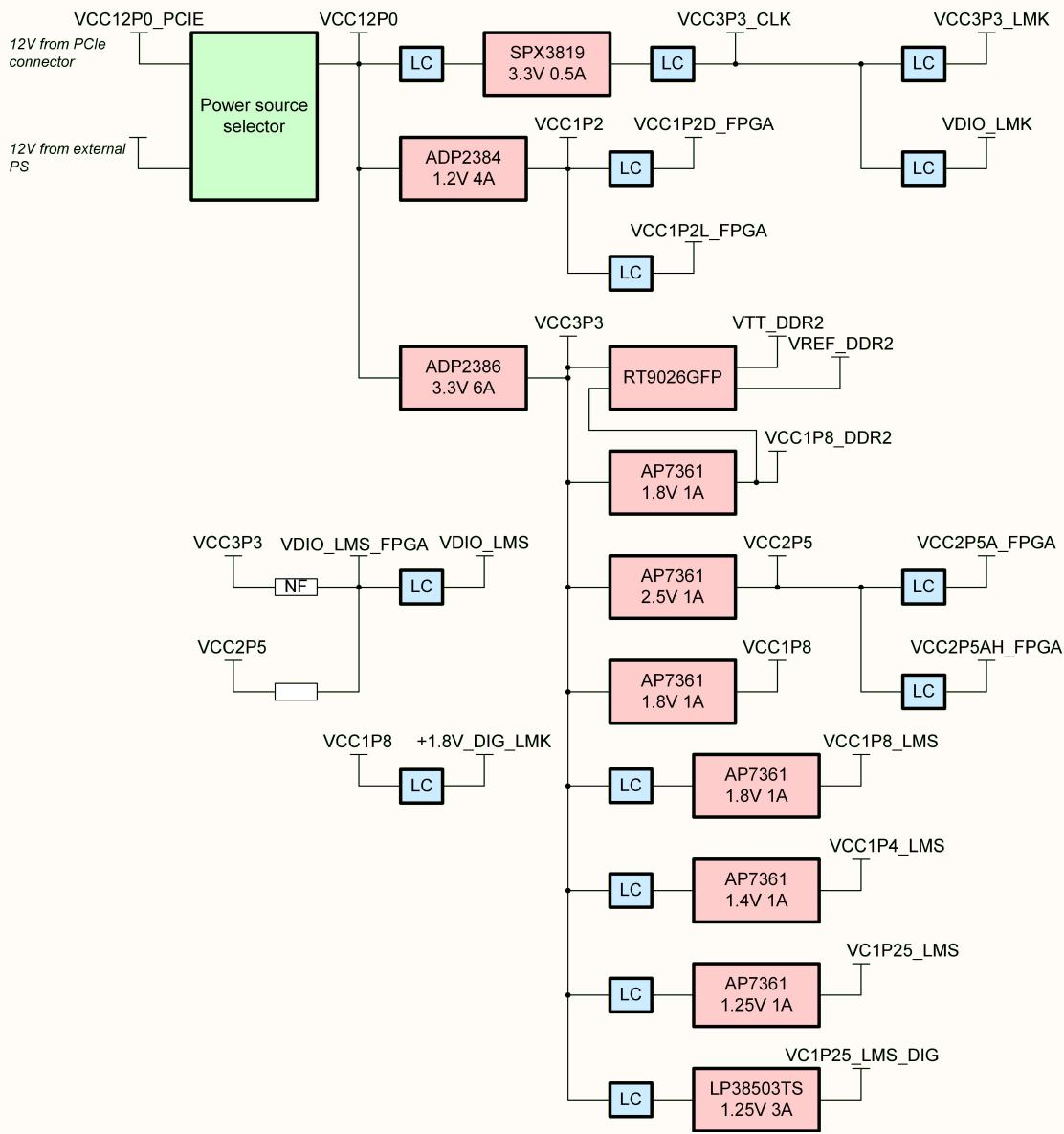
Date: **2017-03-17** Time: **19:35:50** Sheet **1** of **16**

File: **01_BlockDiagram.SchDoc**

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Surrey
United Kingdom



Power diagram



Project name: **LimeSDR-PCIe_Iv3.PrjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.3**

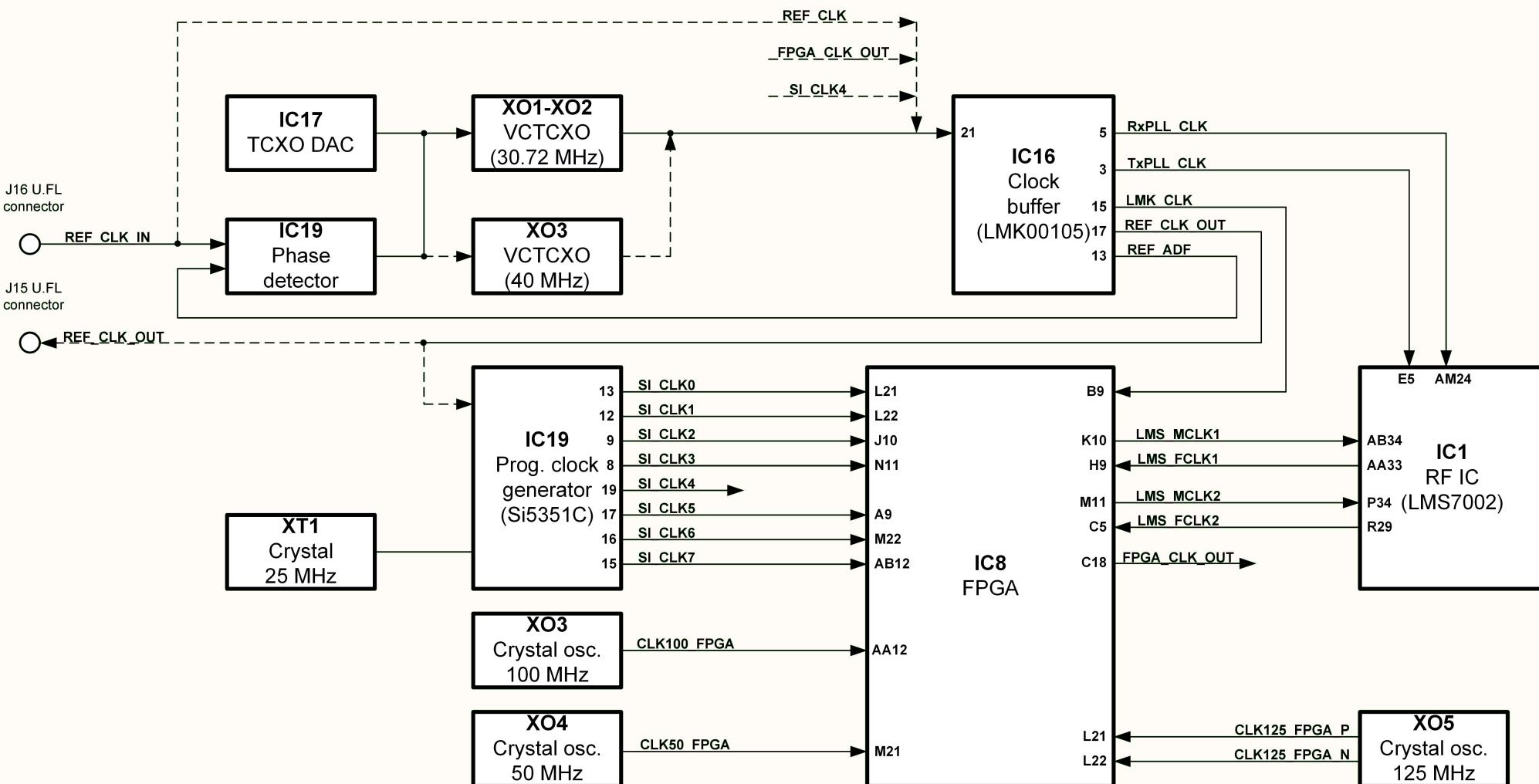
Date: **2017-03-17** Time: **19:35:55** Sheet**2** of **16**

File: **02_PowerDiagram.SchDoc**

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Surrey
United Kingdom



Clock diagram



Project name: *LimeSDR-PCIe_Iv3.PrjPcb*

Title: *Clock diagram*

Size: A4 Revision: v1.3

Date: 2017-03-17 Time: 19:36:04 Sheet 3 of 16

File: 03_ClockDiagram.SchDoc

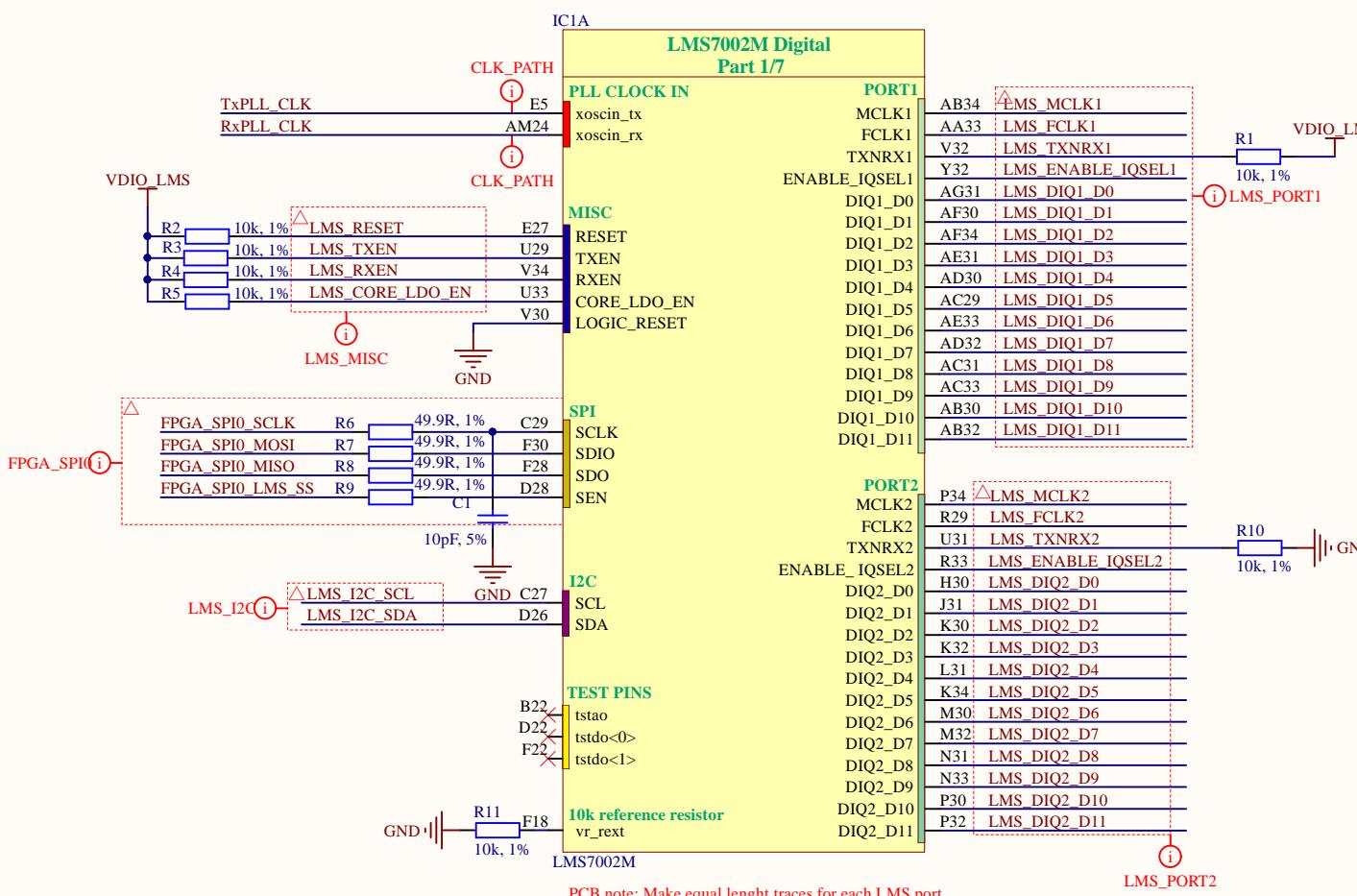
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United Kingdom



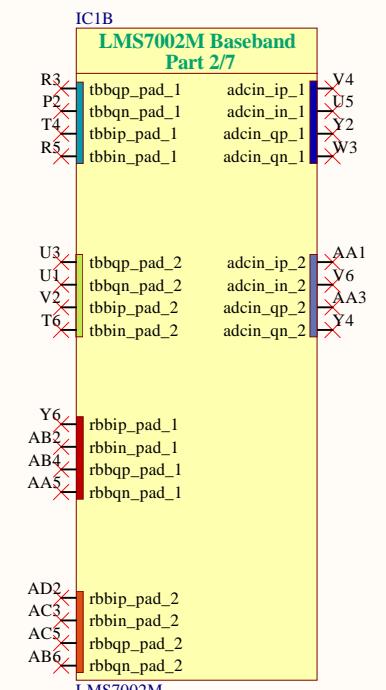
NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M misc

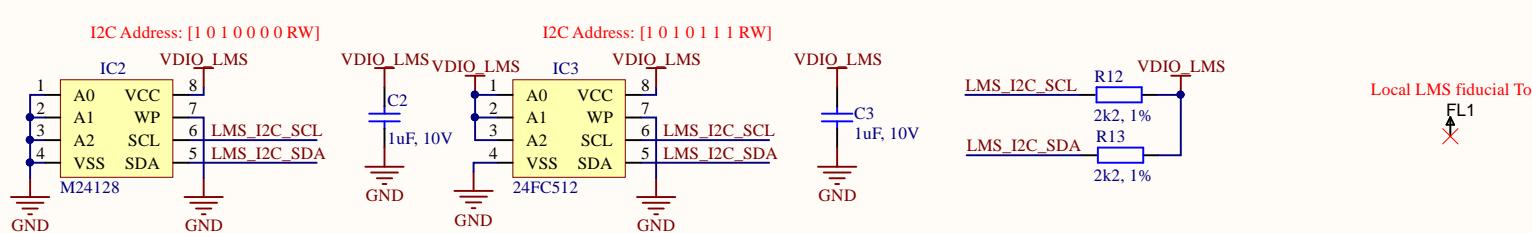
Digital interfaces



Baseband external IO



LMS EEPROMs



Project name: LimeSDR-PCIe_1v3.PrbPcb

Title: LMS7002M misc

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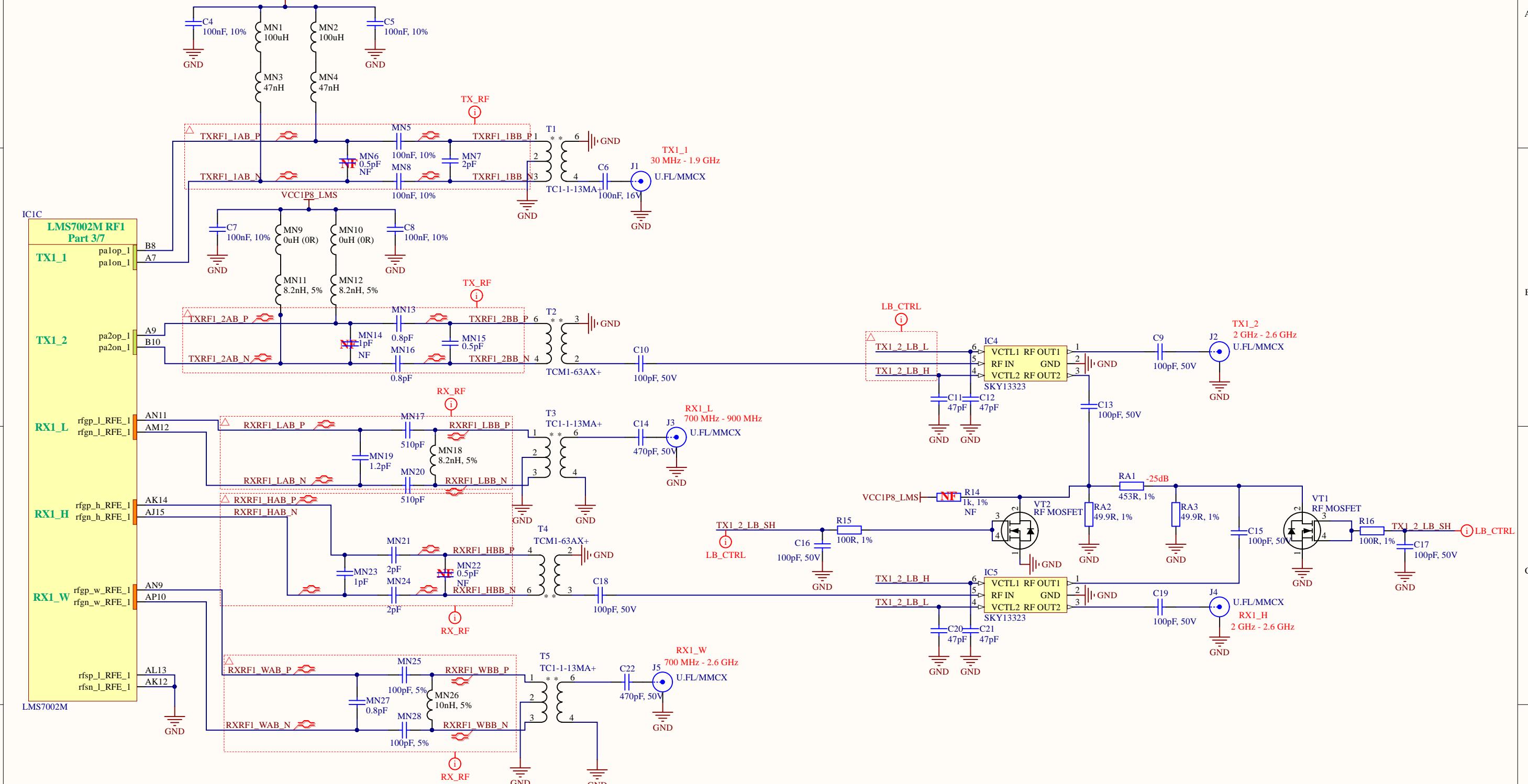
Size: A3 Revision: v1.3

Date: 2017-03-17 Time: 19:36:11 Sheet 4 of 16

File: 04_LMS7002M_Misc.SchDoc

NF elements on sheet: MN6, MN14, MN22, R14, MECH1-MECH10
Number of NF elements on sheet: 14

LMS7002M RF1 circuits



Project name: LimeSDR-PCIe_iv3.PrbPcb

Title: LMS7002M RF

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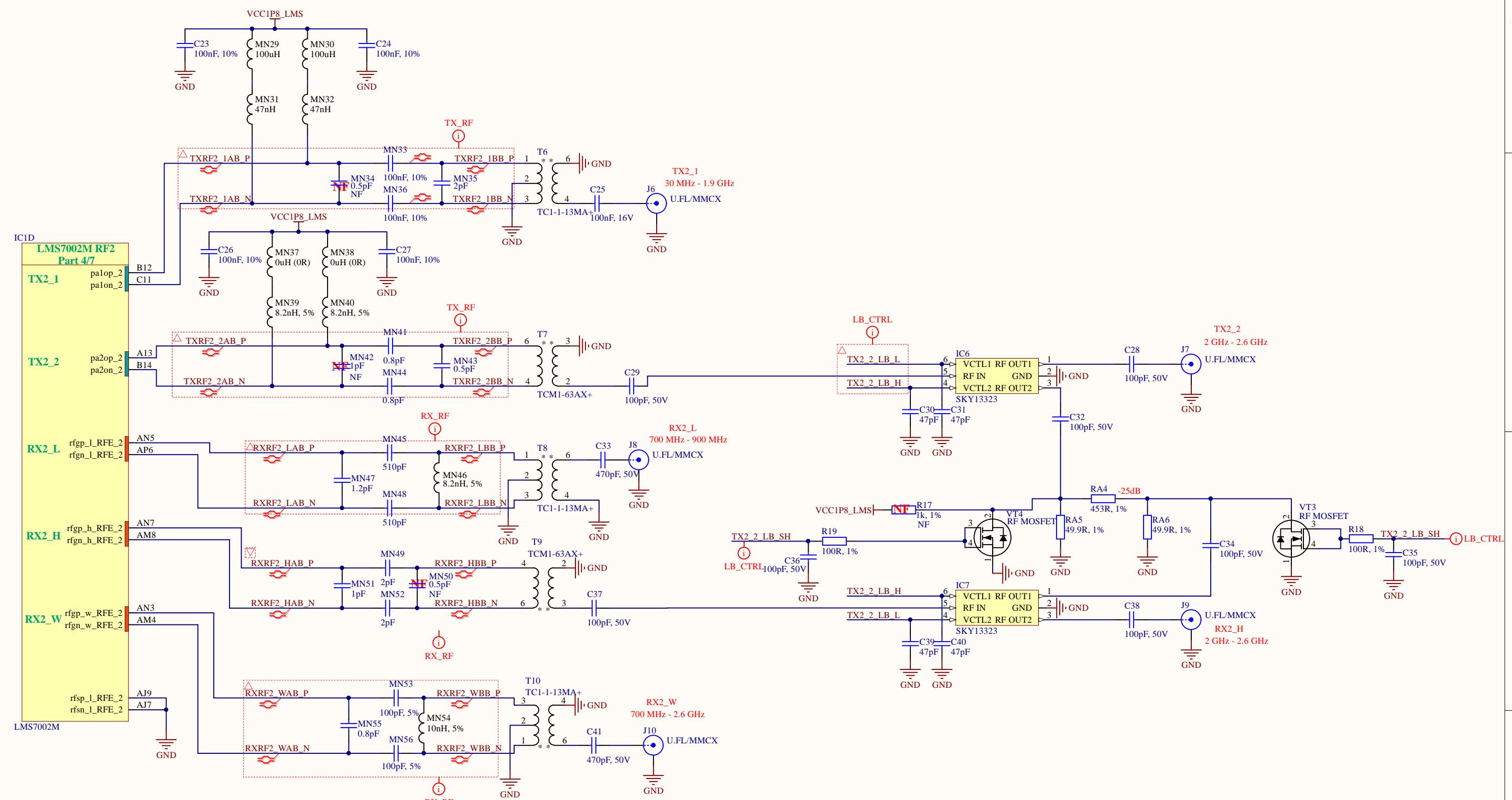
Size: A3 Revision: v1.3

Date: 2017-03-17 Time: 19:36:13 Sheet 5 of 16

File: 05_LMS7002M_RF1.SchDoc

NF elements on sheet: MN34, MN42, MN50, R17
Number of NF elements on sheet: 4

LMS7002M RF2 circuits



Project name: LimeSDR-PCIe_1v3.PnjPcb

Title: LMS7002M RF

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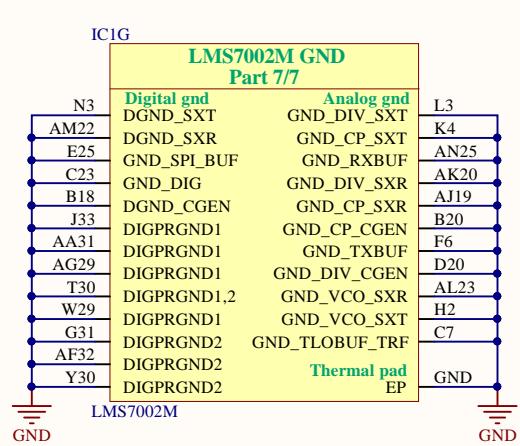
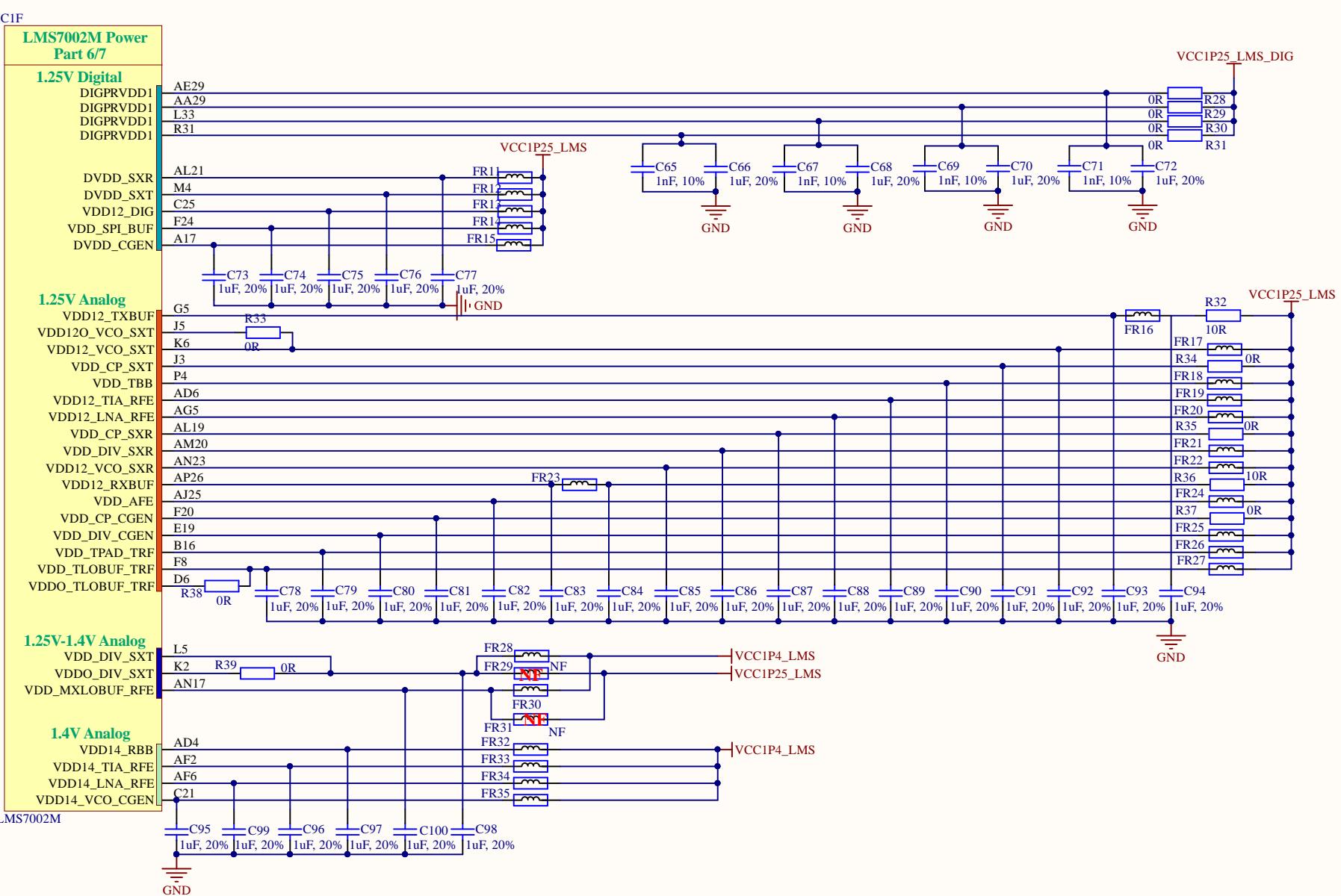
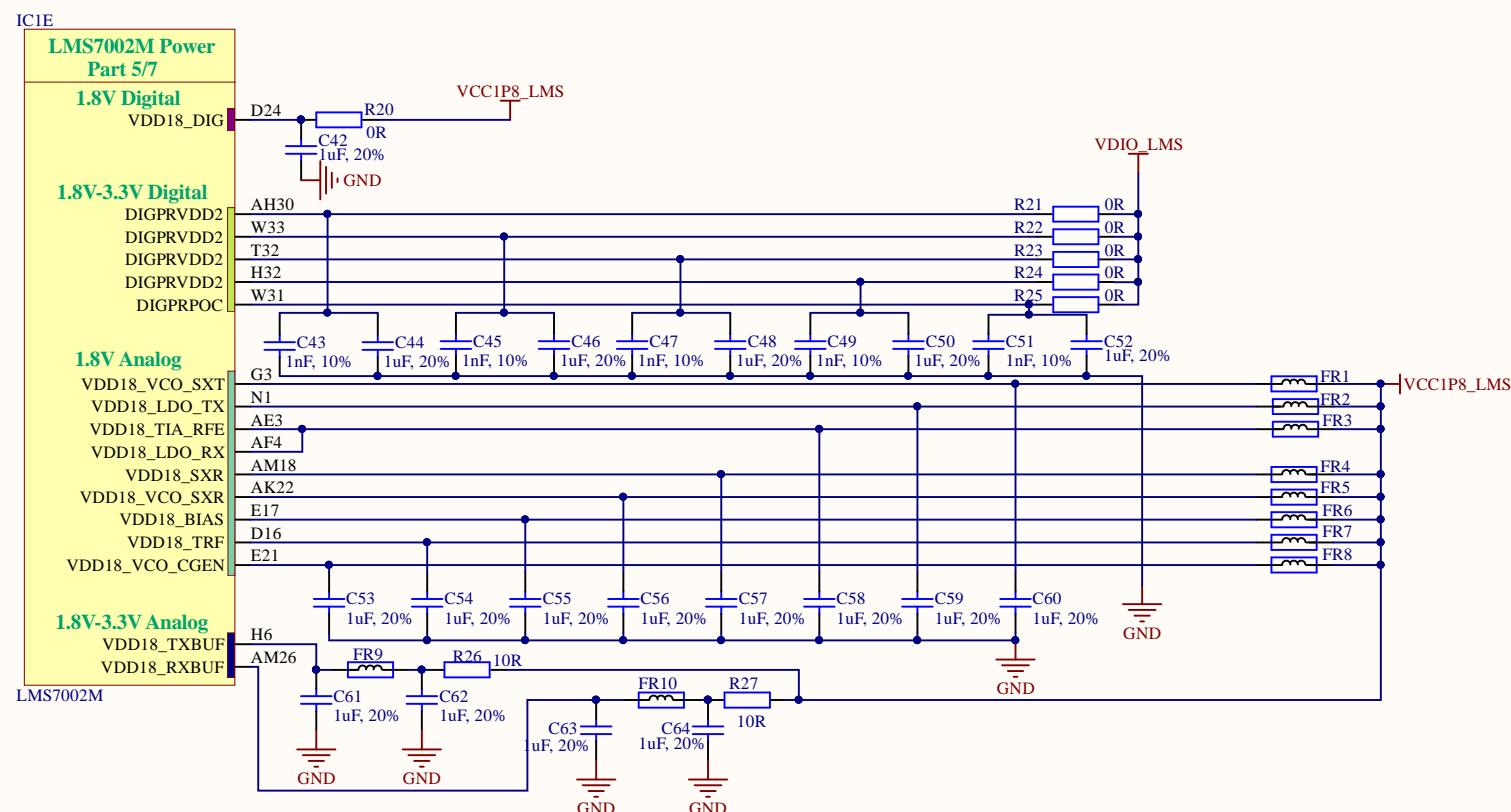
Size: A3 Revision: v1.3

Date: 2017-03-17 Time: 19:36:16 Sheet 6 of 16

File: 06_LMS7002M_RF2.SchDoc

NF elements on sheet: FR29, FR31
Number of NF elements on sheet: 2

LMS7002M power supply circuit



Project name: LimeSDR-PCIe_1v3.PnjPcb

Title: LMS7002M power supply

Size: A3 | Revision: v1.3

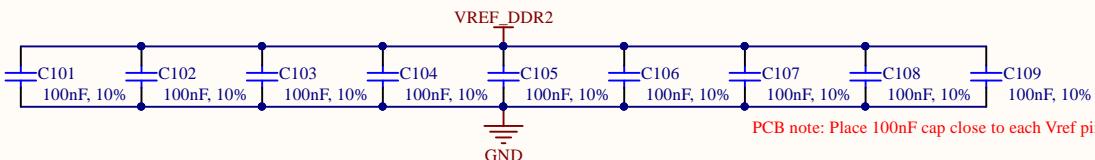
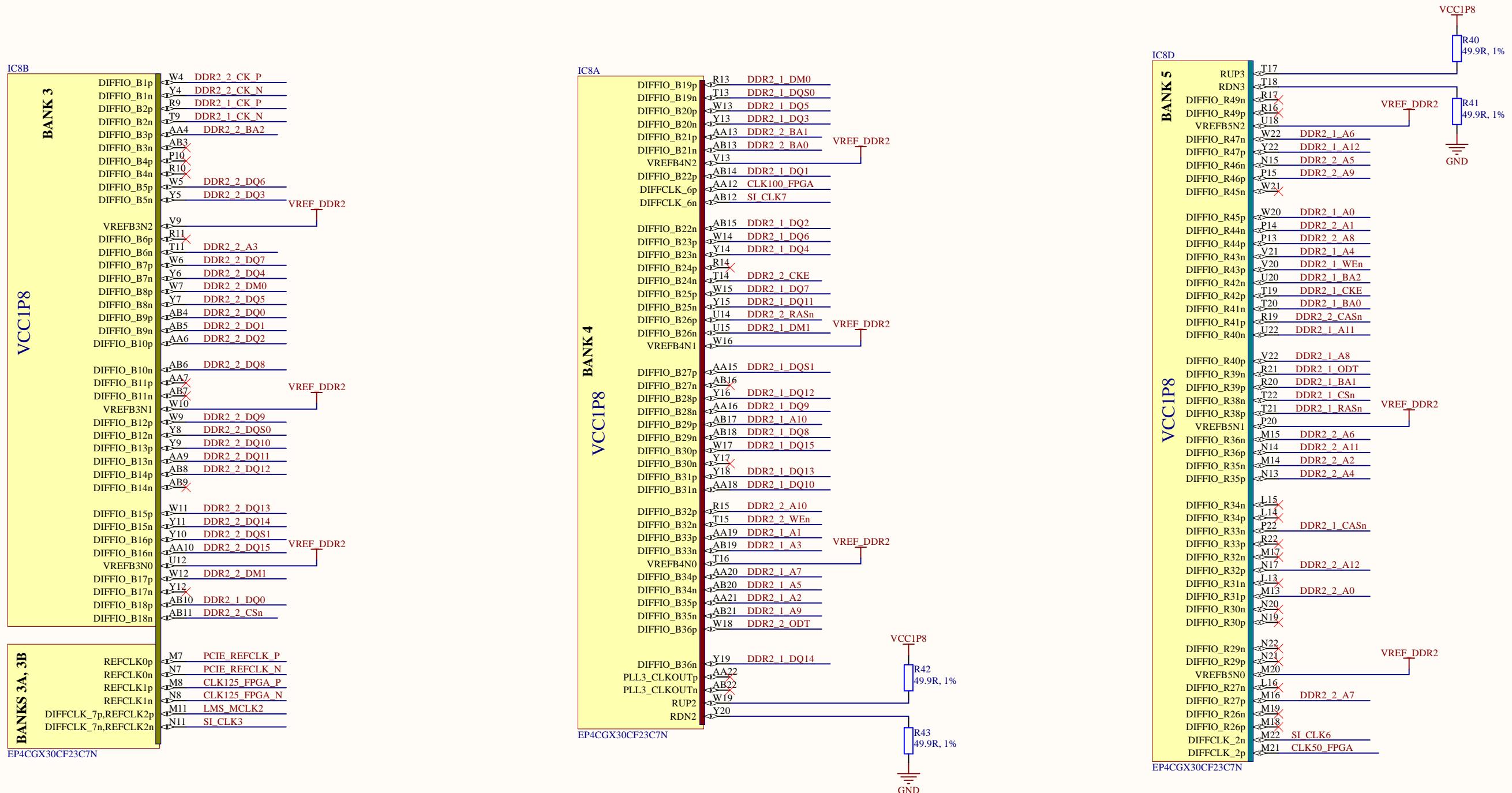
Date: 2017-03-17 Time: 19:36:19 Sheet 7 of 16

File: 07_LMS7002M_Power.SchDoc



FPGA banks 3, 4, 5

NF elements on sheet: -
Number of NF elements on sheet: 0

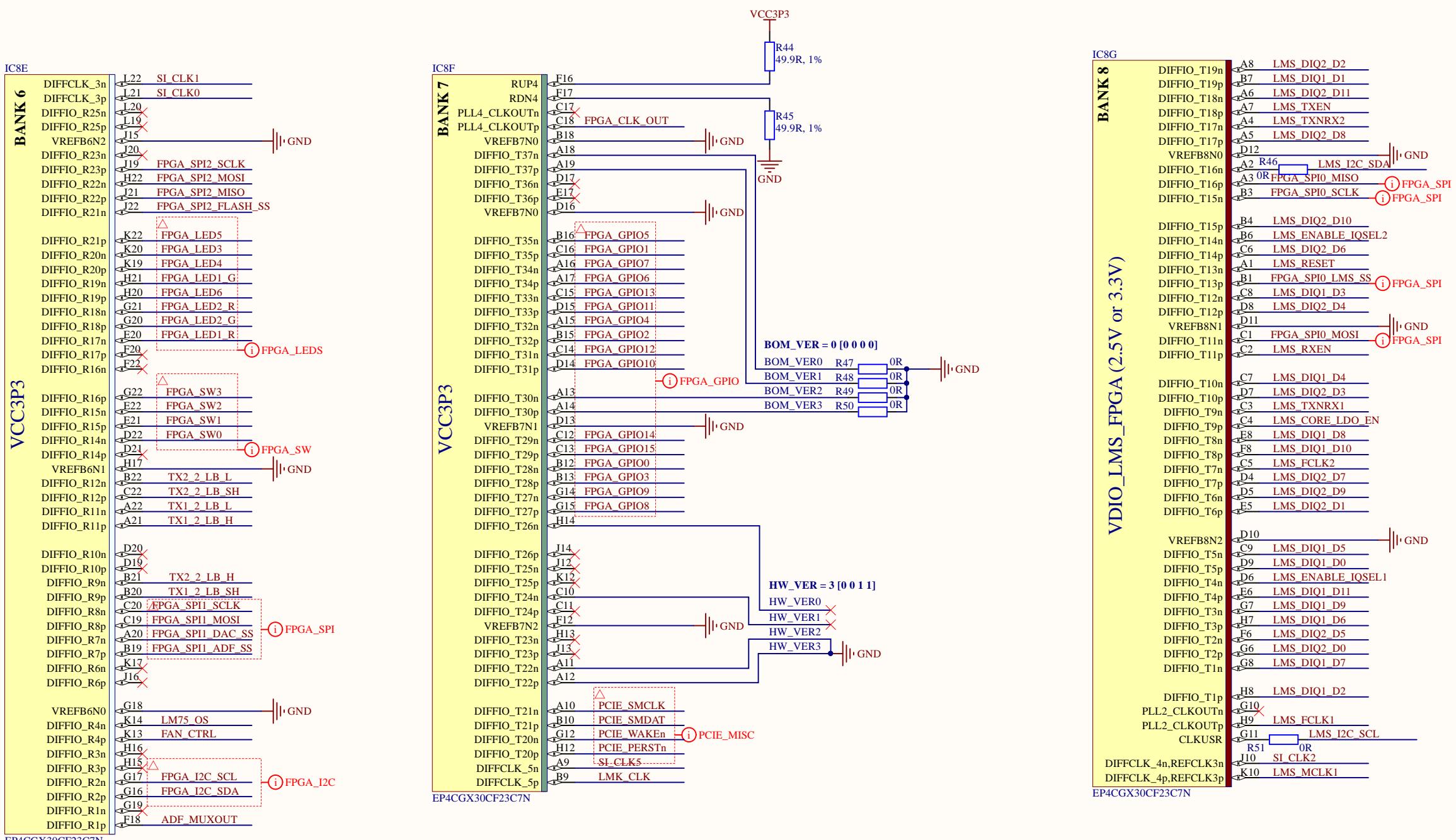


Local FPGA fiducial Top
FL2

Project name: LimeSDR-PCIe_1v3.PrbPcb	
Title: FPGA banks 3, 4, 5	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.3
Date: 2017-03-17	Time: 19:36:22
File: 08_FPGA_banks_3_4_5.SchDoc	Sheet 8 of 16

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 6, 7, 8



Project name: **LimeSDR-PCIe_1v3.PnjPcb**

Title: **FPGA banks 6, 7, 8**

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Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Size: **A3** Revision: **v1.3**

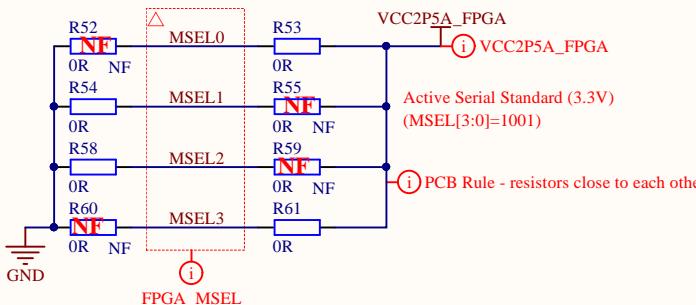
Date: **2017-03-17** Time: **19:36:24** Sheet**9** of **16**

File: **09_FPGA_banks_6_7_8.SchDoc**

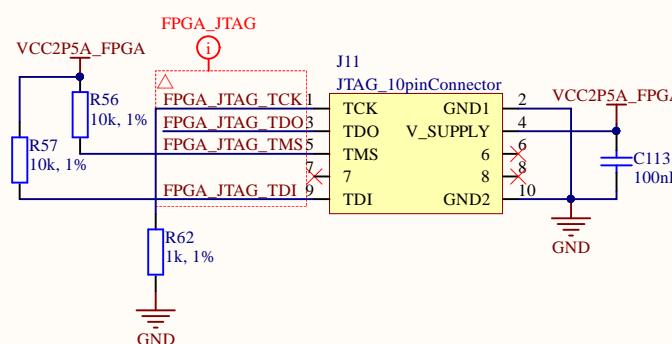
NF elements on sheet: R52, R55, R59, R60, IC9
Number of NF elements on sheet: 5

FPGA misc (clocks, config, PCIe)

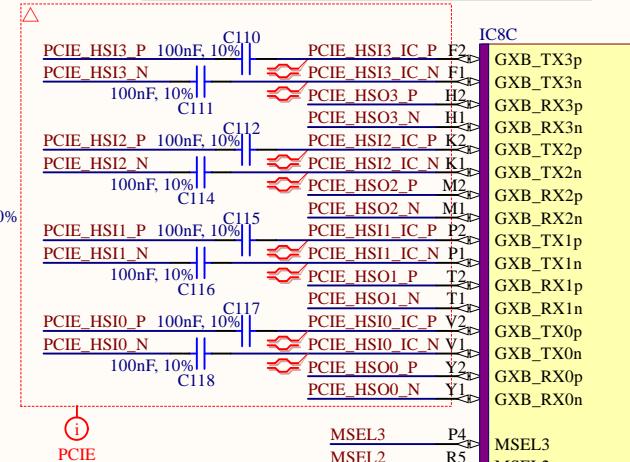
MSEL config



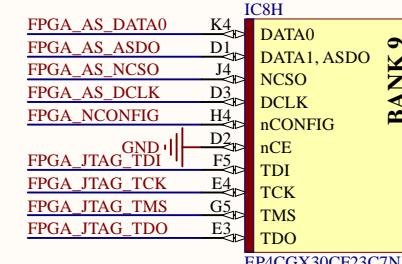
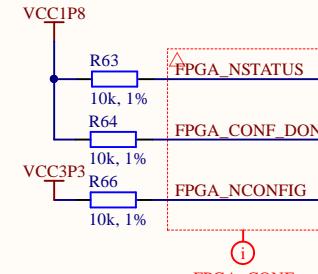
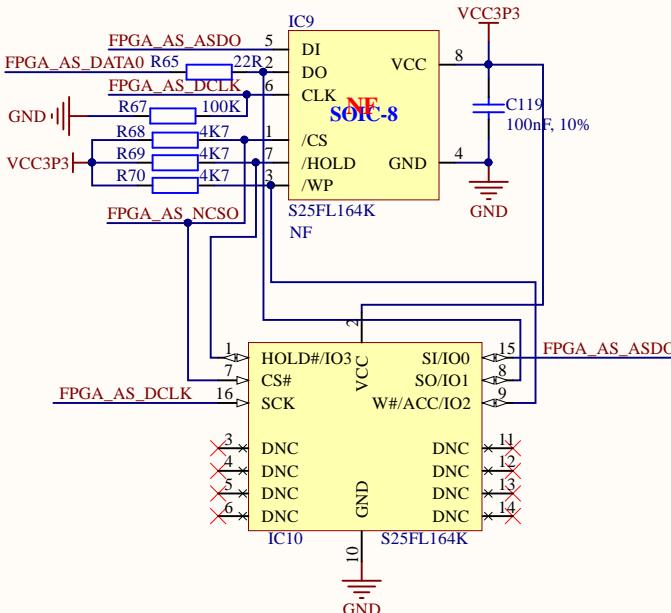
10 pin JTAG connector



FPGA Misc



FPGA Configuration Flash (AS)



Project name: LimeSDR-PCIe_1v3.PrbPcb

Title: **FPGA misc**

Size: A4 Revision: v1.3

Date: 2017-03-17 Time: 19:36:27 Sheet 10 of 16

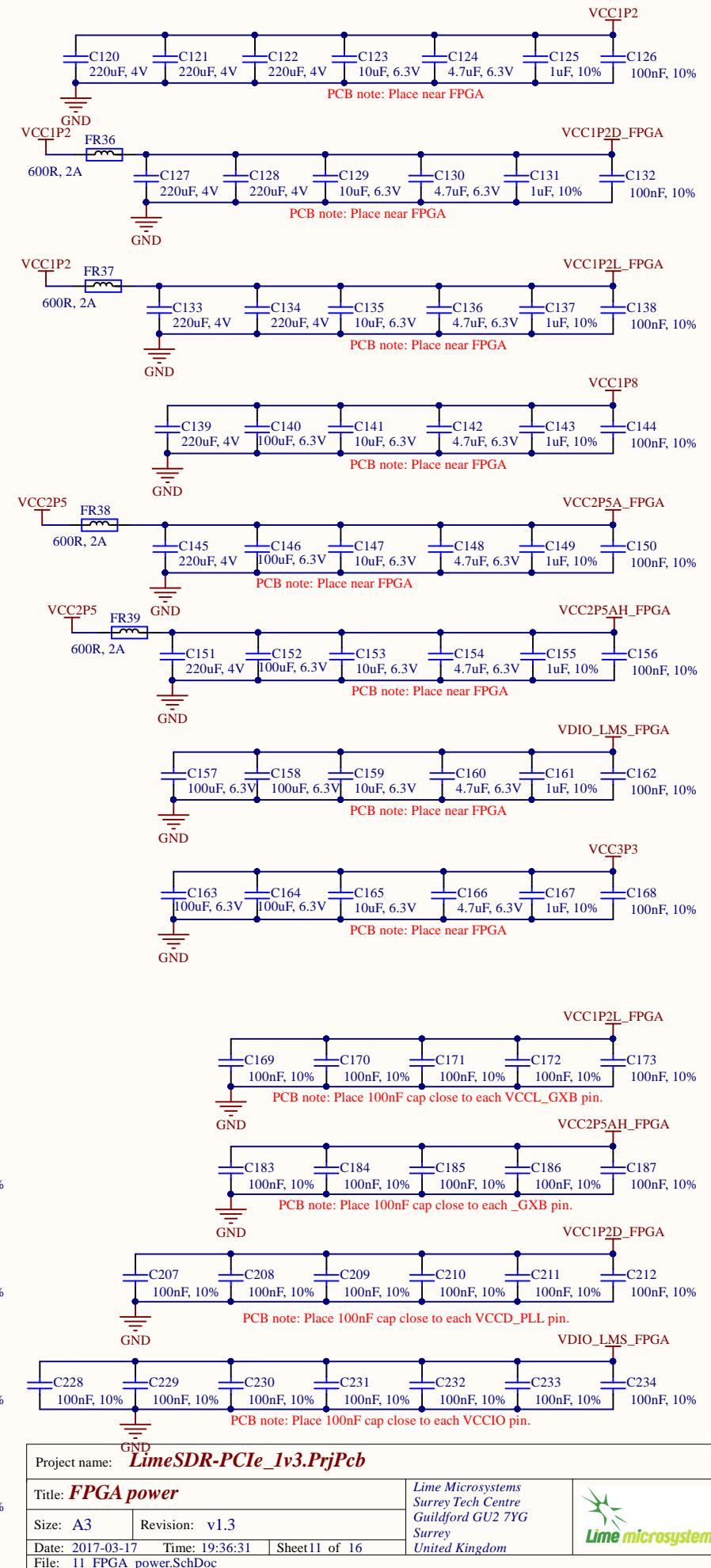
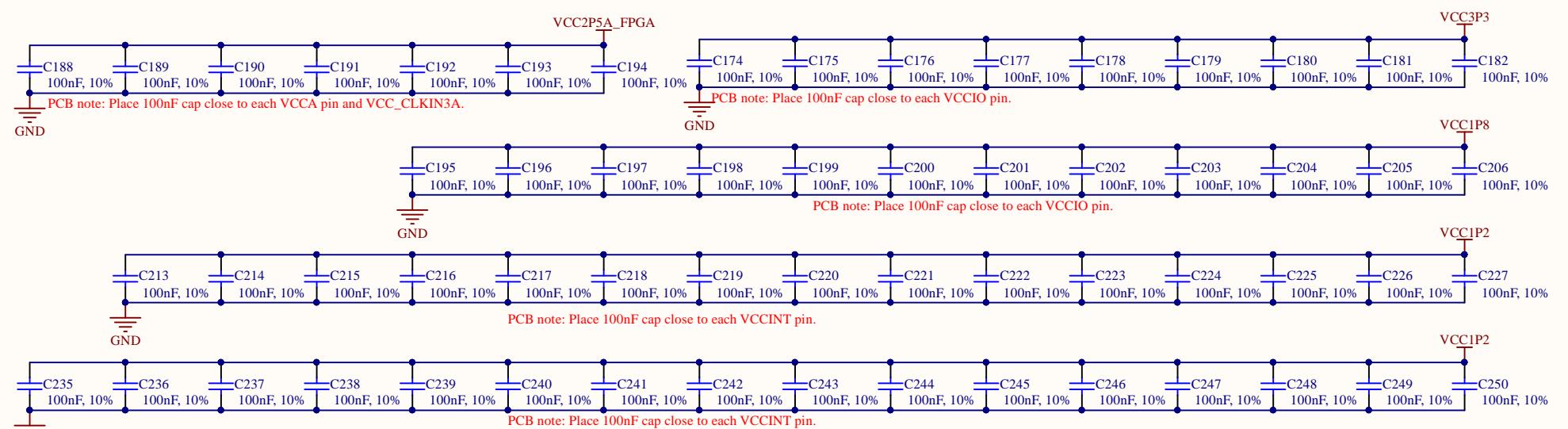
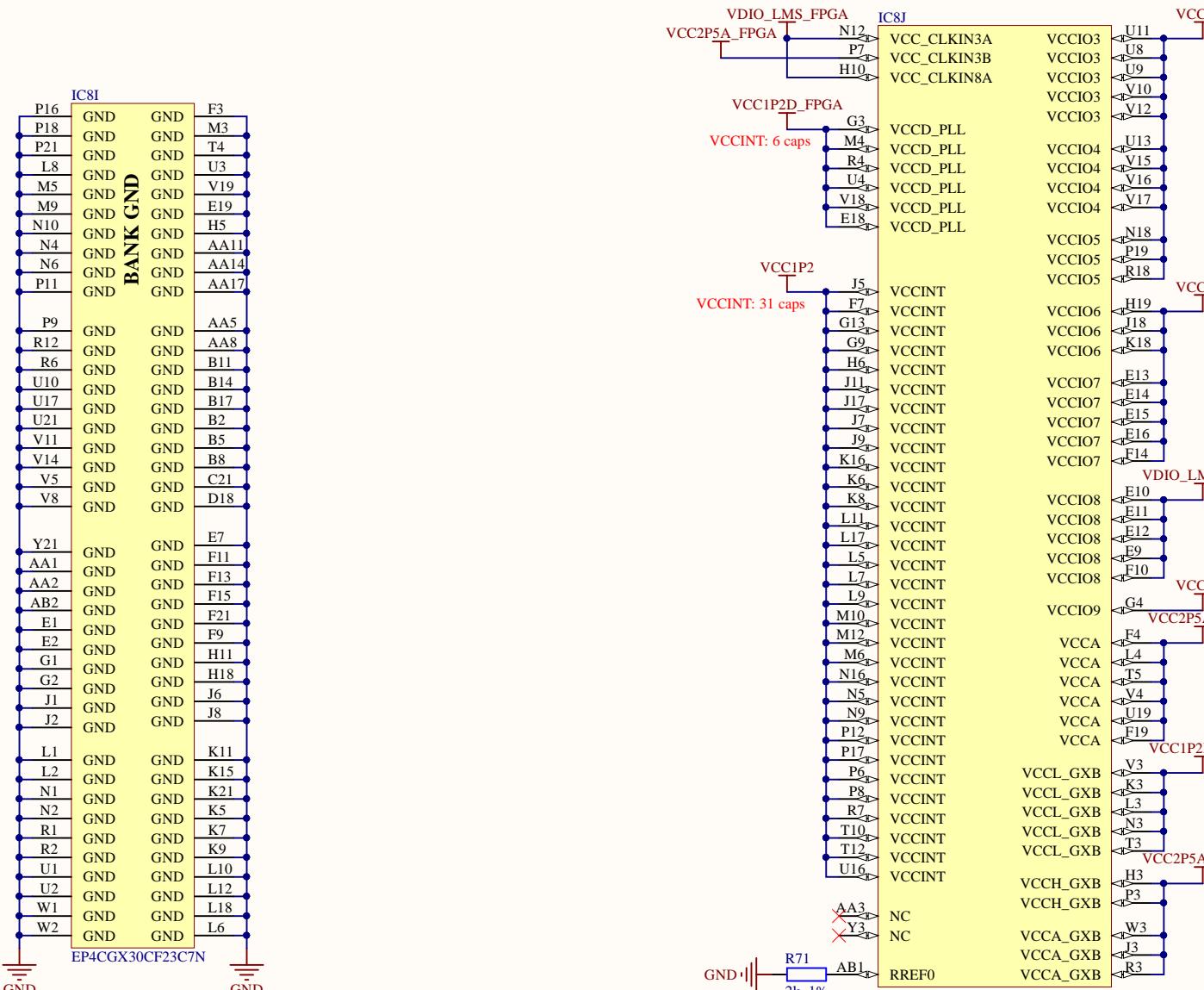
File: 10_FPGA_mis.SchDoc

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United Kingdom



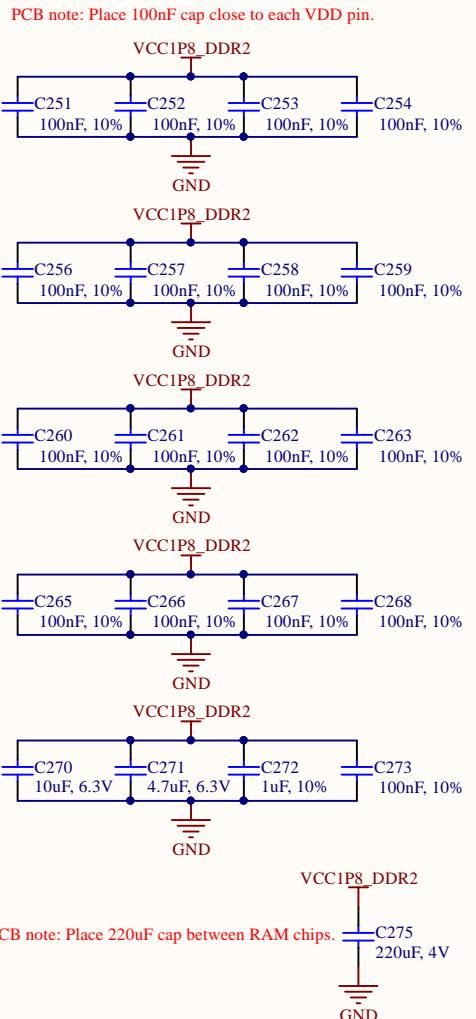
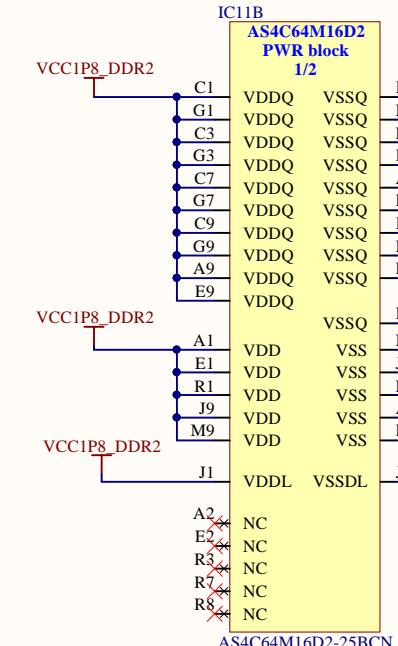
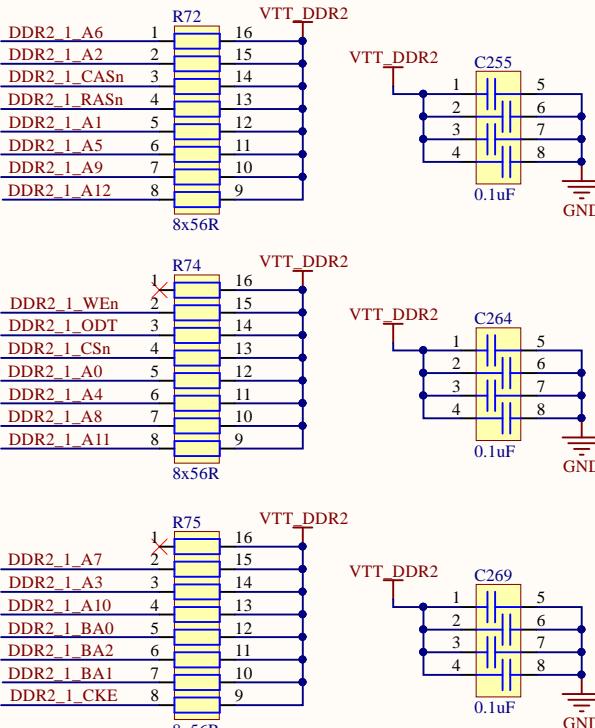
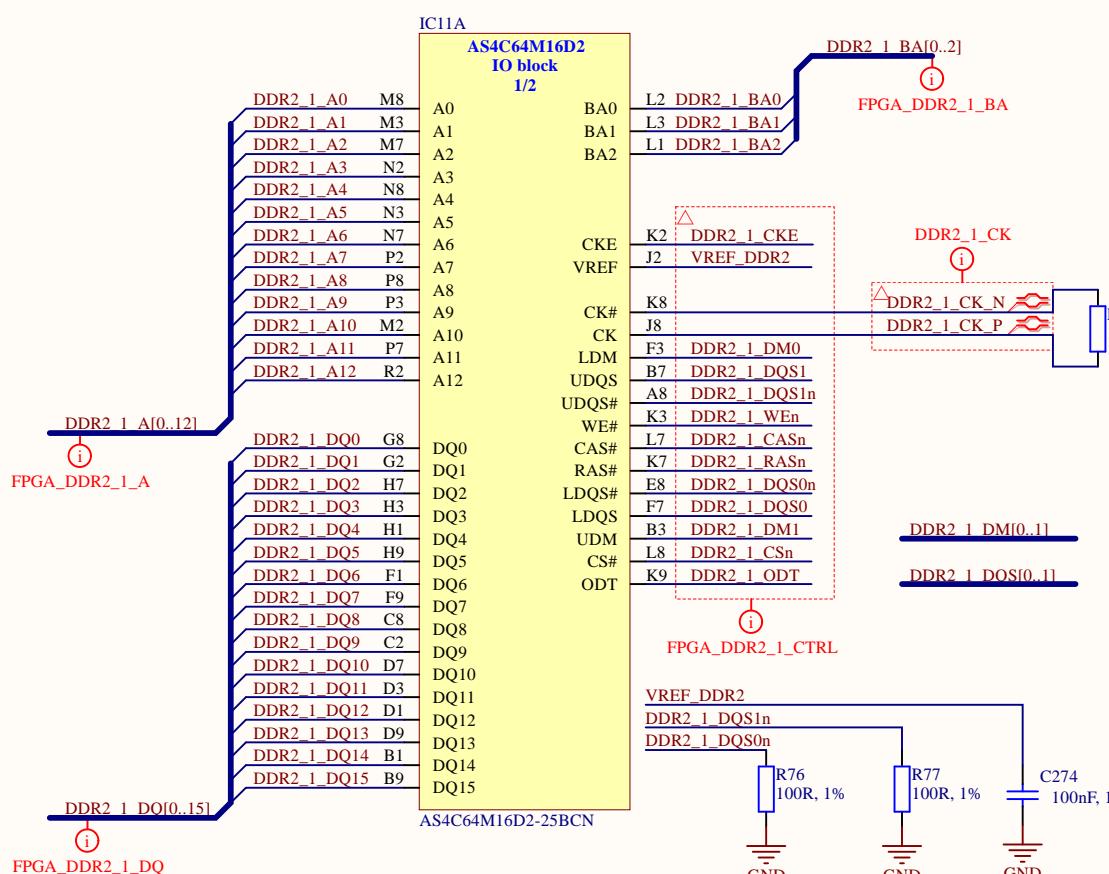
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Number of NF elements on sheet: 0

FPGA power

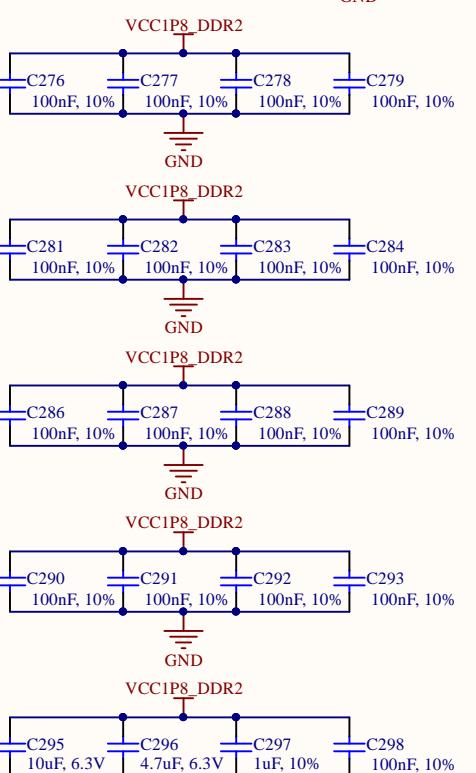
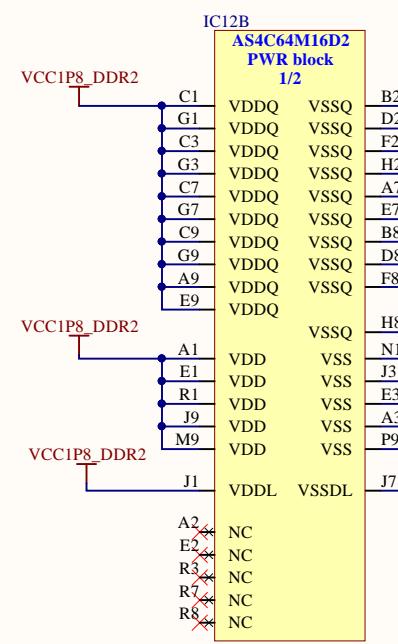
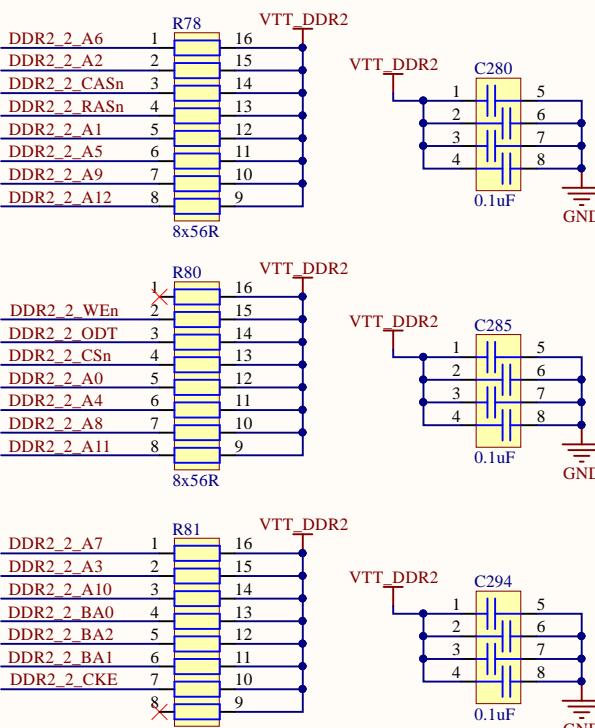
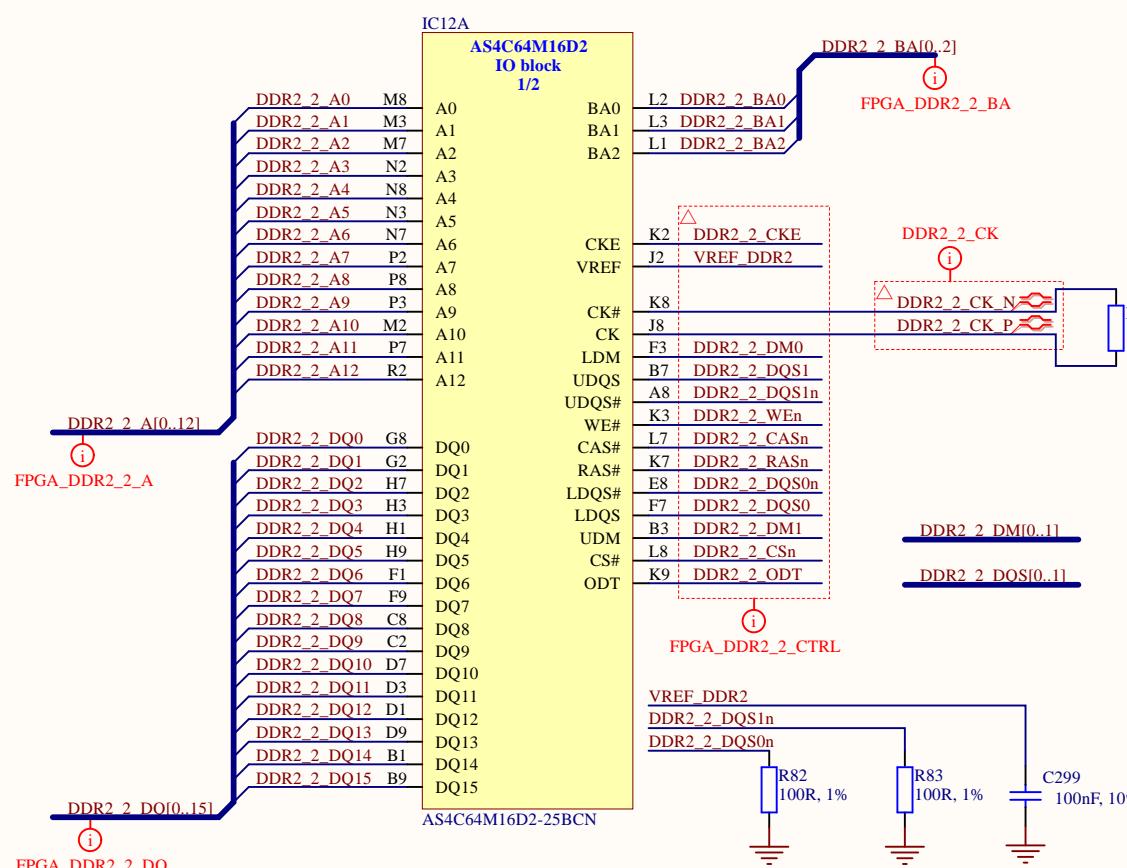


NF elements on sheet: -
Number of NF elements on sheet: 0

DDR2_1 (BOT L)



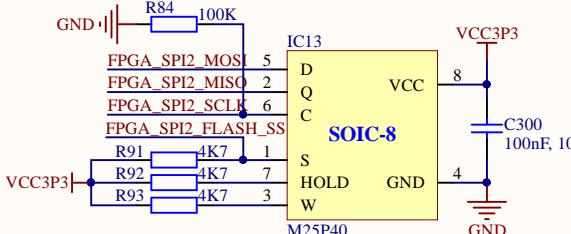
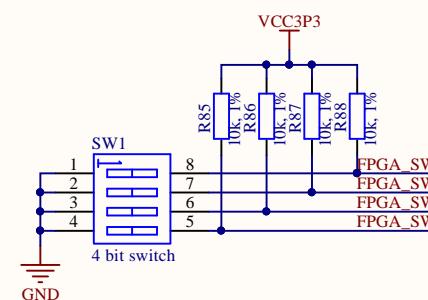
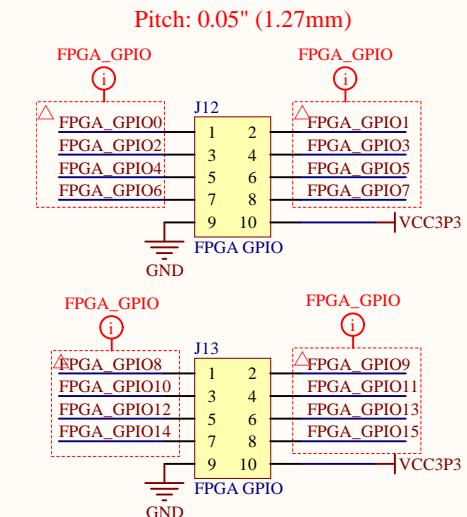
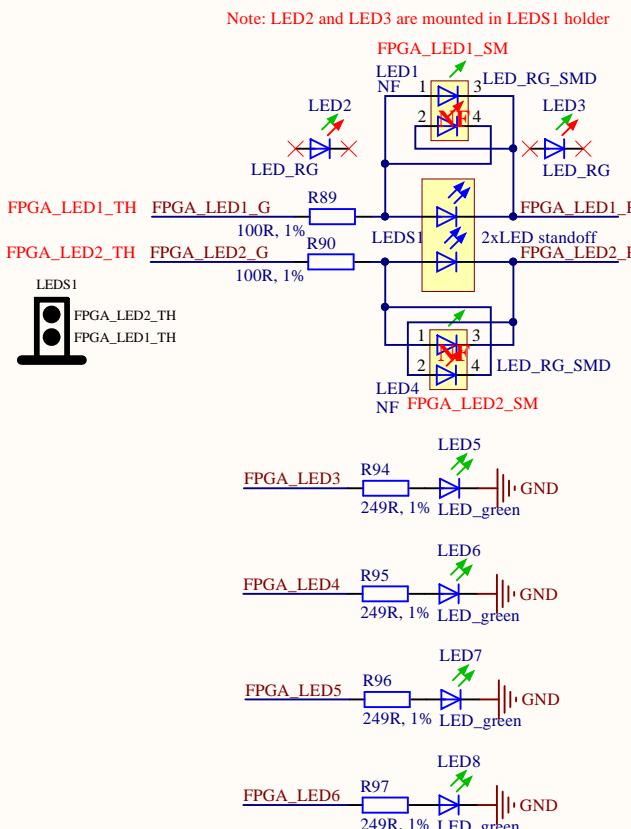
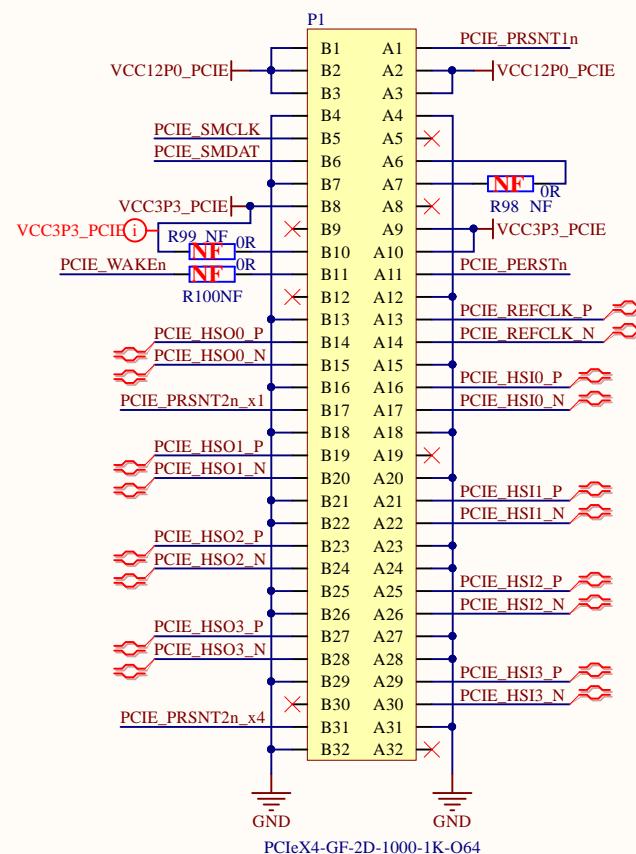
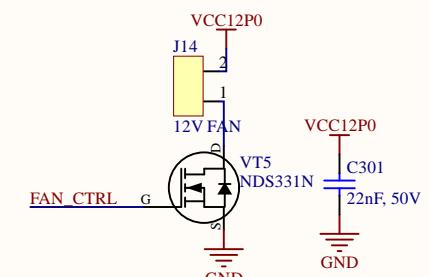
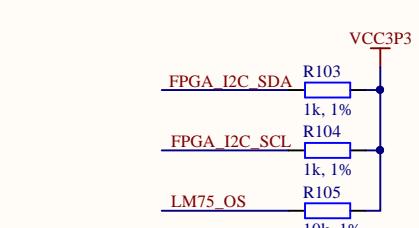
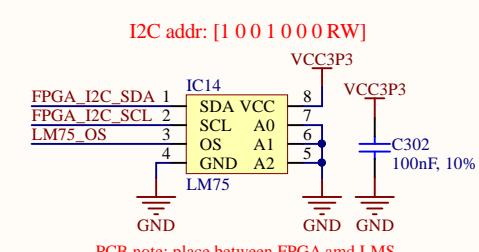
DDR2_2 (BOT R)



Project name: LimeSDR-PCIe_1v3.PjrPcb		 GND
Title: DDR2		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>
Size: A3	Revision: v1.3	
Date: 2017-03-17 Time: 19:36:34		Sheet 12 of 16
File: 12_DDR2_S1.Dwg		

NF elements on sheet: R98, R99, R100, LED1, LED4

Number of NF elements on sheet: 5

Peripherals**FPGA Flash****FPGA SW****FPGA GPIO****FPGA LED****PCI Express x4****FAN control****I2C Temperature sensor**Project name: **LimeSDR-PCIe_1v3.PrjPcb**Title: **Peripherals**Size: **A3** Revision: **v1.3**Date: **2017-03-17** Time: **19:36:37** Sheet**13** of **16**File: **13_Periph.SchDoc**Lime Microsystems
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Guildford GU2 7YG
Surrey
United Kingdom

PCB note: Place 100nF cap close to each PCIe power pin.
 VCC3P3_PCIE
 C304 100nF, 10% C305 100nF, 10% C306 100nF, 10%
 GND
 VCC12P0_PCIE
 C307 22nF, 50V C308 22nF, 50V C309 22nF, 50V C310 22nF, 50V C311 22nF, 50V
 GND

PCB note: Place 22nF cap close to each PCIe power pin.
 VCC3P3_PCIE
 C304 100nF, 10% C305 100nF, 10% C306 100nF, 10%
 GND
 VCC12P0_PCIE
 C307 22nF, 50V C308 22nF, 50V C309 22nF, 50V C310 22nF, 50V C311 22nF, 50V
 GND

A

A

B

B

C

C

D

D

1

2

3

4

5

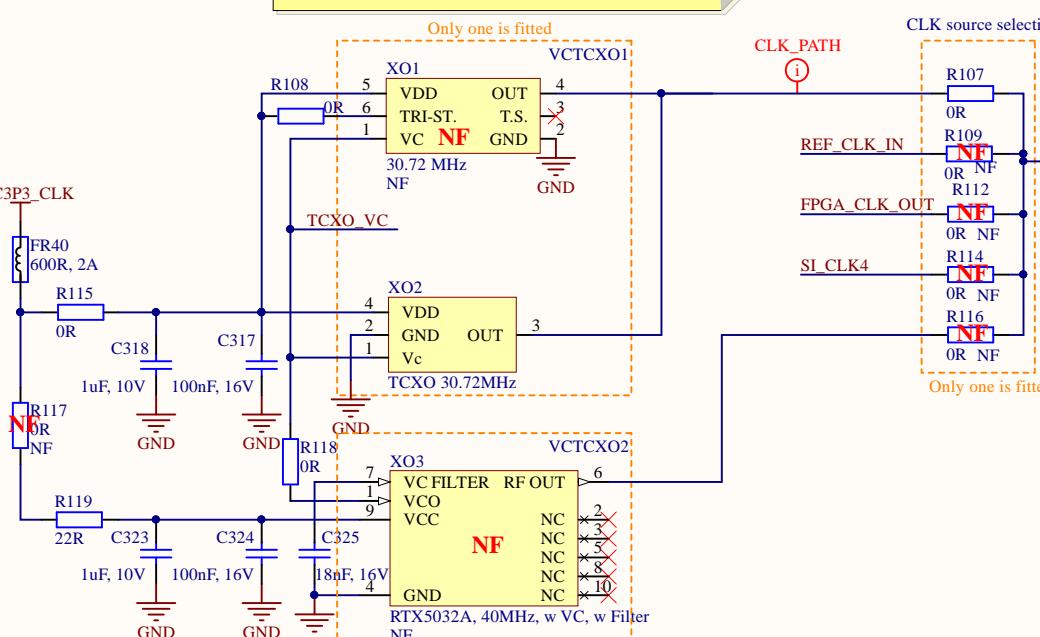
6

7

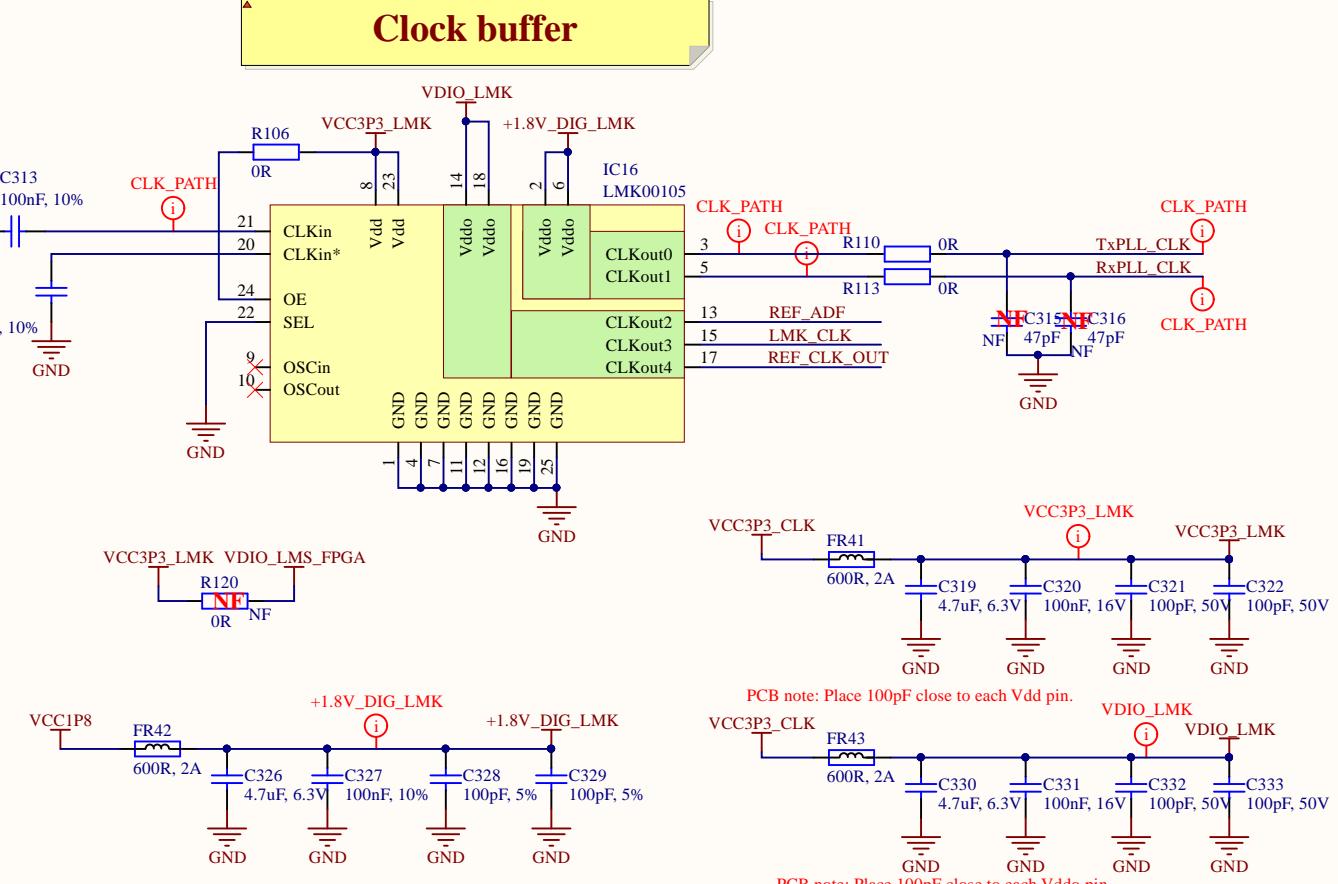
8

Clock circuits 1

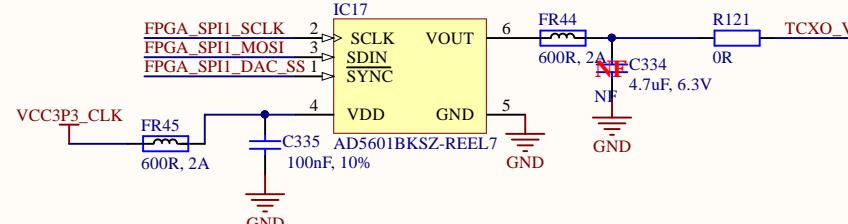
(VC)TCXO



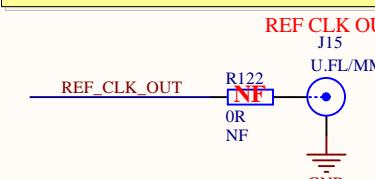
Clock buffer



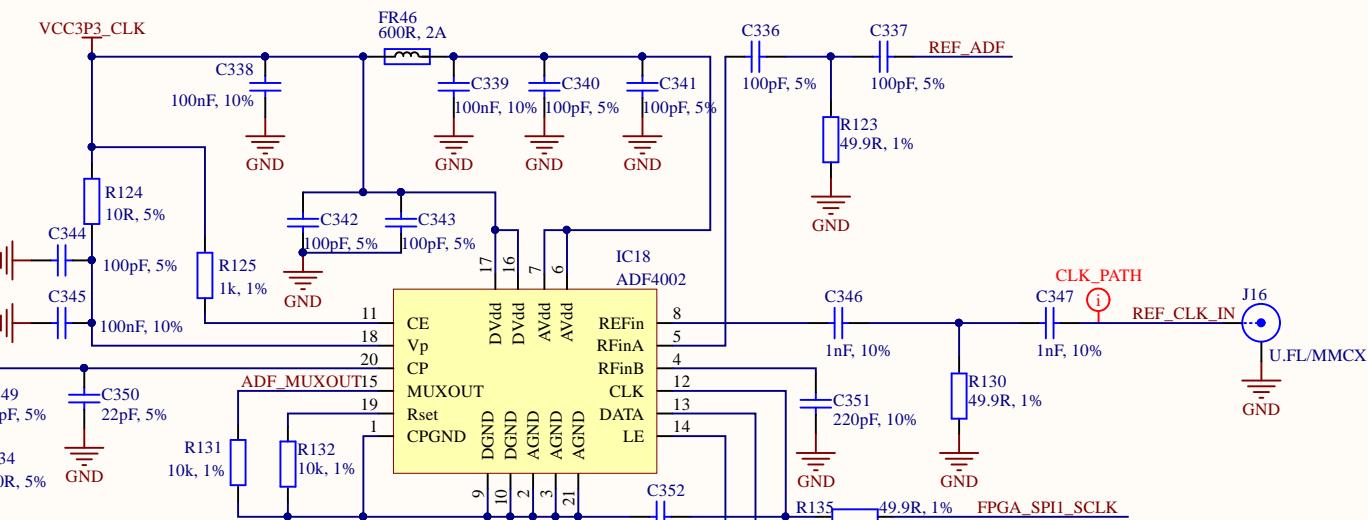
DAC



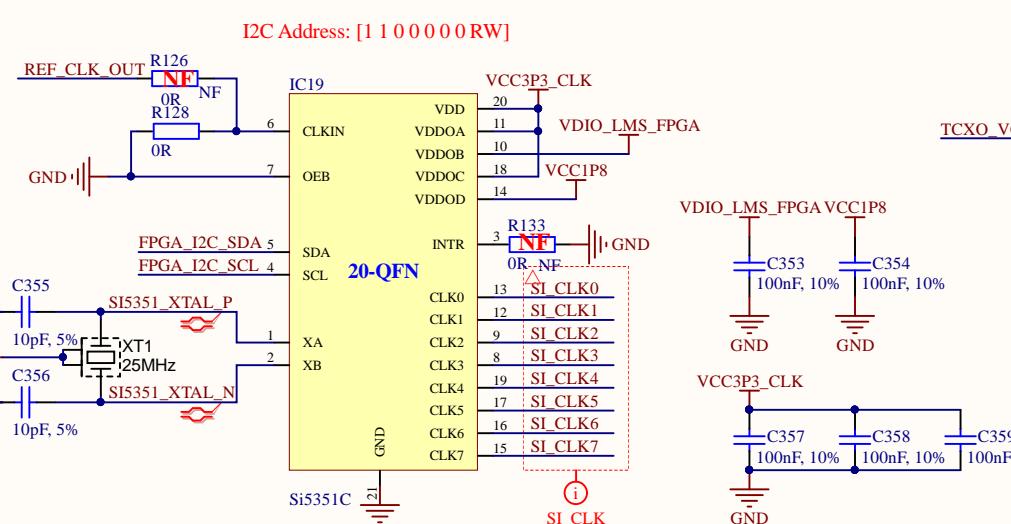
REF CLK OUT



Phase Detector



Clock generator



Project name: LimeSDR-PCIe_1v3.PrjPcb

Title: Clocks 1

Size: A3 Revision: v1.3

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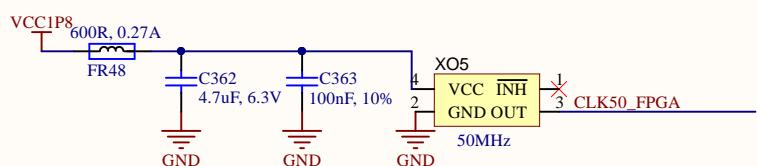
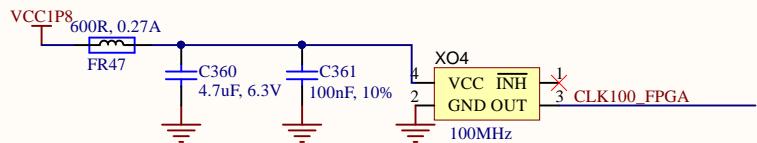
Date: 2017-03-17 Time: 19:36:40 Sheet 14 of 16

File: 14_Clocks_1.SchDoc

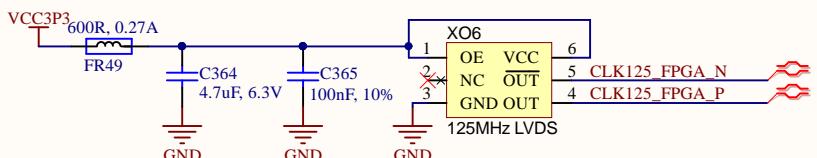
NF elements on sheet: -
Number of NF elements on sheet: 0

Clock circuits 2

SE Crystal Oscillators



LVDS Crystal Oscillators



Project name: LimeSDR-PCIe_Inv3.PrjPcb

Title: Clocks 2

Size: A4 Revision: v1.3

Date: 2017-03-17 Time: 19:36:43 Sheet 15 of 16

File: 15_Clocks_2.SchDoc

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Board power circuits

