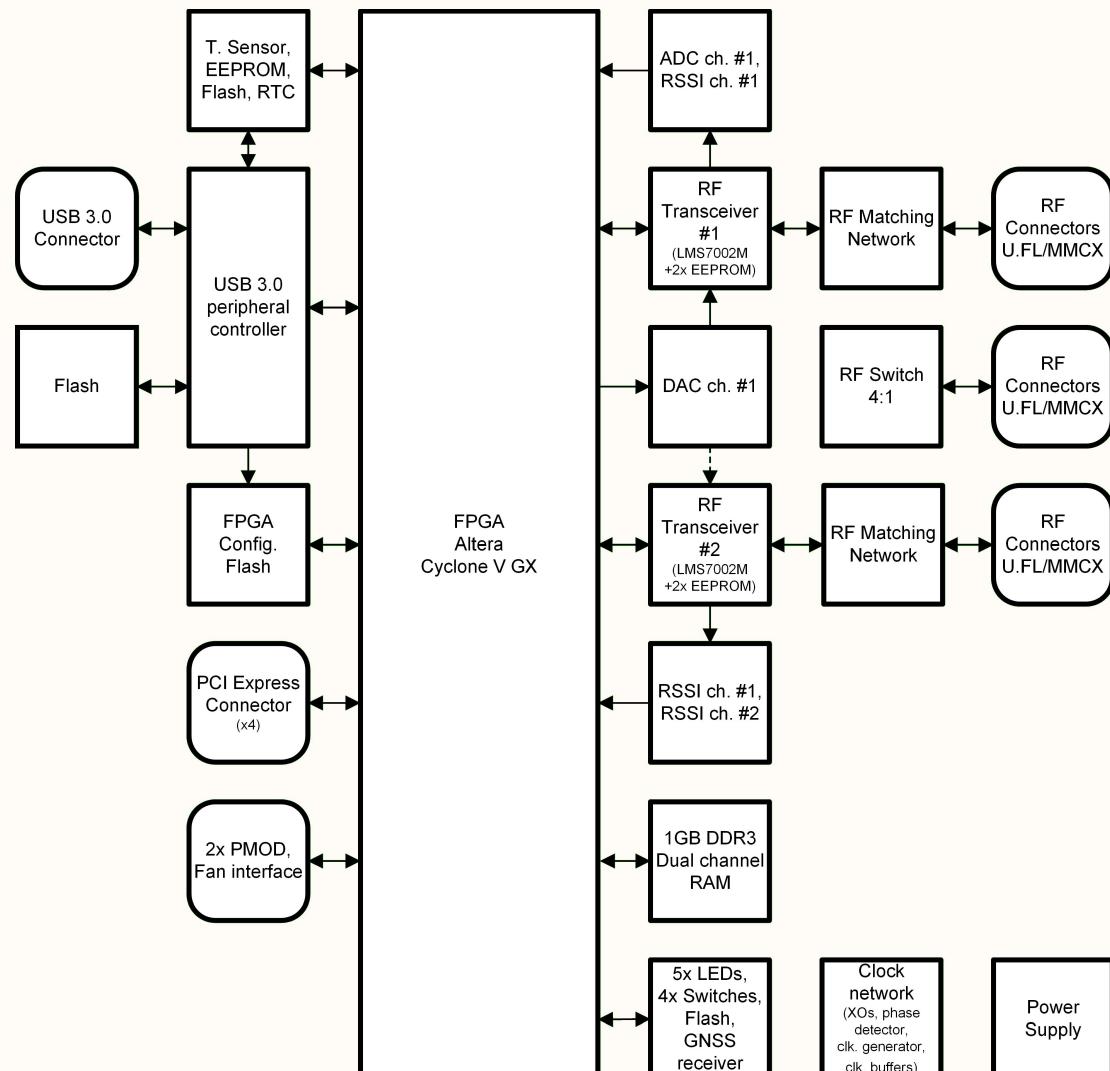


Block diagram



Project name: **LimeSDR-QPCIE_Iv2.PjrPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.2**

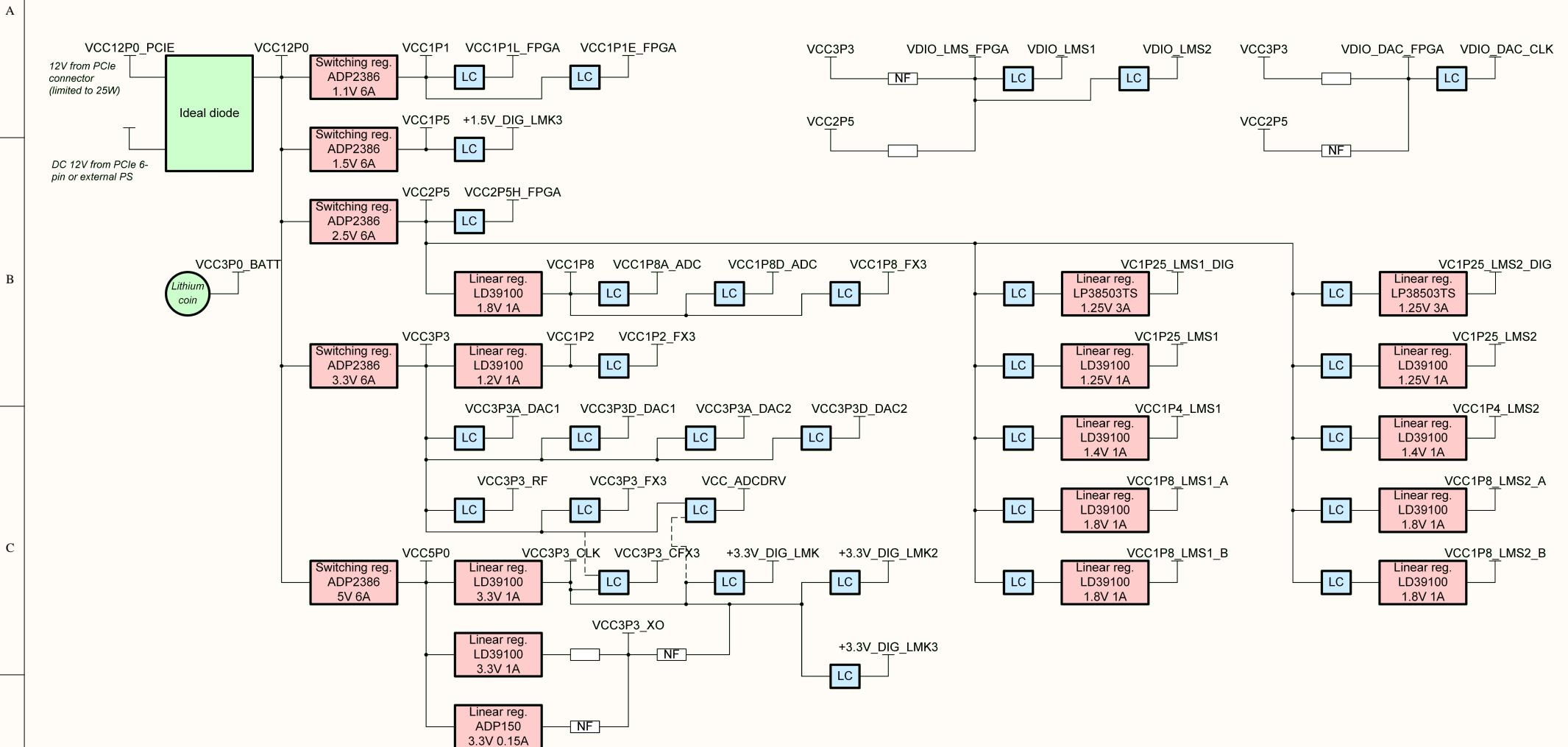
Date: **2017-09-22** Time: **15:47:08** Sheet **1** of **27**

File: **01_BlockDiagram.SchDoc**

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Surrey
United Kingdom



Power diagram



Project name: **LimeSDR-QPCIE_Inv2.PrbPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.2**

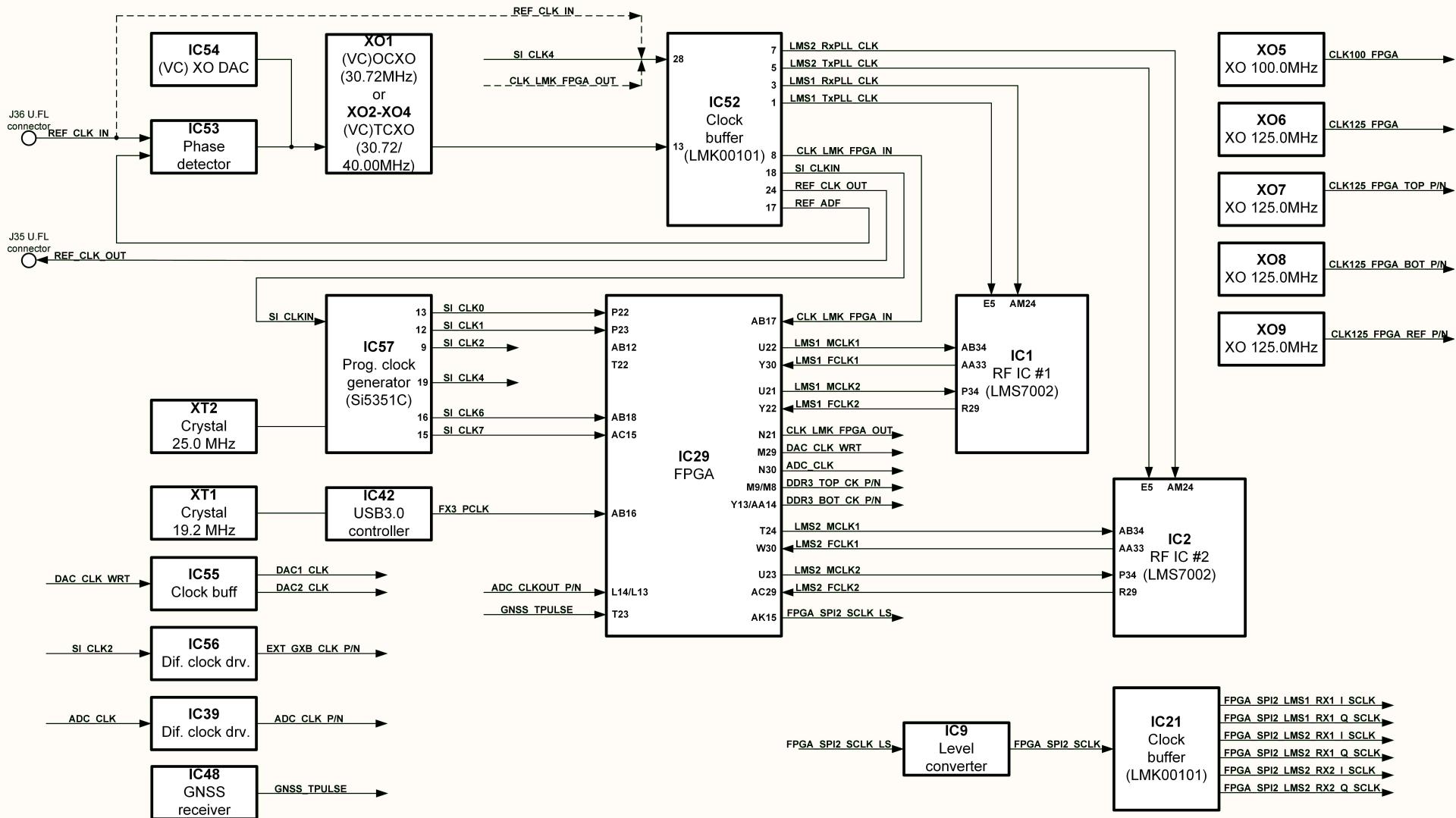
Date: **2017-09-22** Time: **15:47:19** Sheet **2** of **27**

File: **02_PowerDiagram.SchDoc**

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Surrey
United Kingdom



Clock diagram



Project name: *LimeSDR-QPCe_Inv2.PrbPcb*

Title: *Clock diagram*

Size: **A4** Revision: **v1.2**

Date: **2017-09-22** Time: **15:47:39** Sheet**3** of **27**

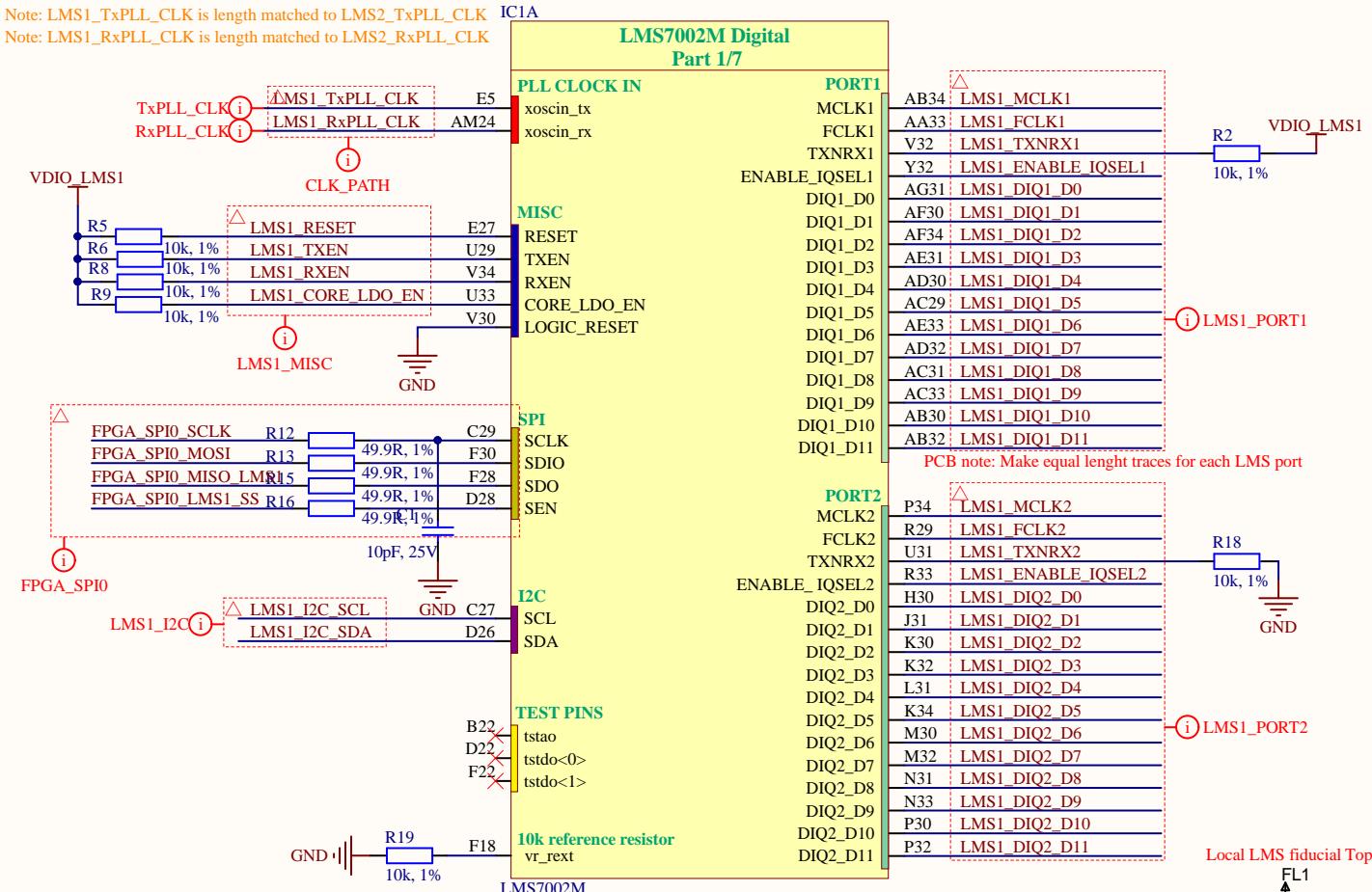
File: **03_ClockDiagram.SchDoc**

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United Kingdom

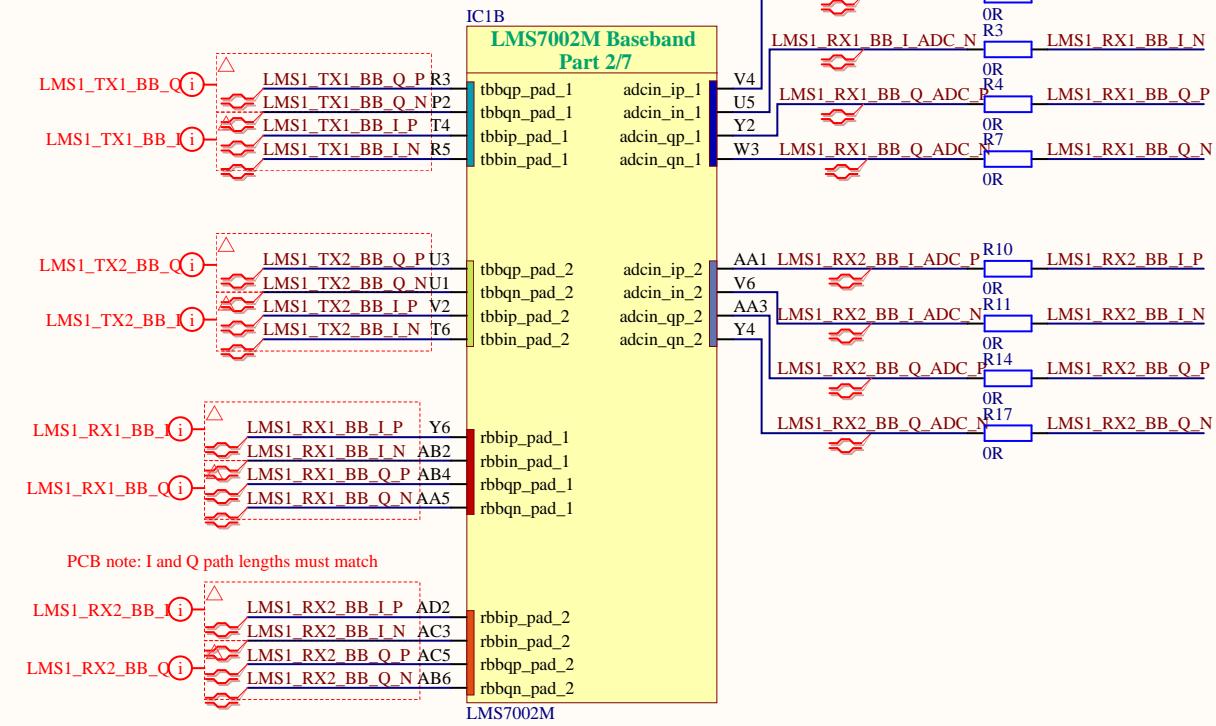


NF elements on sheet: -
Number of NF elements on sheet: 0

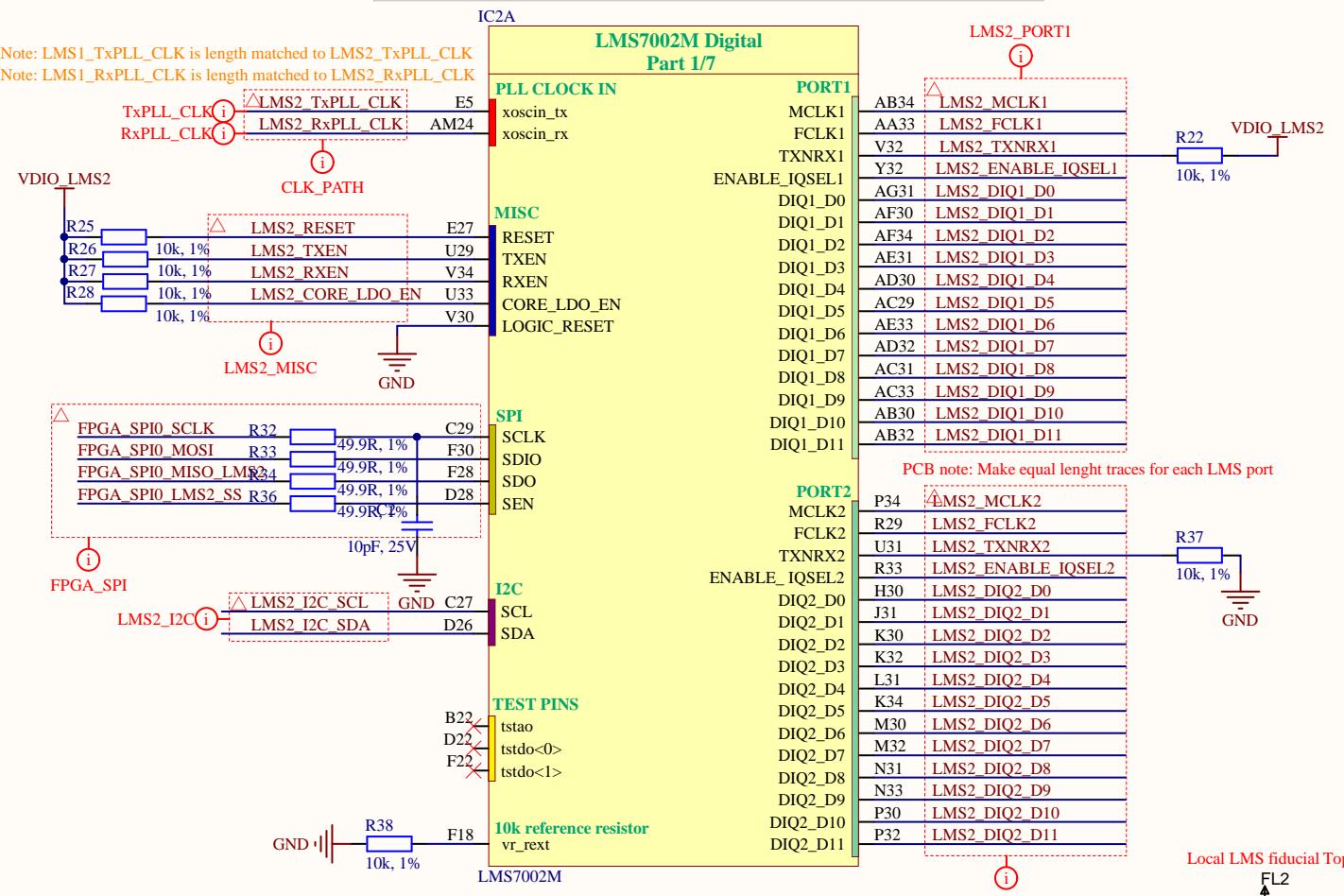
LMS7002M #1 digital



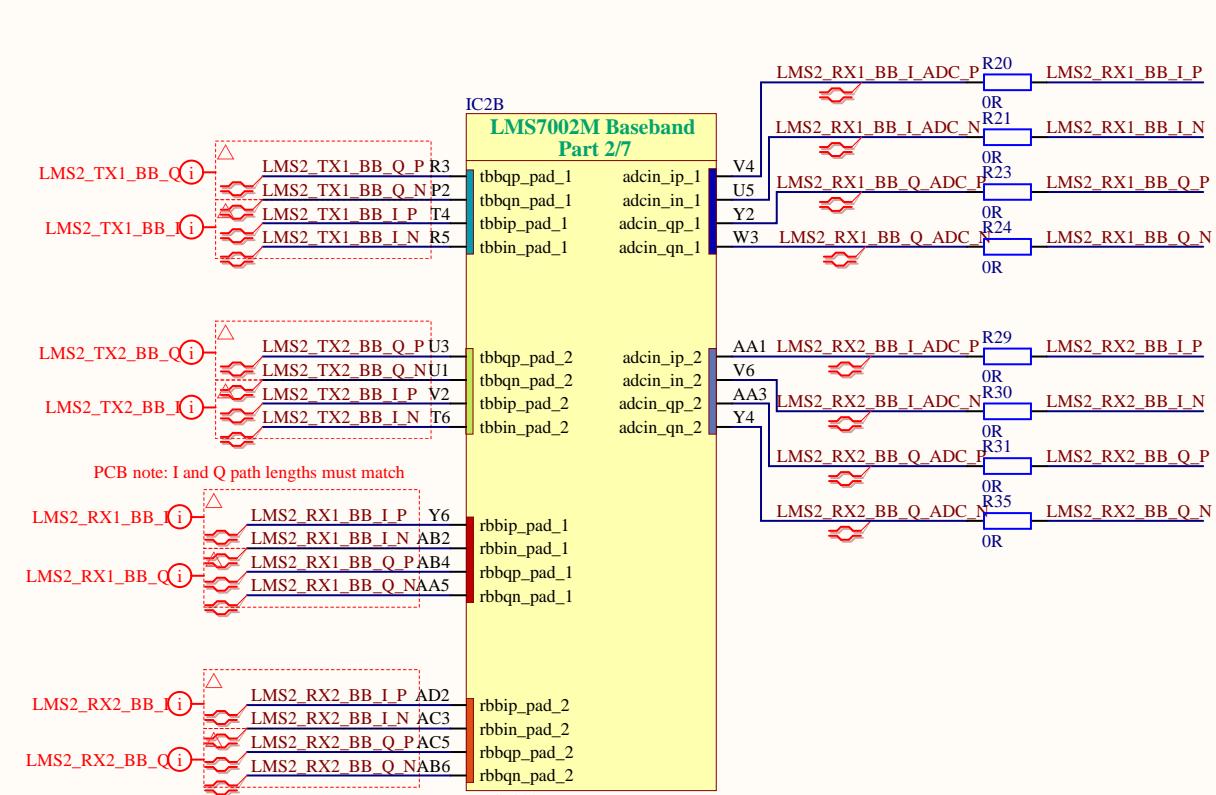
LMS #1 BB



LMS7002M #2 digital



LMS #2 BB



Project name: LimeSDR-QPCIe_1v2.PrbPcb

Title: LMS7002M #1 digital circuit

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Size: A3 Revision: v1.2

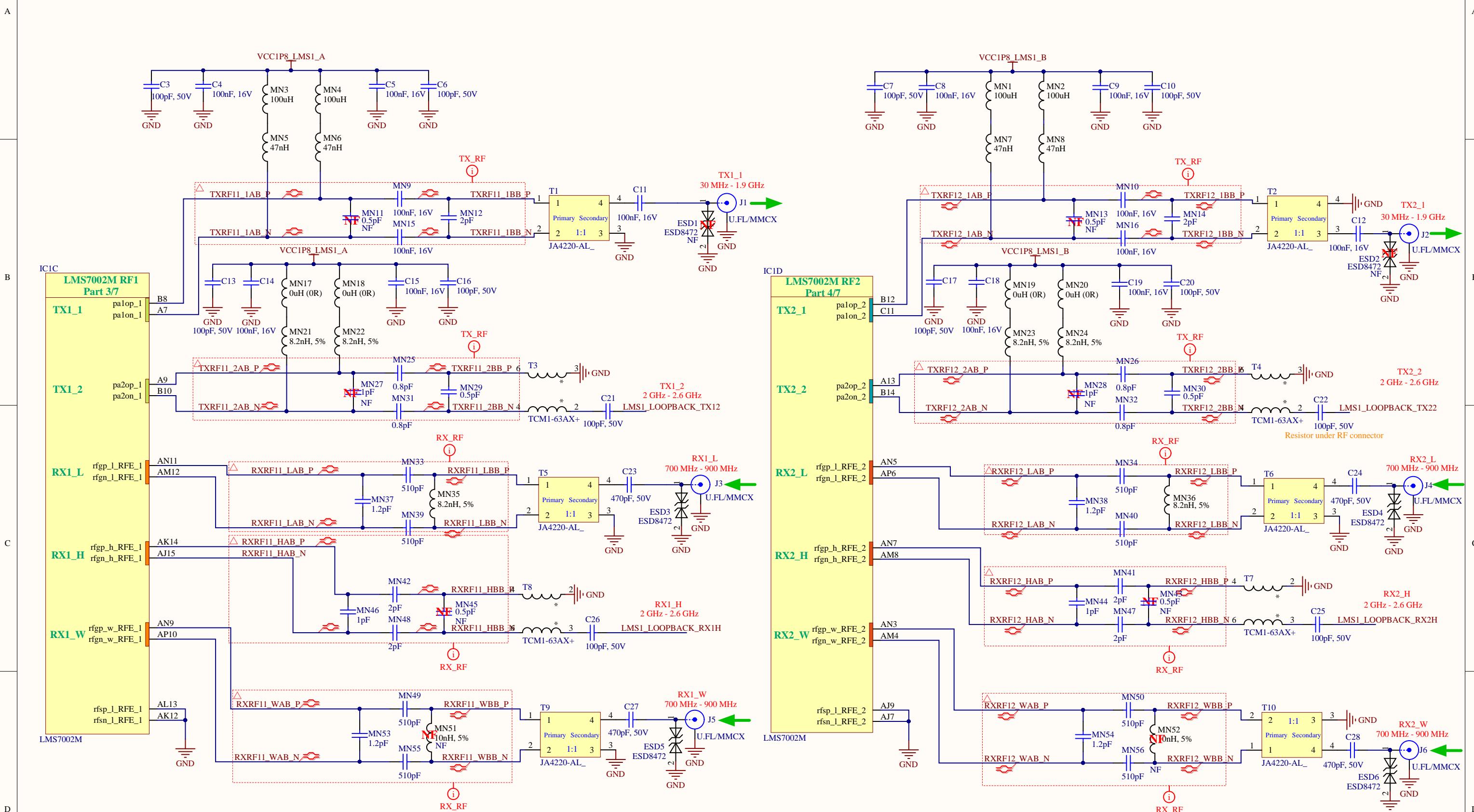
Date: 2017-09-22 Time: 15:47:53 Sheet 4 of 27

File: 04 LMS7002M_Digital.SchDoc

NF elements on sheet: MN11, MN13, MN27, MN28, MN43, MN45, MN51, MN52, ESD1, ESD2

Number of NF elements on sheet: 10

LMS7002M #1 RF circuits



Project name: LimeSDR-QPCIE_1v2.PrcPcb

Title: LMS7002M #1 RF

Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:47:58 Sheet 5 of 27

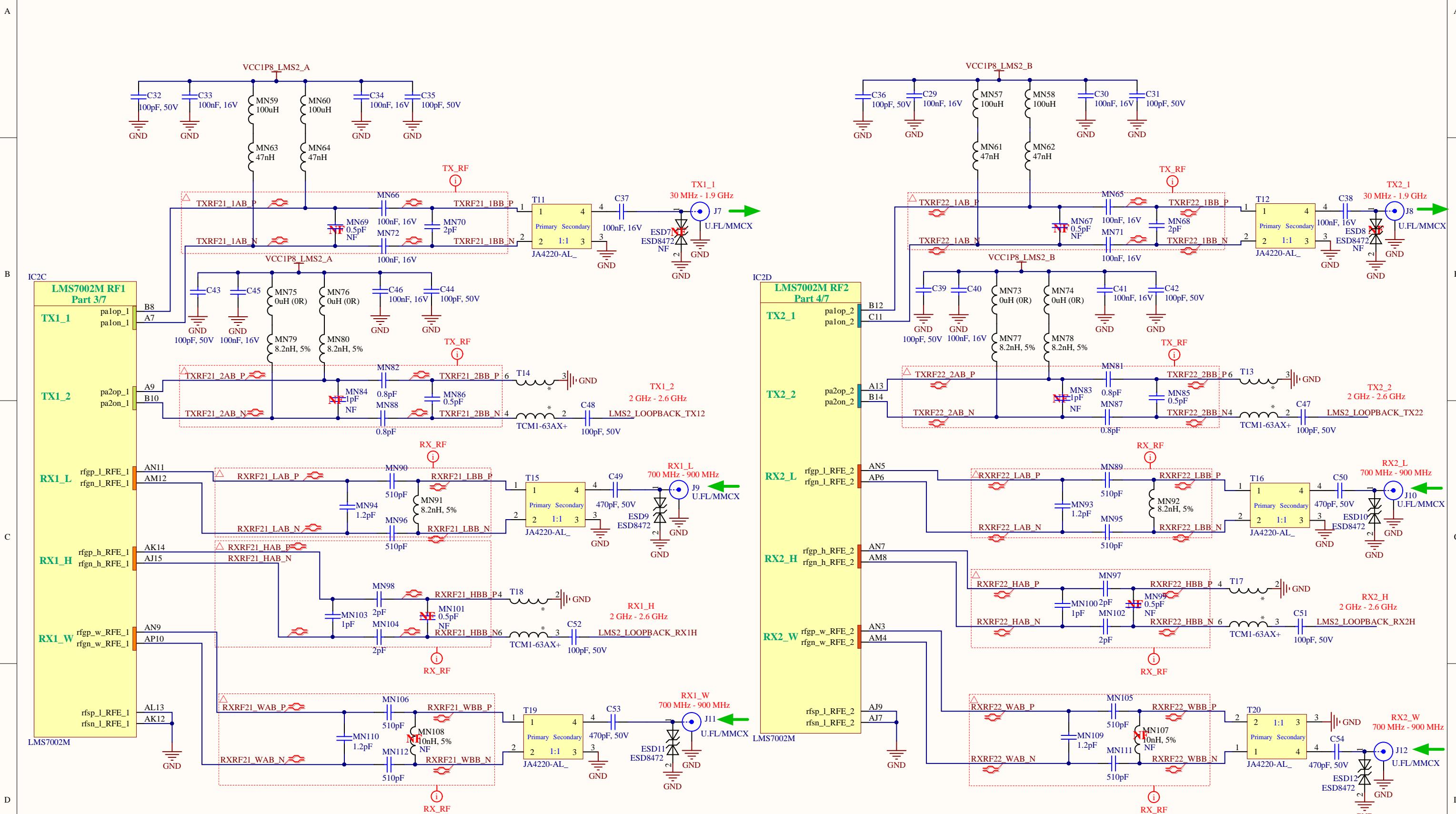
File: 05_LMS7002M_1_RF.SchDoc

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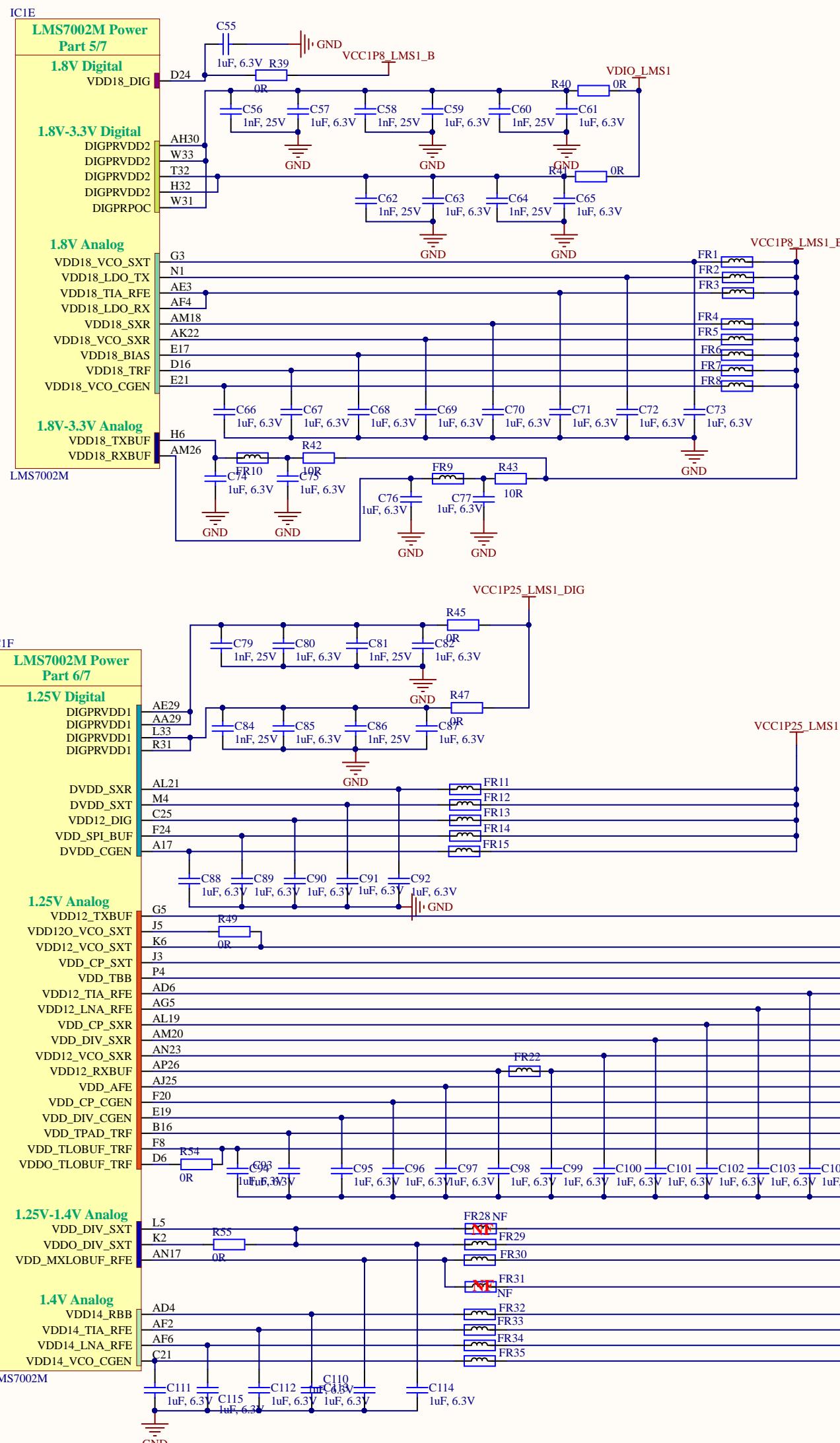
NF elements on sheet: MN67, MN69, MN83, MN84, MN101, MN99, MN107, MN108, ESD7, ESD8
Number of NF elements on sheet: 10

LMS7002M #2 RF circuits



NF elements on sheet: FR28, FR31
Number of NF elements on sheet: 2

LMS7002M #1 power supply circuit



IC1G		LMS7002M GND Part 7/7	
N3	Digital gnd	Analog gnd	L3
AM22	DGND_SXT	GND_DIV_SXT	K4
E25	DGND_SXR	GND_CP_SXT	AN25
C23	GND_SPL_BUF	GND_RXBUF	AK20
B18	GND_DIG	GND_DIV_SXR	AJ19
J33	DGND_CGEN	GND_CP_SXR	B20
AA31	DIGPRGND1	GND_CP_CGEN	F6
AG29	DIGPRGND1	GND_TXBUF	D20
T30	DIGPRGND1	GND_DIV_CGEN	AL23
W29	DIGPRGND1,2	GND_VCO_SXR	H2
G31	DIGPRGND1	GND_VCO_SXT	C7
AF32	DIGPRGND2	GND_TLOBUF_TRF	GND
Y30	DIGPRGND2	Thermal pad	
	DIGPRGND2	EP	

LMS7002M

Lia - SDR - ORGI - 1.0 B - ID: 1

Project name: LimeSDR-QPCIe_NV

Title: LM37002M #1 power

Date: 2017-09-22 Time: 15:48:08 Sheet 7 of 27

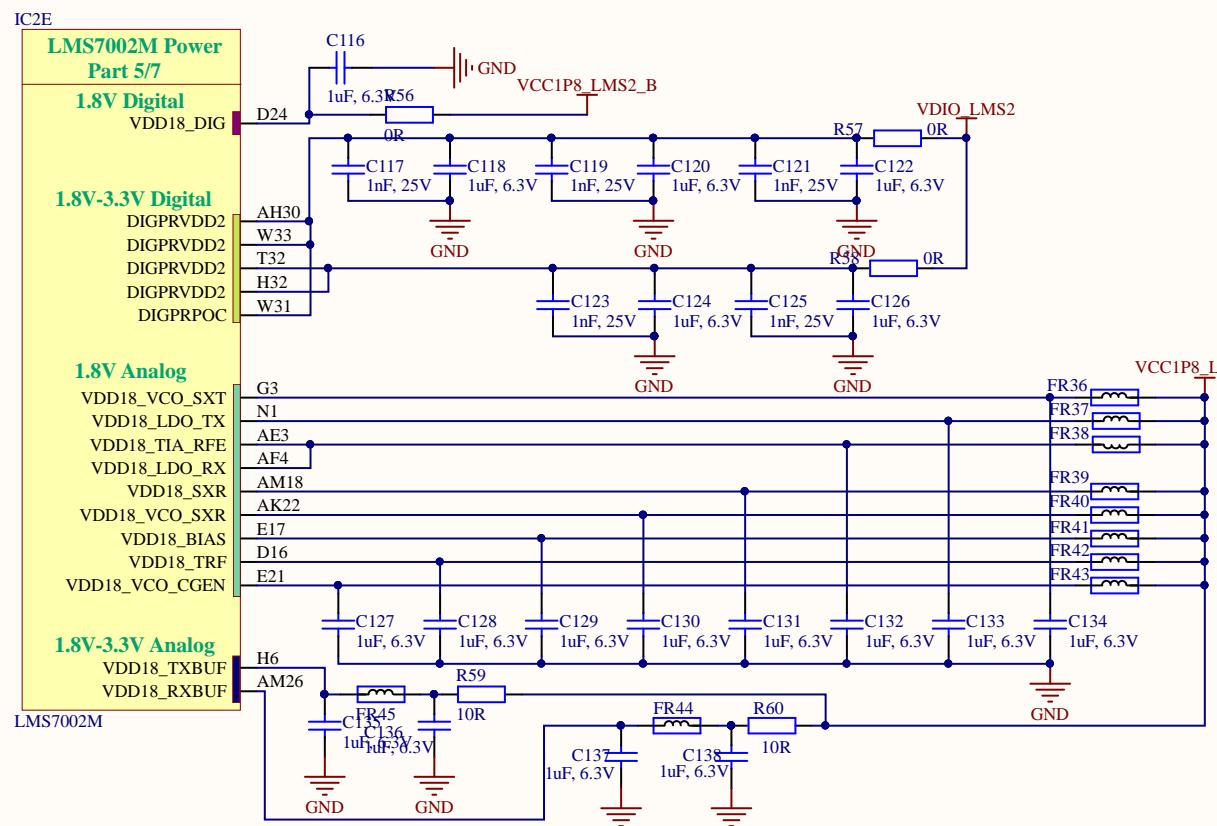
Date: 2017-09-22 Time: 15:48:08
File: 07_LMS7002M_1_Power.SchDoc

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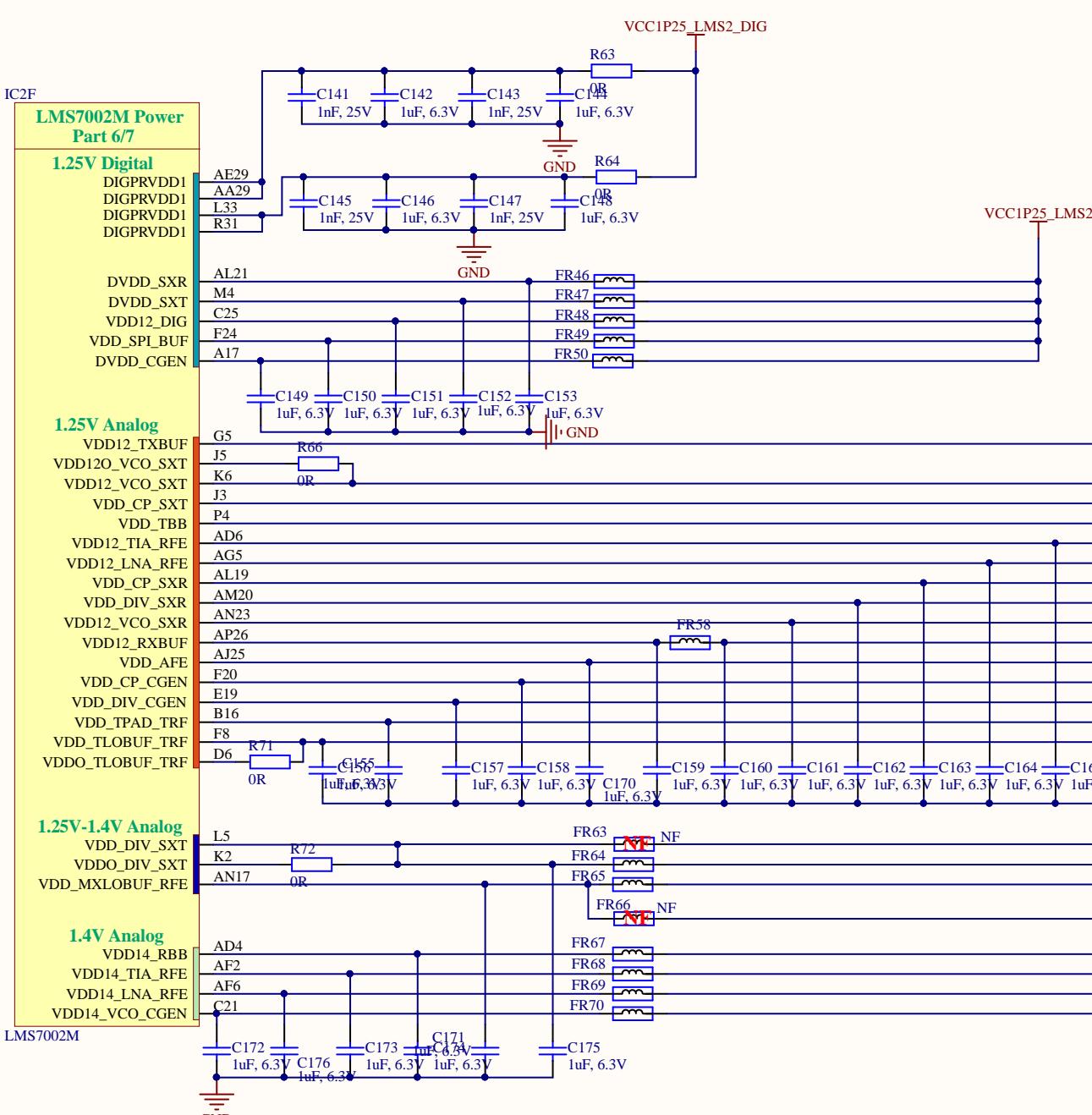
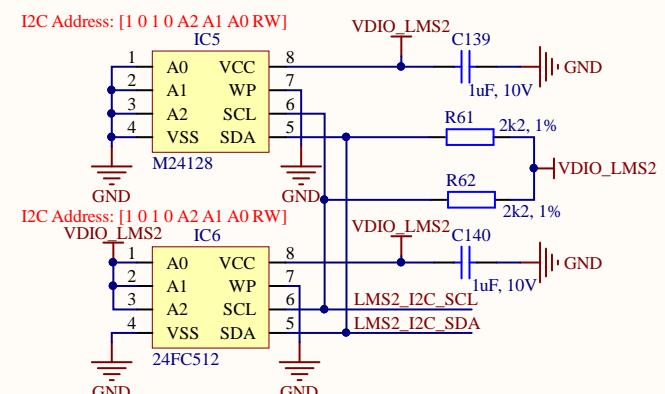


NF elements on sheet: FR63, FR66
Number of NF elements on sheet: 2

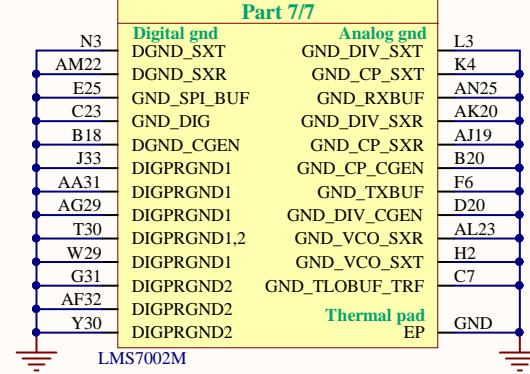
LMS7002M #2 power supply circuit



LMS #2 EEPROMs



LMS7002M GND Part 7/7



Project name: LimeSDR-QPCIE_1v2.PrbPcb

Title: LMS7002M #2 power supply

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Size: A3 Revision: v1.2

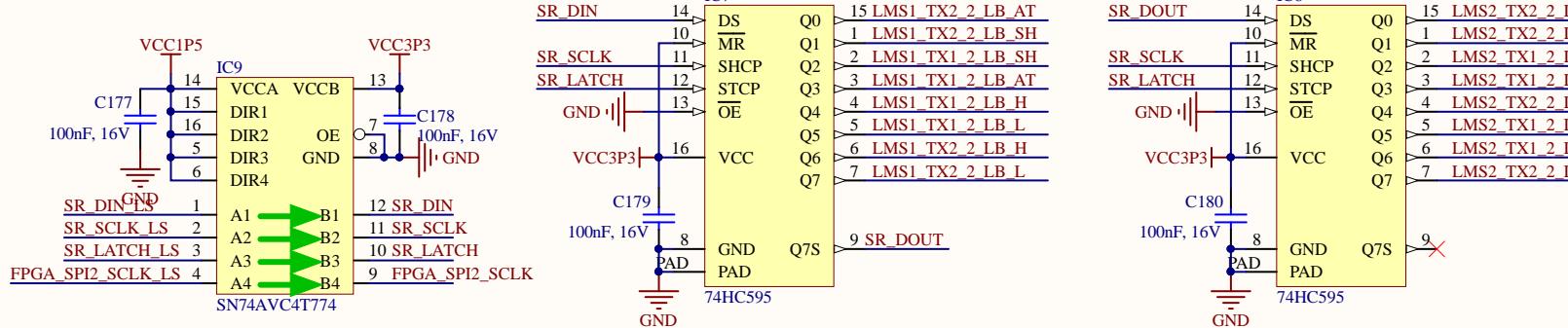
Date: 2017-09-22 Time: 15:48:14 Sheet 8 of 27

File: 08_LMS7002M_2_Power.SchDoc

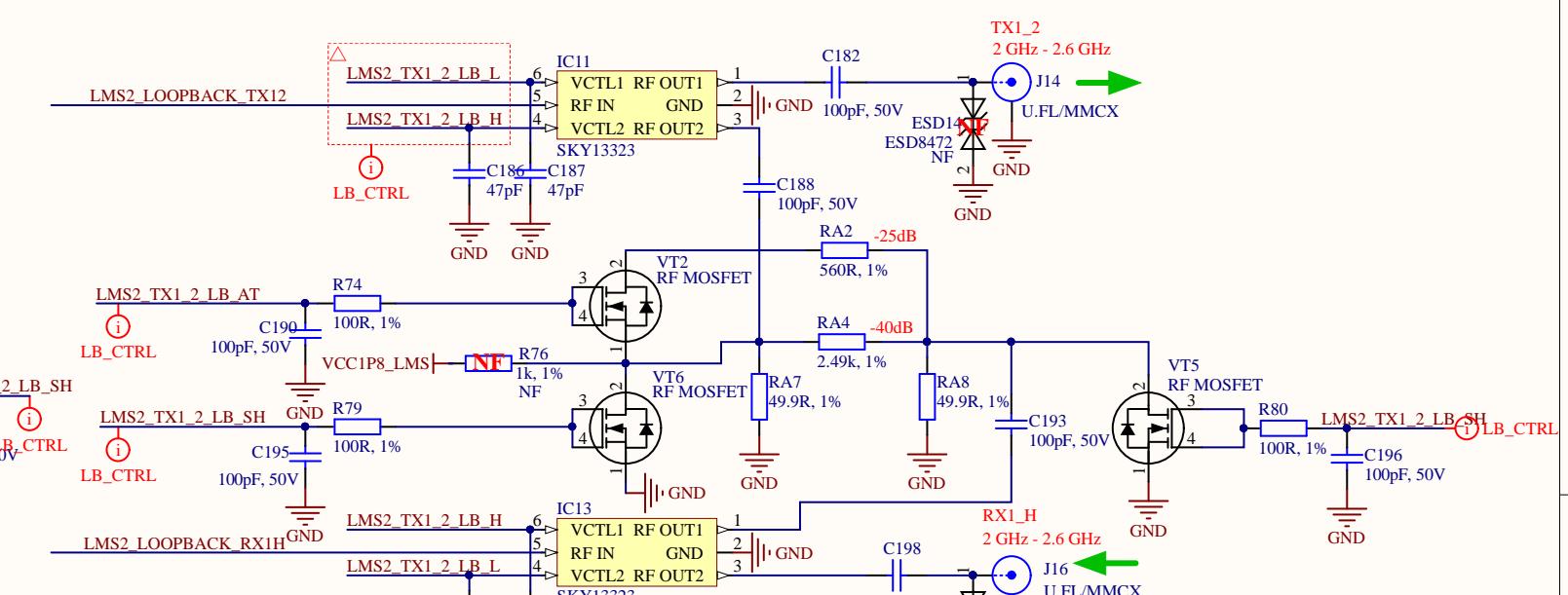
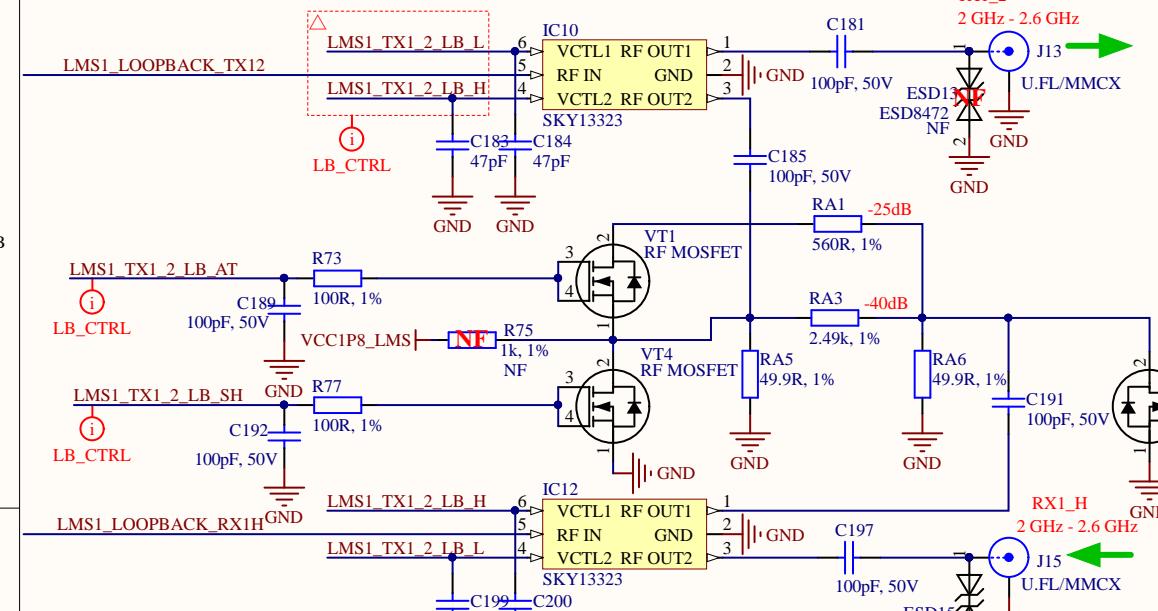
NF elements on sheet: R75, R76, R83, R84, MECH1-MECH18, ESD13, ESD14, ESD17, ESD18

Number of NF elements on sheet: 26

Loopback shift registers



LMS7002M #1 RF loopbacks



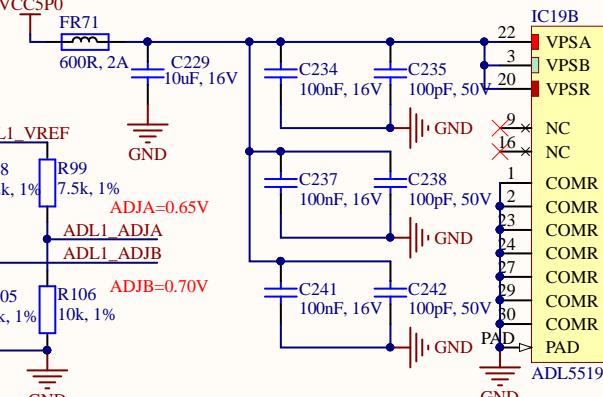
Project name: **LimeSDR-OPCIe_1v2.PrjPcb**

Title: Loopback		Lime Microsystems Surry Tech Centre Guildford GU2 7YG Surrey United Kingdom	 Lime microsystems
Size: A3	Revision: v1.2		
Date: 2017-09-22	Time: 15:48:19	Sheet 9 of 27	
File: 09_BE_Loopback_SchDoc			

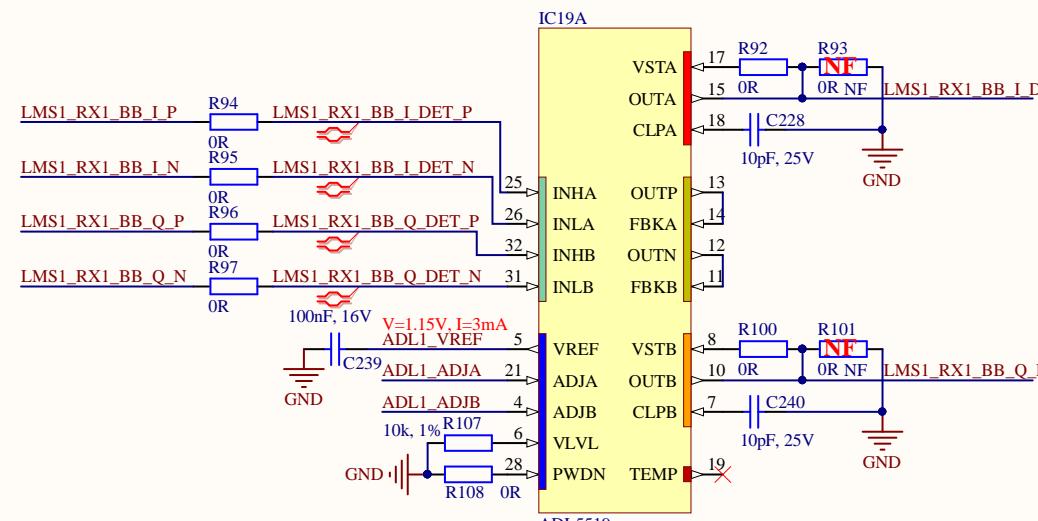
NF elements on sheet: C225, R93, C236, R101, ESD21, ESD22, ESD23, ESD24, ESD25

Number of NF elements on sheet: 9

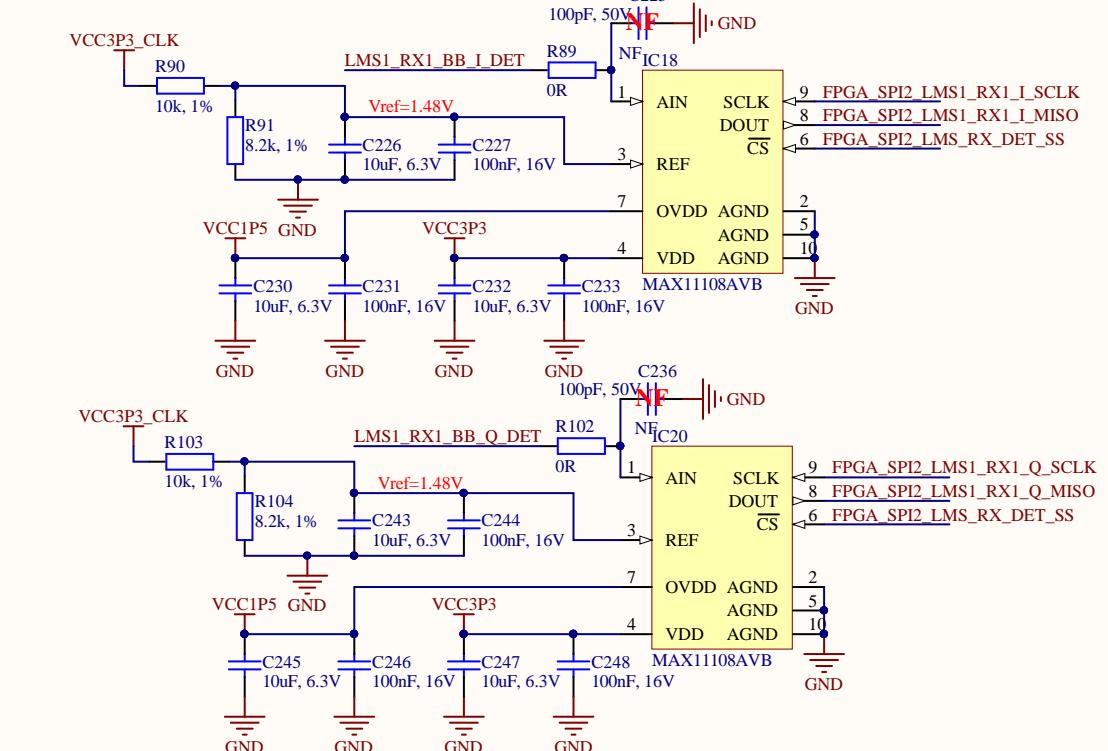
Log Detector



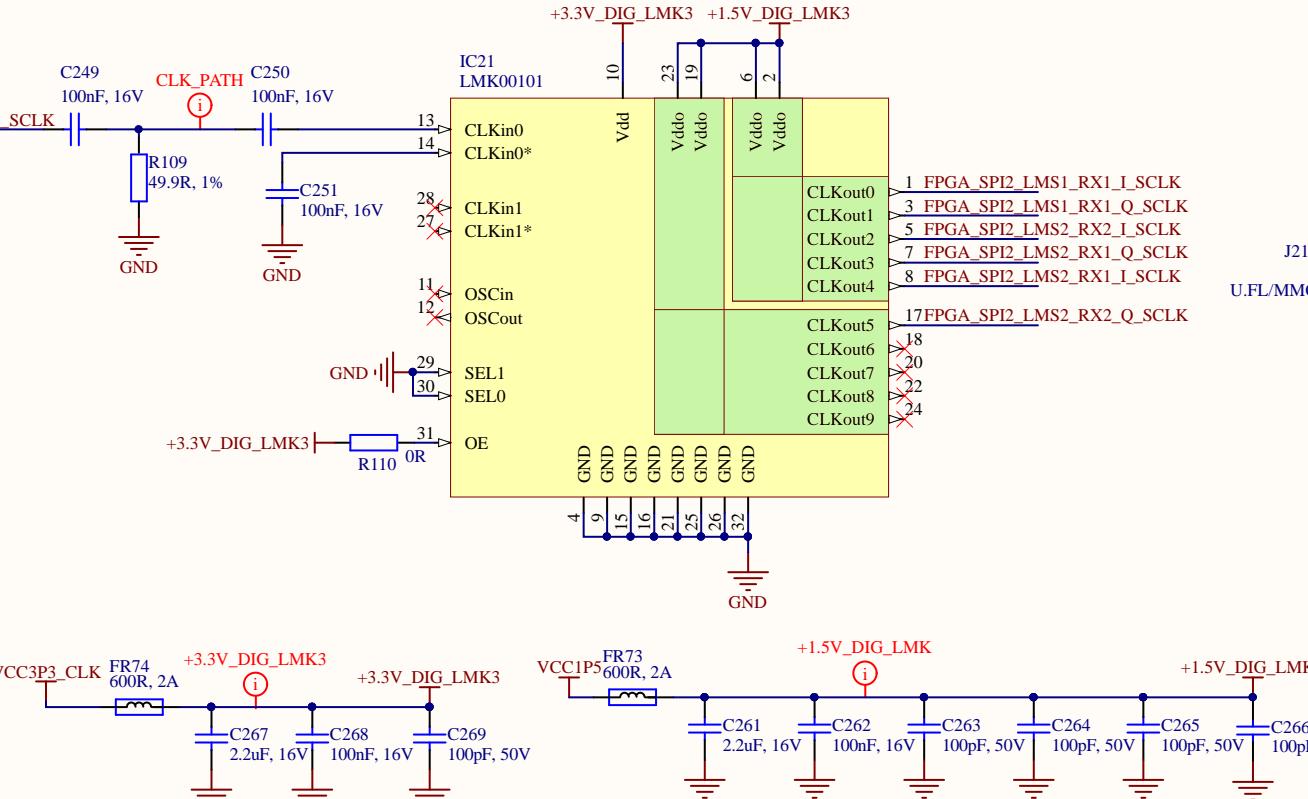
LMS1_RX1_BI



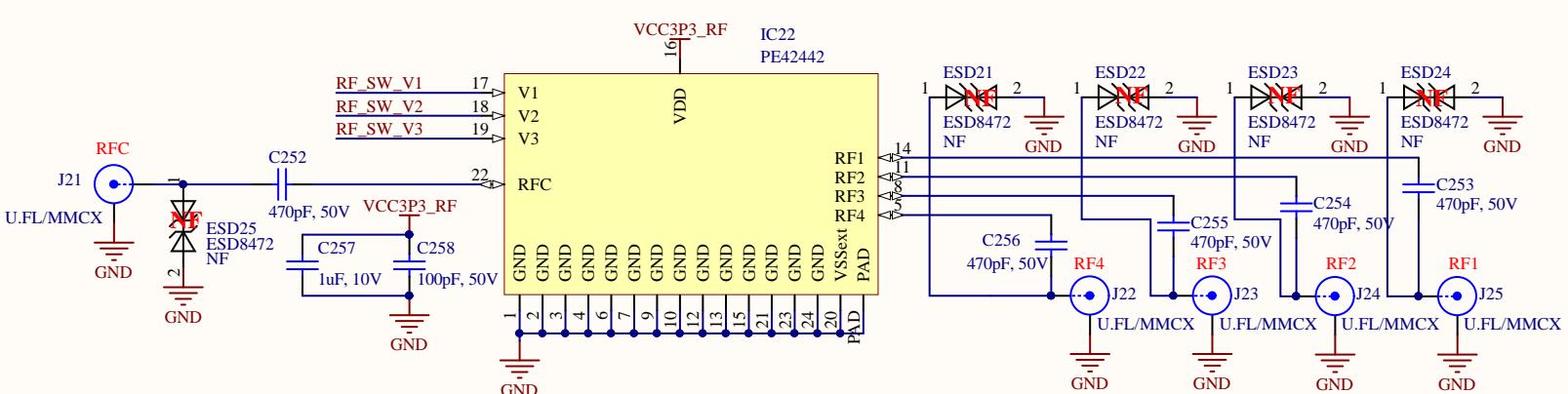
ADC



RSSI ADC SCLK buffer



RF SW



PCB note: Place 100pF close to each Vdd pin

PCB note: Place 100pF close to each Vddo pin

Project name: **LimeSDR-OPCIe_1v2.PrjPcb**

Title: **RSSII**

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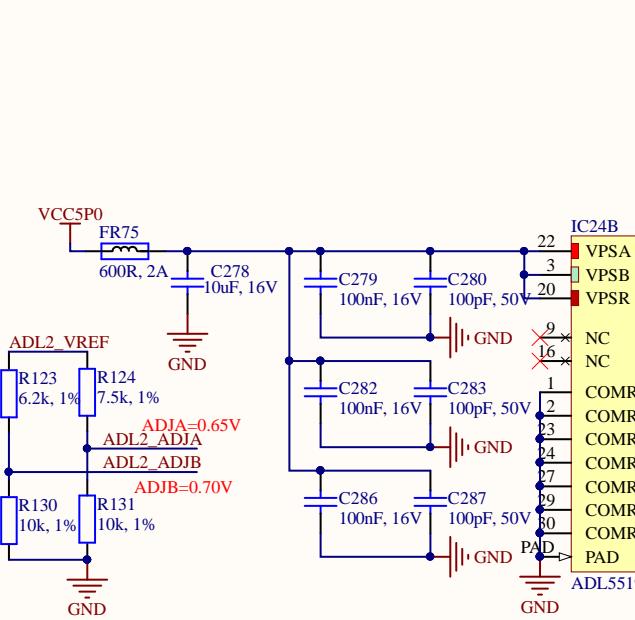
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Date: 2017-09-22 Time: 15:48:26

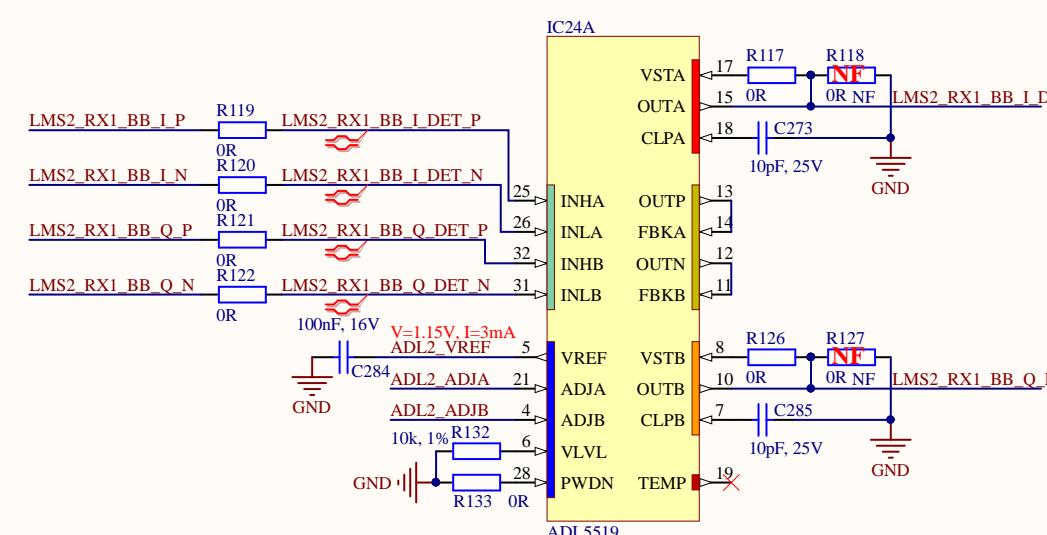
File: 10_RSSI1.SchDoc

NF elements on sheet: C270, R118, C281, R127, C294, R138, C305, R146
Number of NF elements on sheet: 8

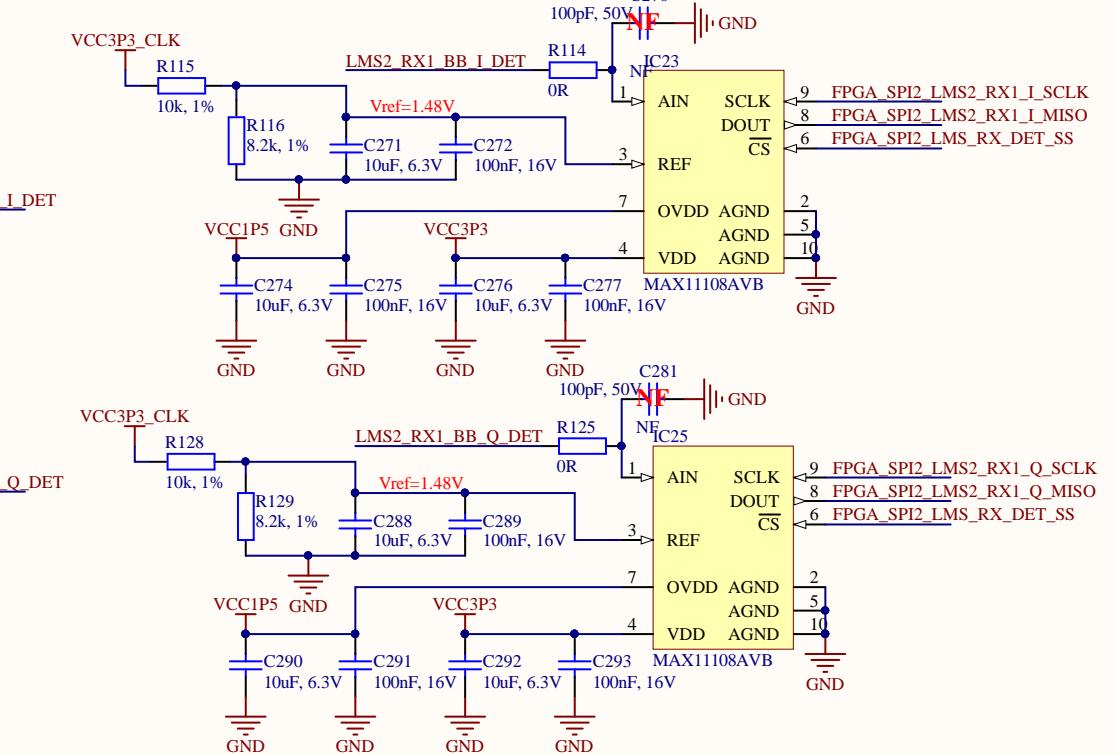
Log Detector



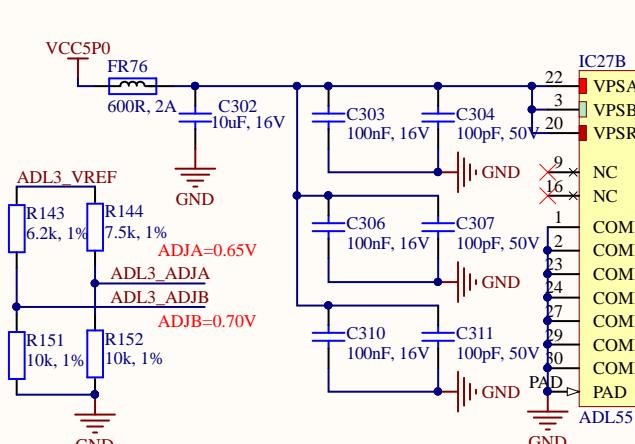
LMS2_RX1_BB



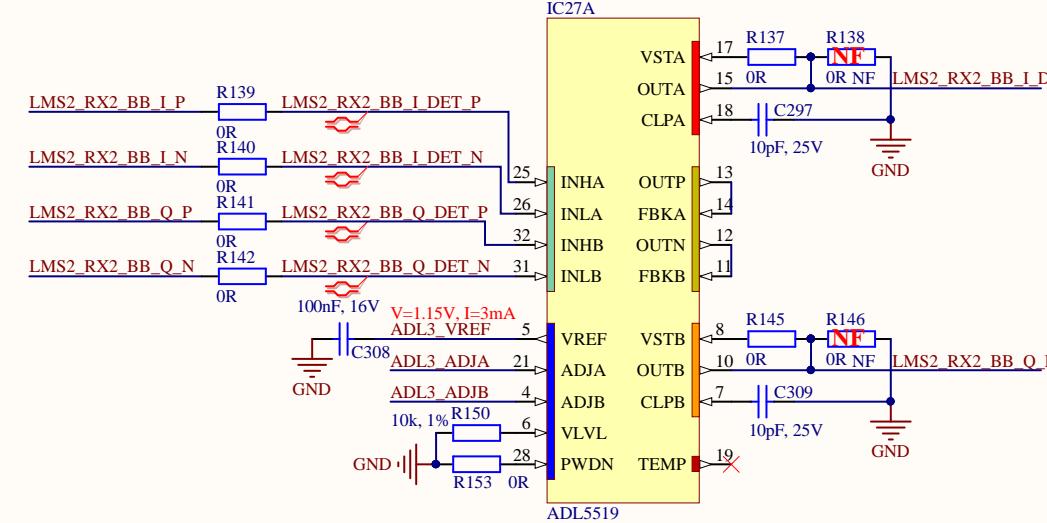
ADC



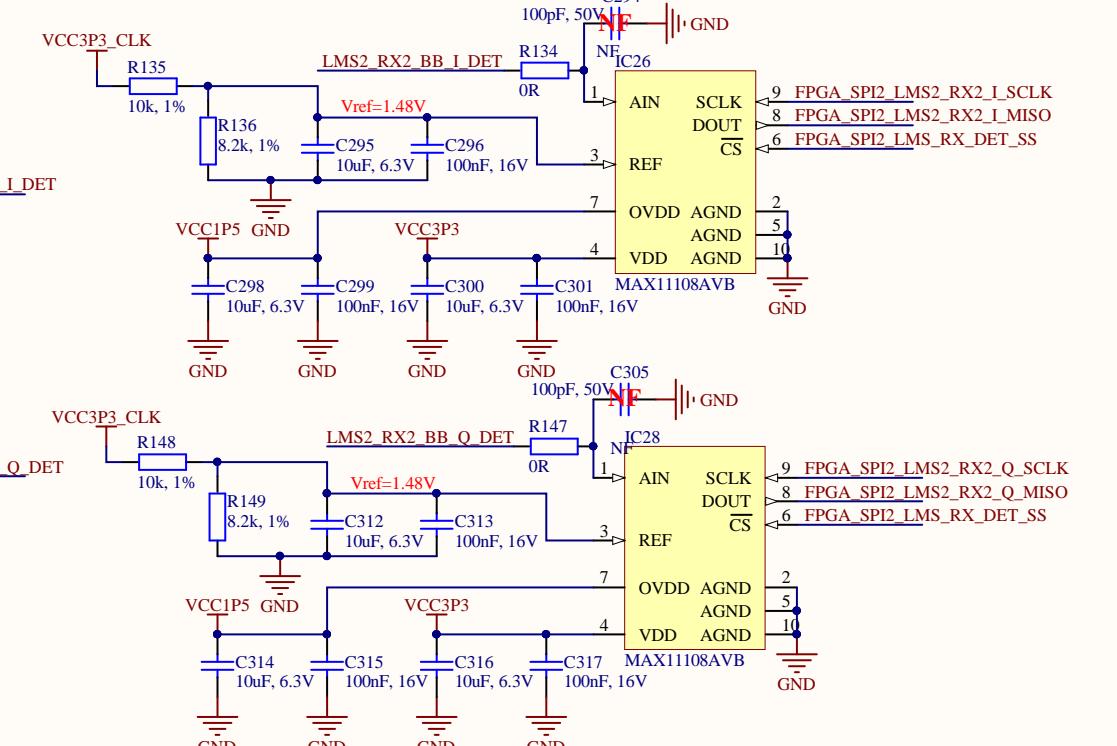
Log Detector



LMS2_RX2_BB



ADC



Project name: LimeSDR-QPCIE_1v2.PrjPcb

Title: RSSI2

Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:48:31 Sheet 9 of 27

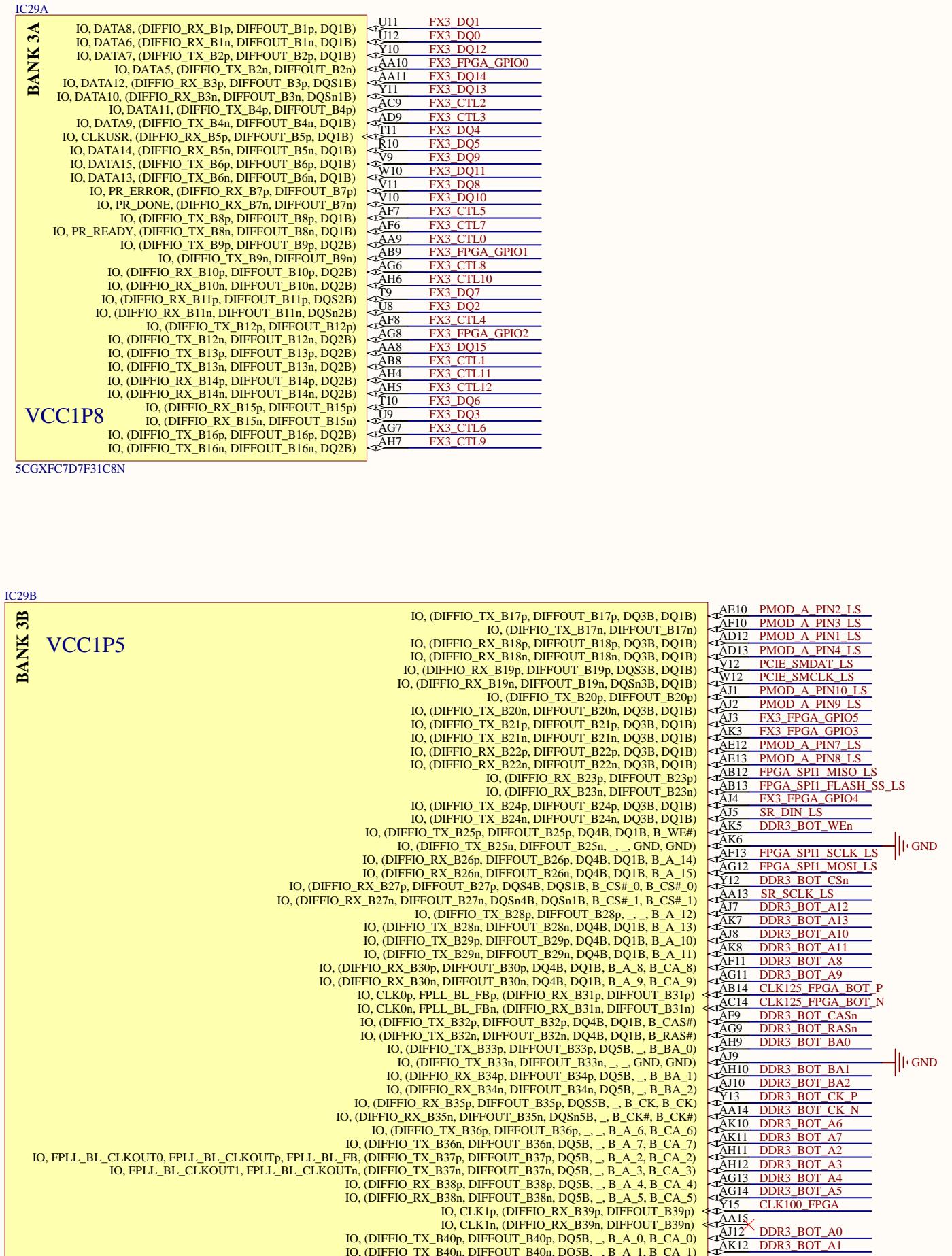
File: 11_RSSI2.SchDoc

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NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 3A, 3B, 4A



Local FPGA + DDR "BOTTOM" fiducial Top



Local FPGA + DDR "TOP" fiducial Top



Project name: LimeSDR-QPCle_1v2.PrfPcb

Title: **FPGA banks 3A, 3B, 4A**

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Size: **A3** Revision: **v1.2**

Date: **2017-09-22** Time: **15:48:37** Sheet 10 of **27**

File: **12_FPGA_banks_3A_3B_4A.SchDoc**

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 5A, 5B, 6A

IC29D

BANK 5A	
IO, RZQ_1, (DIFFIO_RX_R1p, DIFFOUT_R1p, DQ1R)	AD23 LMS2_CORE_LDO_EN
IO, PR_REQUEST, (DIFFIO_RX_R1n, DIFFOUT_R1n, DQ1R)	AC24 LMS1_DIQ1_D8
IO, INIT_DONE, (DIFFIO_RX_R2p, DIFFOUT_R2p)	V22 LMS1_DIQ1_D10
IO, CRC_ERROR, (DIFFIO_RX_R2n, DIFFOUT_R2n)	Y21 LMS1_DIQ2_D2
IO, nCEO, (DIFFIO_RX_R3p, DIFFOUT_R3p, DQ1R)	AD24 LMS2_DIQ2_D3
IO, CvP_CONFDONE, (DIFFIO_RX_R3n, DIFFOUT_R3n, DQ1R)	AD25 LMS2_DIQ1_D0
IO, (DIFFIO_RX_R4p, DIFFOUT_R4p, DQ1R)	Y25 LMS1_CORE_LDO_EN
IO, (DIFFIO_RX_R4n, DIFFOUT_R4n, DQ1R)	Y26 LMS1_RXEN
IO, DEV_OE, (DIFFIO_RX_R5p, DIFFOUT_R5p)	AB26 LMS2_DIQ2_D6
IO, DEV_CLRn, (DIFFIO_RX_R5n, DIFFOUT_R5n, DQ1R)	AA26 LMS1_ENABLE_IQSEL2
IO, nPERSTL0, (DIFFIO_RX_R6p, DIFFOUT_R6p, DQS1R)	V23 LMS1_DIQ1_D1
IO, nPERSTL1, (DIFFIO_RX_R6n, DIFFOUT_R6n, DQS1R)	V24 PCIE_PERSTn
IO, (DIFFIO_RX_R7p, DIFFOUT_R7p, DQ1R)	AC26 LMS1_DIQ2_D5
IO, (DIFFIO_RX_R7n, DIFFOUT_R7n)	AC27 LMS1_DIQ2_D0
IO, (DIFFIO_RX_R8p, DIFFOUT_R8p, DQ1R)	V22 LMS1_FCLK2
IO, (DIFFIO_RX_R8n, DIFFOUT_R8n, DQ1R)	AA23 LMS1_DIQ1_D4
IO, (DIFFIO_RX_R9p, DIFFOUT_R9p)	AA24 LMS1_DIQ1_D11
IO, (DIFFIO_RX_R9n, DIFFOUT_R9n)	AA25 LMS1_DIQ2_D7
IO, (DIFFIO_RX_R10p, DIFFOUT_R10p, DQ2R)	AE23 LMS2_DIQ2_D9
IO, (DIFFIO_RX_R10n, DIFFOUT_R10n, DQ2R)	AF24 LMS2_DIQ2_D7
IO, (DIFFIO_RX_R11p, DIFFOUT_R11p, DQ2R)	AE27 LMS2_DIQ1_D8
IO, (DIFFIO_RX_R11n, DIFFOUT_R11n, DQ2R)	AD27 LMS2_TXEN
IO, (DIFFIO_RX_R12p, DIFFOUT_R12p, DQ2R)	AE25 LMS2_RXEN
IO, (DIFFIO_RX_R12n, DIFFOUT_R12n, DQ2R)	AE26 LMS2_DIQ2_D11
IO, (DIFFIO_RX_R13p, DIFFOUT_R13p, DQS2R)	V21 LMS1_TXEN
IO, (DIFFIO_RX_R13n, DIFFOUT_R13n, DQS2R)	V22 LMS1_DIQ1_D5
IO, (DIFFIO_RX_R14p, DIFFOUT_R14p)	AF25 LMS2_ENABLE_IQSEL2
IO, (DIFFIO_RX_R14n, DIFFOUT_R14n, DQ2R)	AF26 LMS2_DIQ1_D7
IO, (DIFFIO_RX_R15p, DIFFOUT_R15p, DQ2R)	Y27 LMS1_DIQ1_D7
IO, (DIFFIO_RX_R15n, DIFFOUT_R15n, DQ2R)	V27 LMS1_DIQ2_D6
IO, (DIFFIO_RX_R16p, DIFFOUT_R16p, DQ2R)	AH27 LMS2_DIQ1_D2
IO, (DIFFIO_RX_R16n, DIFFOUT_R16n)	AG27 LMS2_DIQ2_D5

VDIO_LMS_FPGA (2.5V or 3.3V)

5CGXFC7D7F31C8N

IC29E

BANK 5B	
IO, (DIFFIO_RX_R17p, DIFFOUT_R17p)	V24 LMS1_DIQ1_D6
IO, (DIFFIO_RX_R17n, DIFFOUT_R17n)	V25 LMS1_DIQ1_D9
IO, (DIFFIO_RX_R18p, DIFFOUT_R18p, DQ3R, DQ1R)	AJ28 LMS2_DIQ1_D6
IO, (DIFFIO_RX_R18n, DIFFOUT_R18n, DQ3R, DQ1R)	AJ29 LMS2_DIQ1_D9
IO, (DIFFIO_RX_R19p, DIFFOUT_R19p, DQ3R, DQ1R)	AA28 LMS2_DIQ2_D0
IO, (DIFFIO_RX_R19n, DIFFOUT_R19n, DQ3R, DQ1R)	Y28 LMS1_DIQ2_D4
IO, (DIFFIO_RX_R20p, DIFFOUT_R20p, DQ3R, DQ1R)	AH29 LMS1_DIQ2_D9
IO, (DIFFIO_RX_R20n, DIFFOUT_R20n, DQ3R, DQ1R)	AG29 LMS2_DIQ2_D10
IO, (DIFFIO_RX_R21p, DIFFOUT_R21p, DQS3R, DQS1R)	V26 LMS1_DIQ2_D8
IO, (DIFFIO_RX_R21n, DIFFOUT_R21n, DQS3nR, DQS1R)	U26 LMS1_TXNRX2
IO, (DIFFIO_RX_R22p, DIFFOUT_R22p)	AJ30 LMS2_DIQ2_D1
IO, (DIFFIO_RX_R22n, DIFFOUT_R22n, DQ3R, DQ1R)	AH30 LMS2_DIQ2_D8
IO, (DIFFIO_RX_R23p, DIFFOUT_R23p, DQ3R, DQ1R)	AE30 LMS2_DIQ1_D3
IO, (DIFFIO_RX_R23n, DIFFOUT_R23n, DQ3R, DQ1R)	AD30 LMS2_DIQ1_D5
IO, (DIFFIO_RX_R24p, DIFFOUT_R24p, DQ3R, DQ1R)	AG28 LMS2_DIQ2_D4
IO, (DIFFIO_RX_R24n, DIFFOUT_R24n)	AF28 LMS2_TXNRX1
IO, CLK7p, FPLL_BR_FBp, (DIFFIO_RX_R25p, DIFFOUT_R25p)	J21 LMS1_MCLK2
IO, CLK7n, FPLL_BR_FBp, (DIFFIO_RX_R25n, DIFFOUT_R25n)	U22 LMS1_MCLK1
IO, (DIFFIO_RX_R26p, DIFFOUT_R26p, DQ4R, DQ1R)	AF29 LMS2_ENABLE_IQSEL1
IO, (DIFFIO_RX_R26n, DIFFOUT_R26n, DQ4R, DQ1R)	AJ30 LMS2_DIQ1_D11
IO, (DIFFIO_RX_R27p, DIFFOUT_R27p, DQ4R, DQ1R)	V27 LMS1_DIQ2_D10
IO, (DIFFIO_RX_R27n, DIFFOUT_R27n, DQ4R, DQ1R)	W28 LMS1_DIQ2_D11
IO, (DIFFIO_RX_R28p, DIFFOUT_R28p, DQ4R, DQ1R)	AE28 LMS2_DIQ1_D4
IO, (DIFFIO_RX_R28n, DIFFOUT_R28n, DQ4R, DQ1R)	AD28 LMS2_DIQ1_D10
IO, (DIFFIO_RX_R29p, DIFFOUT_R29p, DQS4R, DQ1R)	U27 LMS1_TXNRX1
IO, (DIFFIO_RX_R29n, DIFFOUT_R29n, DQS4nR, DQ1R)	J28 LMS1_ENABLE_IQSEL1
IO, (DIFFIO_RX_R30p, DIFFOUT_R30p)	AD29 LMS2_DIQ1_D1
IO, (DIFFIO_RX_R30n, DIFFOUT_R30n, DQ4R, DQ1R)	AC29 LMS2_FCLK2
IO, (DIFFIO_RX_R31p, DIFFOUT_R31p, DQ4R, DQ1R)	AA29 LMS1_DIQ2_D3
IO, (DIFFIO_RX_R31n, DIFFOUT_R31n, DQ4R, DQ1R)	AA30 LMS2_RESET
IO, (DIFFIO_RX_R32p, DIFFOUT_R32p, DQ4R, DQ1R)	AB27 LMS1_DIQ2_D1
IO, (DIFFIO_RX_R32n, DIFFOUT_R32n)	AB28 LMS1_DIQ1_D2
IO, CLK6p, (DIFFIO_RX_R33p, DIFFOUT_R33n)	U23 LMS2_MCLK2
IO, CLK6n, (DIFFIO_RX_R33n, DIFFOUT_R33n)	T24 LMS2_MCLK1
IO, (DIFFIO_RX_R34p, DIFFOUT_R34p, DQS5R)	AB29 LMS2_DIQ2_D2
IO, (DIFFIO_RX_R34n, DIFFOUT_R34n, DQS5R)	AC30 LMS2_TXNRX2
IO, (DIFFIO_RX_R35p, DIFFOUT_R35p, DQS5R)	T28 LMS1_DIQ1_D0
IO, (DIFFIO_RX_R35n, DIFFOUT_R35n, DQS5R)	T29 LMS1_DIQ1_D3
IO, (DIFFIO_RX_R36p, DIFFOUT_R36p, DQS5R)	Y30 LMS1_FCLK1
IO, (DIFFIO_RX_R36n, DIFFOUT_R36n, DQS5R)	W30 LMS2_FCLK1
IO, (DIFFIO_RX_R37p, DIFFOUT_R37p, DQS5R)	T25 FPGA_SPI0_SCLK
IO, (DIFFIO_RX_R37n, DIFFOUT_R37n, DQS5R)	R26 FPGA_SPI0_MOSI
IO, (DIFFIO_RX_R38p, DIFFOUT_R38p)	V29 FPGA_SPI0_LMS1_SS
IO, (DIFFIO_RX_R38n, DIFFOUT_R38n, DQS5R)	W29 FPGA_LED5_G
IO, (DIFFIO_RX_R39p, DIFFOUT_R39p, DQS5R)	Z30 FPGA_LED5_R
IO, (DIFFIO_RX_R39n, DIFFOUT_R39n, DQS5R)	R30 FPGA_SPI0_MISO_LMS1
IO, (DIFFIO_RX_R40p, DIFFOUT_R40p, DQS5R)	T29 FPGA_SPI0_LMS2_SS
IO, (DIFFIO_RX_R40n, DIFFOUT_R40n)	V30 FPGA_SPI0_MISO_LMS2

VDIO_LMS_FPGA (2.5V or 3.3V)

5CGXFC7D7F31C8N

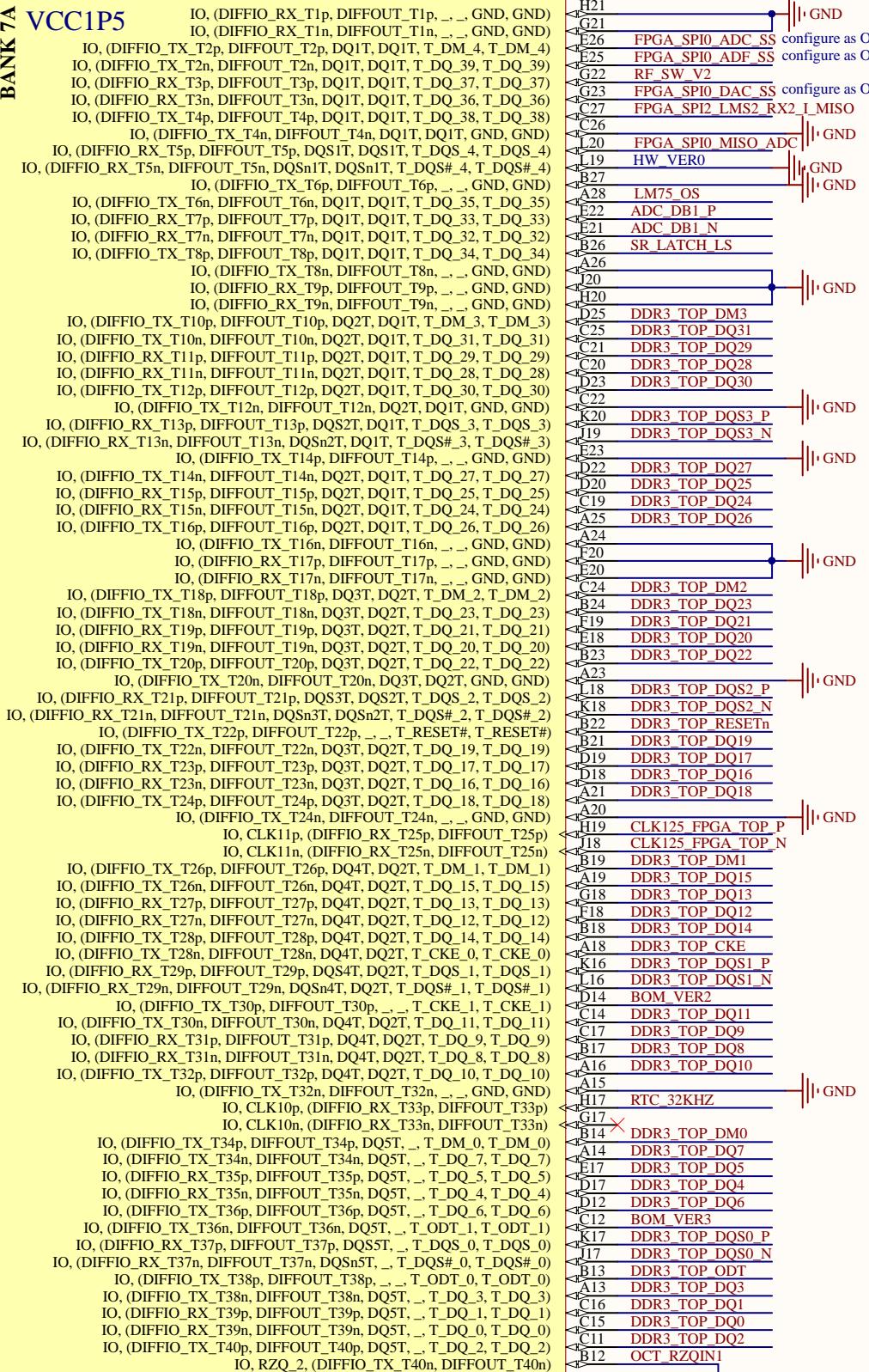
IC29F
BANK 6A

IO, CLK5p, (DIFFIO_RX_R41p, DIFFOUT_R41p)	T23 GNSS_TPULSE
IO, CLK5n, (DIFFIO_RX_R41n, DIFFOUT_R41n)	R23 GNSS_FIX
IO, (DIFFIO_RX_R42p, DIFFOUT_R42p, DQ6R)	P28 DAC2_DB0
IO, (DIFFIO_RX_R42n, DIFFOUT_R42n, DQ6R)	N29 DAC2_DA4
IO, (DIFFIO_RX_R43p, DIFFOUT_R43p, DQ6R)	P29 DAC2_DA12
IO, (DIFFIO_RX_R43n, DIFFOUT_R43n, DQ6R)	P30 DAC2_DA3
IO, FPLL_TR_CLKOUT0, FPLL_TR_CLKOUTp, FPLL_TR_FBp, (DIFFIO_RX_R44p, DIFFOUT_R44p, DQ6R)	T24 GNSS_RX
IO, FPLL_TR_CLKOUT1, FPLL_TR_CLKOUTn, (DIFFIO_RX_R44n, DIFFOUT_R44n, DQ6R)	N30 ADC_CLK
IO, (DIFFIO_RX_R45p, DIFFOUT_R45p, DQS6R)	P25 DAC2_DB2
IO, (DIFFIO_RX_R45n, DIFFOUT_R45n, DQS6R)	R25 DAC2_DB4
IO, (DIFFIO_RX_R46p, DIFFOUT_R46p)	S28 DAC2_DA8
IO, (DIFFIO_RX_R46n, DIFFOUT_R46n, DQ6R)	K28 DAC1_DB5
IO, (DIFFIO_RX_R47p, DIFFOUT_R47p, DQ6R)	R27 DAC2_DA0
IO, (DIFFIO_RX_R47n, DIFFOUT_R47n, DQ6R)	R28 DAC2_DB3
IO, (DIFFIO_RX_R48p, DIFFOUT_R48p, DQ6R)	M27 DAC2_DA5
IO, (DIFFIO_RX_R48n, DIFFOUT_R48n, DQS6R)	M28 DAC2_DA6
IO, CLK4p, FPLL_TR_FBp, (DIFFIO_RX_R49p, DIFFOUT_R49p)	E22 SI_CLK0
IO, CLK4n, FPLL_TR_FBp, (DIFFIO_RX_R49n, DIFFOUT_R49n)	K25 GNSS_RX
IO, (DIFFIO_RX_R50p, DIFFOUT_R50p, DQ7R, DQ2R)	K26 DAC2_DA1
IO, (DIFFIO_RX_R50n, DIFFOUT_R50n, DQ7R, DQ2R)	N26 DAC2_DA13
IO, (DIFFIO_RX_R51p, DIFFOUT_R51p, DQ7R, DQ2R)	N27 DAC2_DA2
IO, (DIFFIO_RX_R51n, DIFFOUT_R51n, DQ7R, DQ2R)	S29 DAC2_DA9
IO, (DIFFIO_RX_R52p, DIFFOUT_R52p, DQ7R, DQ2R)	L30 DAC2_DA11
IO, (DIFFIO_RX_R52n, DIFFOUT_R52n, DQ7R, DQ2R)	N24 DAC2_DB6
IO, (DIFFIO_RX_R53p, DIFFOUT_R53p, DQS7R, DQS2R)	N25 DAC2_DB1
IO, (DIFFIO_RX_R53n, DIFFOUT_R53n, DQS7R, DQS2R)	K30 DAC1_DB4
IO, (DIFFIO_RX_R54p, DIFFOUT_R54p, DQ5R, DQ2R)	I30 DAC1_DB8
IO, (DIFFIO_RX_R54n, DIFFOUT_R54n, DQ5R, DQ2R)	E25 DAC2_DA10
IO, (DIFFIO_RX_R55p, DIFFOUT_R55p, DQ5R, DQ2R)	G27 FPGA_LED2
IO, (DIFFIO_RX_R56p, DIFFOUT_R56p, DQ5R, DQ2R)	G28 FPGA_LED1
IO, (DIFFIO_RX_R56n, DIFFOUT_R56n, DQ5R, DQ2R)	R21 DAC2_DB12
IO, (DIFFIO_RX_R57p, DIFFOUT_R57p, DQ5R, DQ2R)	R22 DAC2_DB13
IO, (DIFFIO_RX_R58p, DIFFOUT_R58p, DQ8R, DQ2R)	S28 DAC1_DB2
IO, (DIFFIO_RX_R58n, DIFFOUT_R58n, DQ8R, DQ2R)	K27 DAC2_DB5
IO, (DIFFIO_RX_R59p, DIFFOUT_R59p, DQ8R, DQ2R)	E27 FPGA_LED3
IO, (DIFFIO_RX_R59n, DIFFOUT_R59n, DQ8R, DQ2R)	H29 DAC1_DB10
IO, (DIFFIO_RX_R60p, DIFFOUT_R60p, DQ8R, DQ2R)	H30 DAC1_DB11
IO, (DIFFIO_RX_R61p, DIFFOUT_R61p, DQ8R, DQ2R)	N22 DAC2_DB9
IO, (DIFFIO_RX_R61n, DIFFOUT_R61n, DQS8R, DQ2R)	M23 DAC2_DB7
IO, (DIFFIO_RX_R62p, DIFFOUT_R62p)	H27 DAC1_DB8
IO, (DIFFIO_RX_R62n, DIFFOUT_R62n, DQ8R, DQ2R)	G26 PCIE_WAKEEn
IO, (DIFFIO_RX_R63p, DIFFOUT_R63p, DQ8R, DQ2R)	F25 DAC1_DA1
IO, (DIFFIO_RX_R63n, DIFFOUT_R63n, DQ8R, DQ2R)	F26 DAC1_DA4
IO, (DIFFIO_RX_R64p, DIFFOUT_R64p, DQ8R, DQ2R)	E30 DAC1_DB1
IO, (DIFFIO_RX_R64n, DIFFOUT_R64n, DQ8R, DQ2R)	R20 DAC2_DB10
IO, (DIFFIO_RX_R65p, DIFFOUT_R65p, DQ8R, DQ2R)	G29 DAC1_DB6
IO, (DIFFIO_RX_R65n, DIFFOUT_R65n, DQ8R, DQ2R)	F29 DAC1_DB3
IO, (DIFFIO_RX_R66p, DIFFOUT_R66p, DQ9R, DQ3R)	E30 DAC1_DA5
IO, (DIFFIO_RX_R66n, DIFFOUT_R66n, DQ9R, DQ3R)	L20 DAC2_SLEEP
IO, (DIFFIO_RX_R67p, DIFFOUT_R67p, DQ9R, DQ3R)	D23 DAC2_MODE
IO, (DIFFIO_RX_R67n, DIFFOUT_R67n, DQ9R, DQ3R)	L24 DAC2_SLEEP
IO, (DIFFIO_RX_R68p, DIFFOUT_R68p, DQ9R, DQ3R)	D30 DAC1_DA10
IO, (DIFFIO_RX_R68n, DIFFOUT_R68n, DQ9R, DQ3R)	C30 DAC1_DA8
IO, (DIFFIO_RX_R69p, DIFFOUT_R69p, DQS9R, DQS3R)	N21 CLK_LMK_FPGA_OUT
IO, (DIFFIO_RX_R69n, DIFFOUT_R69n, DQS9R, DQS3R)	M22 DAC2_DB8
IO, (DIFFIO_RX_R70p, DIFFOUT_R70p)	E28 DAC1_DB0
IO, (DIFFIO_RX_R70n, DIFFOUT_R70n, DQ9R, DQ3R)	K21 PD_ADC_DRV
IO, (DIFFIO_RX_R71p, DIFF	

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 7A, 8A

IC29G

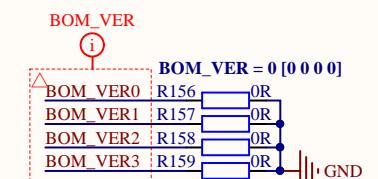


SCGXFC7D7F31C8N

R155
100R, 1%

GND

HW_VER = 2 [0 0 1 0]
 HW_VER0
 HW_VER1
 HW_VER2
 HW_VER3



Project name: LimeSDR-QPCIE_1v2.PrjPcb

Title: FPGA banks 7A, 8A

Size: A3 Revision: v1.2

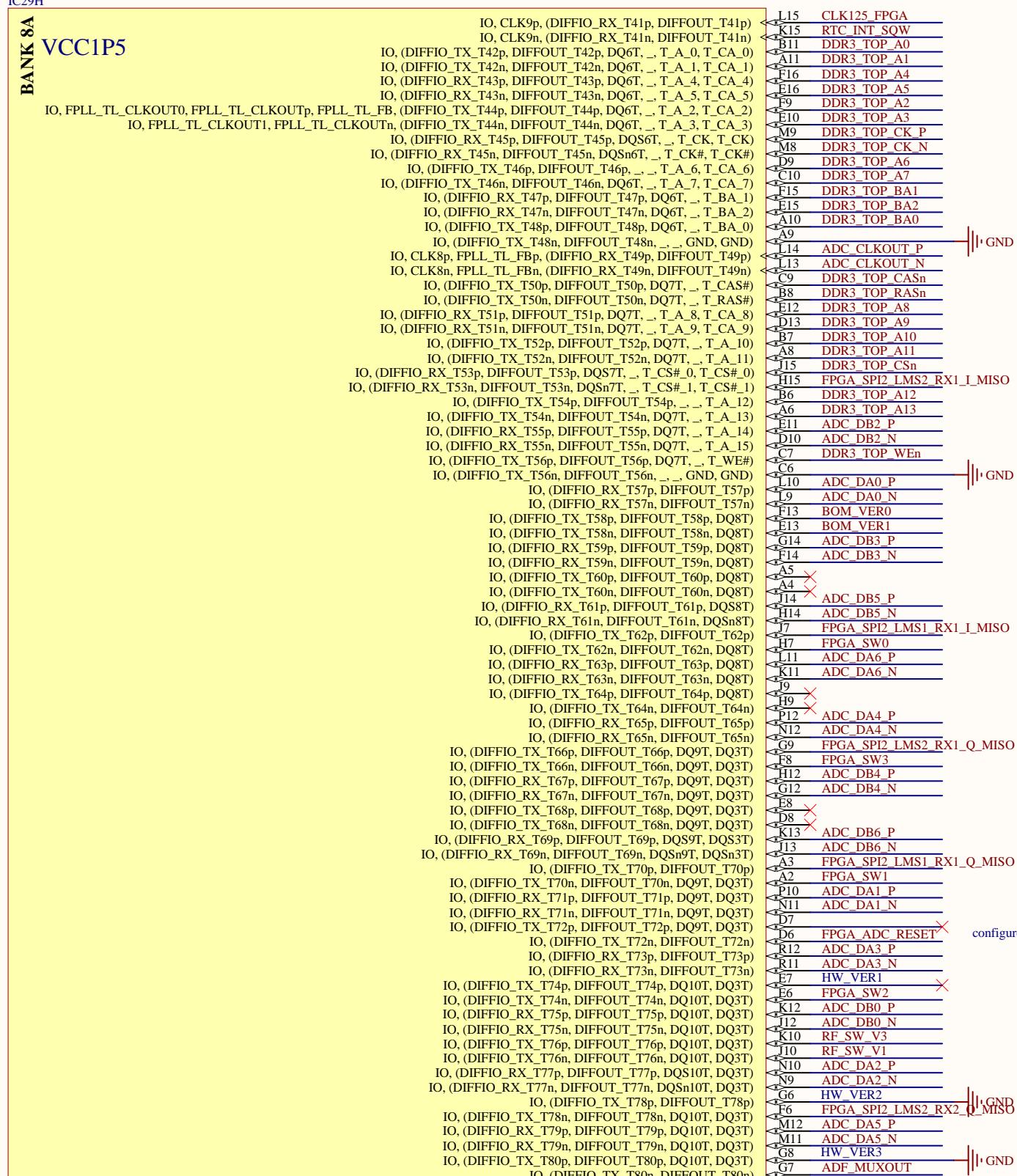
Date: 2017-09-22 Time: 15:48:48 Sheet 12 of 27

File: 14 FPGA banks 7A, 8A.SchDoc

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 United Kingdom



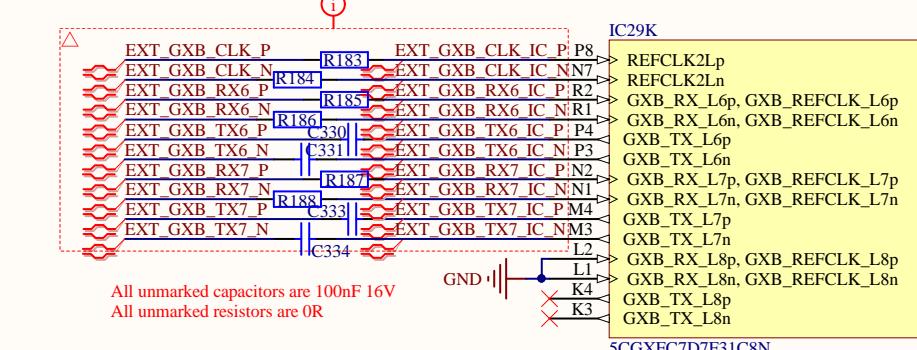
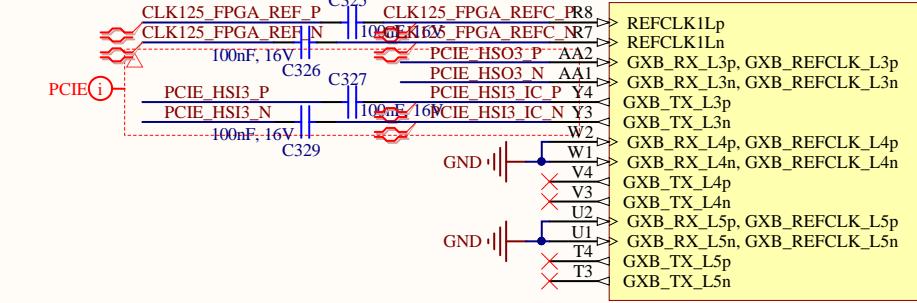
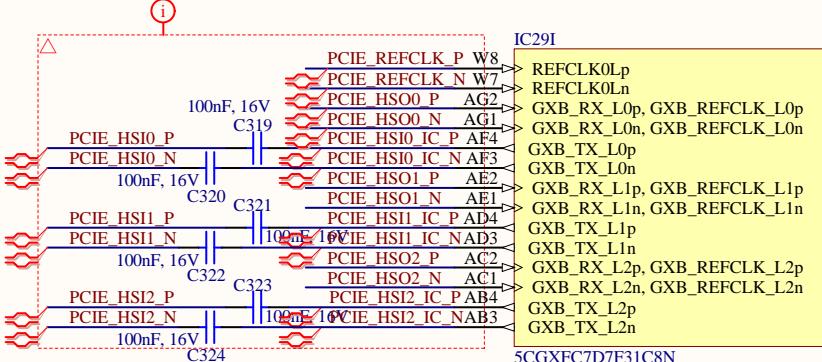
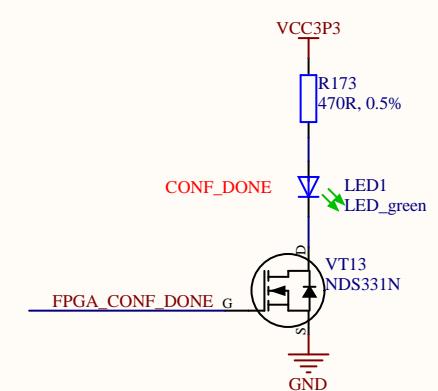
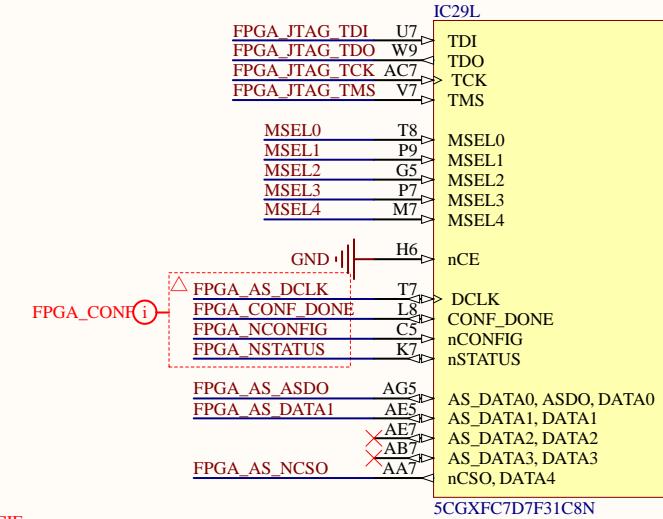
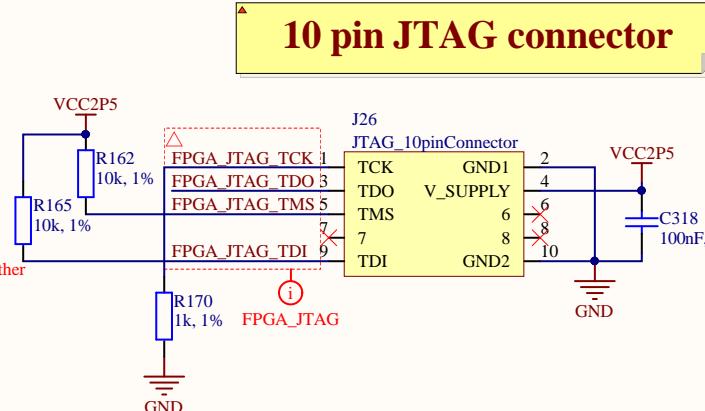
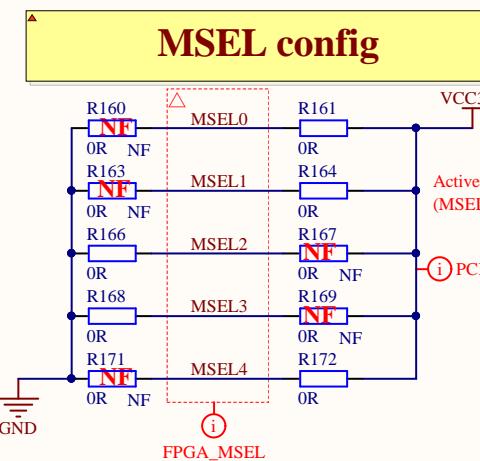
IC29H



SCGXFC7D7F31C8N

NF elements on sheet: R160, R163, R167, R169, R171, IC30
Number of NF elements on sheet: 6

FPGA misc banks

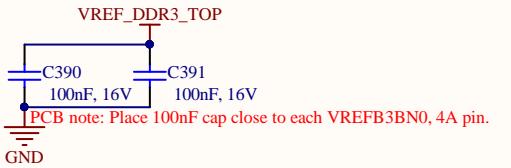
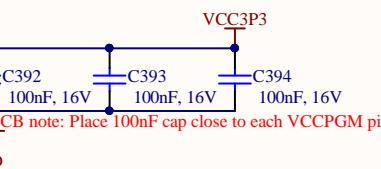
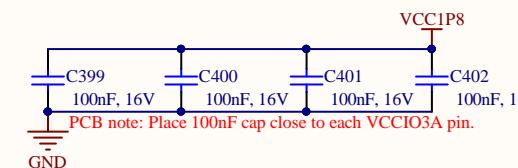
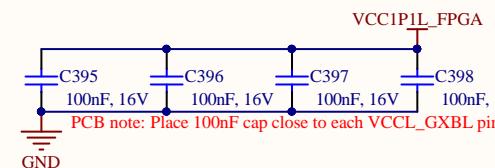


Project name: LimeSDR-QPCIe_1v2.PrjPcb			
Title: FPGA misc		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom	
Size: A3	Revision: v1.2		
Date: 2017-09-22	Time: 15:48:55	Sheet 13 of 27	
File: 15_FPGA_mis...SchDoc			

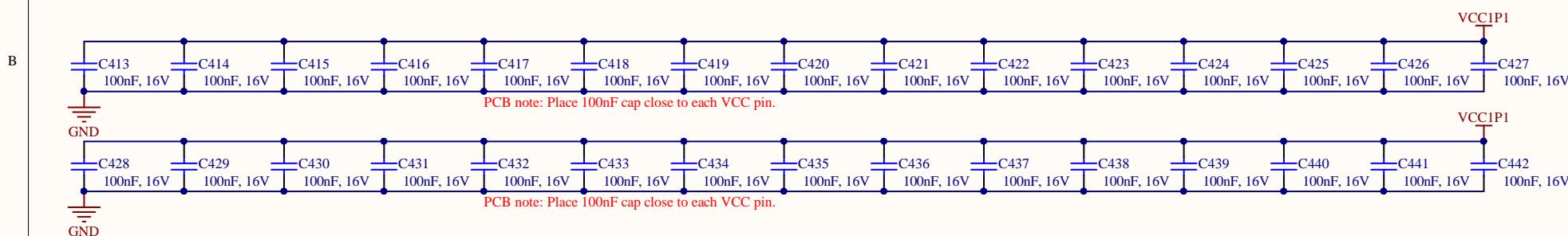
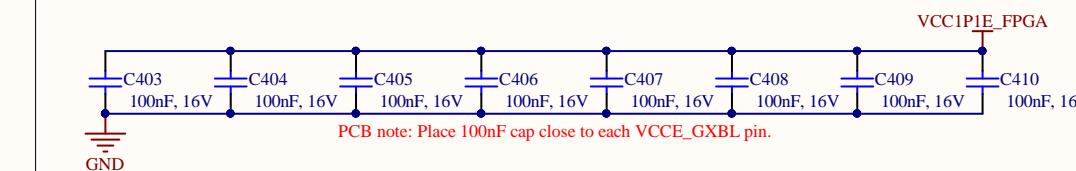
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FPGA Decoupling

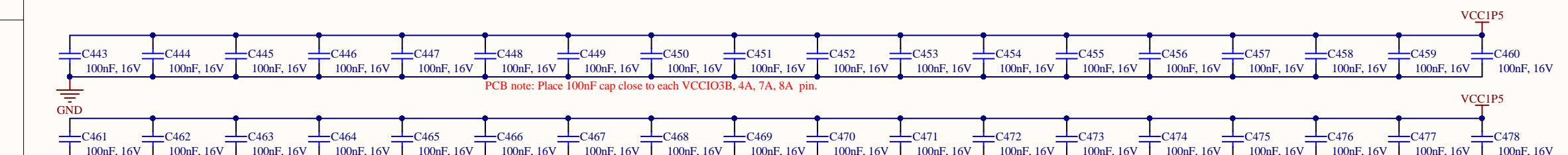
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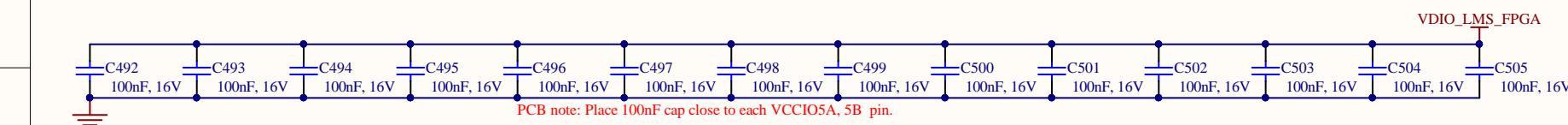
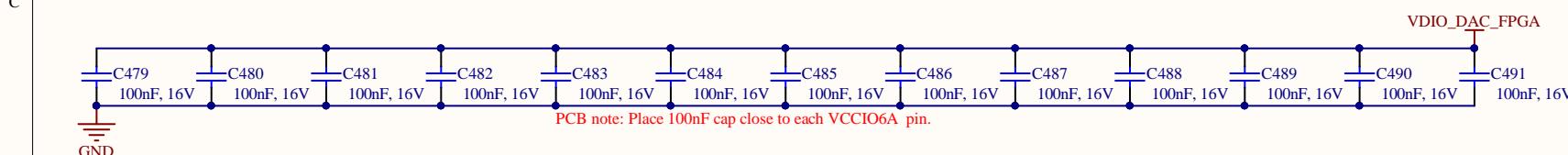
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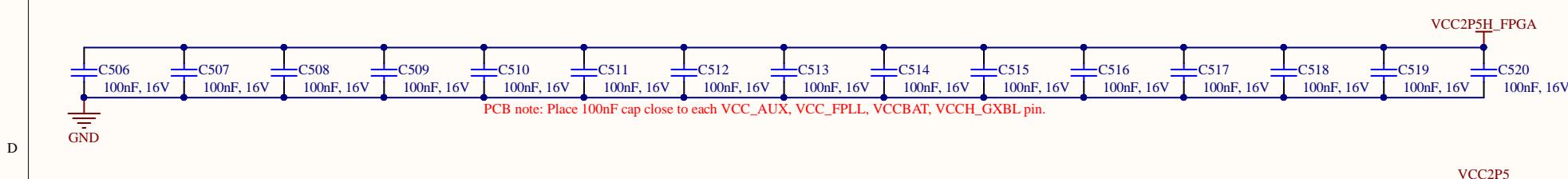
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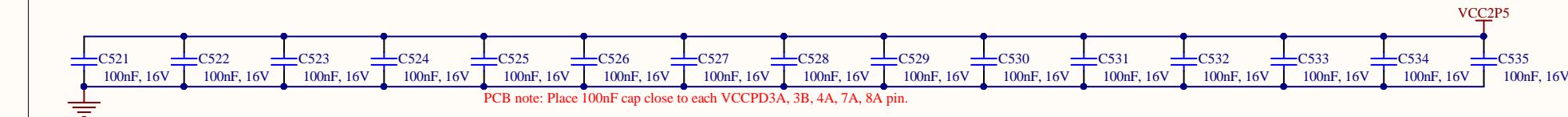
D



D



D



Project name: LimeSDR-QPCIe_1v2.PrcPcb

Title: **FPGA Decoupling**

Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:49:07 Sheet 15 of 27

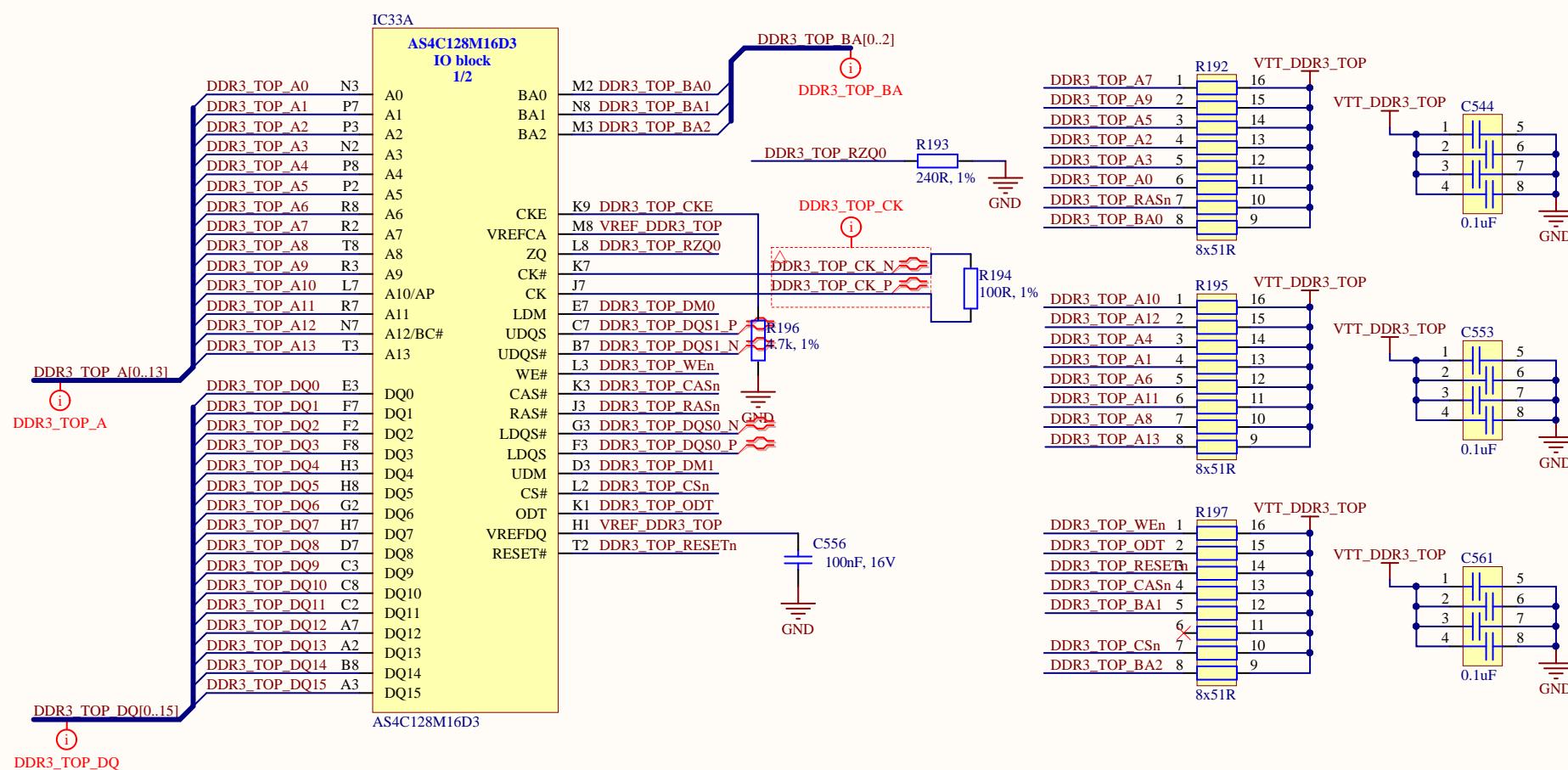
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Surrey
United Kingdom

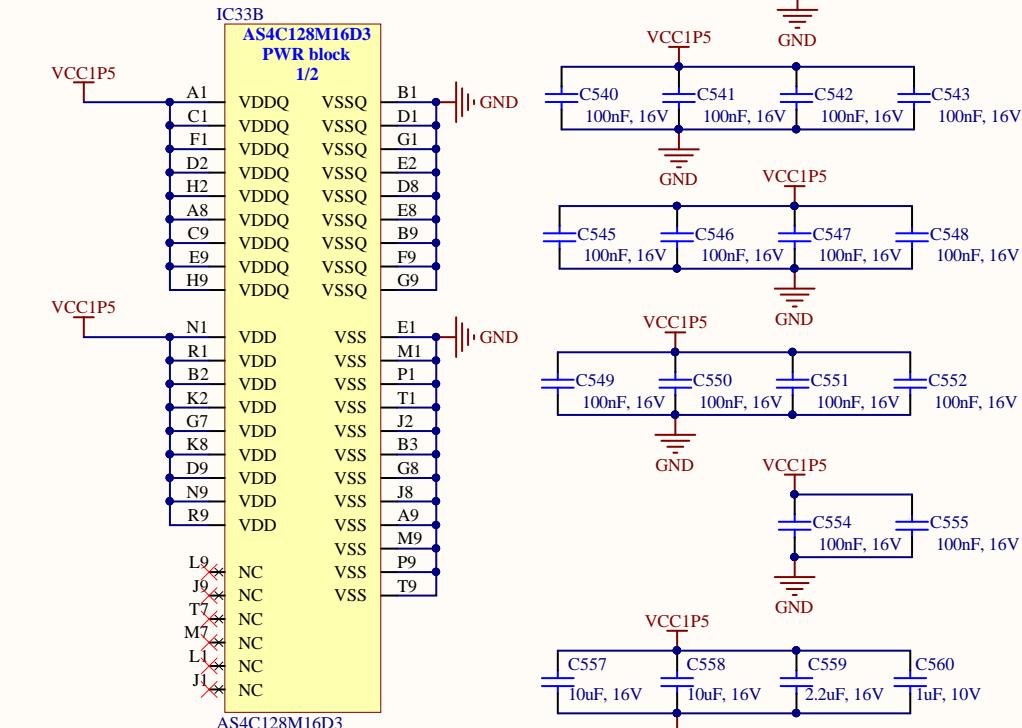
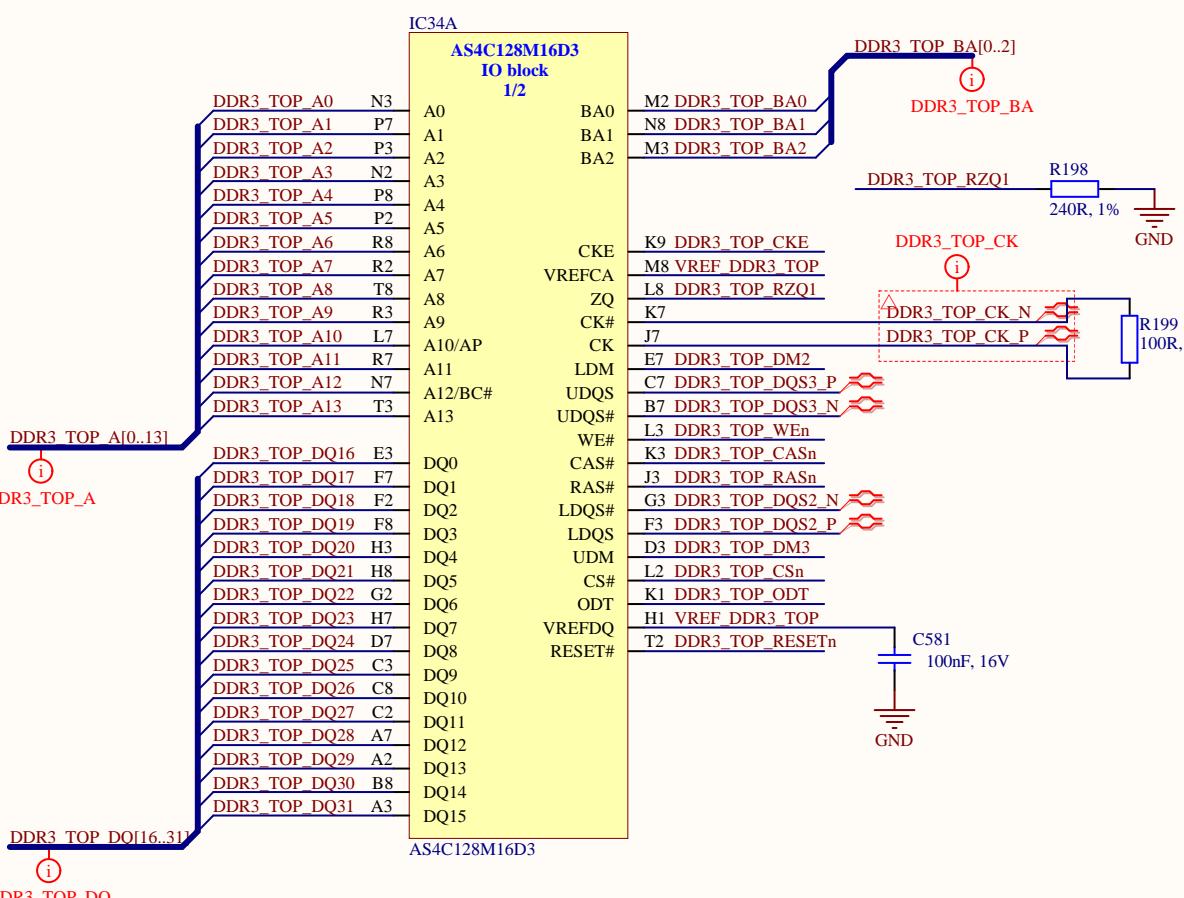


NF elements on sheet: -
Number of NF elements on sheet: 0

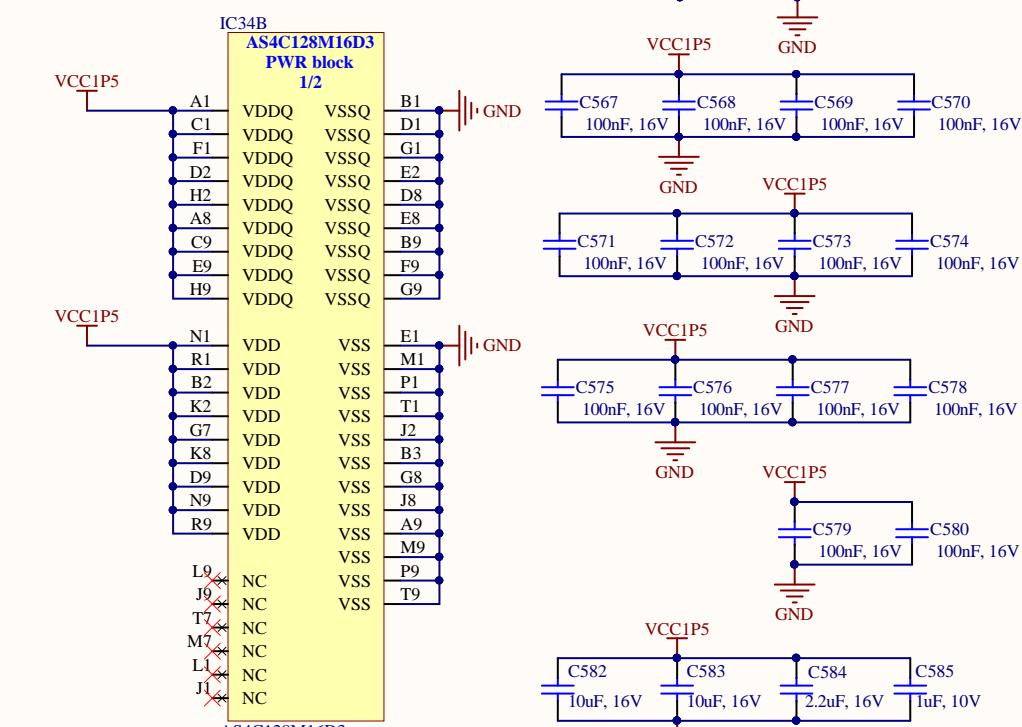
DDR3 A (top)



DDR3 B (top)



PCB note: Place 220uF cap between RAM chips. C562
220uF, 4V

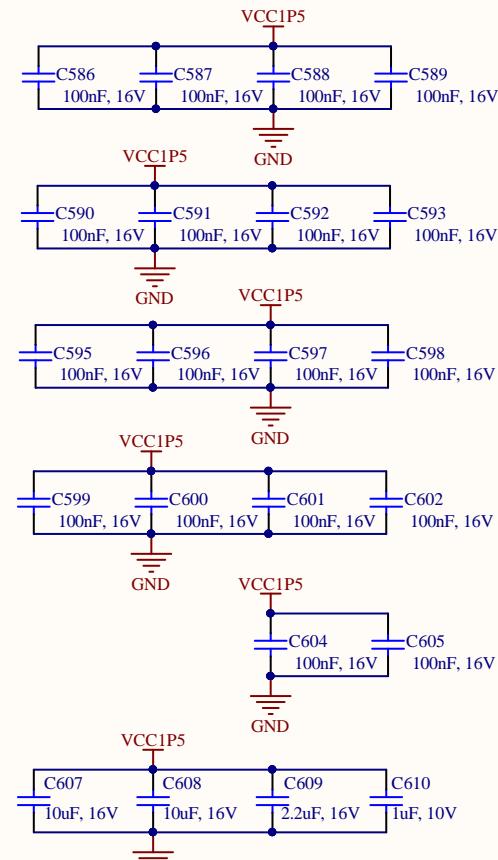
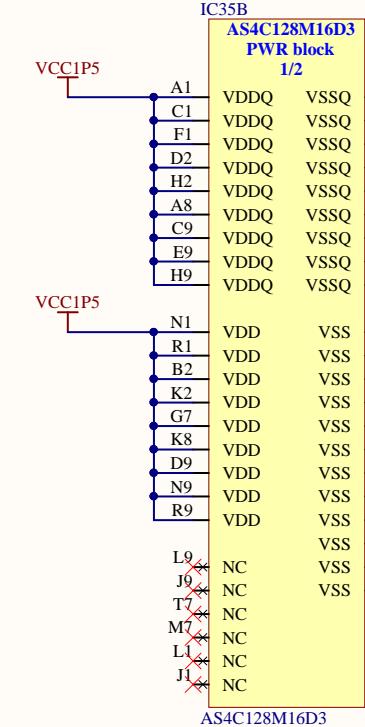
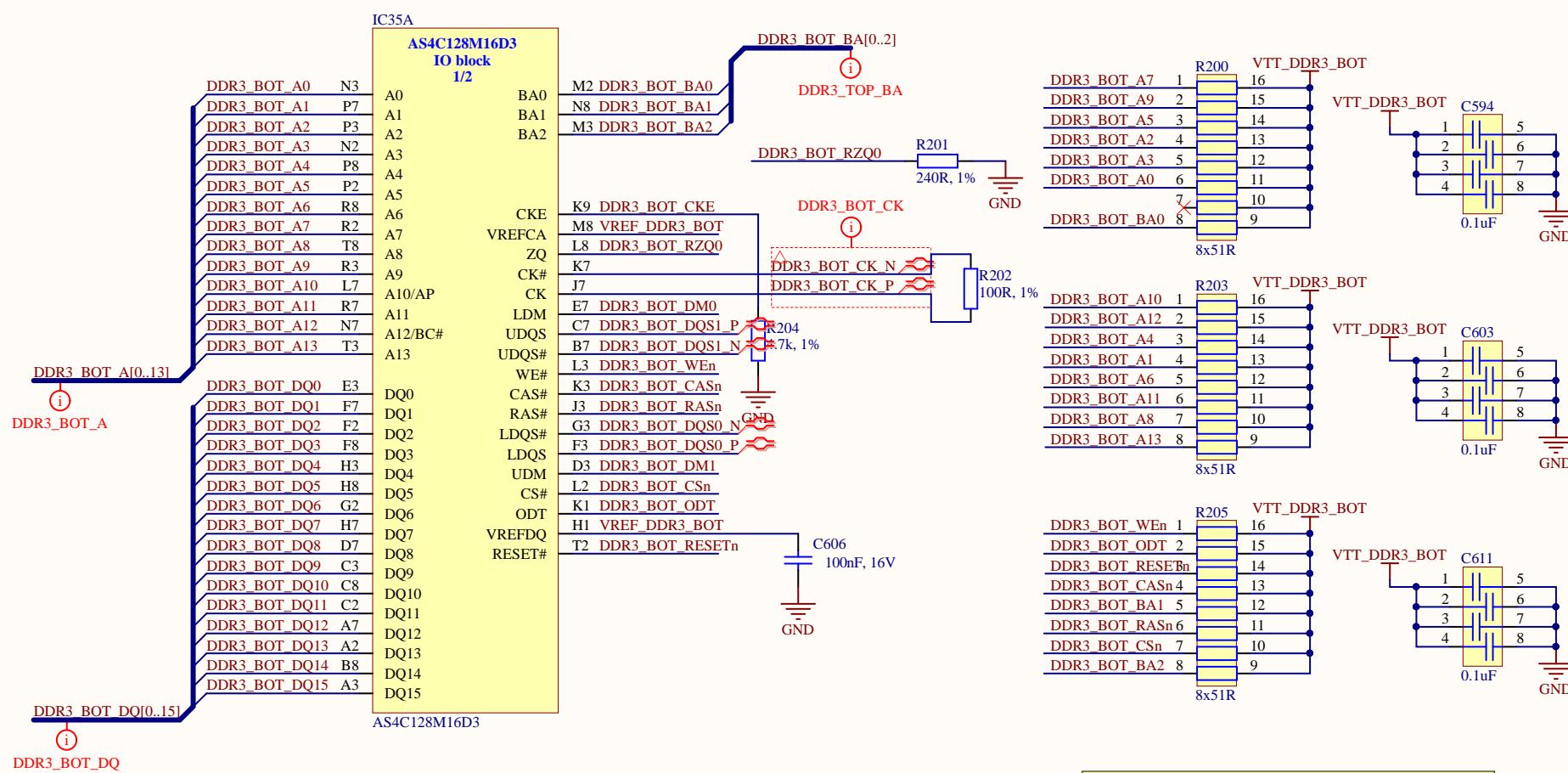


Project name: **LimeSDR-OPCIE 1v2.PrjPcb**

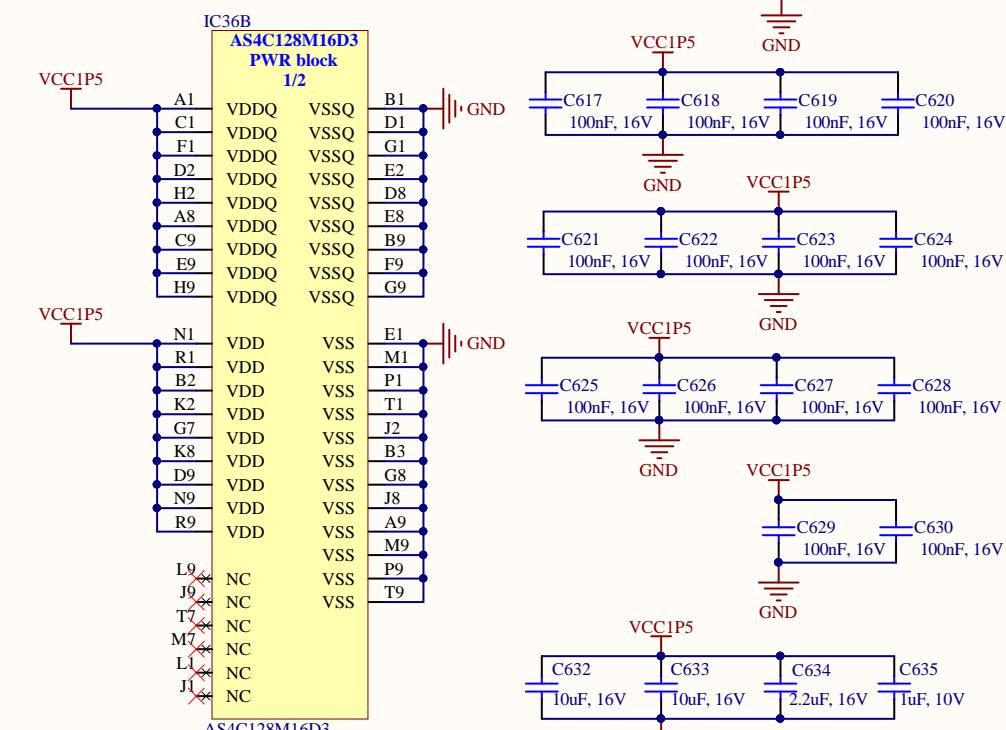
Title: <i>DDR3 top</i>		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surry United Kingdom
Size: A3	Revision: v1.2	
Date: 2017-09-22 Time: 15:49:13		Sheet 16 of 27
File: 18 DDR3_TOP.SchDoc		

NF elements on sheet: -
Number of NF elements on sheet: 0

DDR3 A (bot)



DDR3 B (bot)



Project name: LimeSDR-QPCIe_1v2.PrcPcb

Title: DDR3 bot

Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:49:19 Sheet 17 of 27

File: 19_DDR3_BOT.SchDoc

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Guildford GU2 7YG
Surrey
United Kingdom

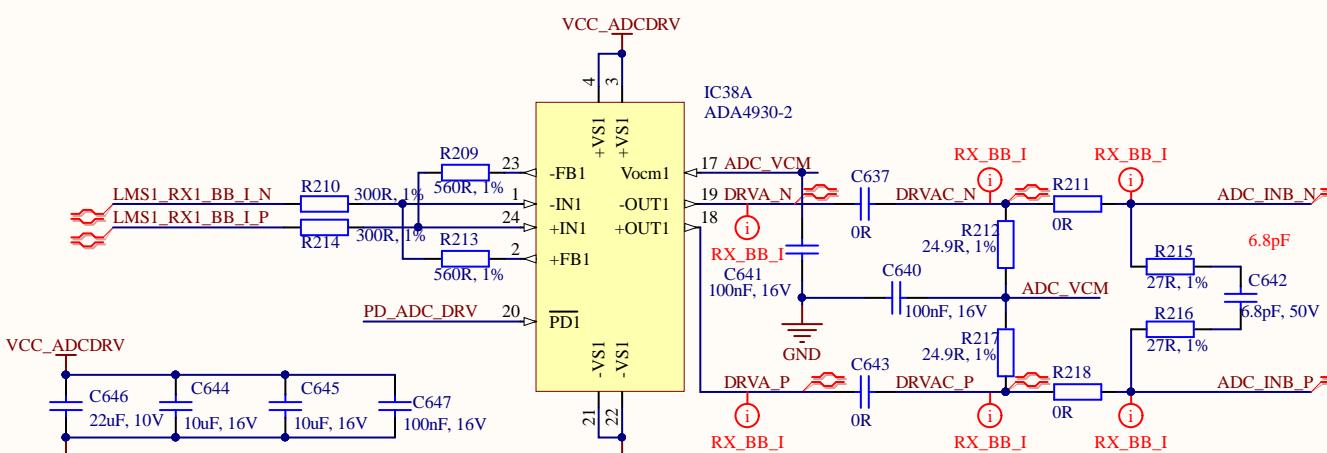


NF elements on sheet: R223, R234, R235, R236, R237

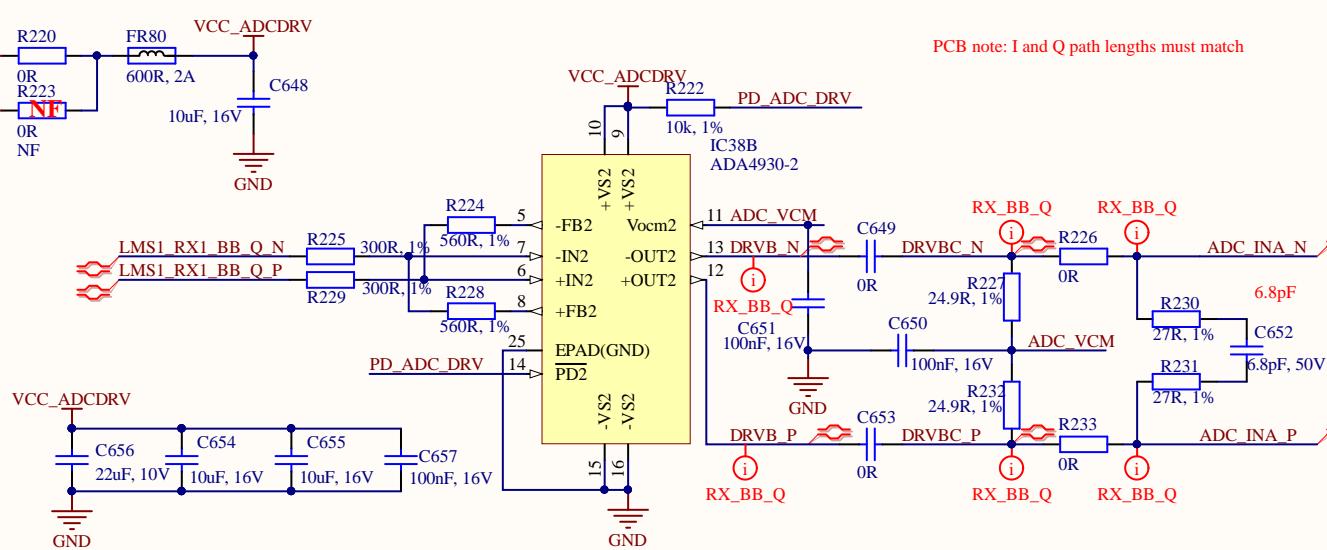
Number of NF elements on sheet: 5

ADC

ADC Drivers

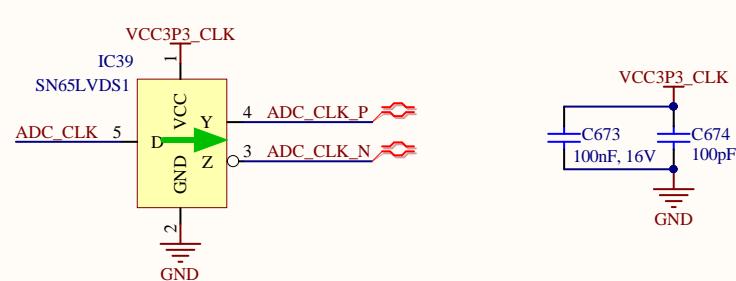


PCB note: I and Q path lengths must match



PCB note: I and Q path lengths must match

CLK converter

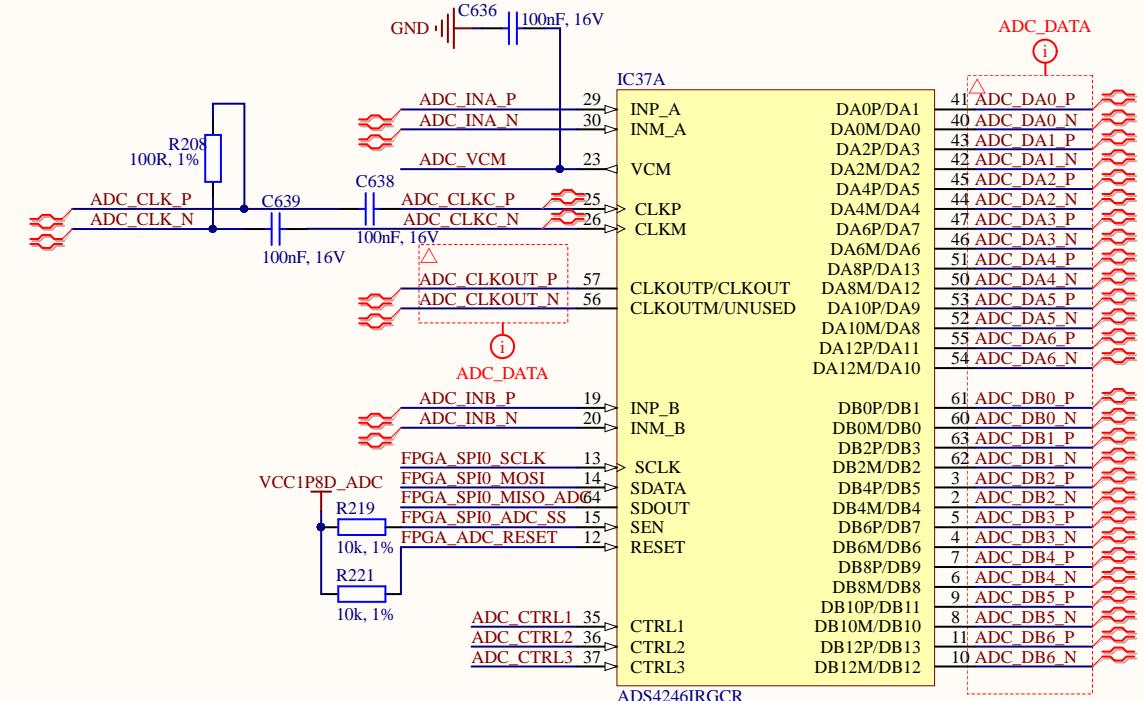


Local ADC and DAC fiducial Top



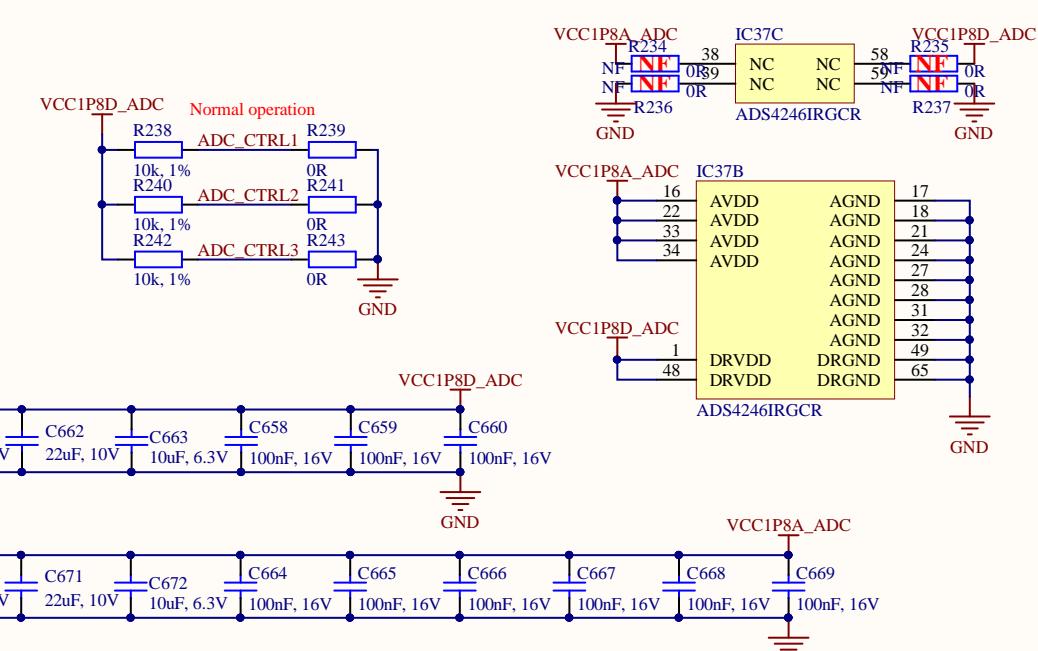
ADC

2 ch., 14-bit, 160MSPS



PCB note: Make equal lenght traces for ADC_DATA

ADC Control & Power



Project name: LimeSDR-QPCIe_1v2.PrjPcb

Title: ADC

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Guildford GU2 7YG
Surrey
United Kingdom

Size: A3

Revision: v1.2

Date: 2017-09-22

Time: 15:49:26

Sheet 18 of 27

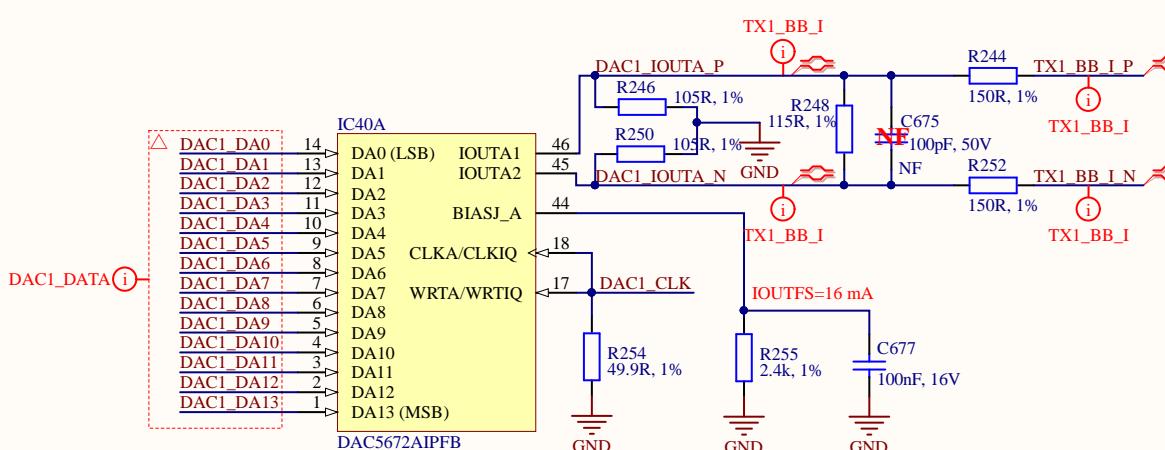
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NF elements on sheet: C675, C676, C679, C680, R269, R272, R273, R276, R277, R280, R281, R283
Number of NF elements on sheet: 12

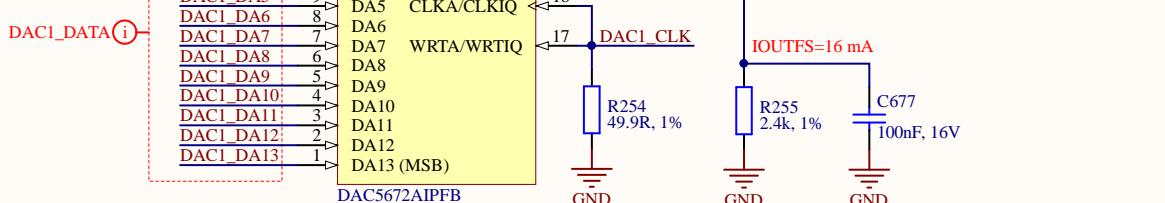
DAC #1

2 ch., 14-bit, 275MSPS

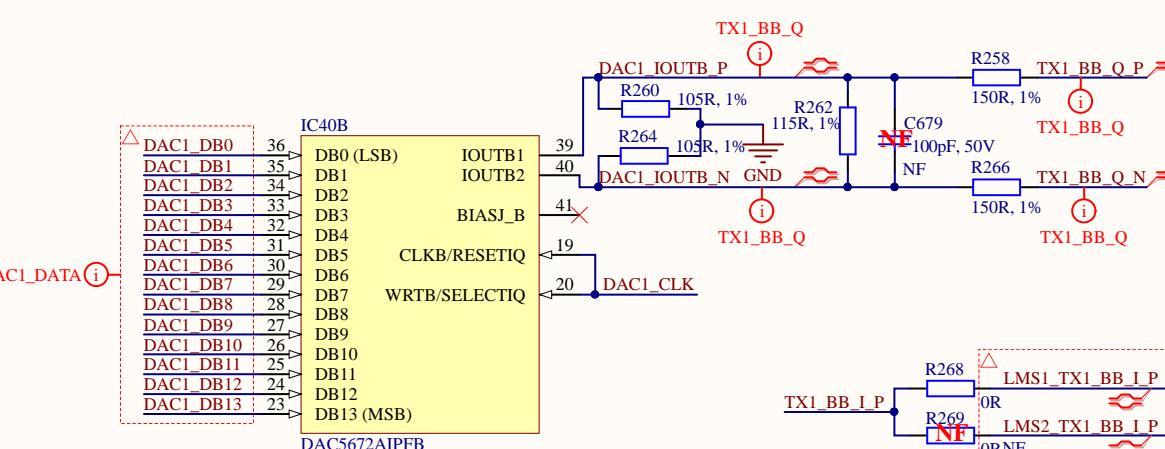


DAC #2

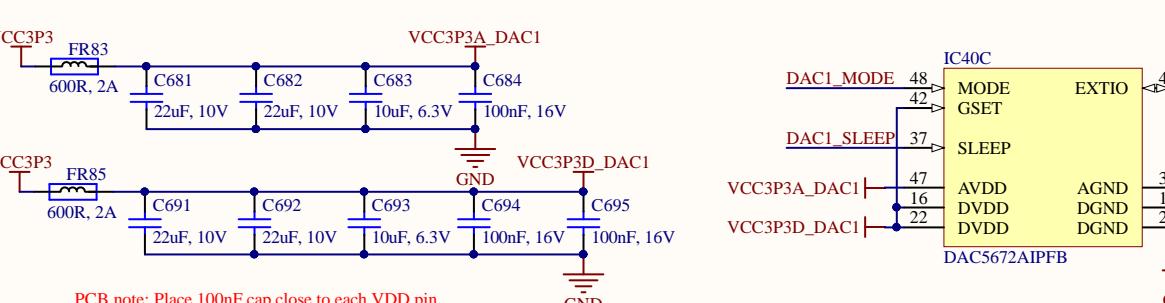
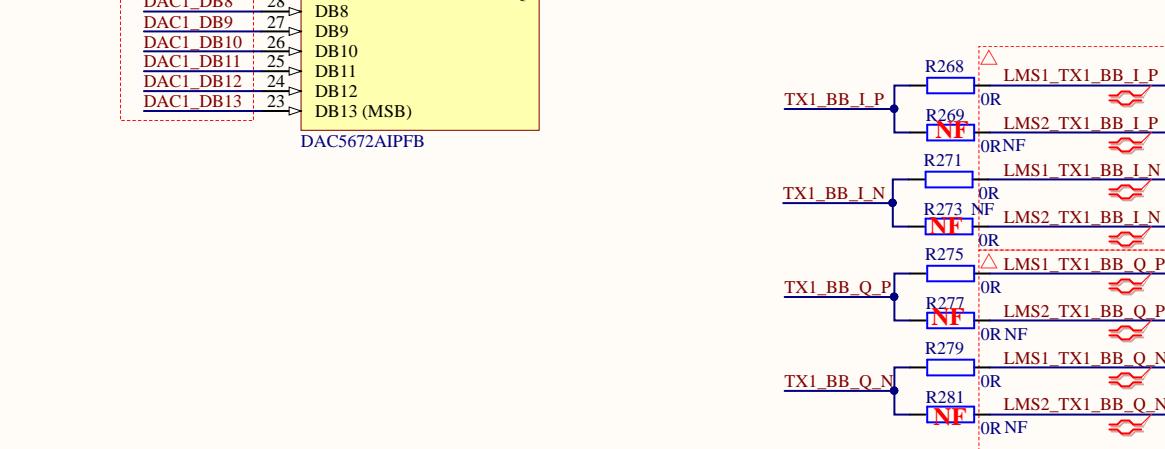
2 ch., 14-bit, 275MSPS



PCB note: I and Q path lengths must match
PCB note: Make equal lenght traces for DAC_DATA



PCB note: Make equal lenght traces for DAC_DATA



PCB note: Place 100nF cap close to each VDD pin.

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PCB note: Place 100nF cap close to each VDD pin.

PCB note: Place 100nF cap close to each VDD pin.

PCB note: Place 100nF cap close to each VDD pin.

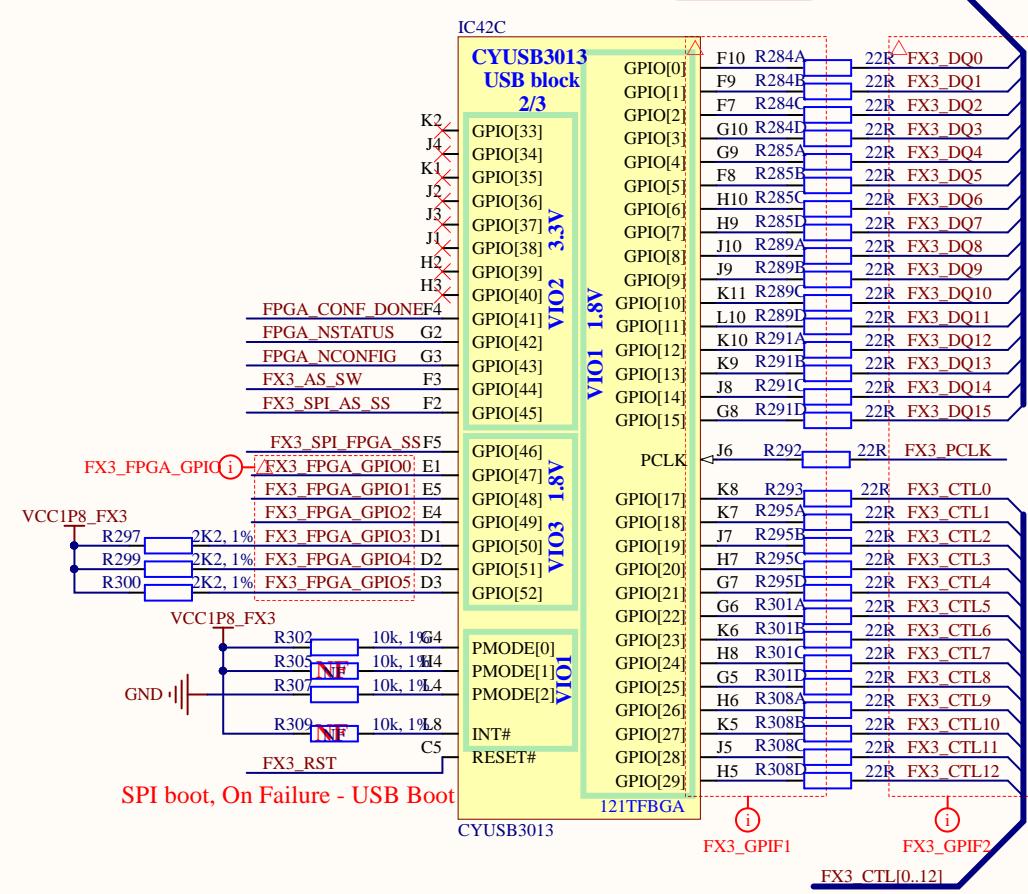
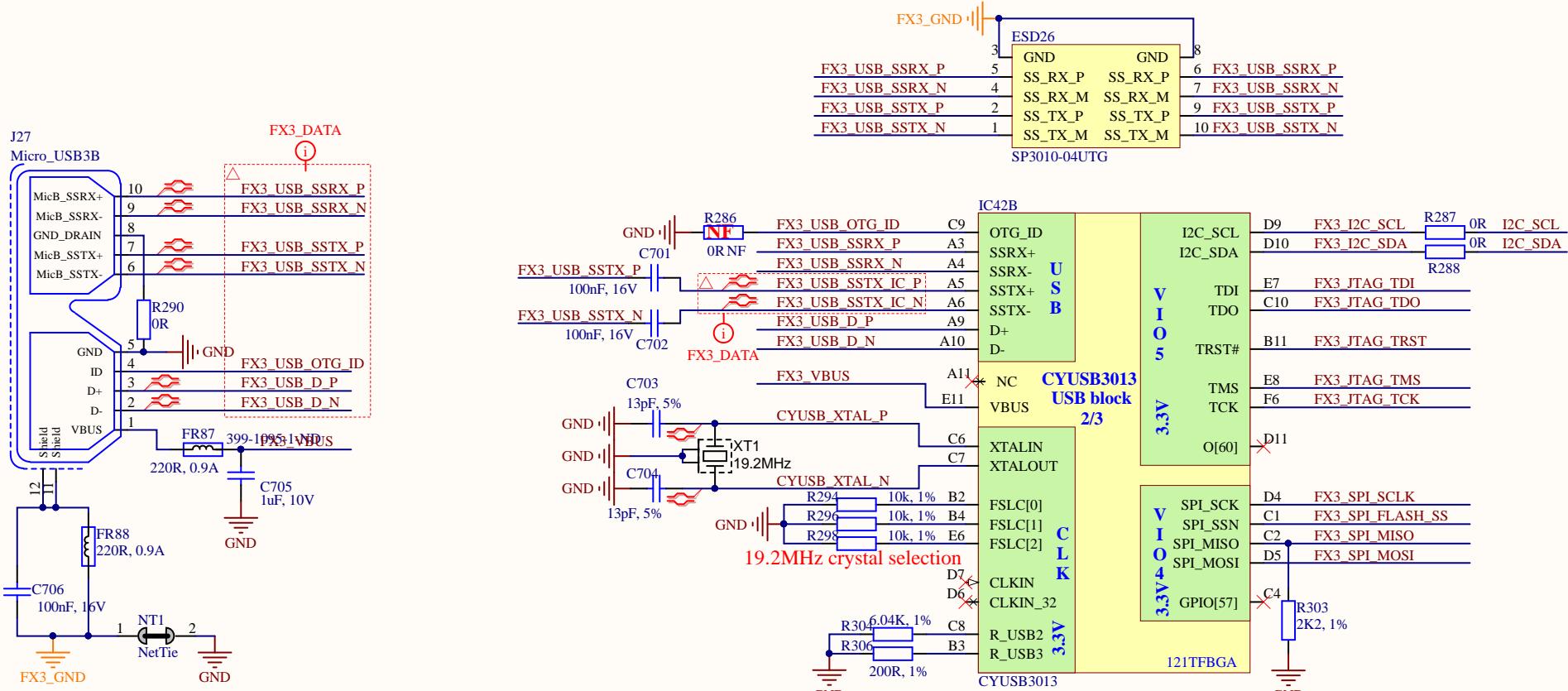
PCB note: Place 100nF cap close to each VDD pin.

PCB note: Place 100nF cap close to each VDD pin.

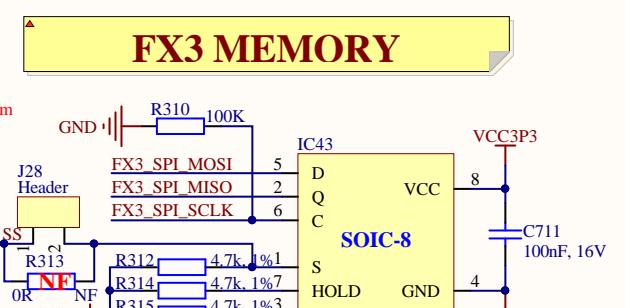
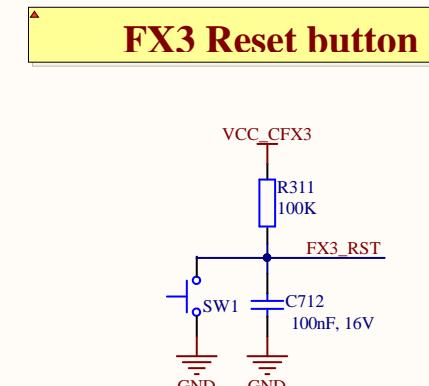
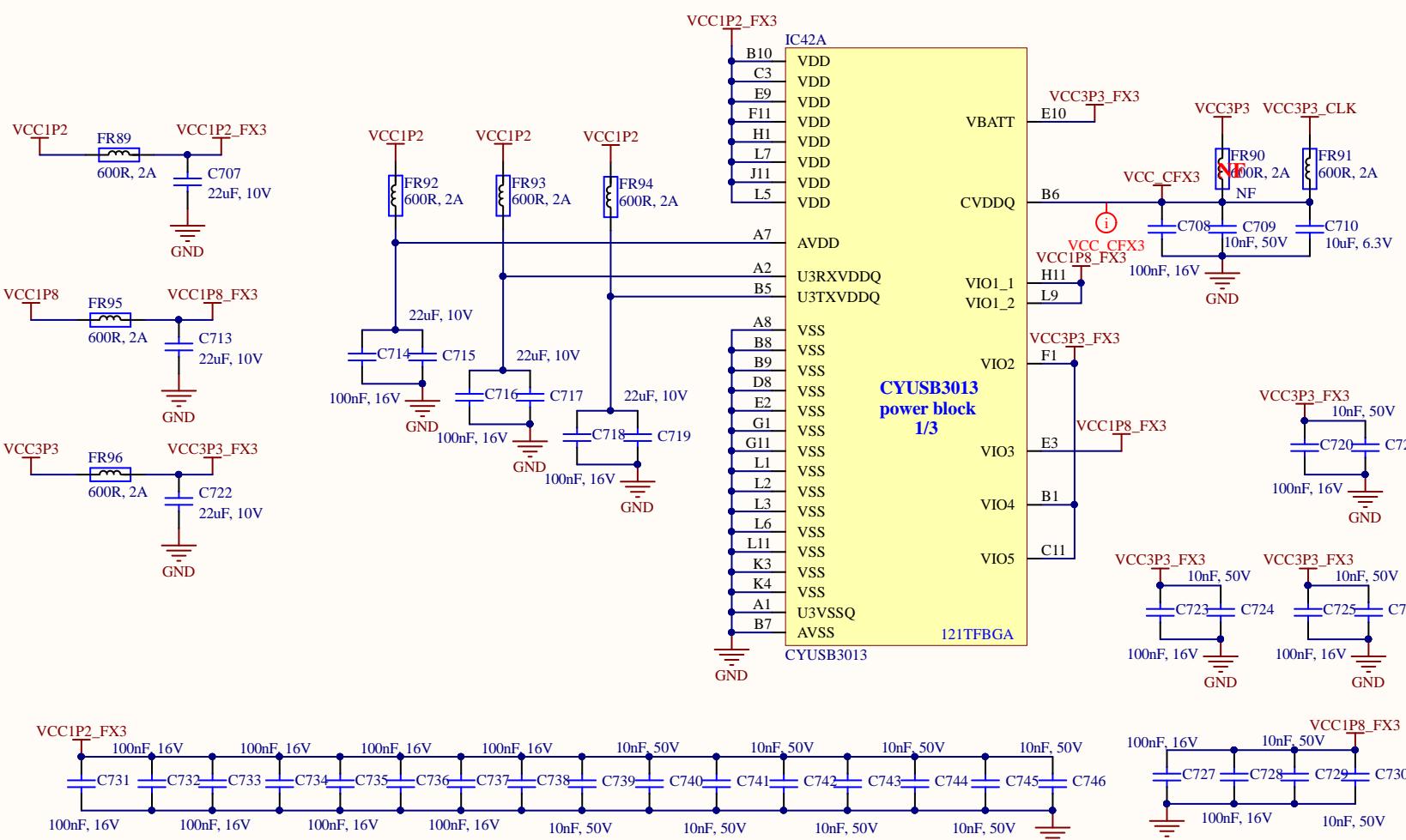
NF elements on sheet: R286, R305, R309, FR90, R313, R316, R317

Number of NF elements on sheet: 7

FX3 (USB3) core



FX3 power



Project name: LimeSDR-OPCJev2 PriPch

Title: *USB3.0 device*

Size: A3

Date: 2017-09-22 Time:

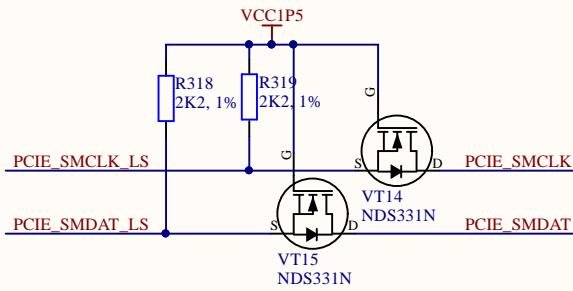
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Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom*



NF elements on sheet: R320, R321, R322, R324
Number of NF elements on sheet: 4

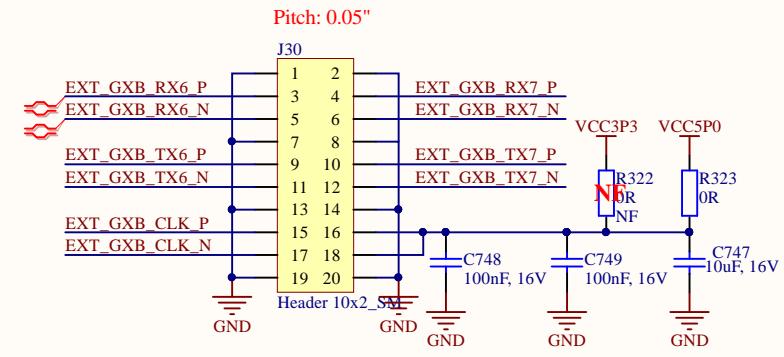
A

PCI Express x4

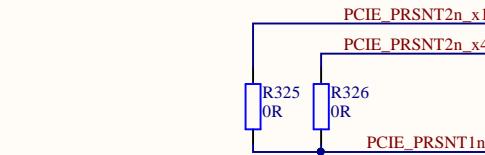


B

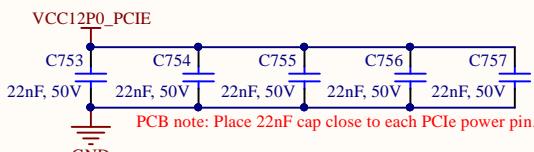
LVDS Connector



C



D



Project name: LimeSDR-QPCIe_Iv2.PrbPcb

Title: PCI Express x4

Size: A4 Revision: v1.2

Date: 2017-09-22 Time: 15:49:45 Sheet 21 of 27

File: 23_PCIE.SchDoc

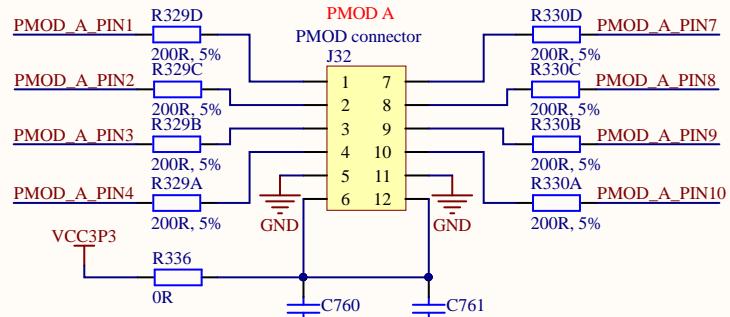
Bracket screws M2.5 x 6mm
Marked on board with symbol



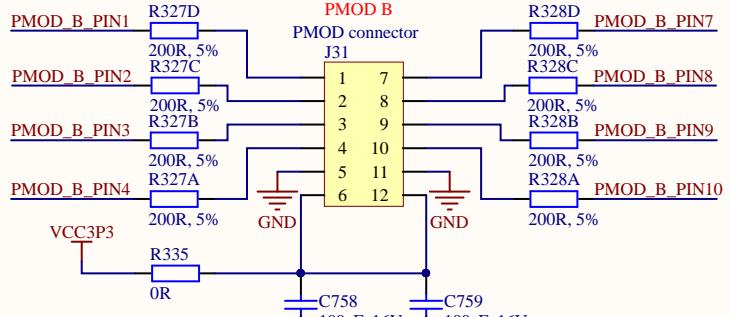
NF elements on sheet: R339, R342, R360
Number of NF elements on sheet: 3

Peripherals

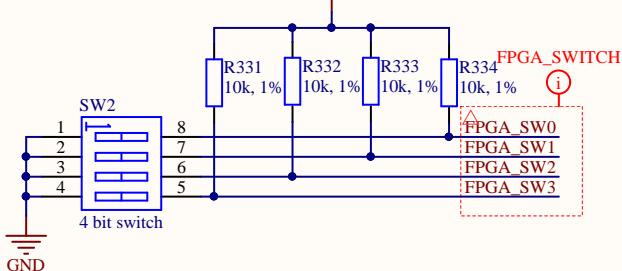
PMOD #A



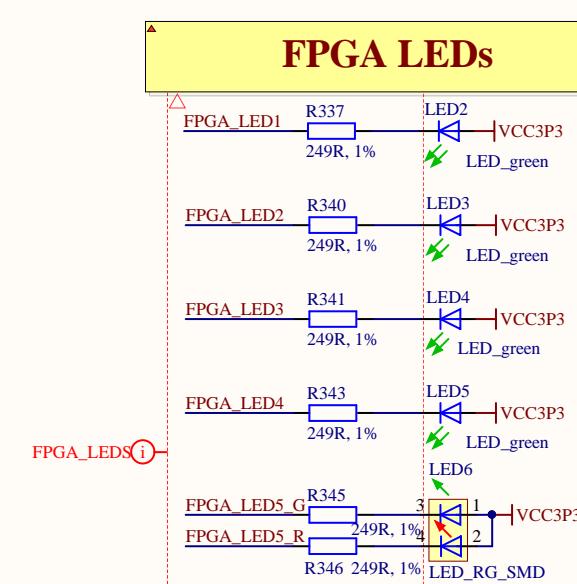
PMOD #B



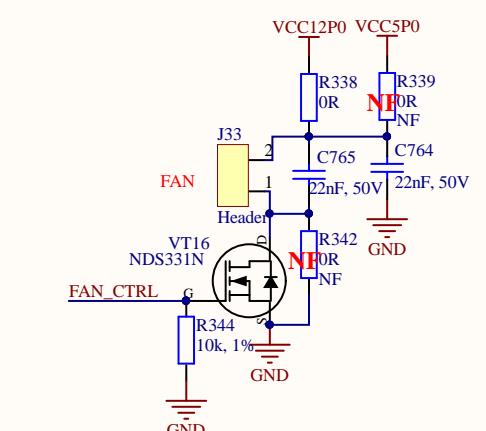
FPGA_SW



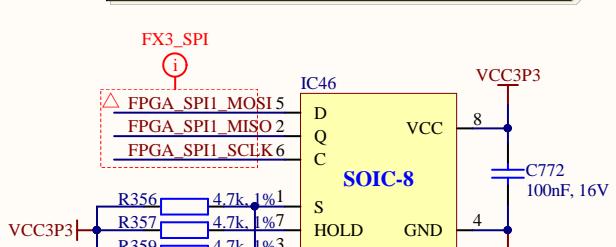
FPGA LEDs



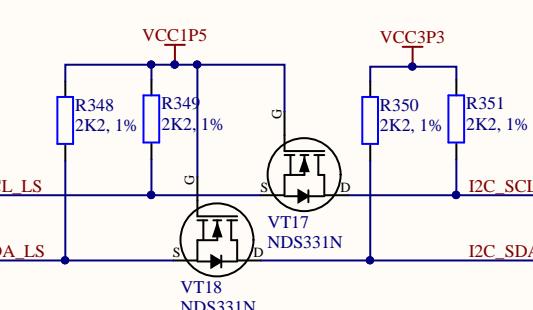
FAN control



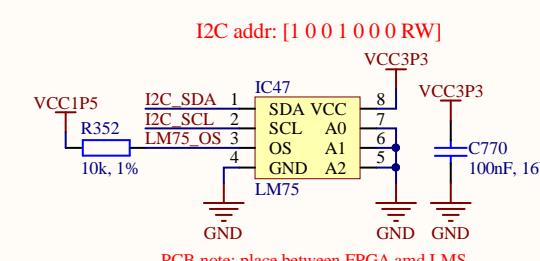
FPGA Flash



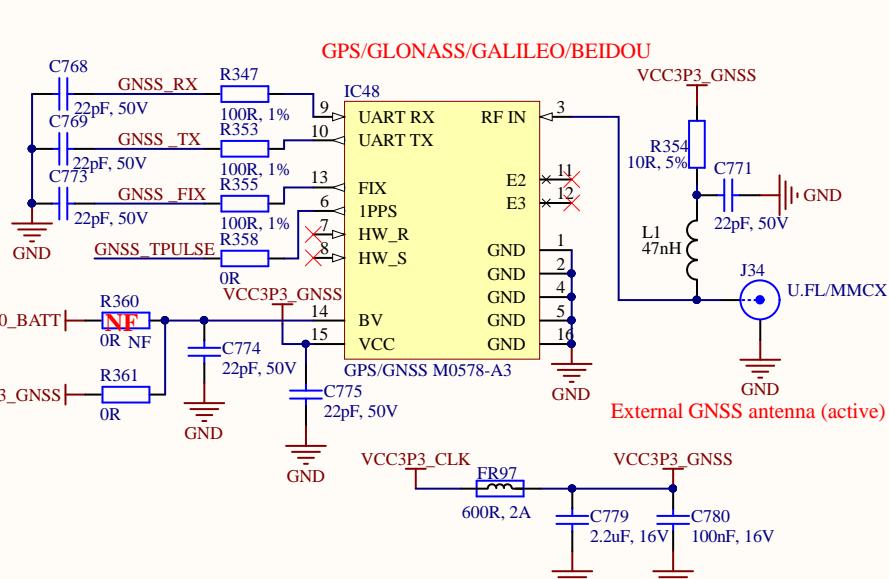
I2C Level converter



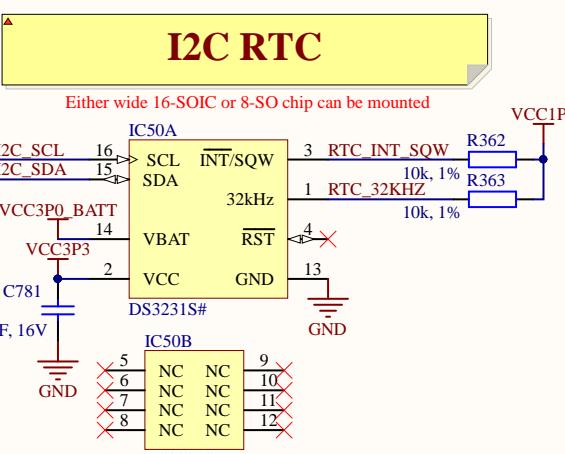
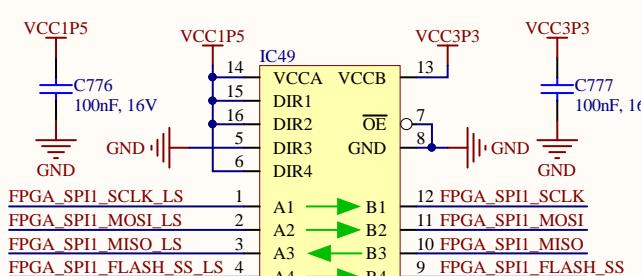
I2C Temperature sensor



GNSS receiver



D



Project name: LimeSDR-QPCIE_1v2.PrjPcb

Title: Peripherals

Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:49:51 Sheet 22 of 27

File: 24_Peripherals.SchDoc

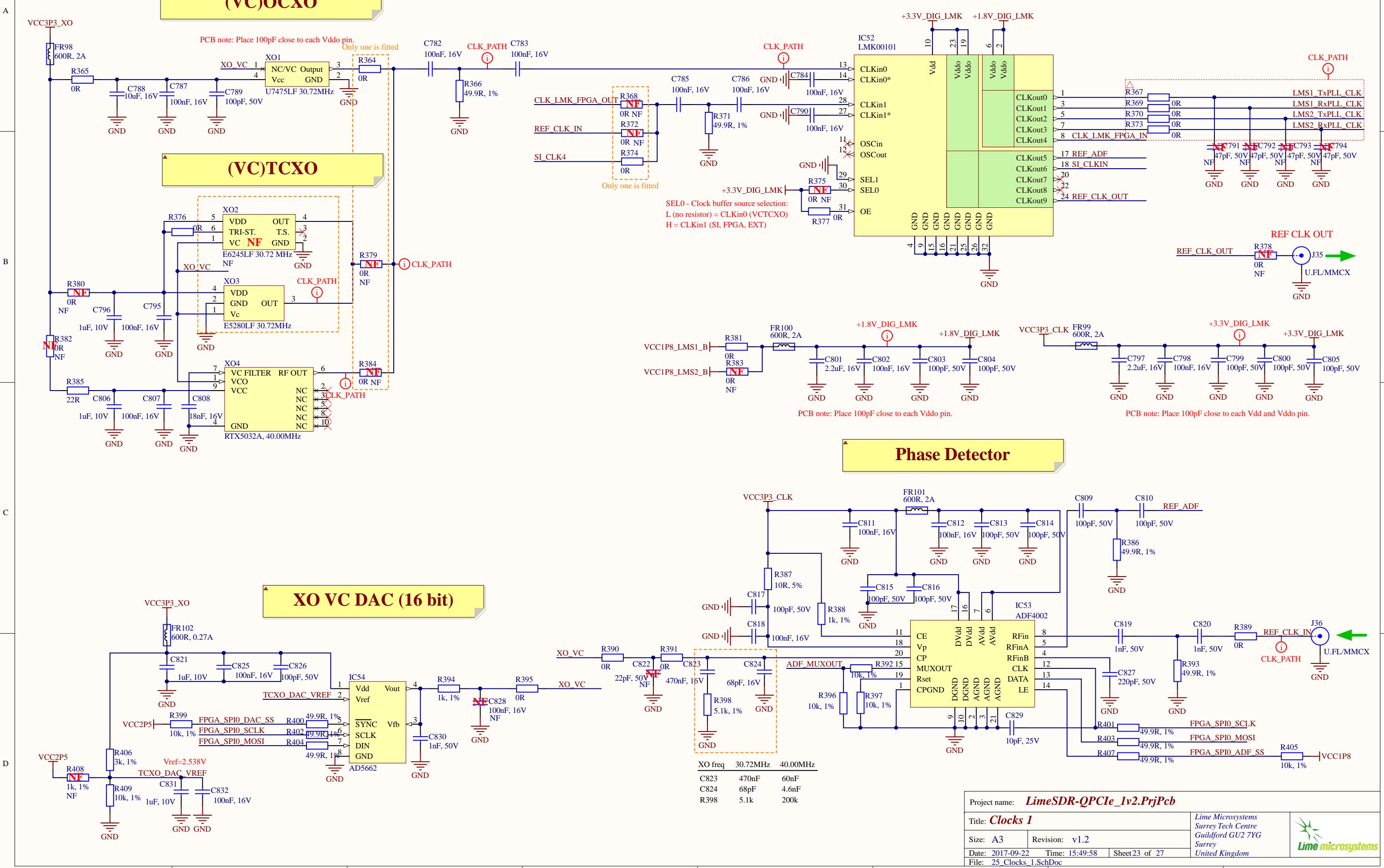
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NF elements on sheet: XO2, R368, R372, R375, C791, C792, C793, C794, R378, R379, R380, R382, R383, R384, R408, C822, C828
Number of NF elements on sheet: 17

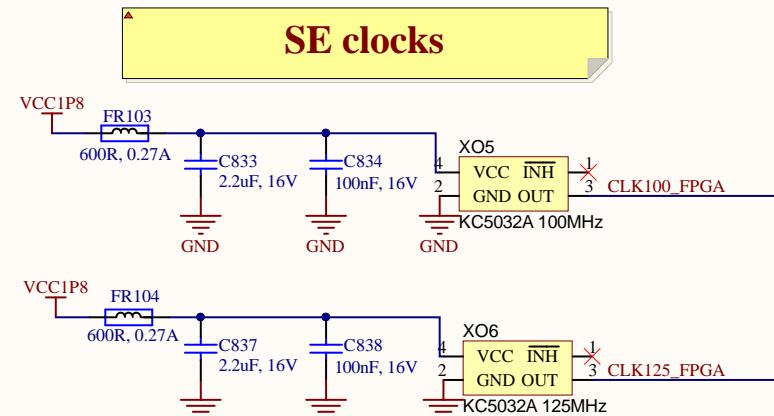
Clock circuits 1

REF CLK OUT

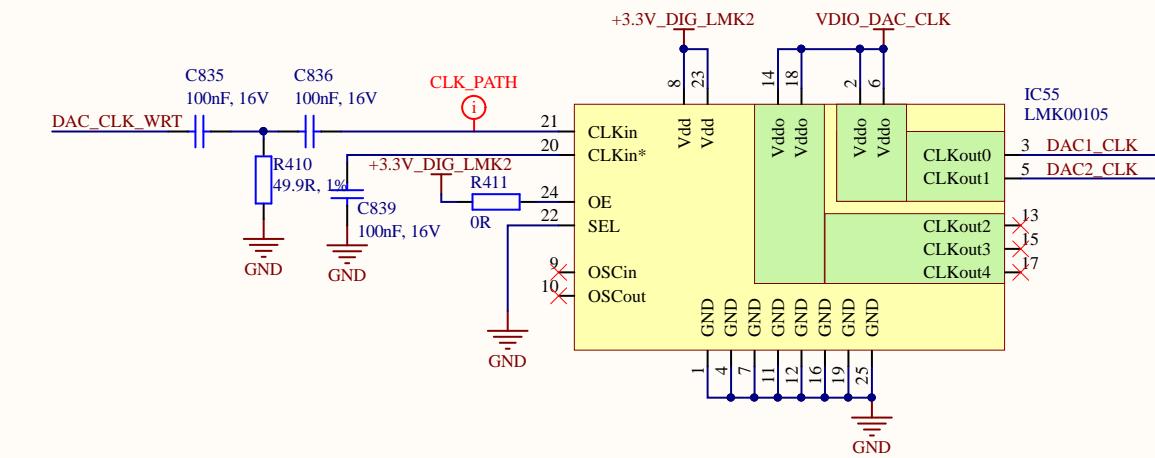


NF elements on sheet: R414, R416
Number of NF elements on sheet: 2

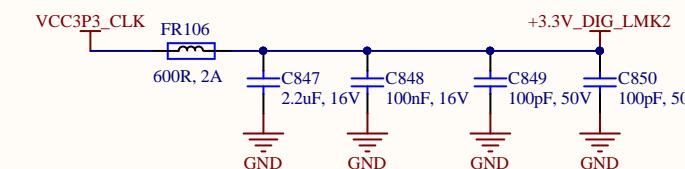
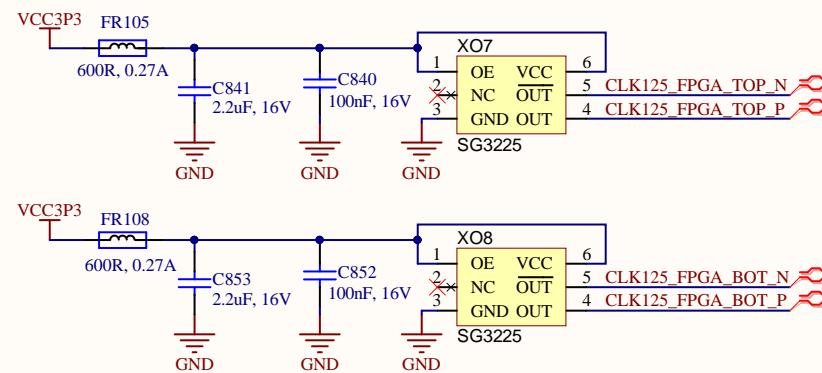
Clock circuits 2



DAC clock buffer



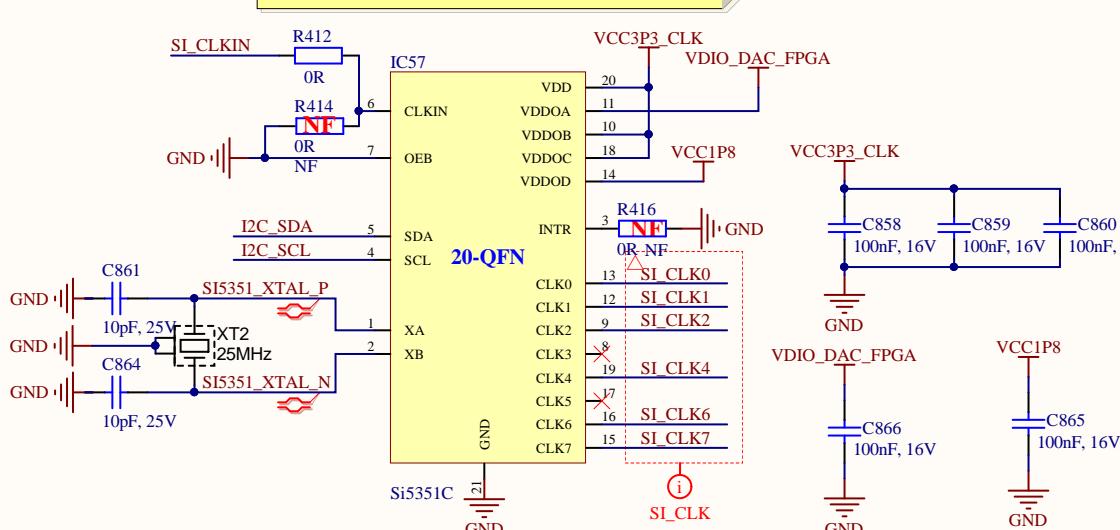
LVDS clocks for RAM



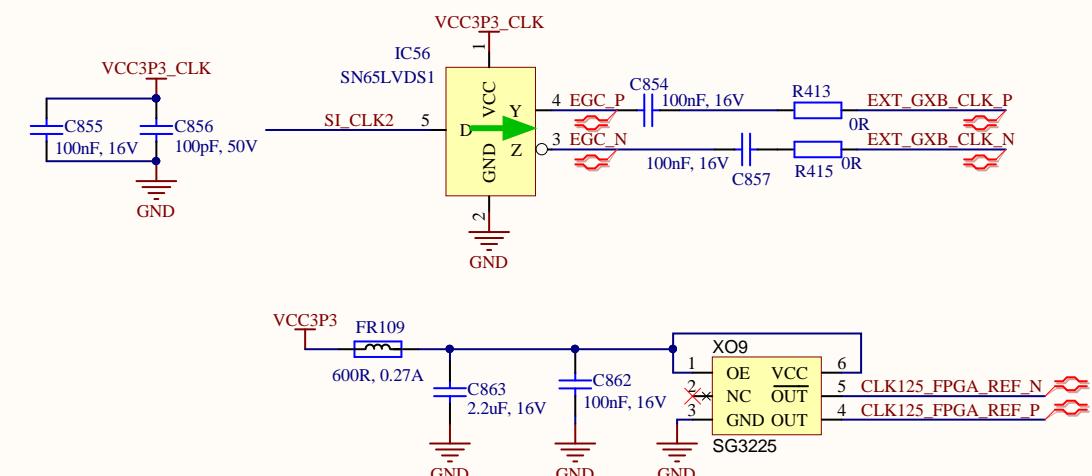
PCB note: Place 100pF close to each Vdd pin.

PCB note: Place 100pF close to each Vdd and Vddo pin.

Clock generator



LVDS clocks for GXB



Project name: LimeSDR-QPCIe_1v2.PrcPcb

Title: Clocks 2

Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:50:04 Sheet 24 of 27

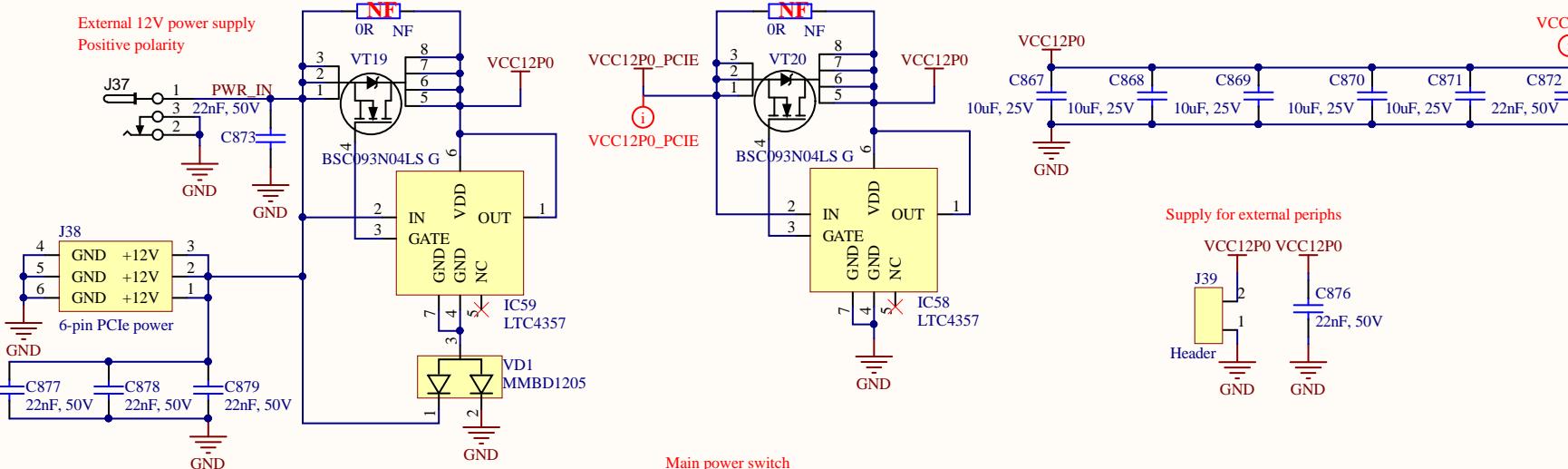
File: 26_Clocks_2.SchDoc

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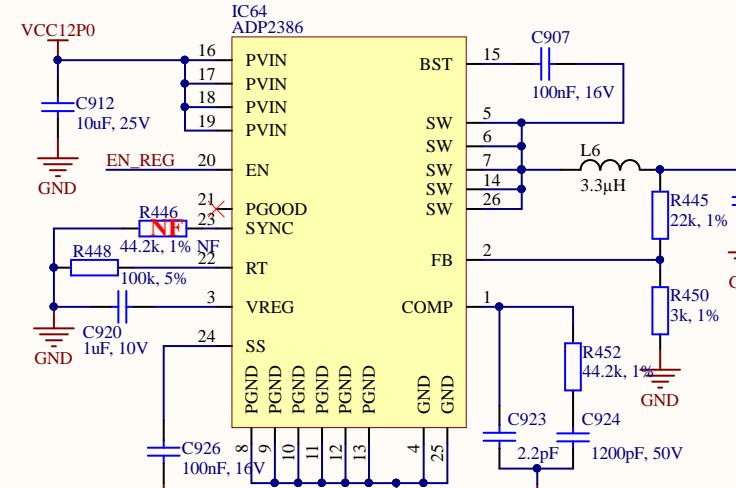
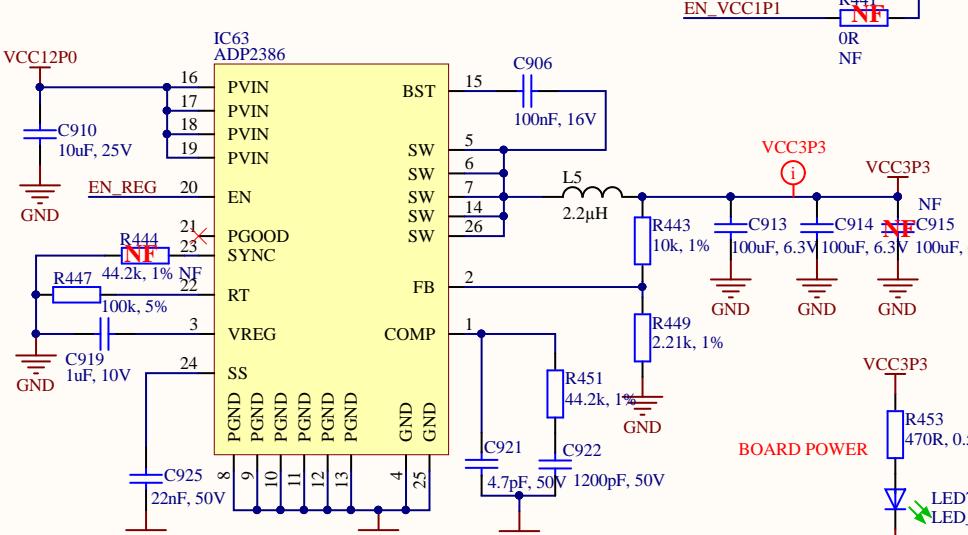
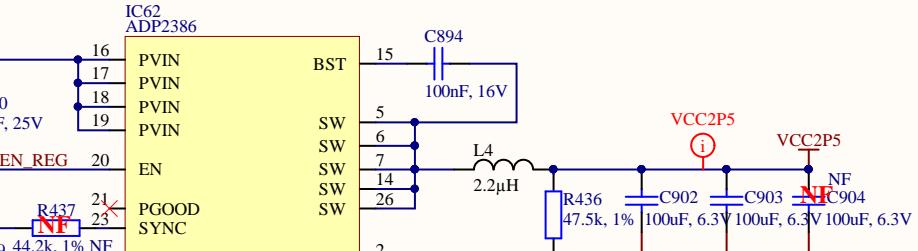
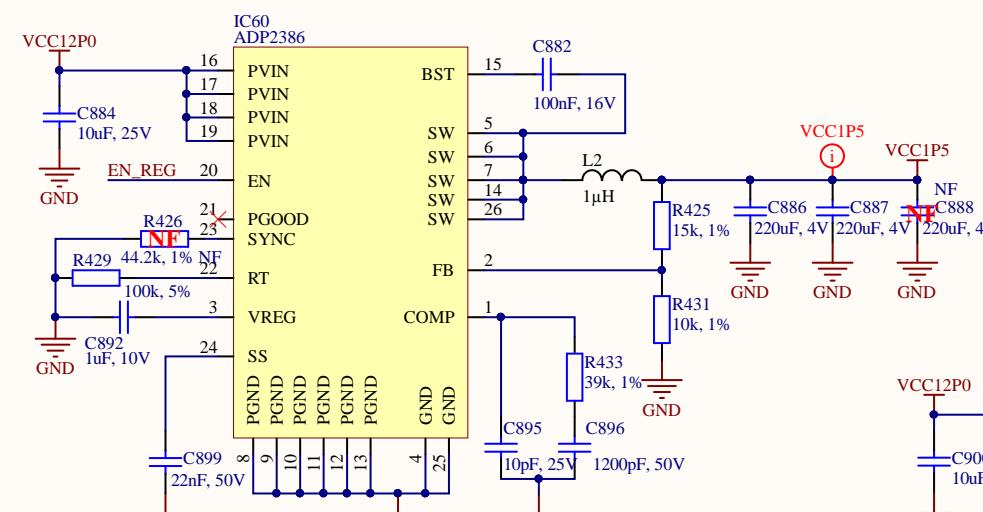
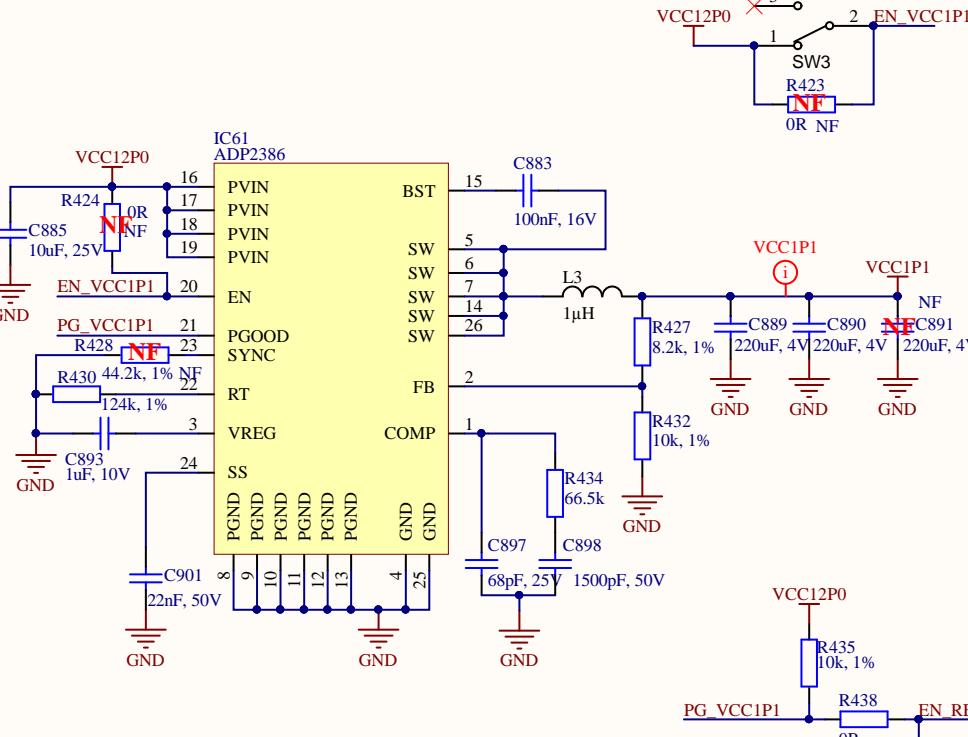
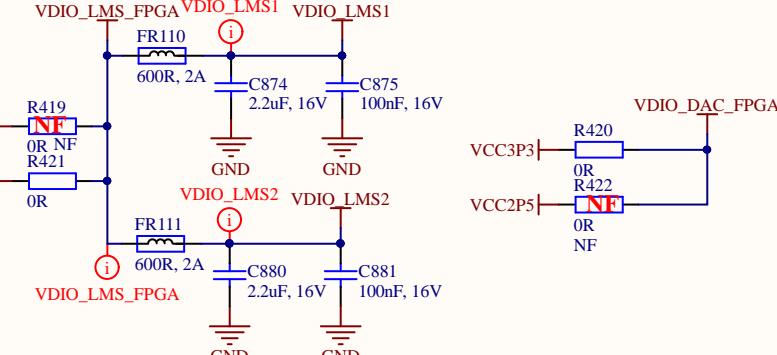


NF elements on sheet: R417, R418, R419, R422, R423, R424, R426, R428, C891, C888, R437, C904, R441, R444, C915, R446, C918
Number of NF elements on sheet: 17

Board power circuits 1



LMS & DAC VIO selection



Project name: LimeSDR-QPCIe_1v2.PrjPcb

Title: Board power supply 1

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Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:50:11 Sheet 25 of 27

File: 27_BoardPowerSupply1.SchDoc

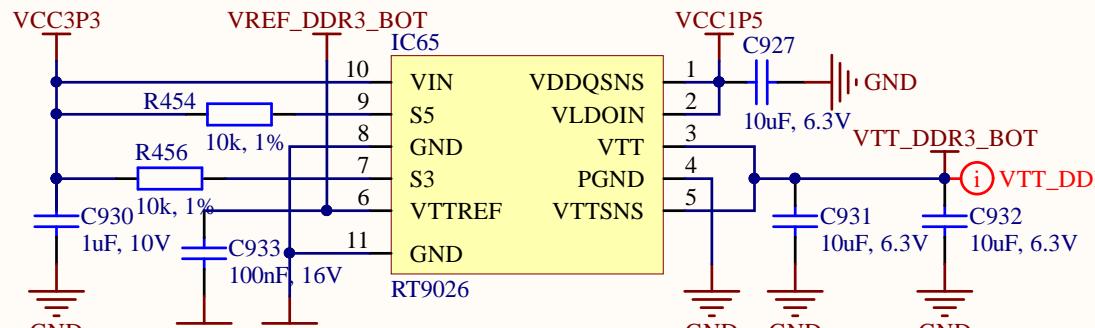


NF elements on sheet: R457, C934, R461, R462, C943, C946, IC70, C948, C947, R469, R472, C949, C952

Number of NF elements on sheet: 13

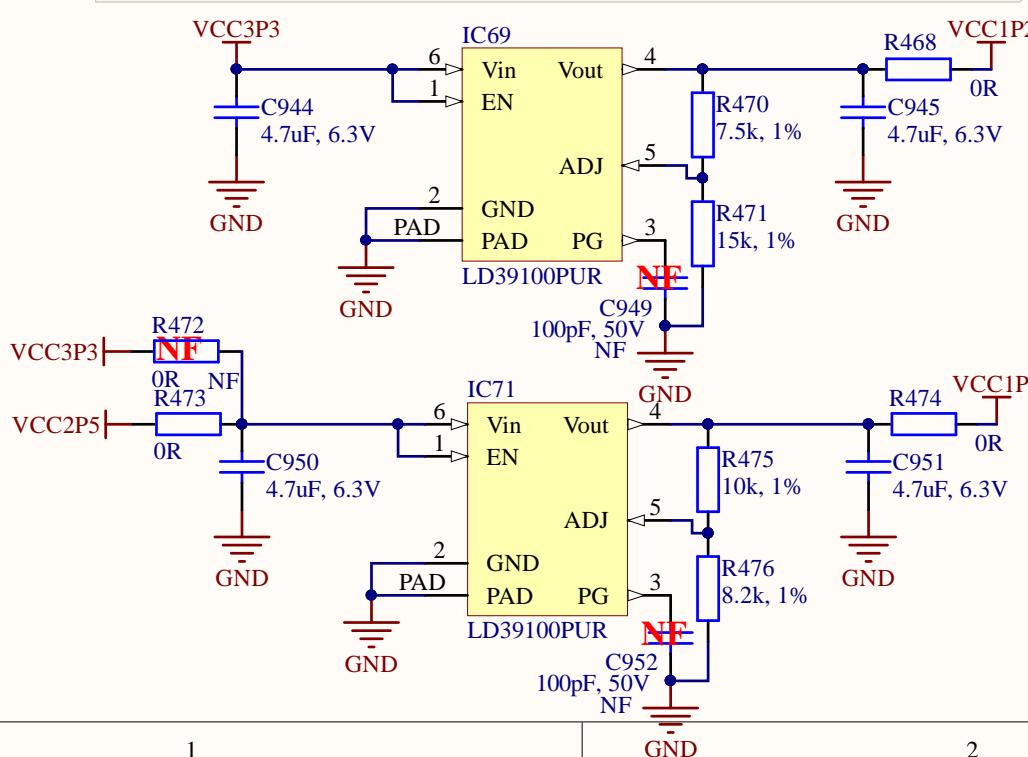
Board power circuits 2

DDR3 VTT

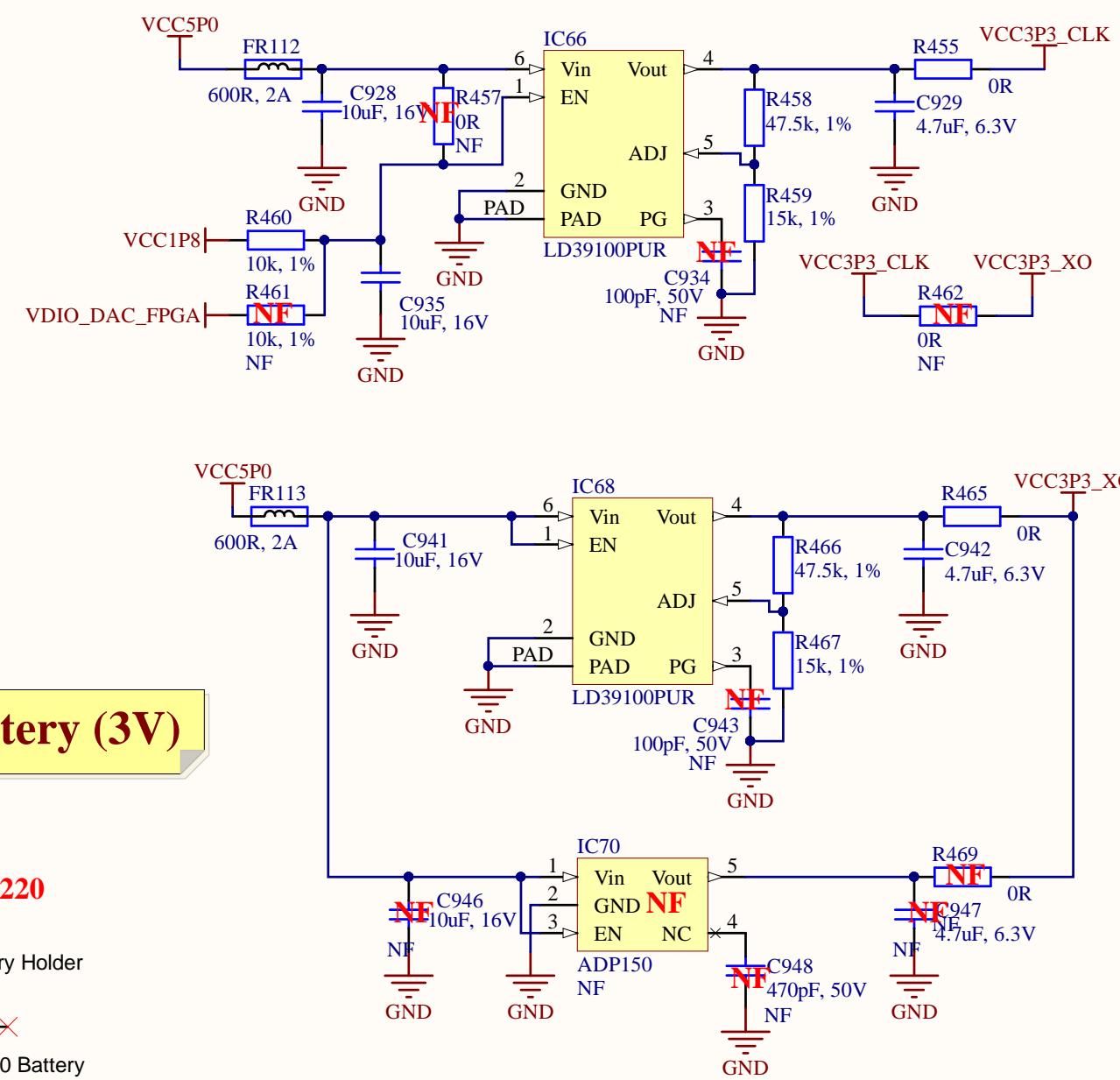


PCB note: Connect VTTNSNS to plus terminal of the output capacitor.

Other

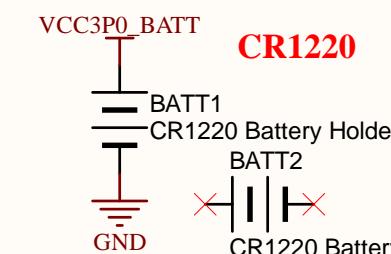


Clock network power



For ADP150 do not need capacitor on pin 4
Possible to use TC1185-3.3VCT713 LDO with bypass capacitor on pin 4

Lithium coin battery (3V)



Project name: LimeSDR-QPCIe_1v2.PrjPcb

Title: Board power supply 2

Size: A4 Revision: v1.2

Date: 2017-09-22 Time: 15:50:17 Sheet 26 of 27

File: 28_BoardPowerSupply 2.SchDoc

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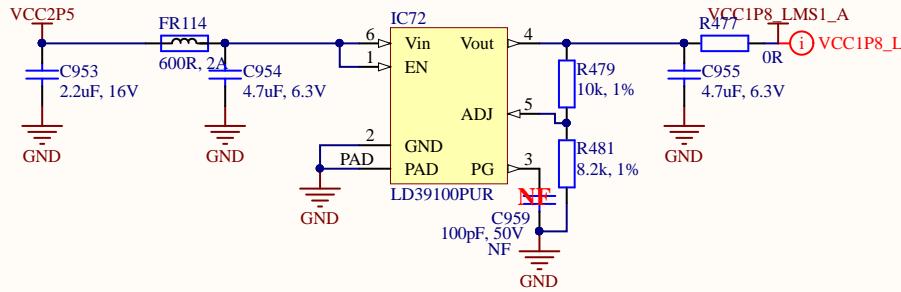


NF elements on sheet: C959, C960, C967, C968, C975, C976, C983, C984
Number of NF elements on sheet: 8
Total number of NF elements on all sheets: 162

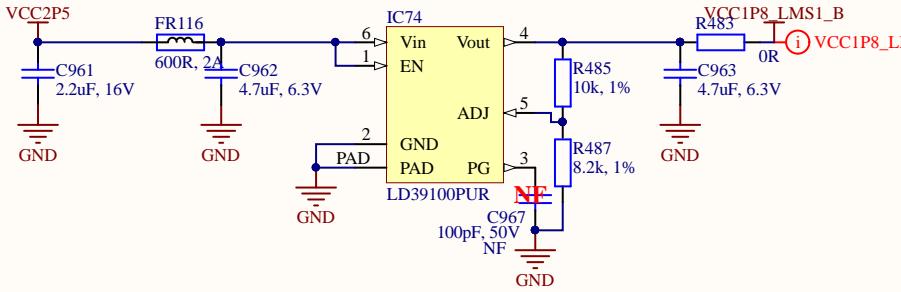
LMS7002M power supply

A

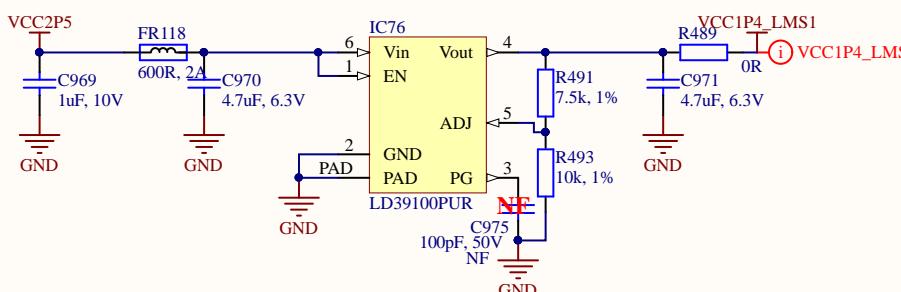
LMS #1



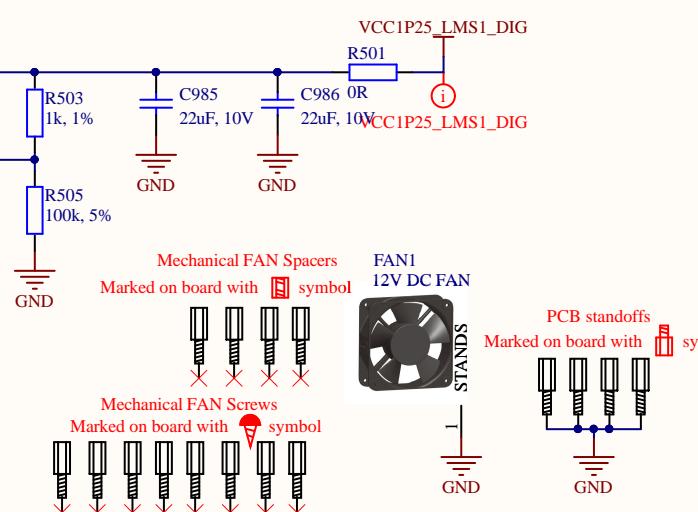
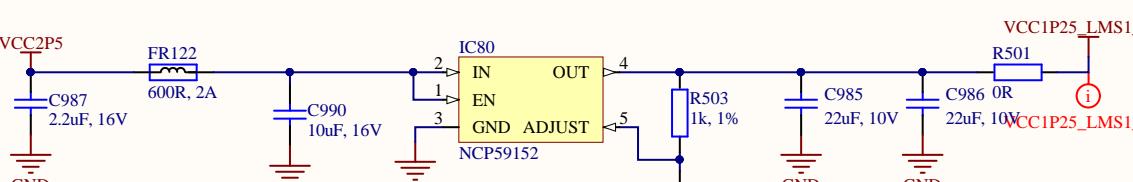
B



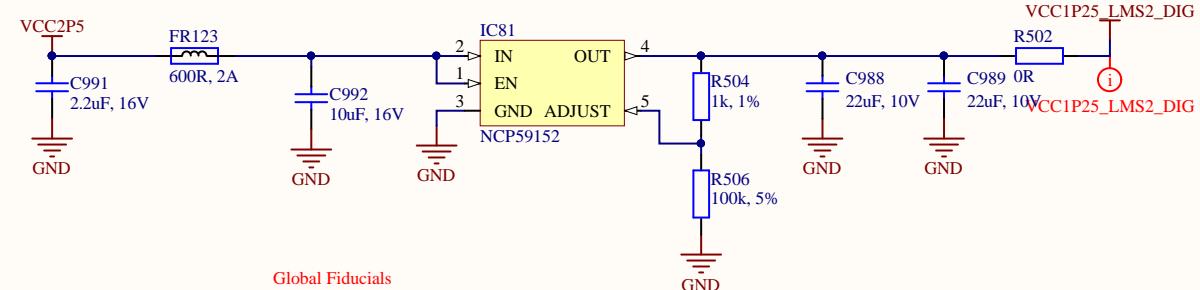
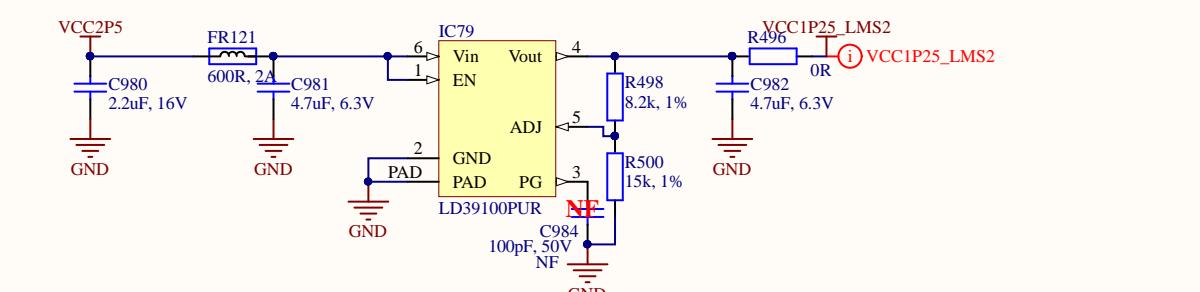
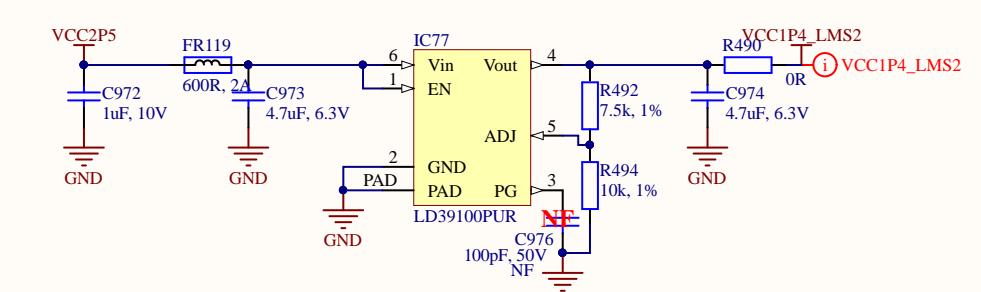
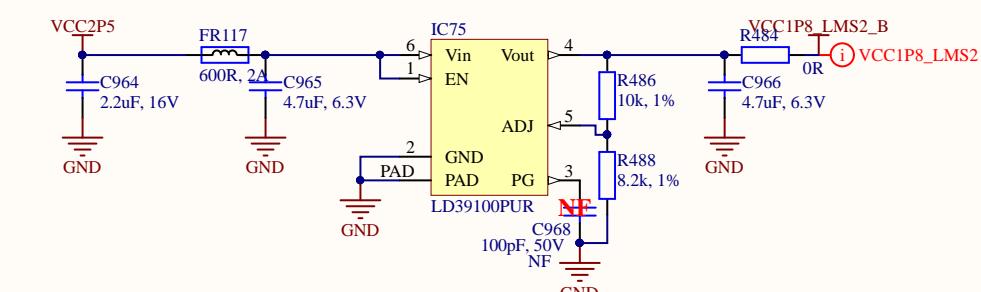
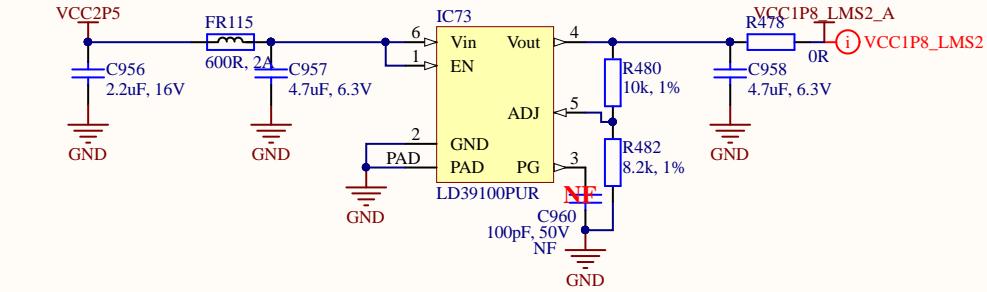
C



D



LMS #2



Project name: LimeSDR-QPCIE_1v2.PrbPcb

Title: LMS7002M power supply

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Size: A3 Revision: v1.2

Date: 2017-09-22 Time: 15:50:24 Sheet 27 of 27

File: 29_LMS7002M_PowerSupply.SchDoc