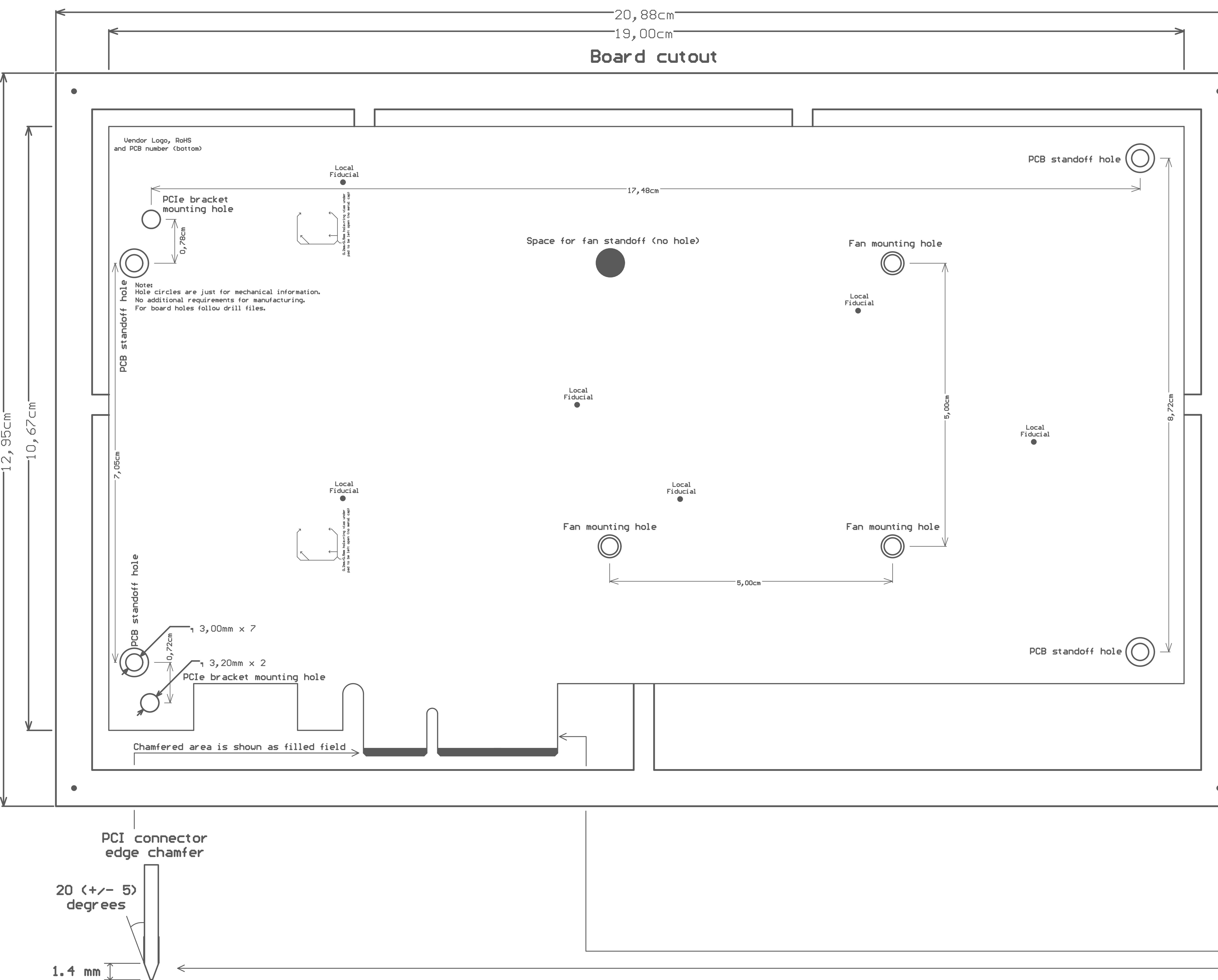
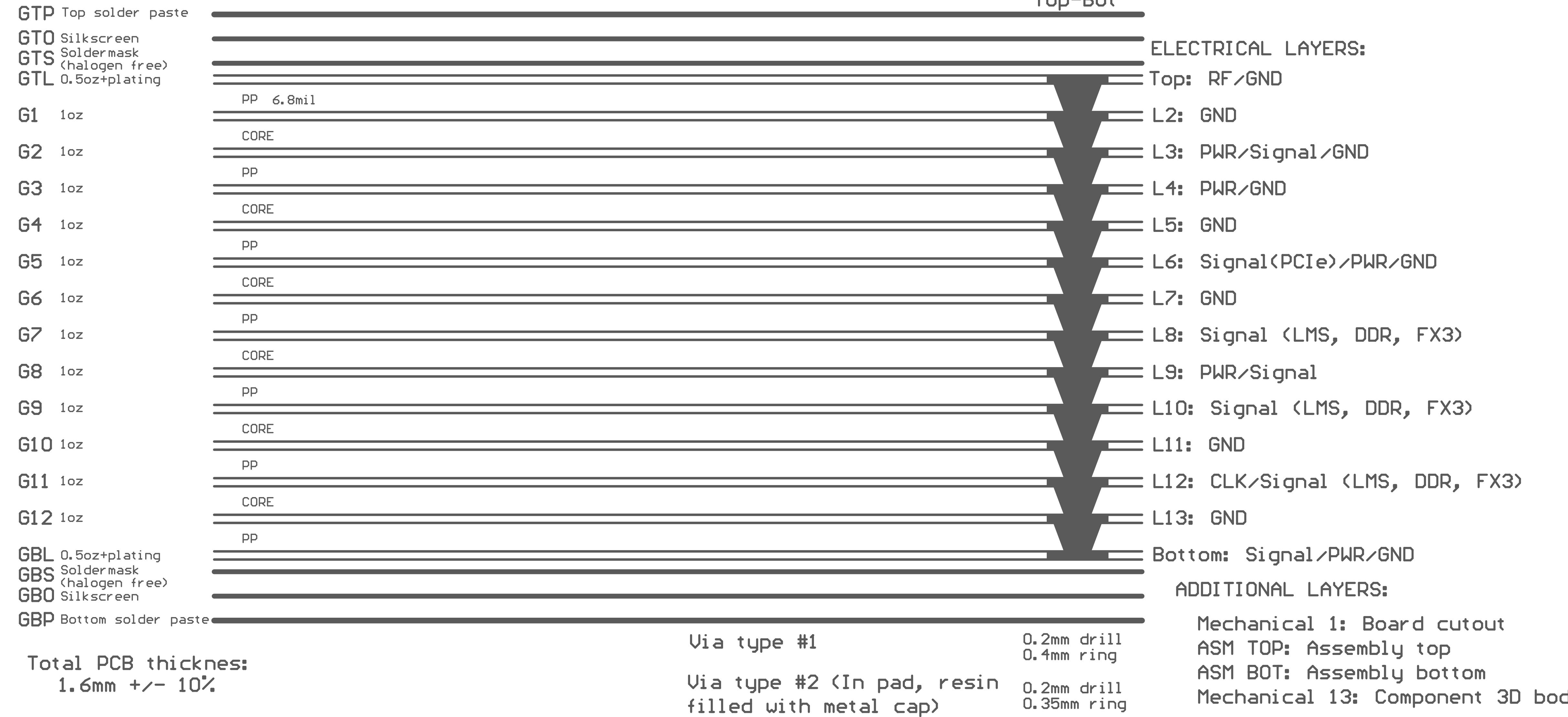


## GERBER LAYER NAMES: STACKUP:



## CONTROLLED IMPEDANCE

### GENERAL PARAMETERS:

Top layer copper foil thickness: 17.5 um  
Dielectric thickness from Top to L2 = 173um (6.8 mils)  
Dielectric between Top layer and 2nd layer relative permittivity ( $\epsilon_r$ ): 4.2  
Ground plane distance to trace on Top layer: 0.1mm

### CALCULATIONS:

#### 50 Ohm coplanar waveguide without ground (Top layer) characteristics:

Top layer copper foil thickness: 17.5 um  
Track width = 0.309 mm (12.165 mils)  
Dielectric thickness from Top to L2 = 173um (6.8 mils)  
Dielectric between Top layer and 2nd layer relative permittivity ( $\epsilon_r$ ): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

#### 100 Ohm coplanar differential pair without ground (Top layer) characteristics:

Top layer copper foil thickness: 17.5 um  
Track width = 0.2 mm (7.874 mils)  
Track spacing = 0.1 mm (3.937 mils)  
Track width/spacing ratio = 2  
Dielectric thickness from top to L2 = 173um (6.8 mils)  
Dielectric between Top layer and 2nd layer relative permittivity ( $\epsilon_r$ ): 4.2

Approximate coupled microstrip line impedance = 100.7 Ohms (+/- 10% tolerance)

#### 50 Ohm coplanar waveguide with GND (Bottom layer) characteristics:

Bottom layer copper foil thickness: 17.5 um  
Track width = 0.254 mm (10 mils)  
Distance to GND: 0.1 mm (3.937 mils)  
Dielectric thickness from Bottom to L13 = 173um (6.8 mils)  
Dielectric between Bottom layer and L13 relative permittivity ( $\epsilon_r$ ): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

#### 90 Ohm coupled microstrip line (Top layer, without GND) characteristics:

Top layer copper foil thickness: 17.5 um  
Track width = 0.2 mm (6.8 mils)  
Track spacing = 0.1 mm (3.93 mils)  
Track width/spacing ratio = 2  
Dielectric thickness from Top to 2nd layer = 173um (6.8 mils)  
Dielectric between Top layer and 2nd layer relative permittivity ( $\epsilon_r$ ): 4.2

Approximate coupled microstrip line impedance = 90.5 Ohms (+/- 10% tolerance)

#### 85 Ohm coupled microstrip line (Top layer, PCI traces) characteristics:

Top layer copper foil thickness: 17.5 um  
Track width = 0.25 mm (9.84 mils)  
Track spacing = 0.1 mm (3.93 mils)  
Track width/spacing ratio = 2.5  
Dielectric thickness from Top to 2nd layer = 173um (6.8 mils)  
Dielectric between Top layer and 2nd layer relative permittivity ( $\epsilon_r$ ): 4.2

Approximate coupled microstrip line impedance = 84.8 Ohms (+/- 10% tolerance)

#### 85 Ohm coupled microstrip line (Bottom layer, PCI traces) characteristics:

Bottom layer copper foil thickness: 17.5 um  
Track width = 0.25 mm (9.84 mils)  
Track spacing = 0.1 mm (3.93 mils)  
Track width/spacing ratio = 2.5  
Dielectric thickness from L13 to Bottom layer = 173um (6.8 mils)  
Dielectric between L13 layer and Bottom layer relative permittivity ( $\epsilon_r$ ): 4.2

Approximate coupled microstrip line impedance = 85 Ohms (+/- 10% tolerance)

## VERY IMPORTANT NOTES:

- 1) 0.35mm ring and 0.2mm drill via-in-pads (IC1 and IC4) must be resin filled with metal cap.
- 2) IC1 and IC4 thermal pad vias with 0.4mm ring and 0.2mm drill must be resin filled with metal cap. IC1 and IC4 thermal pad vias with 0.5mm ring and 0.2mm drill must be left open (NO resin fill with metal cap). 8 vias in total, marked with note.
- 3) Solder mask : DARK BLUE, both sides, halogen free, glossy finish (NOT matte).
- 4) Silkscreen : white epoxy ink, halogen free, both sides. No silkscreen on pads.
- 5) DRCs must be run on Gerber files before building boards
- 6) Hole diameters are final manufactured diameters INCLUDING HOLE METALIZATION.
- 7) Minimum track spacing: 0.1 mm  
Minimum track width: 0.1 mm
- 8) There are plated and non-plated holes on the PCB
- 9) Material:  
IT-180A  
PCB vendor to silkscreen UL and RoHS compliance marks, vendor logo and date code on bottom where shown  
Copper weight: External layers 0.5 oz+plating  
Internal layers 1 oz
- 10) Electrical test : 100 % netlist.
- 11) Boards are to be individually bagged.
- 12) PCI EXPRESS pads (top and bottom) - 30 micro inches of gold over 50 micro inches nickel plating
- 13) Board edge below PCI pads must be chamfered (as shown). Edges must be free of cutting burrs
- 14) Assembly note: Assembly house MUST provide notes in paper with shipped board if there were any changes during assembly and the board is not assembled 100% according to BOM and P&P files. Note example:

Part	Initial BOM asm. note	Status on board	Comment
R1	FIT	NF	Not mounted due to bad footprint
IC5	FIT	NF	Not mounted due to part shortage