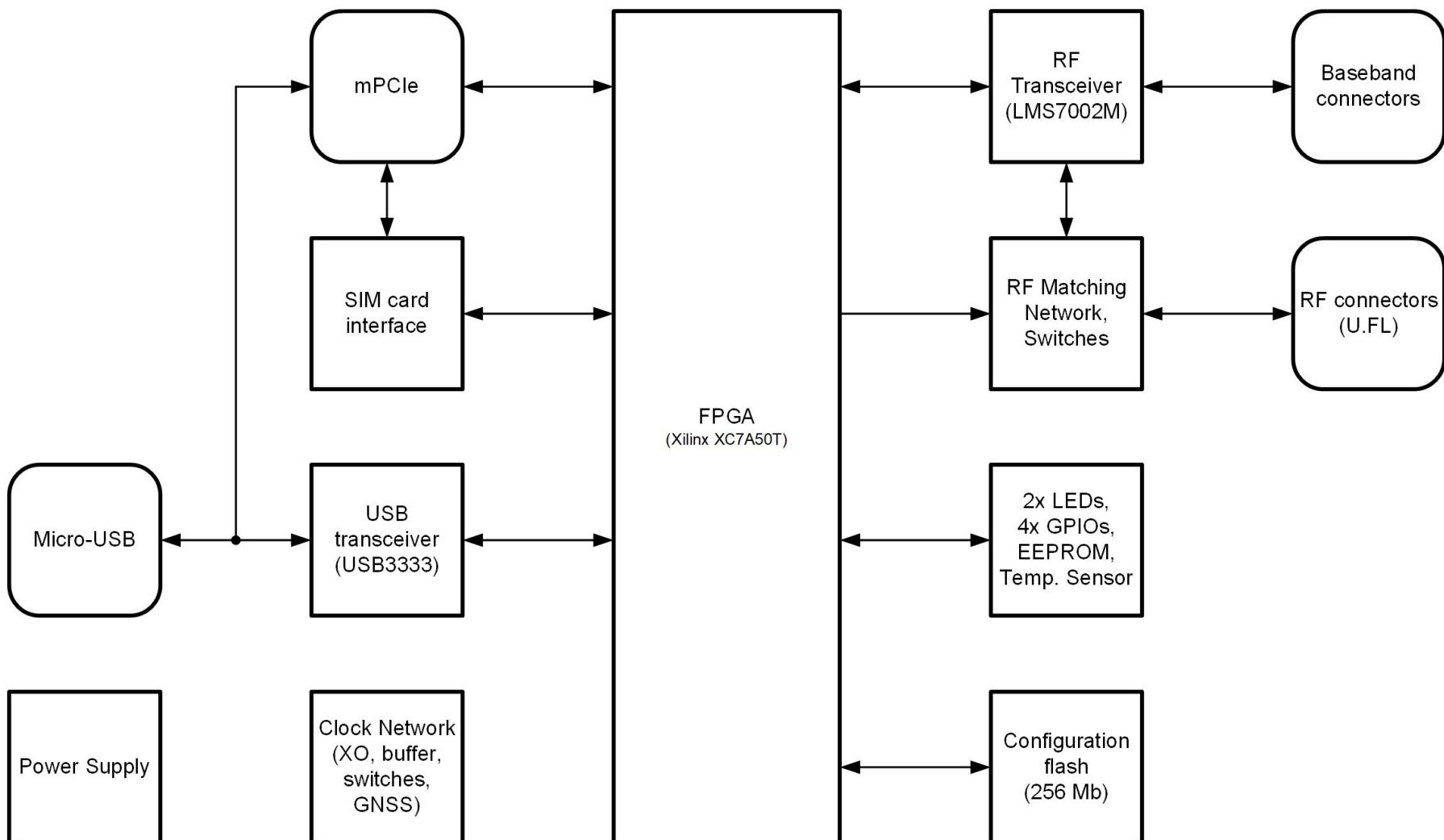


Block diagram



Project name: **LimeSDR-XTRX_Iv3.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.3**

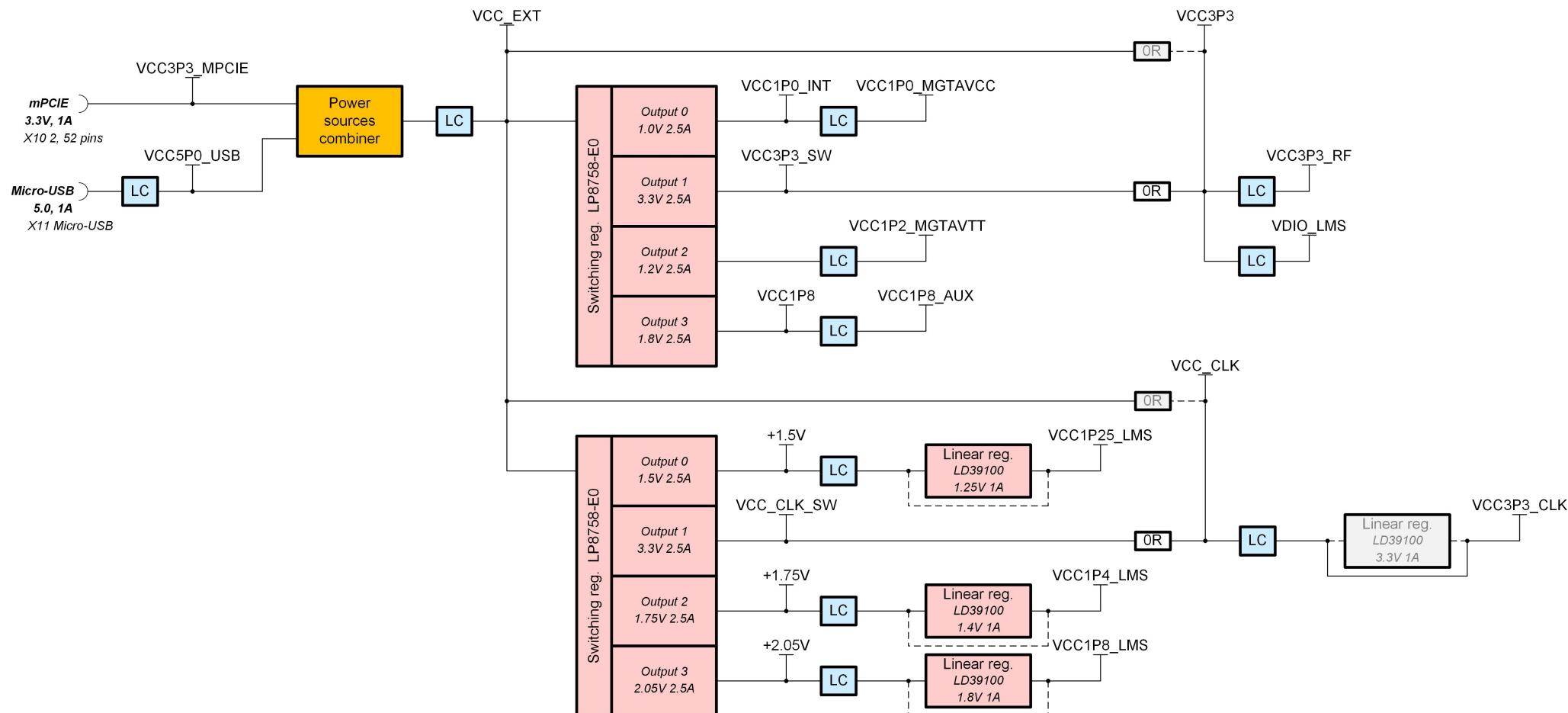
Date: **2025-03-21** Time: **12:46:51** Sheet **1** of **11**

File: **01_Block_Diagram.SchDoc**

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Surrey
United Kingdom



Power diagram



Project name: **LimeSDR-XTRX_Inv3.PnjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.3**

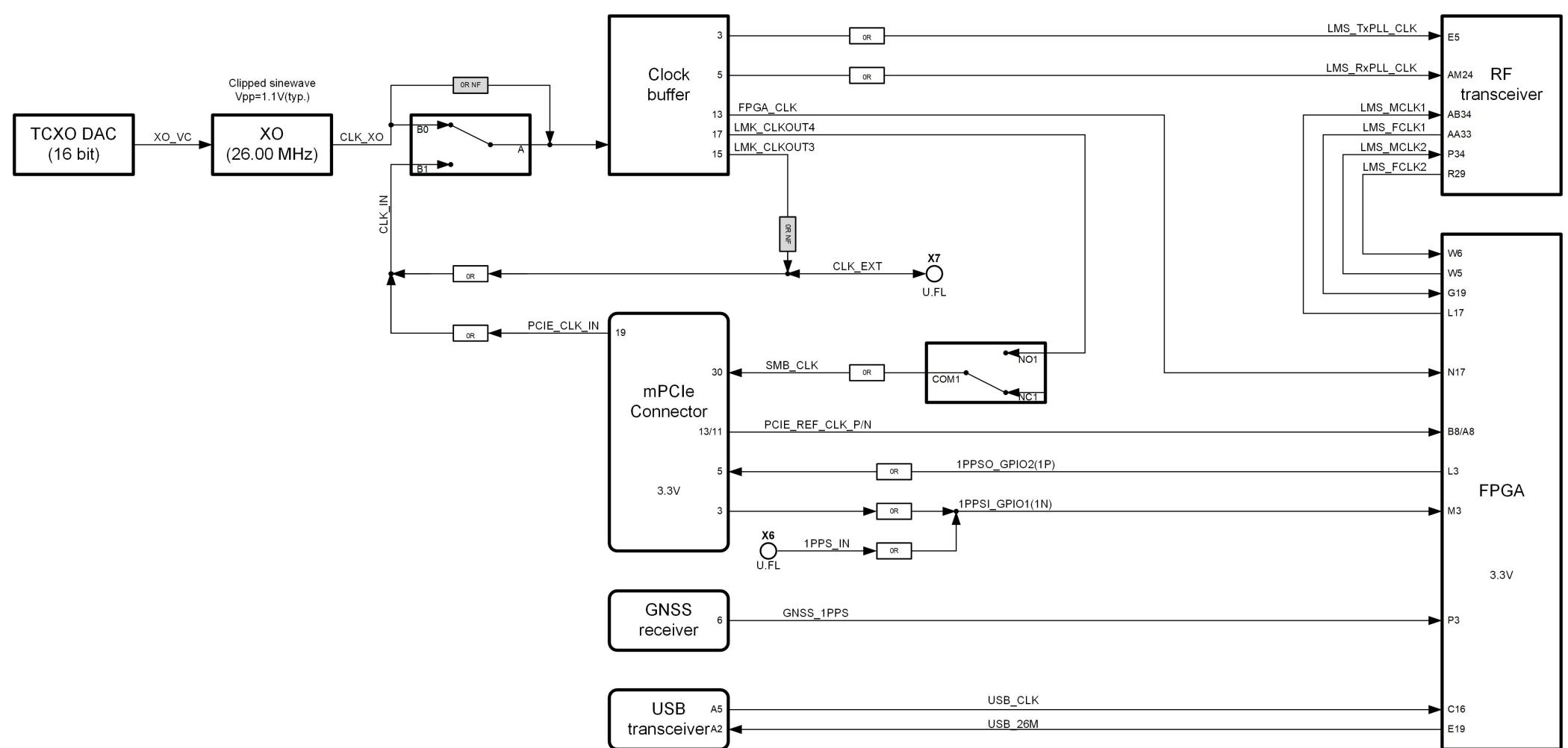
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File: **02_Power_Diagram.SchDoc**

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Clock diagram



Project name: *LimeSDR-XTRX_Iv3.PrjPcb*

Title: *Clock diagram*

Size: *A4* Revision: *v1.3*

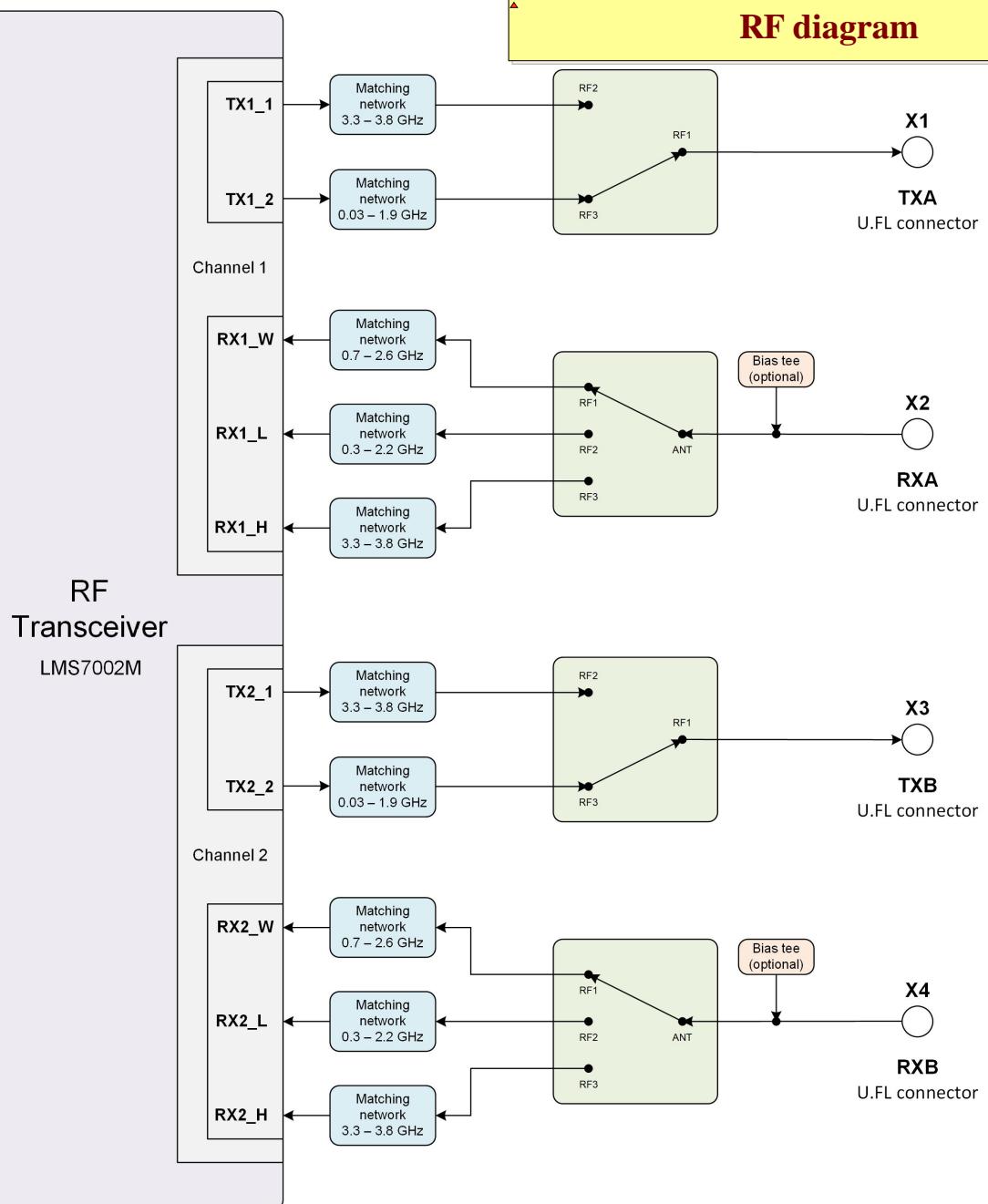
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File: *03_Clock_Diagram.SchDoc*

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RF diagram



Project name: **LimeSDR-XTRX_Iv3.PrjPcb**

Title: **RF diagram**

Size: **A4** Revision: **v1.3**

Date: **2025-03-21** Time: **12:46:56** Sheet **4** of **11**

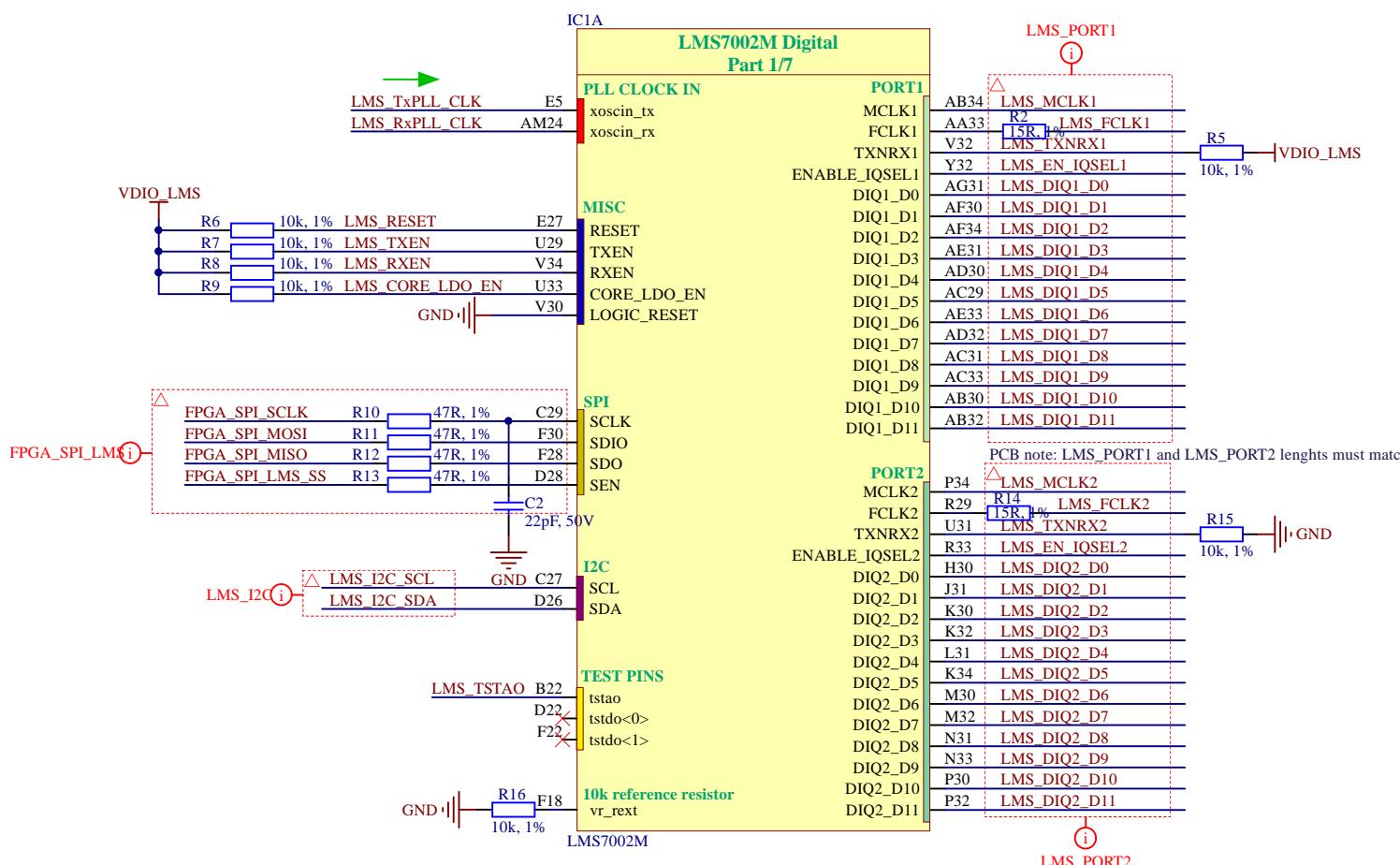
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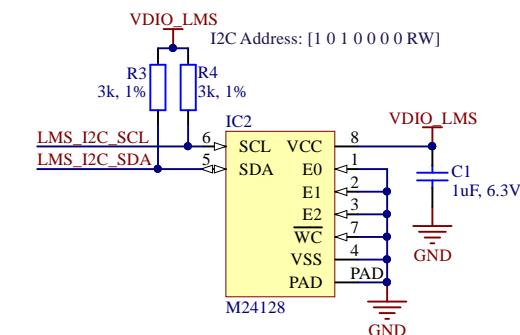


LMS7002M misc

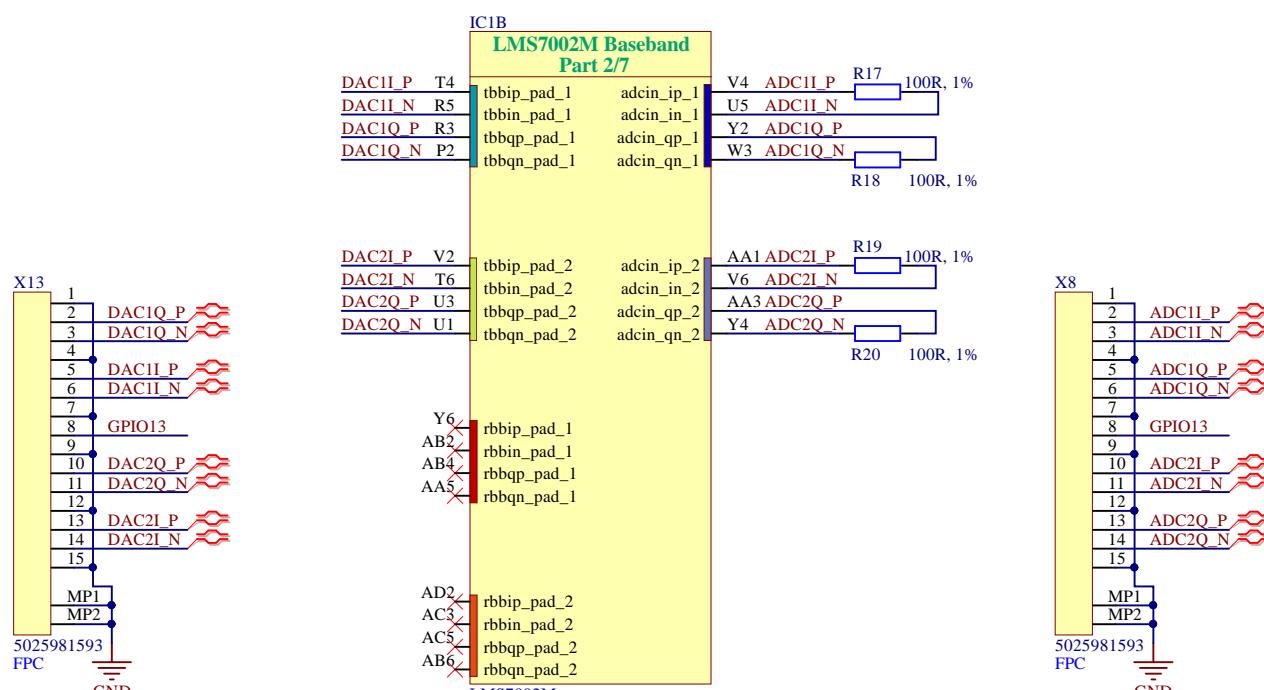
LMS7002M digital circuit



LMS EEPROM



Baseband external IO



Project name: LimeSDR-XTRX_Iv3.PrjPcb

Title: LMS7002M misc

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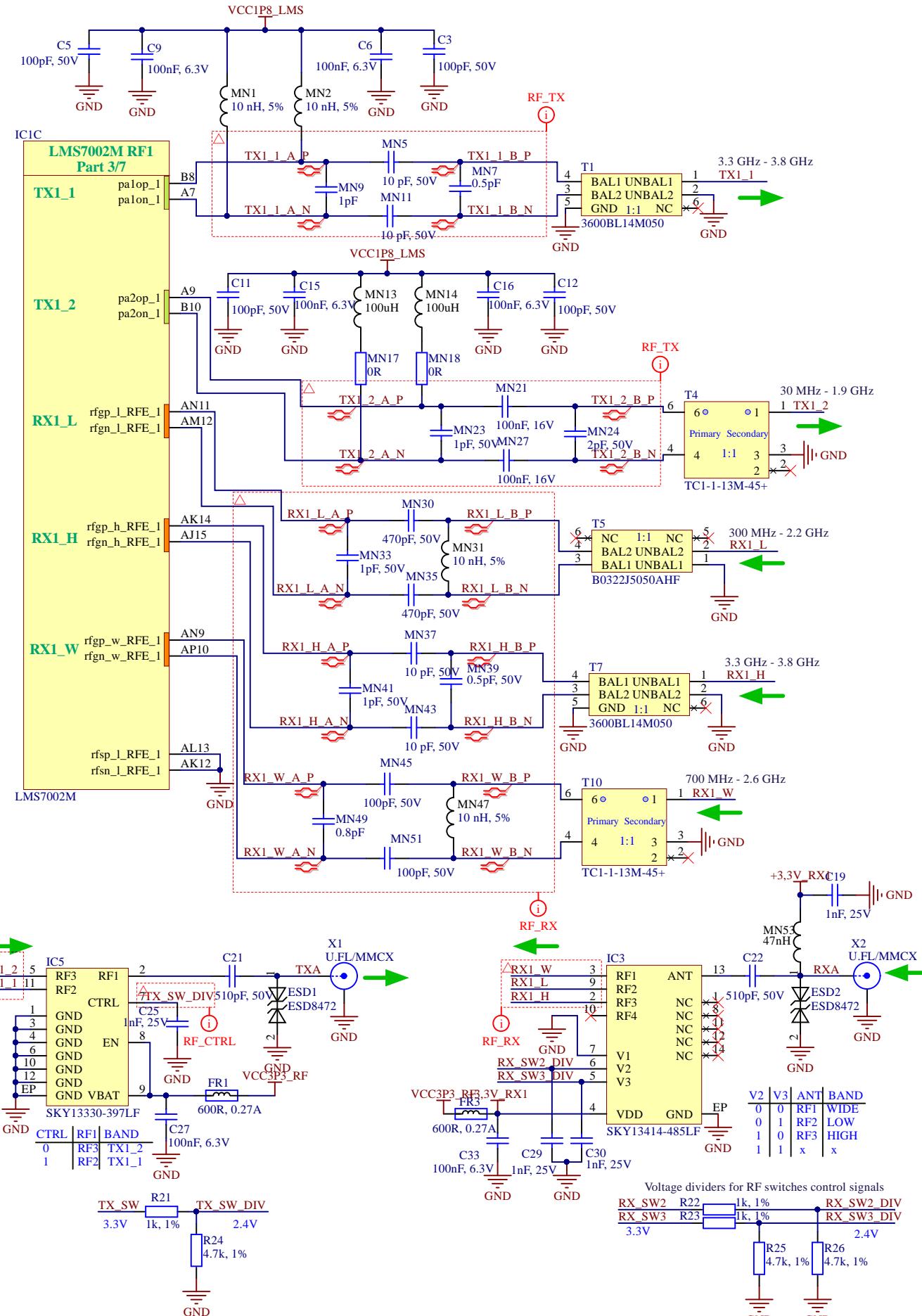
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Date: 2025-03-21 Time: 12:46:59 Sheet 5 of 11

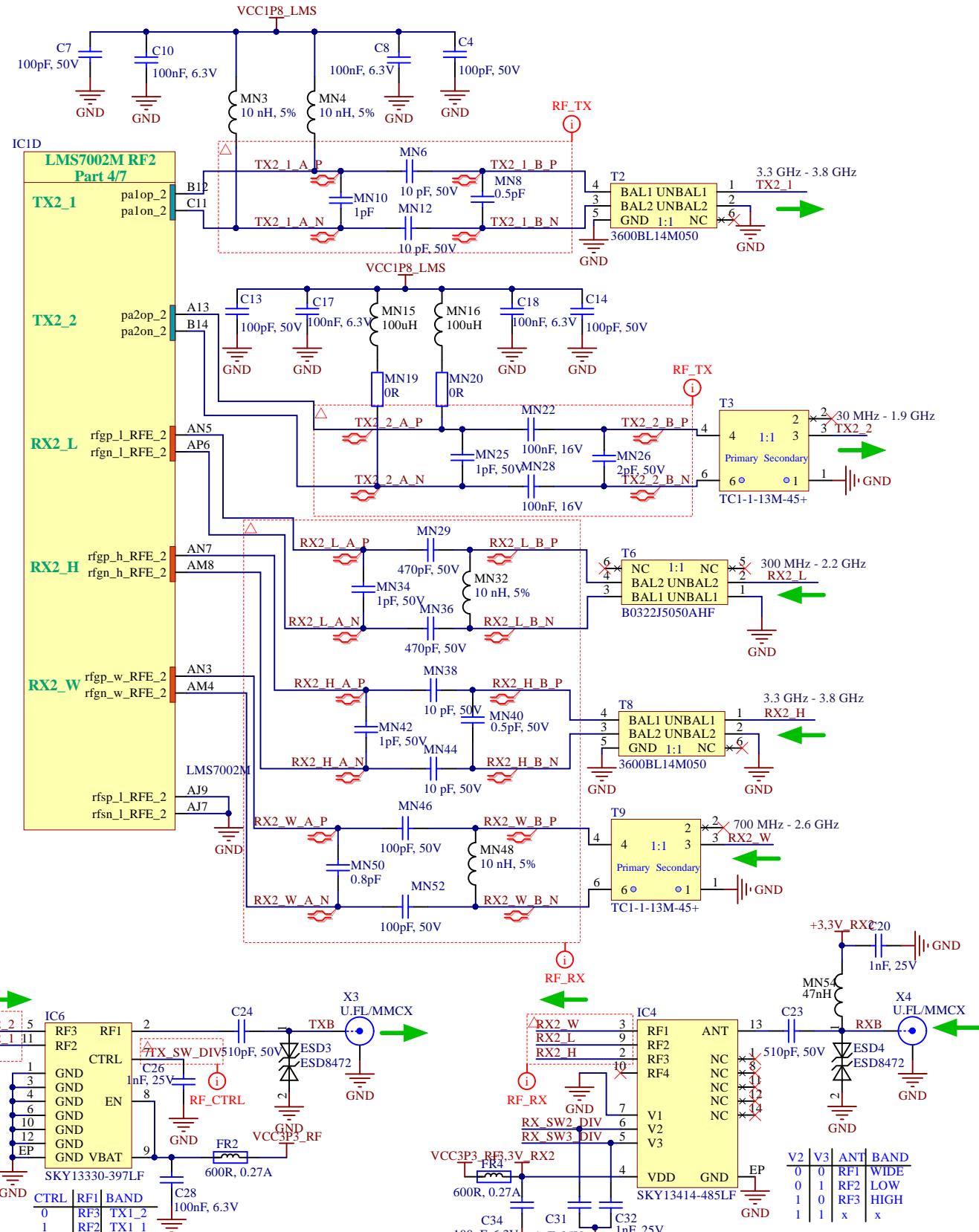
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LMS7002M RF circuits

LMS RF Channel 1

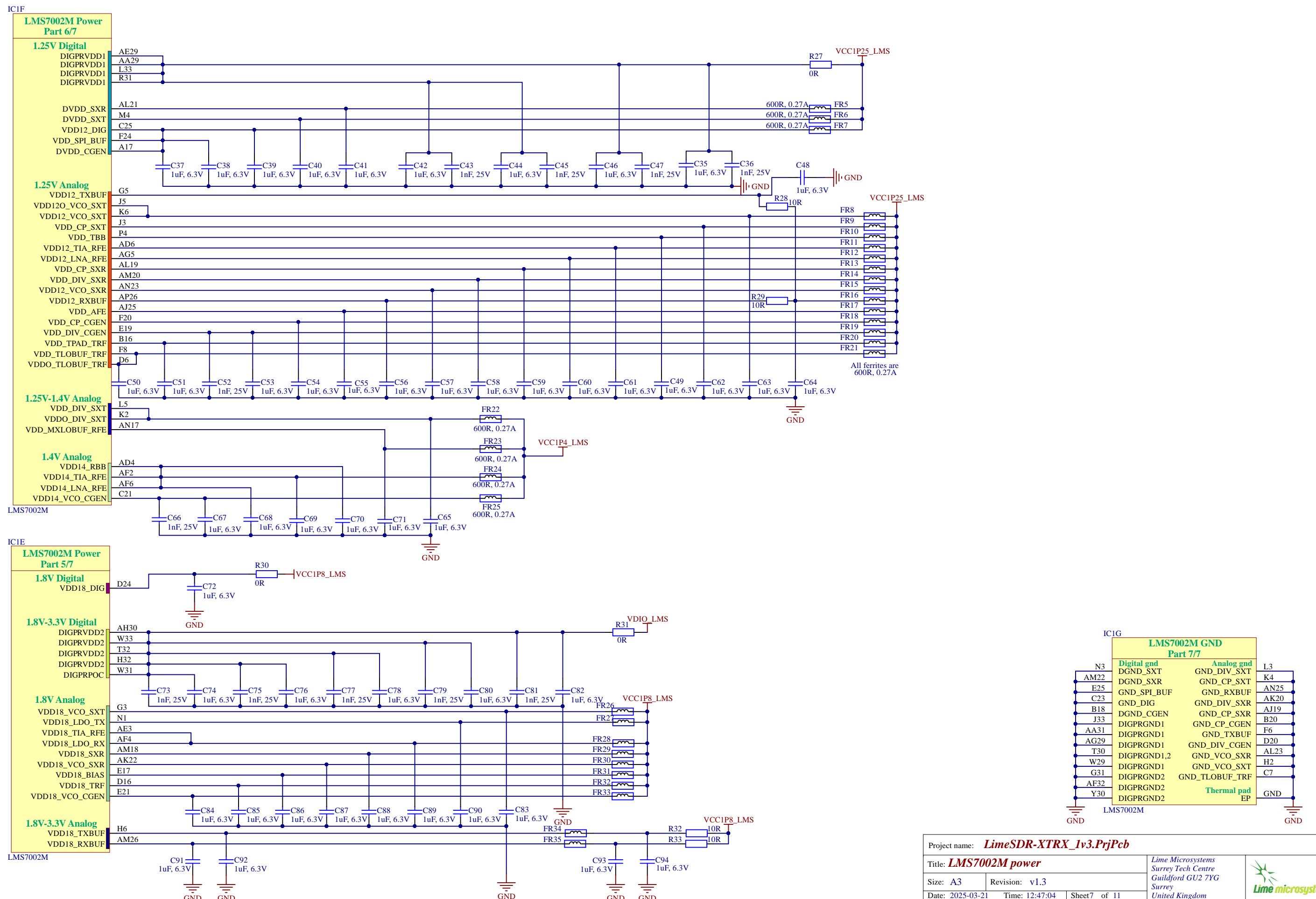


LMS RF Channel 2



| | |
|---|--|
| Project name: LimeSDR-XTRX_Inv3.PrjPcb | |
| Title: LMS7002M RF | <i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i> |
| Size: A3 | Revision: v1.3 |
| Date: 2025-03-21 | Time: 12:47:01 |
| File: 06_LMS7002M_RF.SchDoc |  Lime microsystems |

LMS7002M power supply circuit



Project name: LimeSDR-XTRX_Iv3.PrcPcb

Title: LMS7002M power

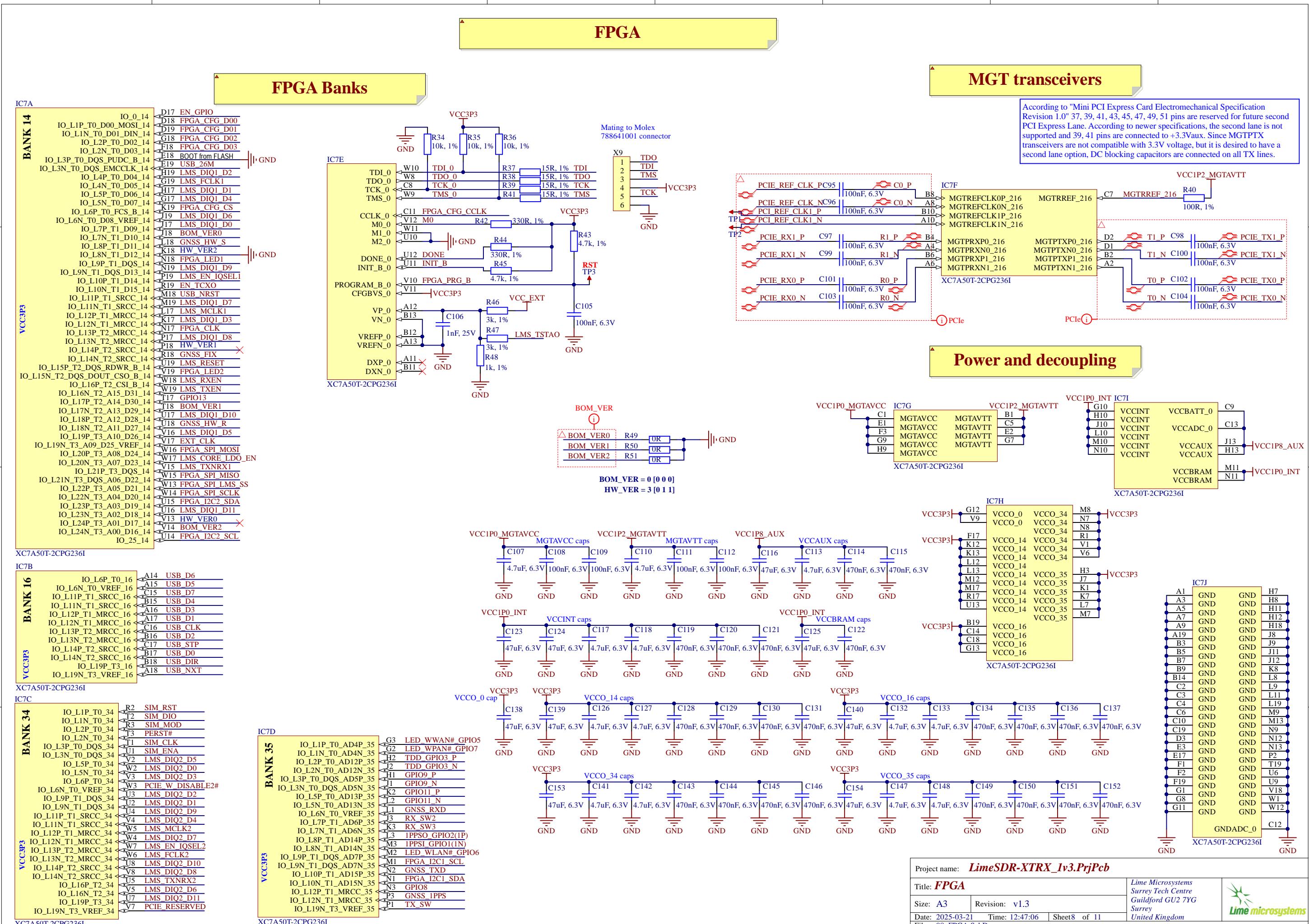
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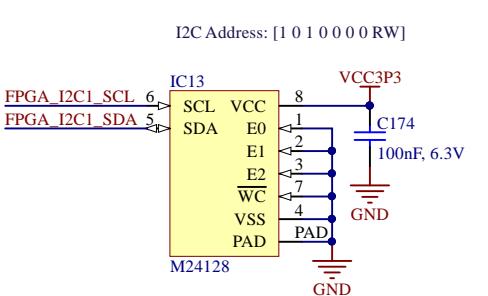
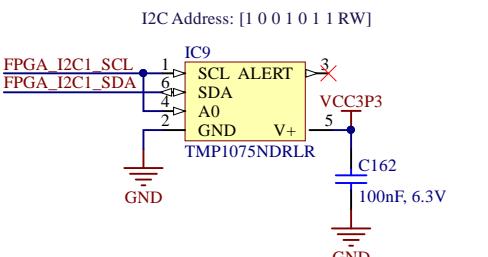
Date: 2025-03-21 Time: 12:47:04 Sheet 7 of 11

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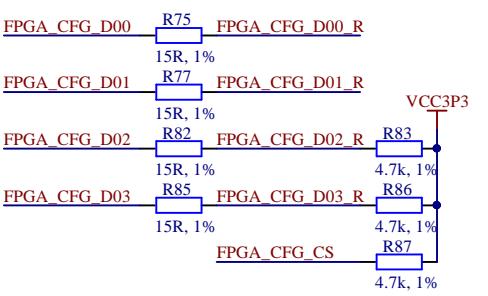
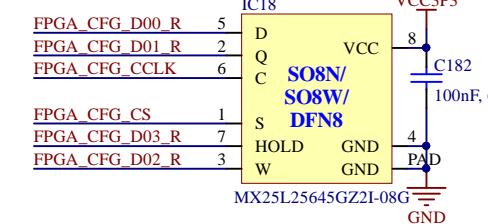
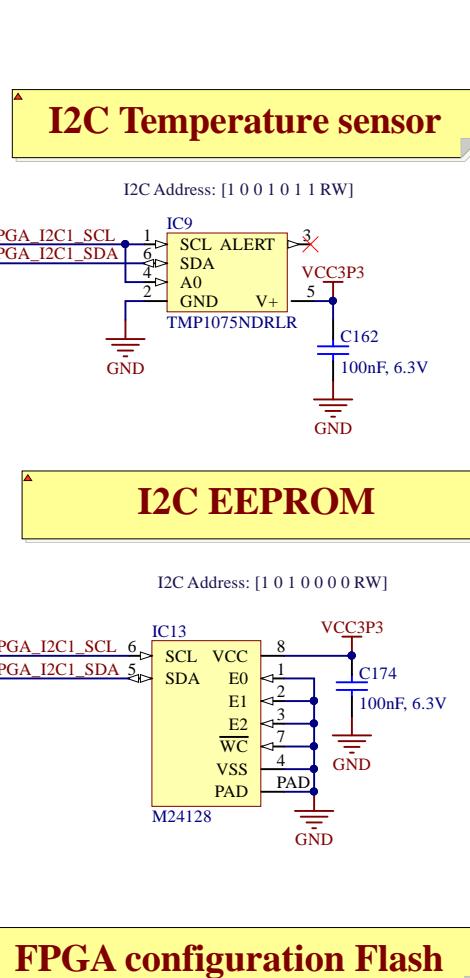
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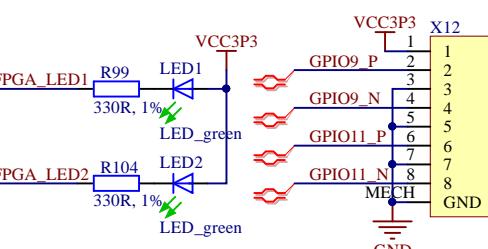




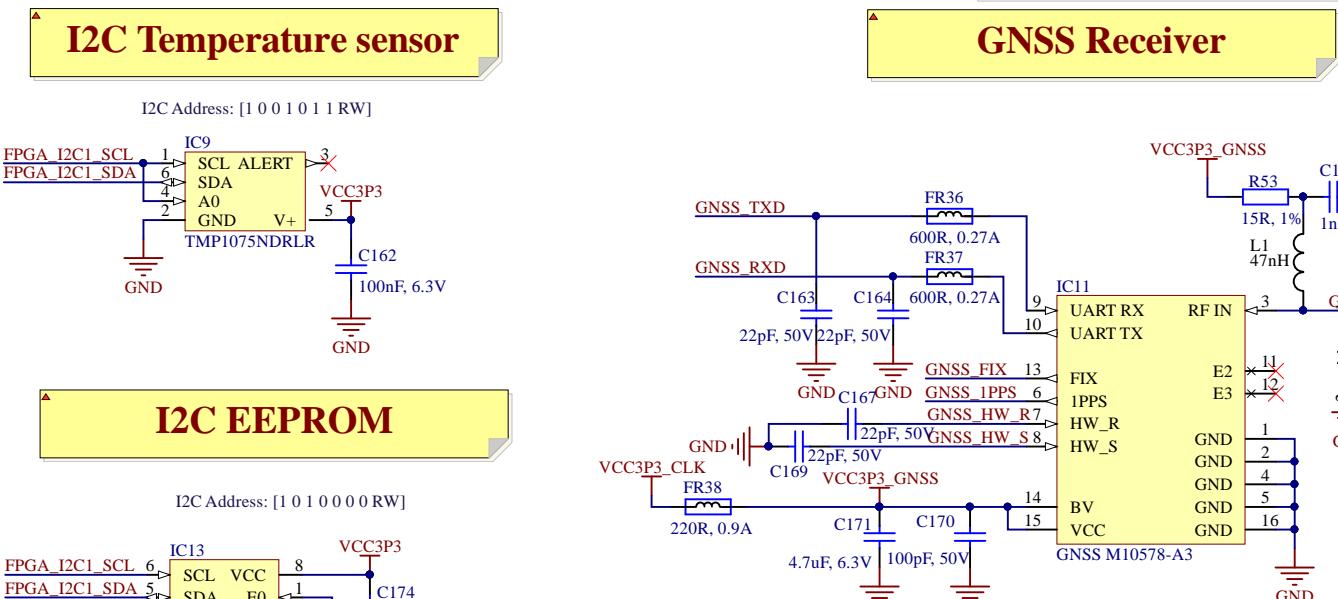
Misc



FPGA LEDs & GPIOs



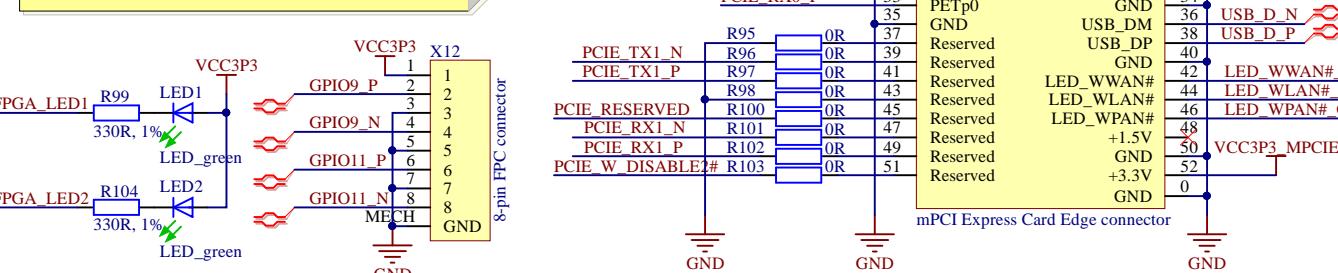
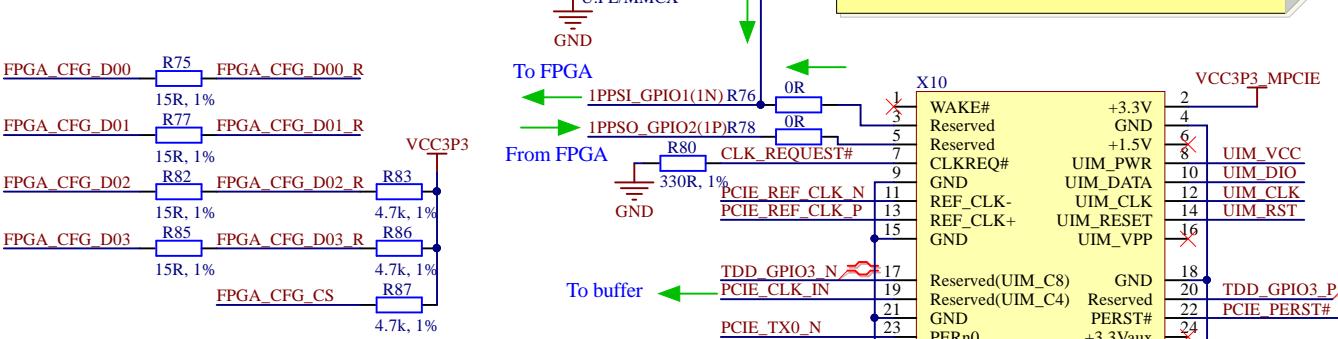
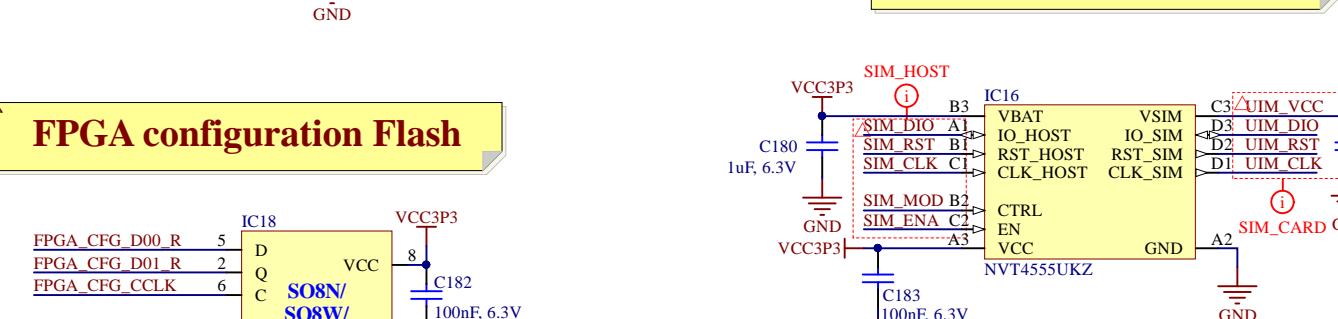
GNSS Receiver



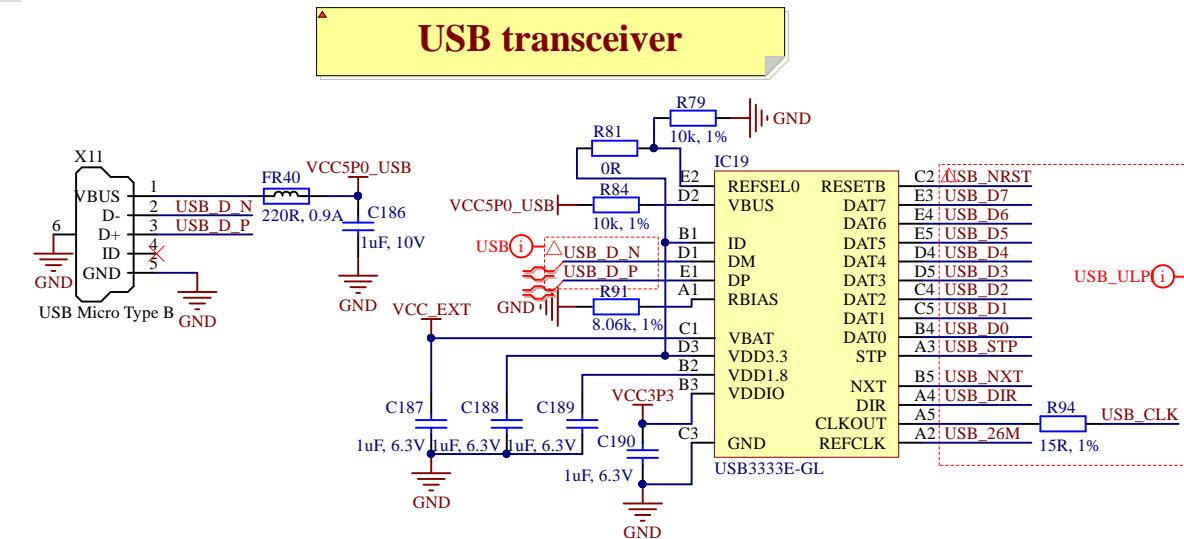
M24128

VSS
PAD
4
GND
PAD
GND

SIM card interface

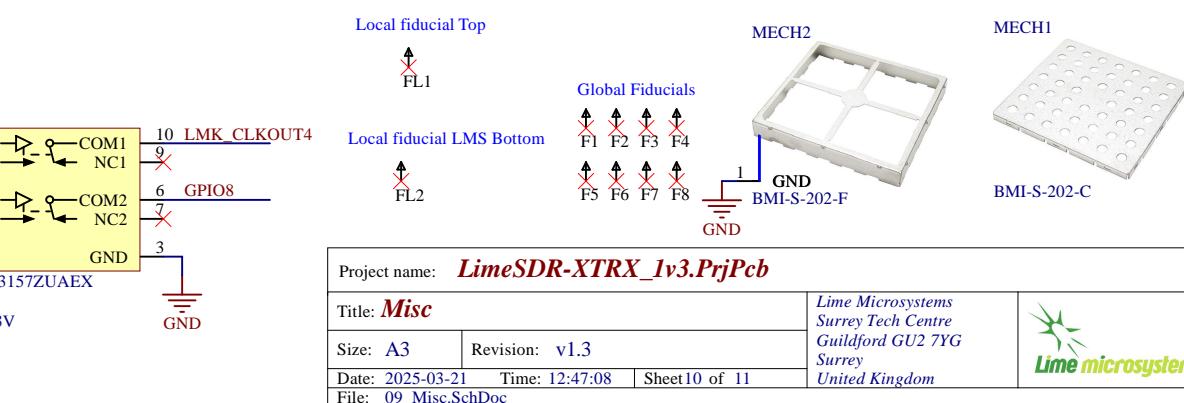


USB transceiver

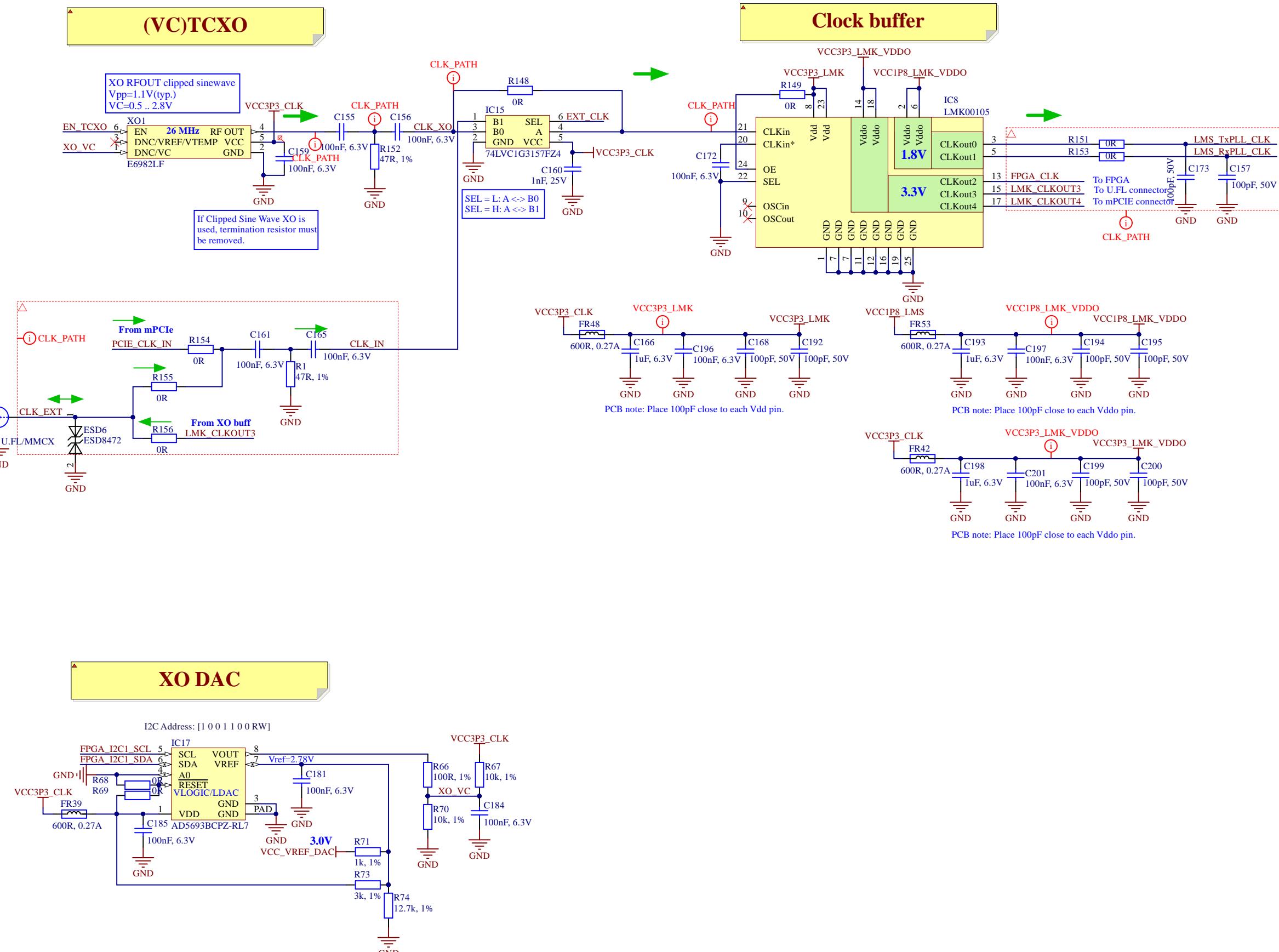


Detailed pinout diagram for the LMK CLKOUT4 module:

- FPCIE_1 (Top):**
 - Pin 35: PETp0
 - Pin 36: GND
 - Pin 37: Reserved
 - Pin 38: USB_D_N
 - Pin 39: USB_DM
 - Pin 40: USB_DP
 - Pin 41: GND
 - Pin 42: Reserved
 - Pin 43: LED_WIWA™_GPIO5
- FPCIE_2 (Bottom):**
 - Pin 1: EN_GPIO
 - Pin 2: SMB_CLK
 - Pin 3: IC20 (Chip)
 - Pin 4: IN1
 - Pin 5: COM1
 - Pin 6: GND
 - Pin 7: LMK_CLKOUT4
 - Pin 8: GND
 - Pin 9: Local fiducial LMS Bottom
- Global Fiducials:** F1, F2, F3, F4



Clock



Project name: LimeSDR-XTRX_Iv3.PrjPcb

Title: Clock

Size: A3 Revision: v1.3

Date: 2025-03-21 Time: 12:47:10 Sheet 10 of 11

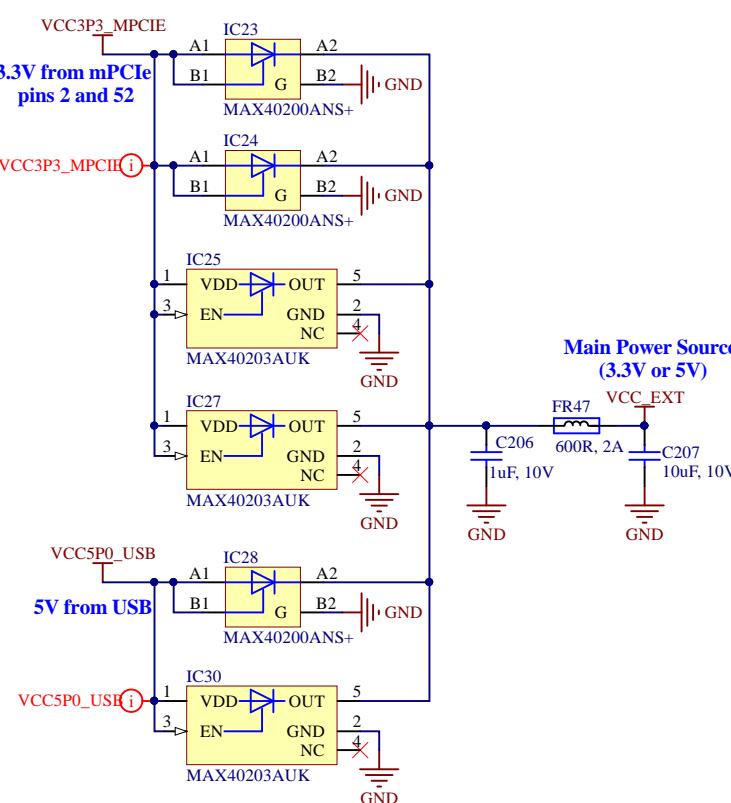
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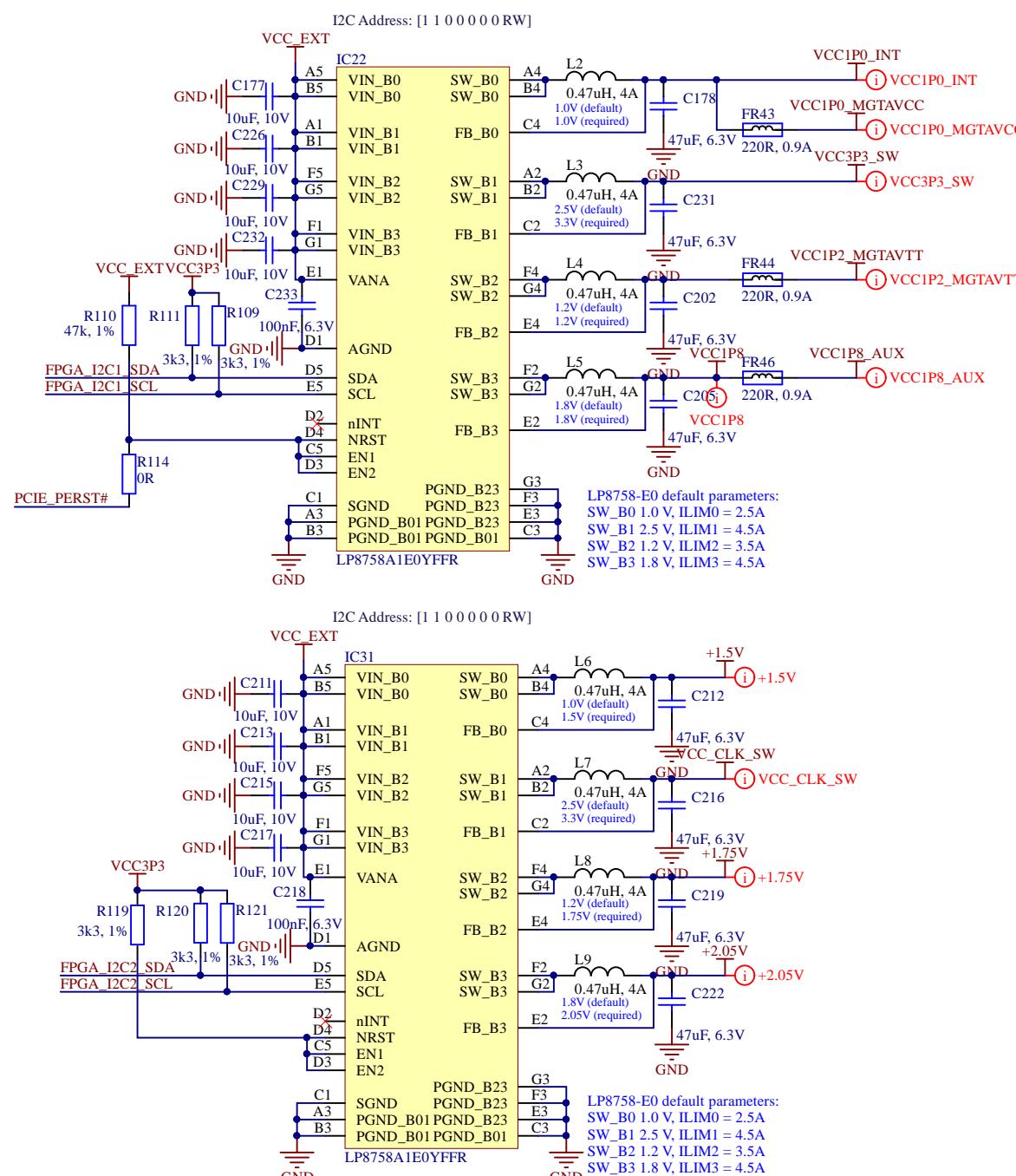


Board power circuits

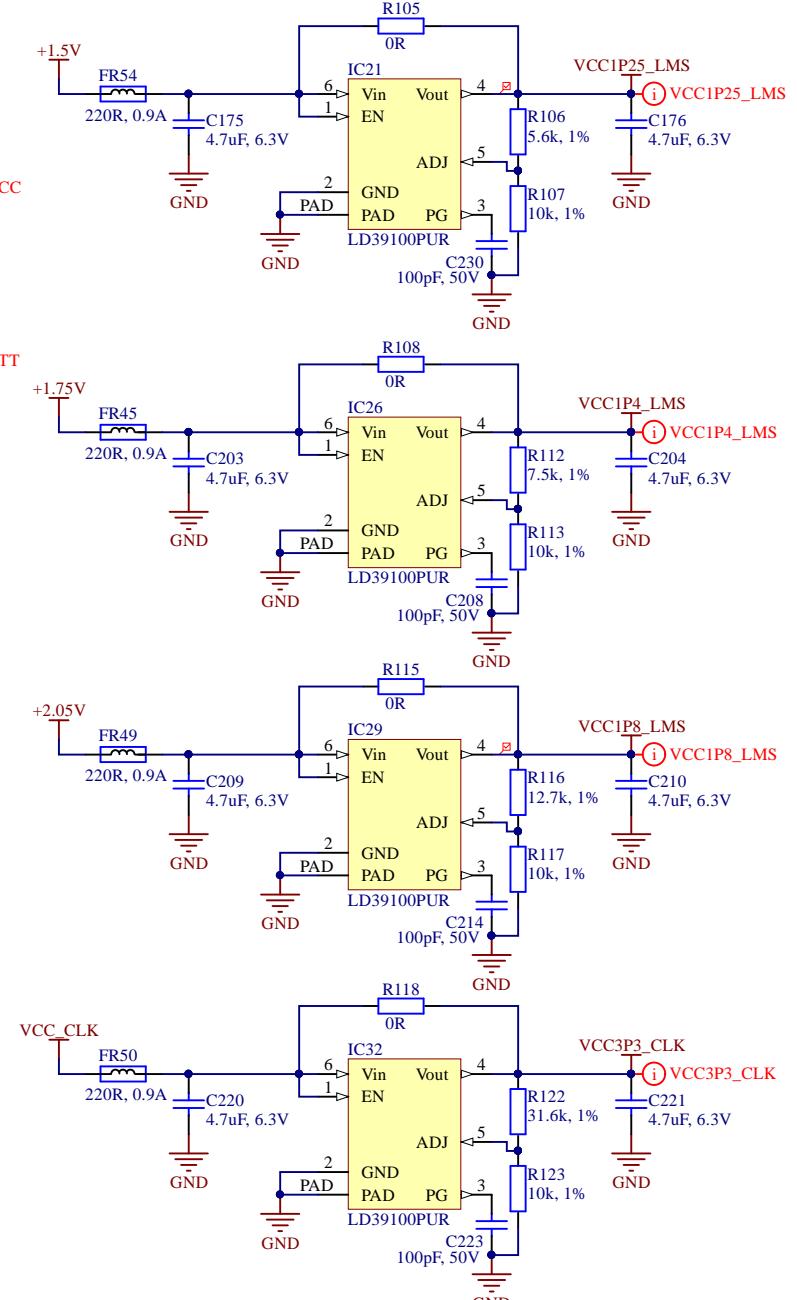
Power input



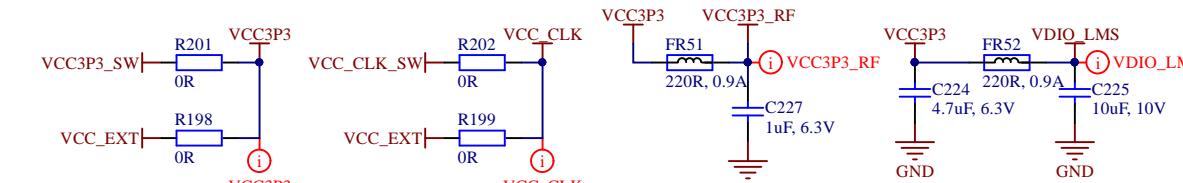
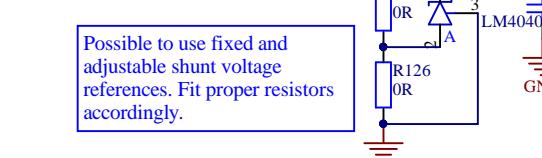
Switching regulators



Linear regulators



Voltage reference



Filters, voltage selection

| | |
|---------------------------------------|--|
| Project name: LimeSDR-XTRX_Iv3.PrjPcb | |
| Title: Power | Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom |
| Size: A3 | Revision: v1.3 |
| Date: 2025-03-21 | Time: 12:47:12 |
| File: 11_Power.SchDoc | Sheet 11 of 11 |

