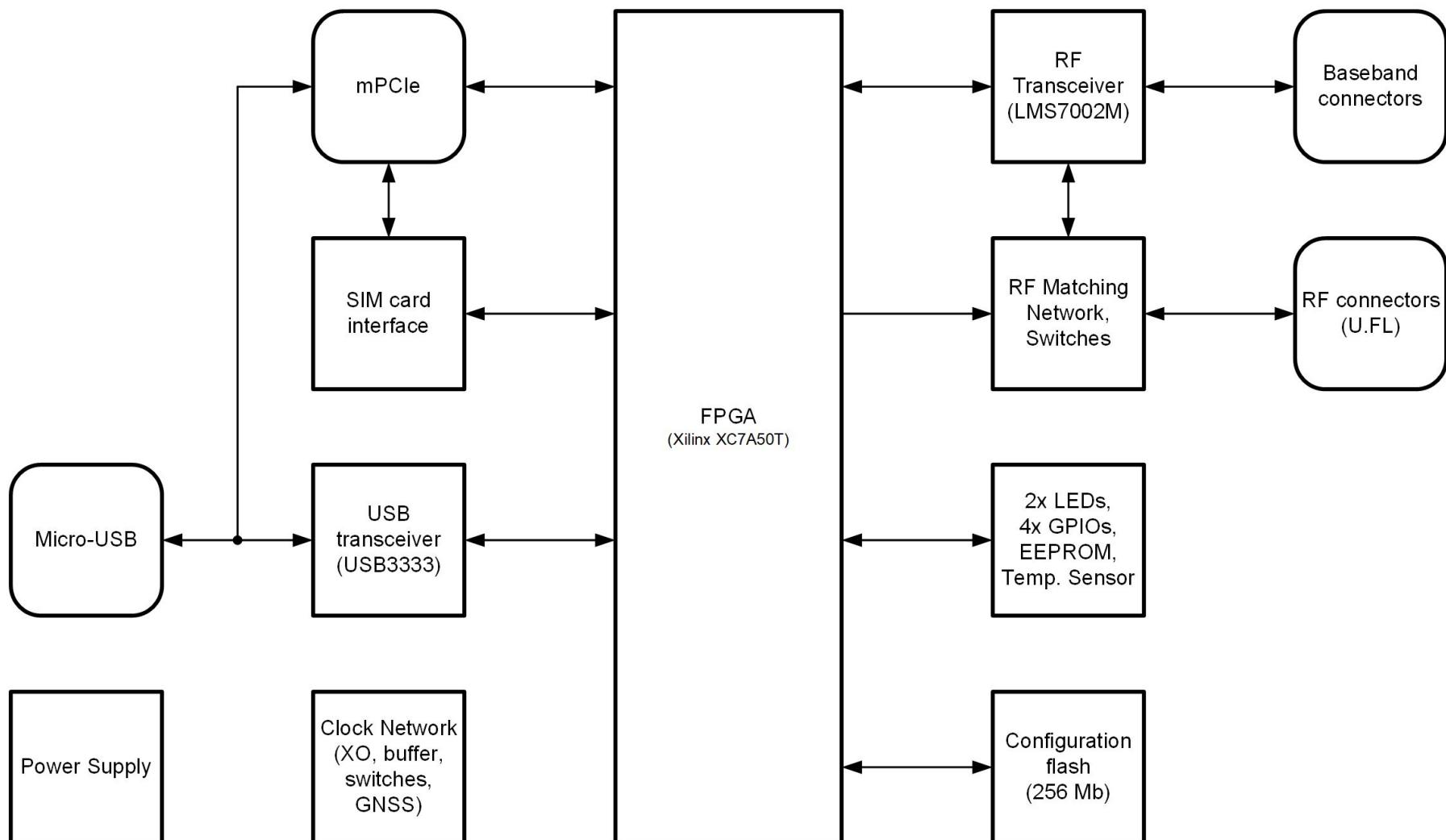


Block diagram



Project name: **LimeSDR-XTRX_Iv3.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.3**

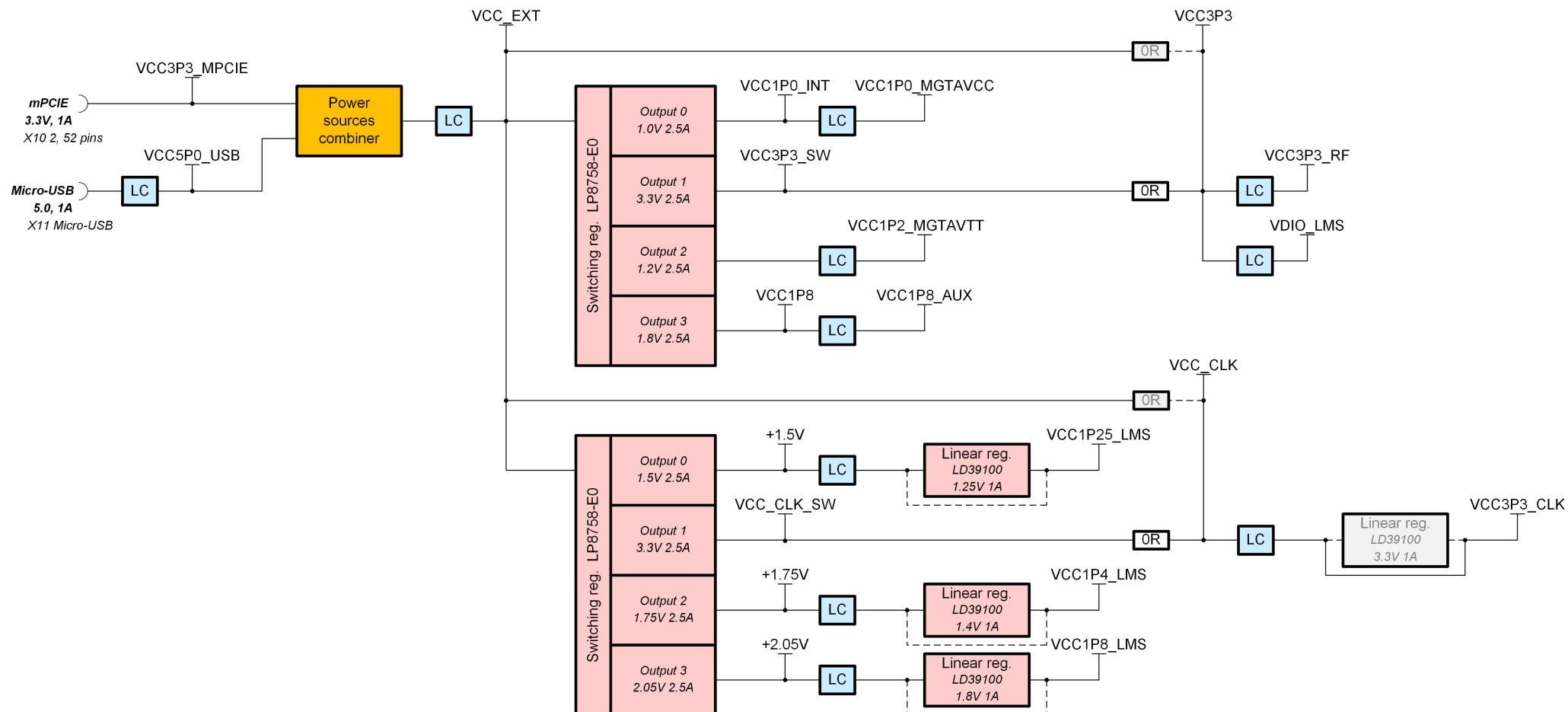
Date: **2024-12-06** Time: **14:32:05** Sheet **1** of **11**

File: **01_Block_Diagram.SchDoc**

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Surrey
United Kingdom



Power diagram



Project name: **LimeSDR-XTRX_Inv3.PrjPcb**

Title: **Power diagram**

Size: **A4** Revision: **v1.3**

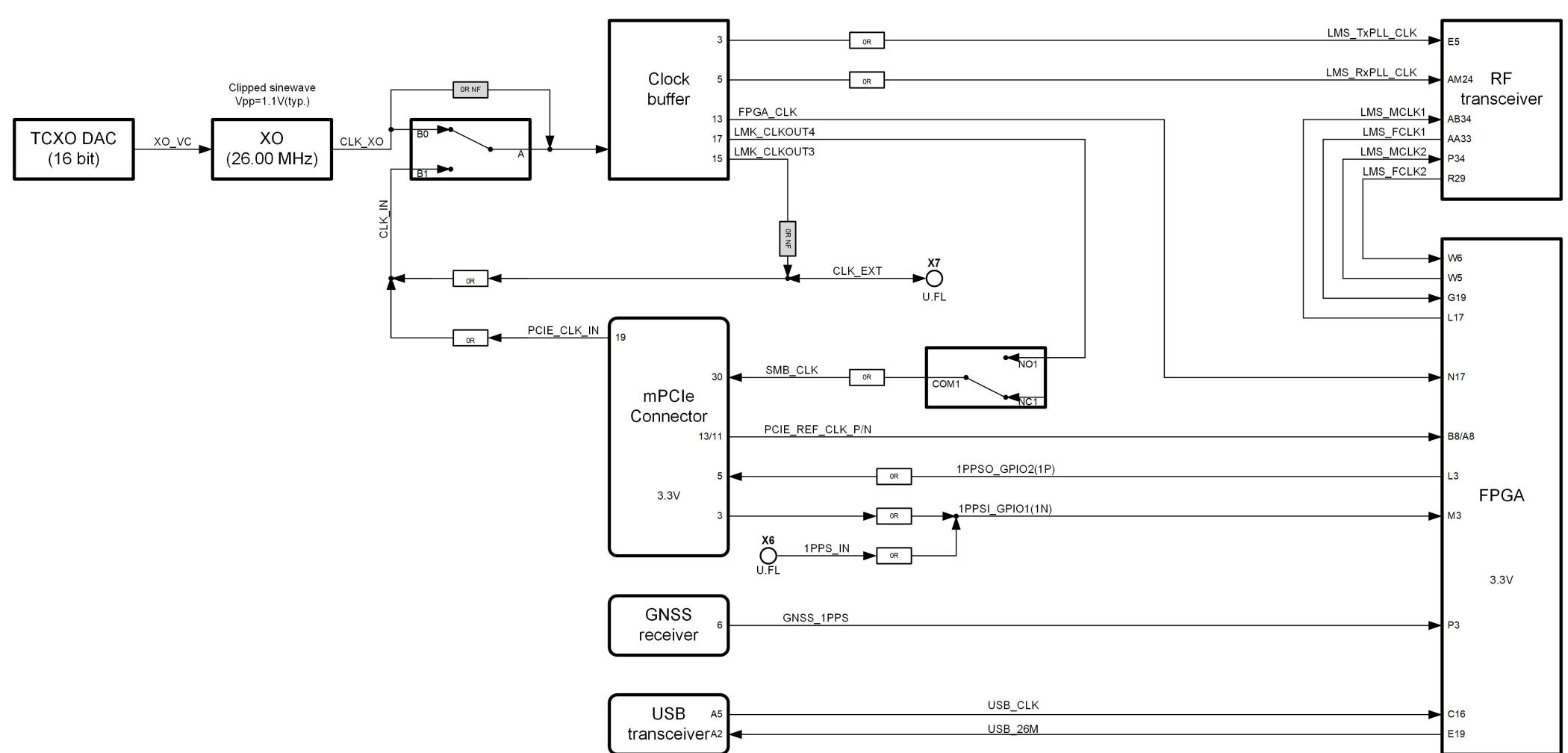
Date: **2024-12-06** Time: **14:32:06** Sheet **2** of **11**

File: **02_Power_Diagram.SchDoc**

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Surrey
United Kingdom



Clock diagram



Project name: *LimeSDR-XTRX_Iv3.PrjPcb*

Title: *Clock diagram*

Size: *A4* Revision: *v1.3*

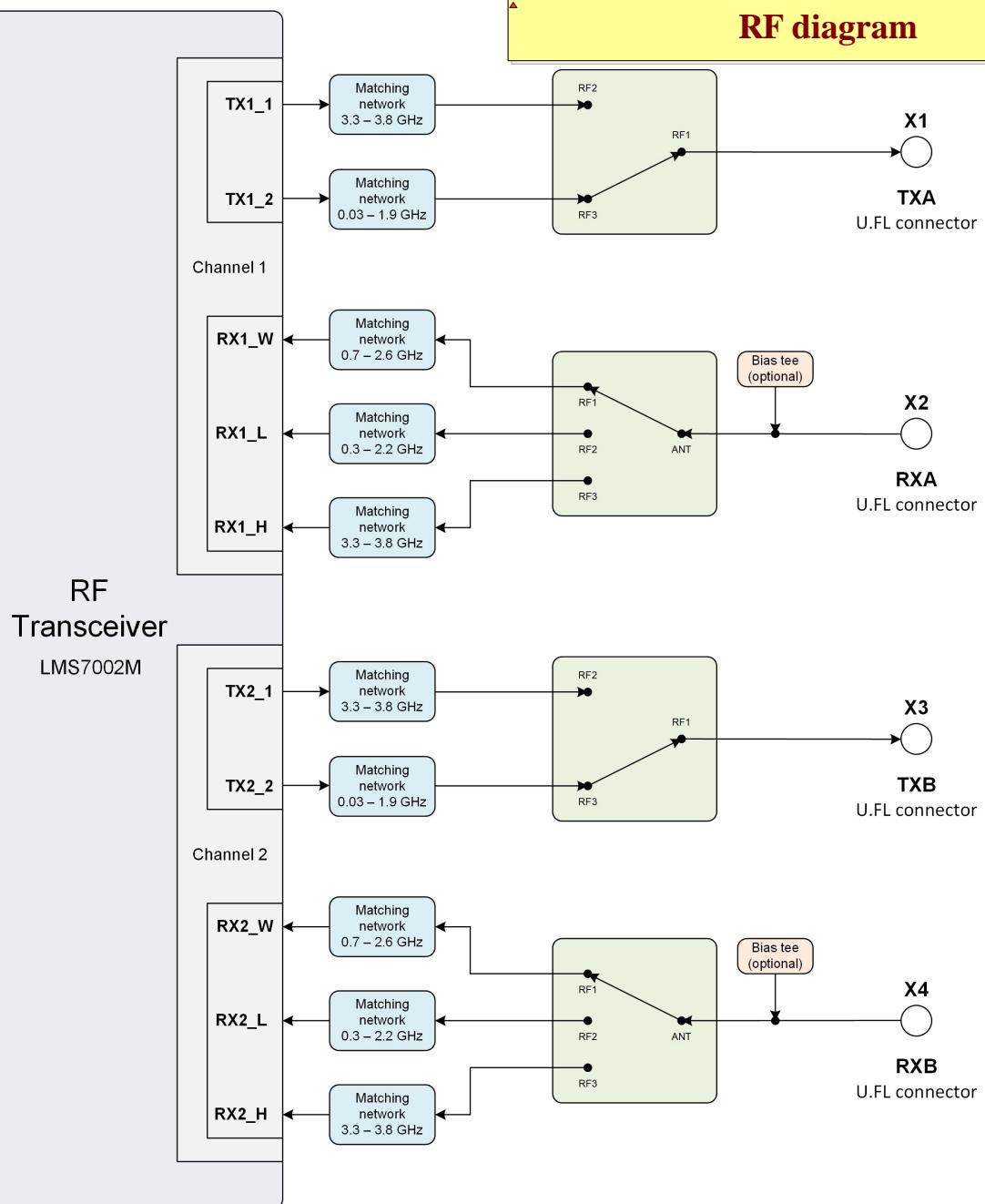
Date: *2024-12-06* Time: *14:32:07* Sheet *3* of *11*

File: *03_Clock_Diagram.SchDoc*

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RF diagram



Project name: **LimeSDR-XTRX_Iv3.PrjPcb**

Title: **RF diagram**

Size: **A4** Revision: **v1.3**

Date: **2024-12-06** Time: **14:32:09** Sheet **4** of **11**

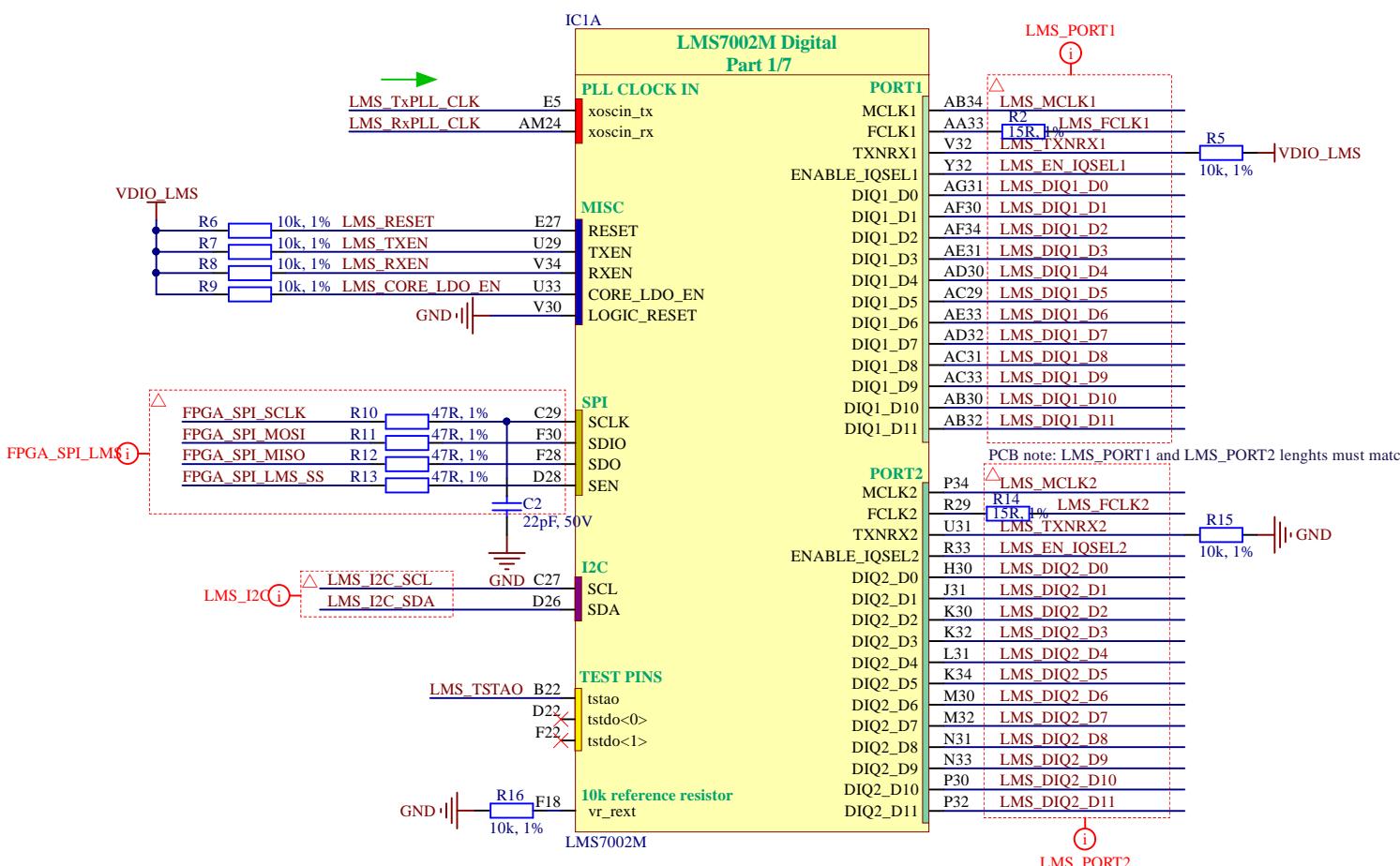
File: **04_RF_Diagram.SchDoc**

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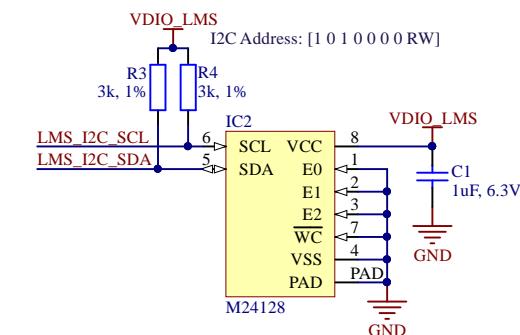


LMS7002M misc

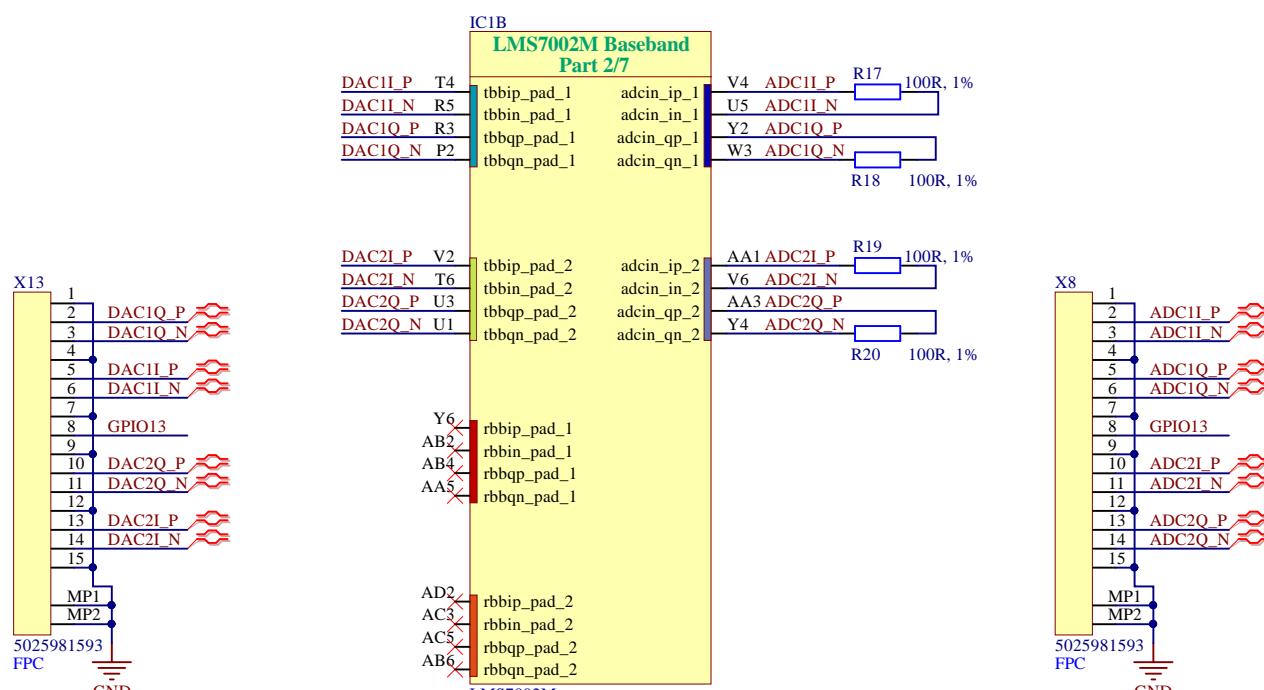
LMS7002M digital circuit



LMS EEPROM



Baseband external IO



Project name: LimeSDR-XTRX_Iv3.PrjPcb

Title: LMS7002M misc

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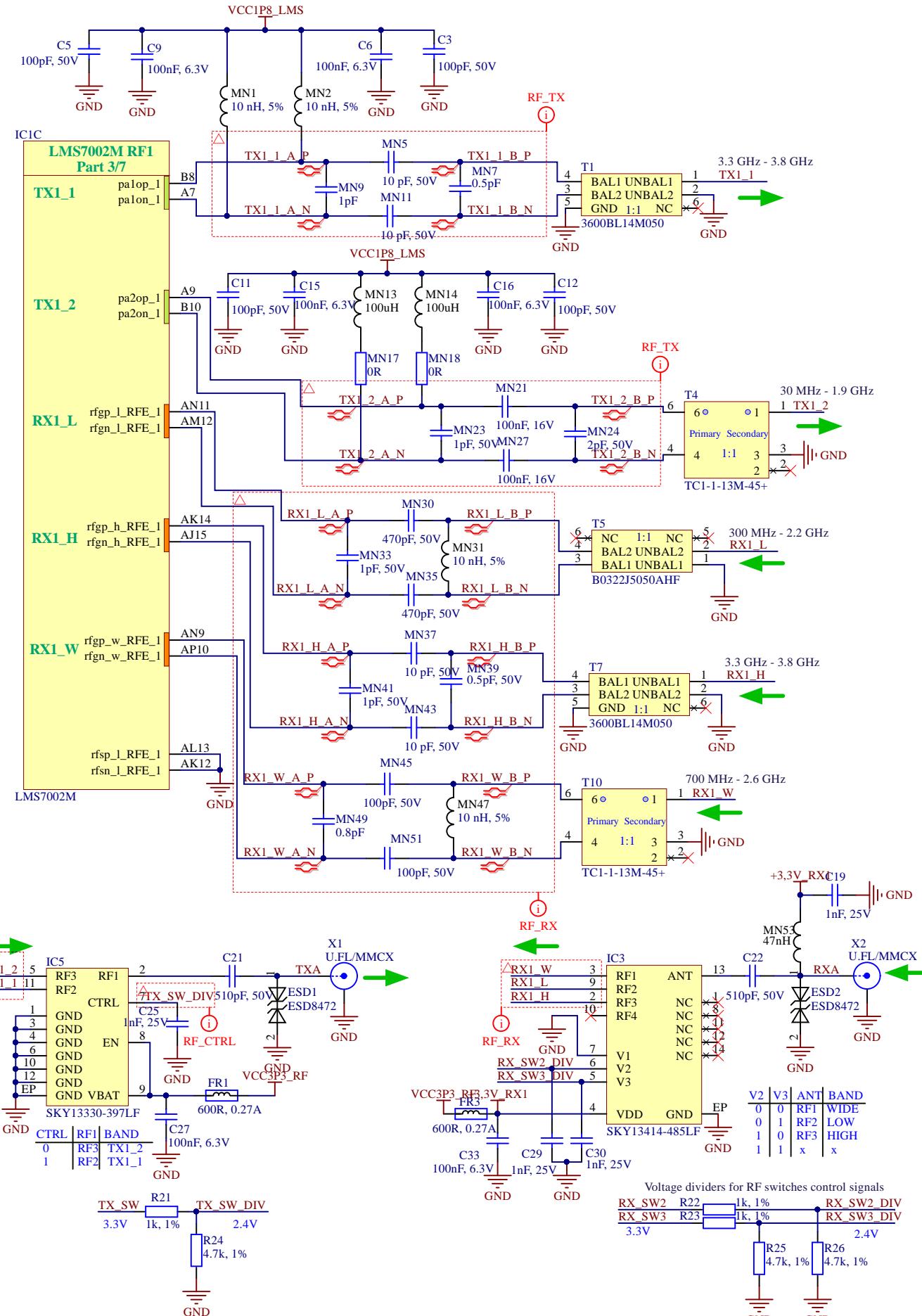
Size: A3 Revision: v1.3

Date: 2024-12-06 Time: 14:32:10 Sheet 5 of 11

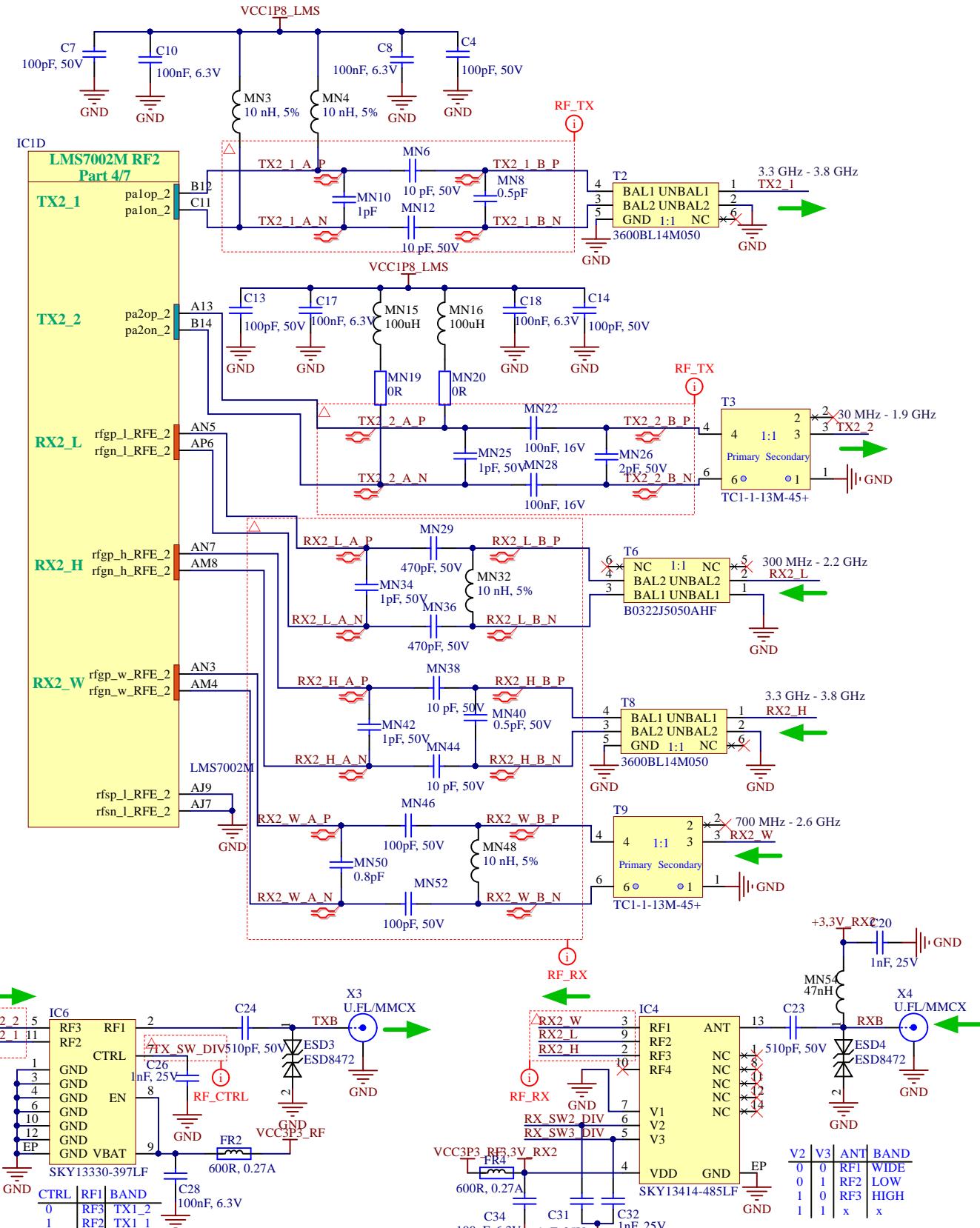
File: 05_LMS7002M_Misc.SchDoc

LMS7002M RF circuits

LMS RF Channel 1

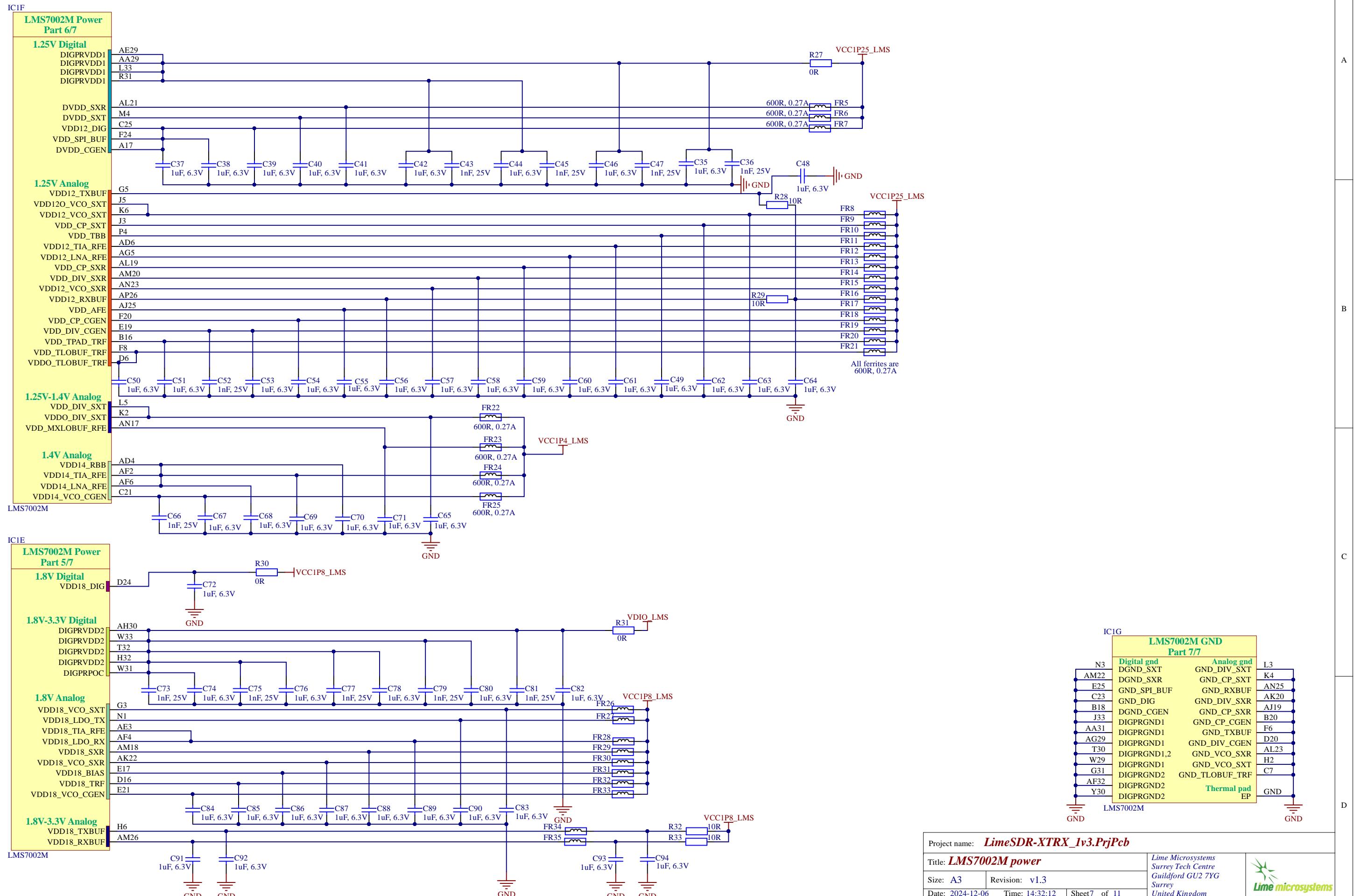


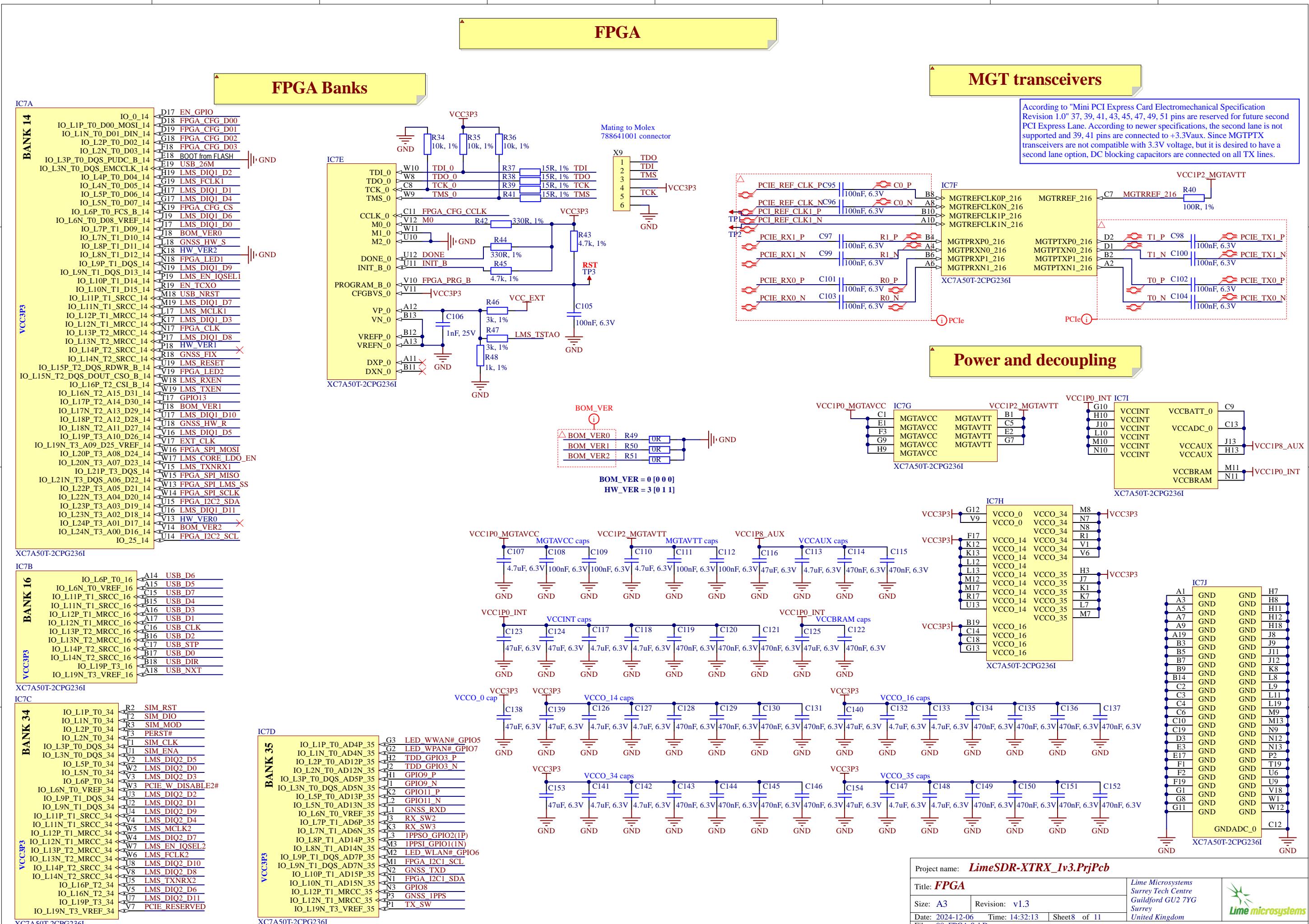
LMS RF Channel 2

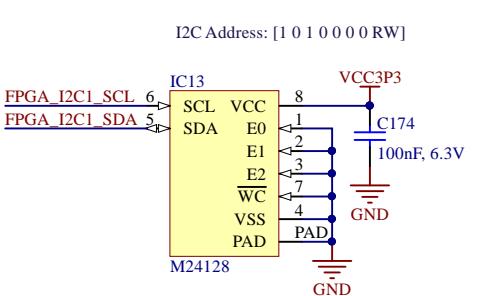
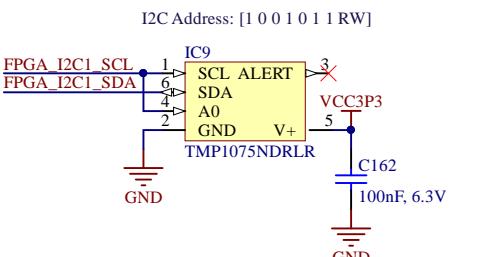


Project name: LimeSDR-XTRX_Inv3.PrjPcb	
Title: LMS7002M RF	<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>
Size: A3	Revision: v1.3
Date: 2024-12-06	Time: 14:32:11
File: 06_LMS7002M_RF.SchDoc	 Lime microsystems

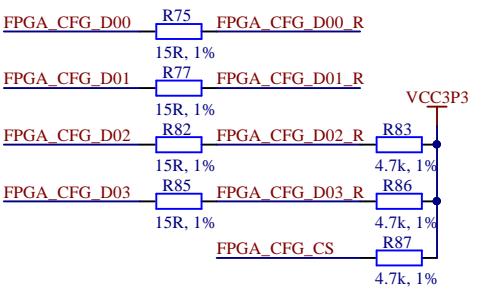
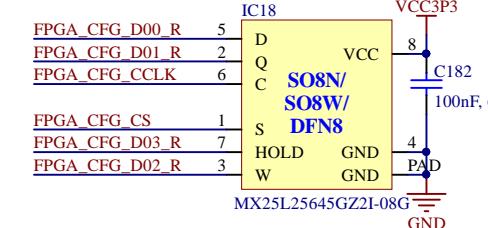
LMS7002M power supply circuit



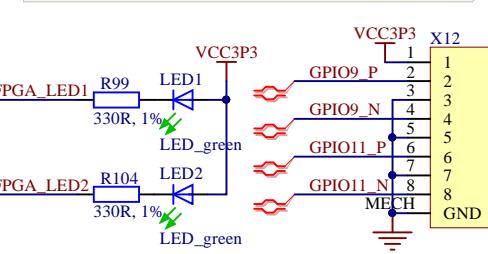




FPGA configuration Flash

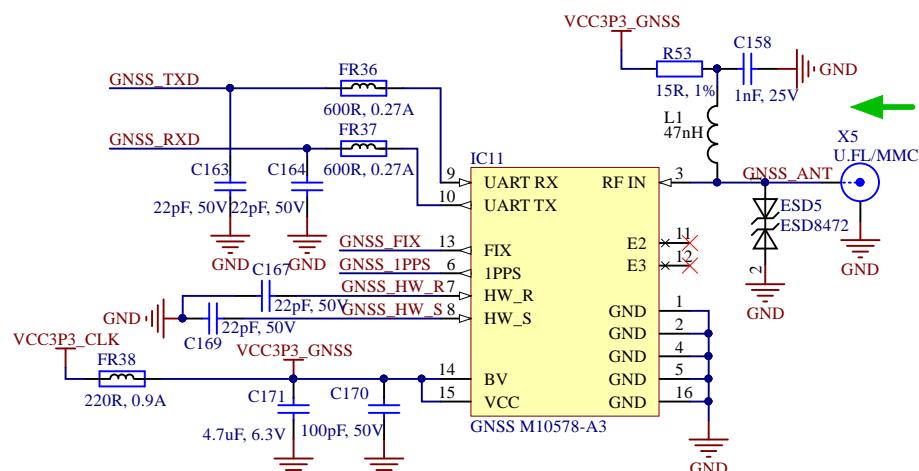


FPGA LEDs & GPIOs

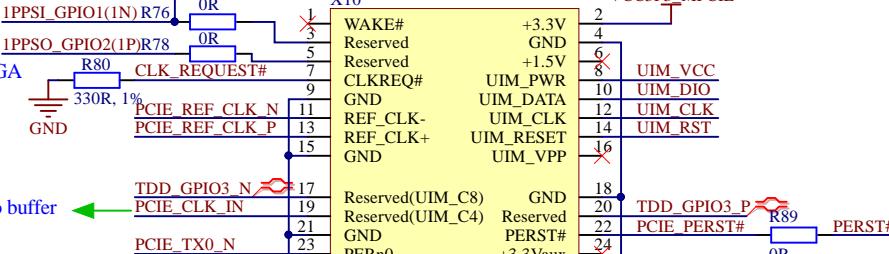


The M24128 SIM card interface diagram shows the following connections:

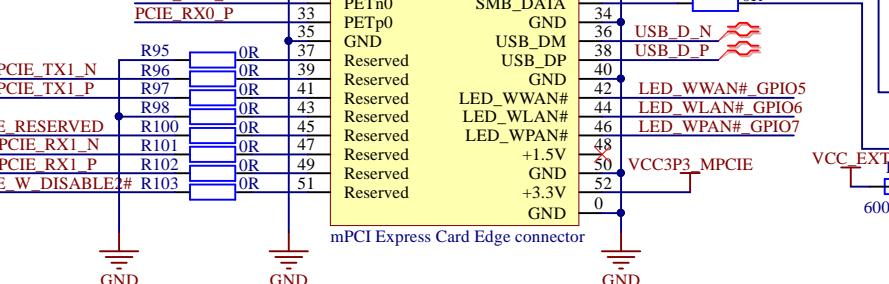
- VSS**: Ground connection.
- PAD**: Pin connection.
- GND**: Ground connection.
- M24128**: The integrated circuit component.



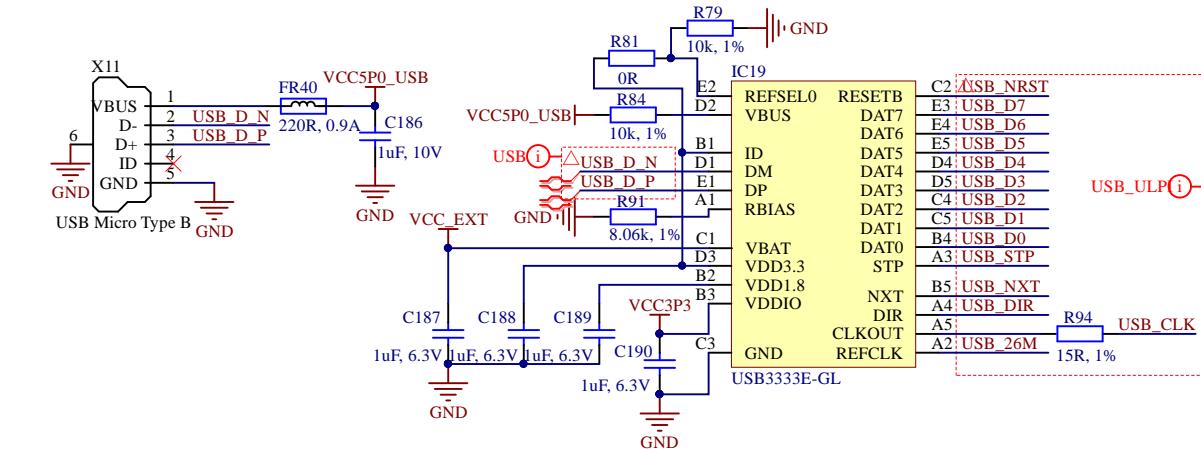
U.FL/MMCX



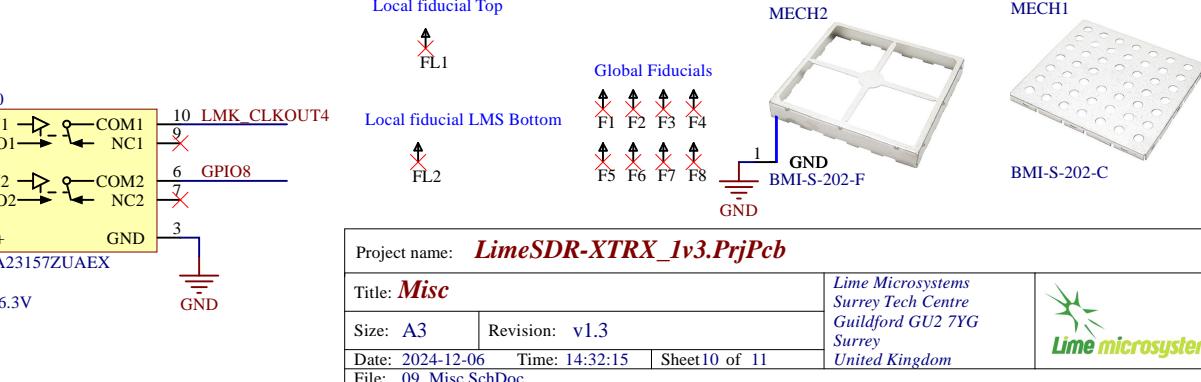
FPGA LEDs & GPIOs

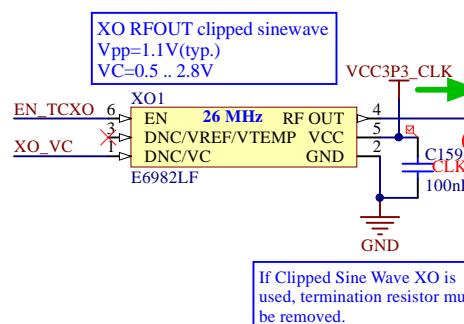
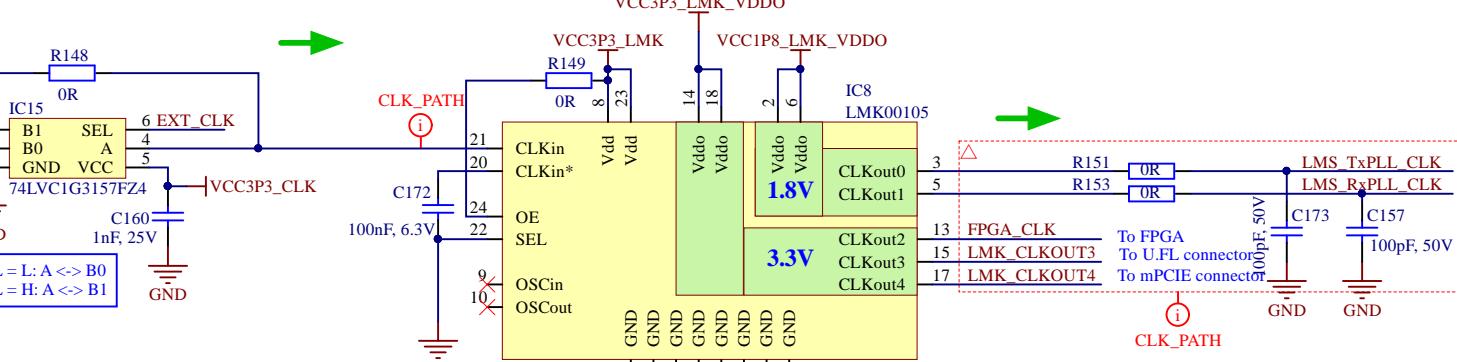


LED_green (GPIO11) is connected to pin 6 of the FPC connector. PCIE_W_DISABLE# (R103) is connected to pin 51 of the FPC connector. The GND connection is shared between the two pins.



FPGA LEDs & GPIOs



Clock**(VC)TCXO****Clock buffer**

A

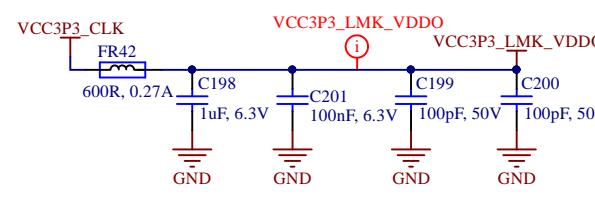
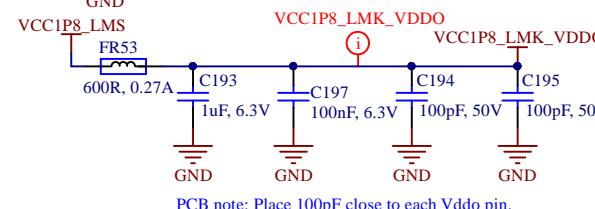
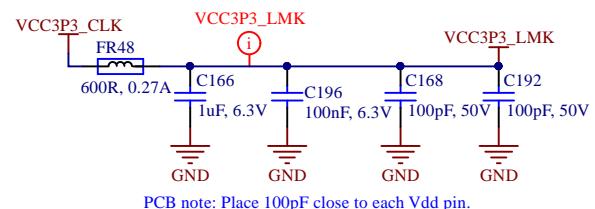
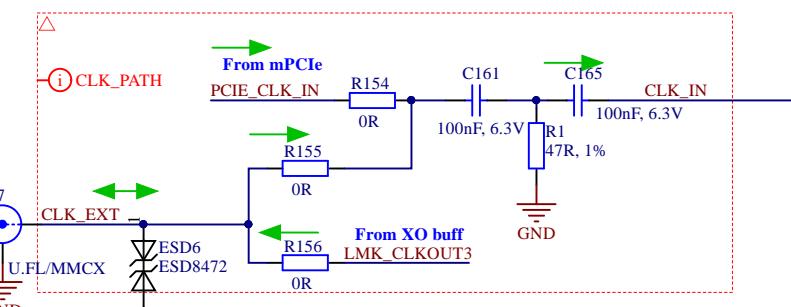
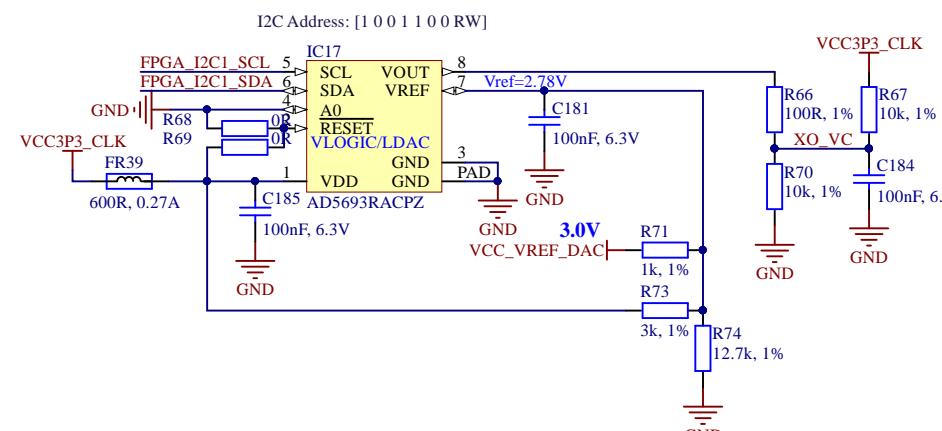
A

B

B

C

C

**XO DAC**

Project name: LimeSDR-XTRX_Iv3.PrjPcb

Title: Clock

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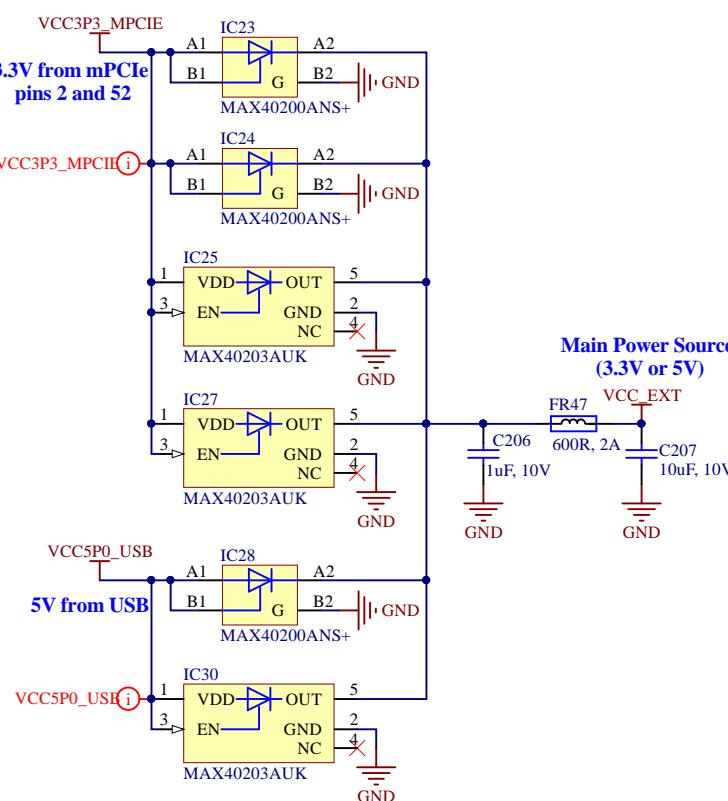
Size: A3 Revision: v1.3

Date: 2024-12-06 Time: 14:32:16 Sheet 10 of 11

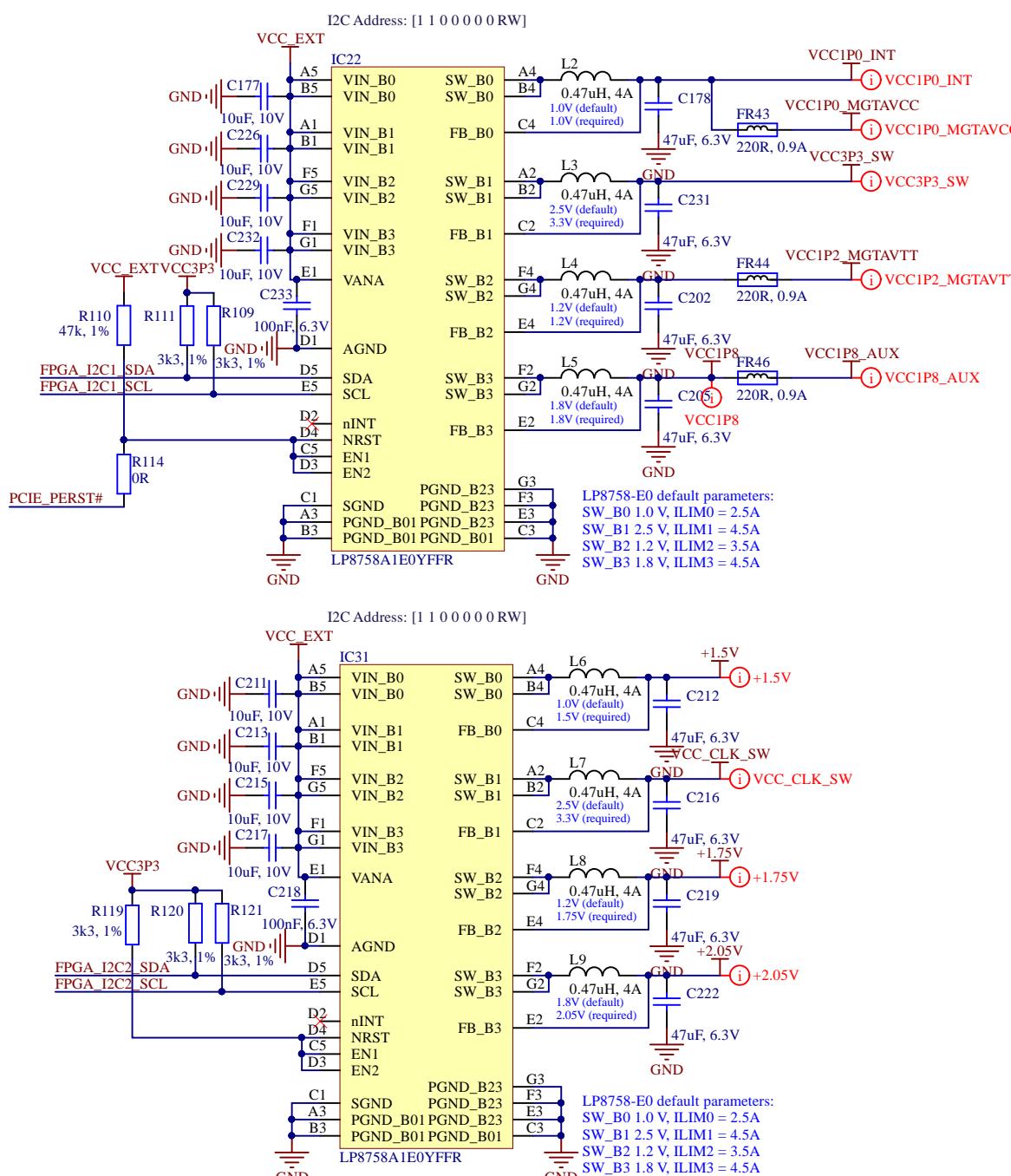
File: 10_Clock.SchDoc

Board power circuits

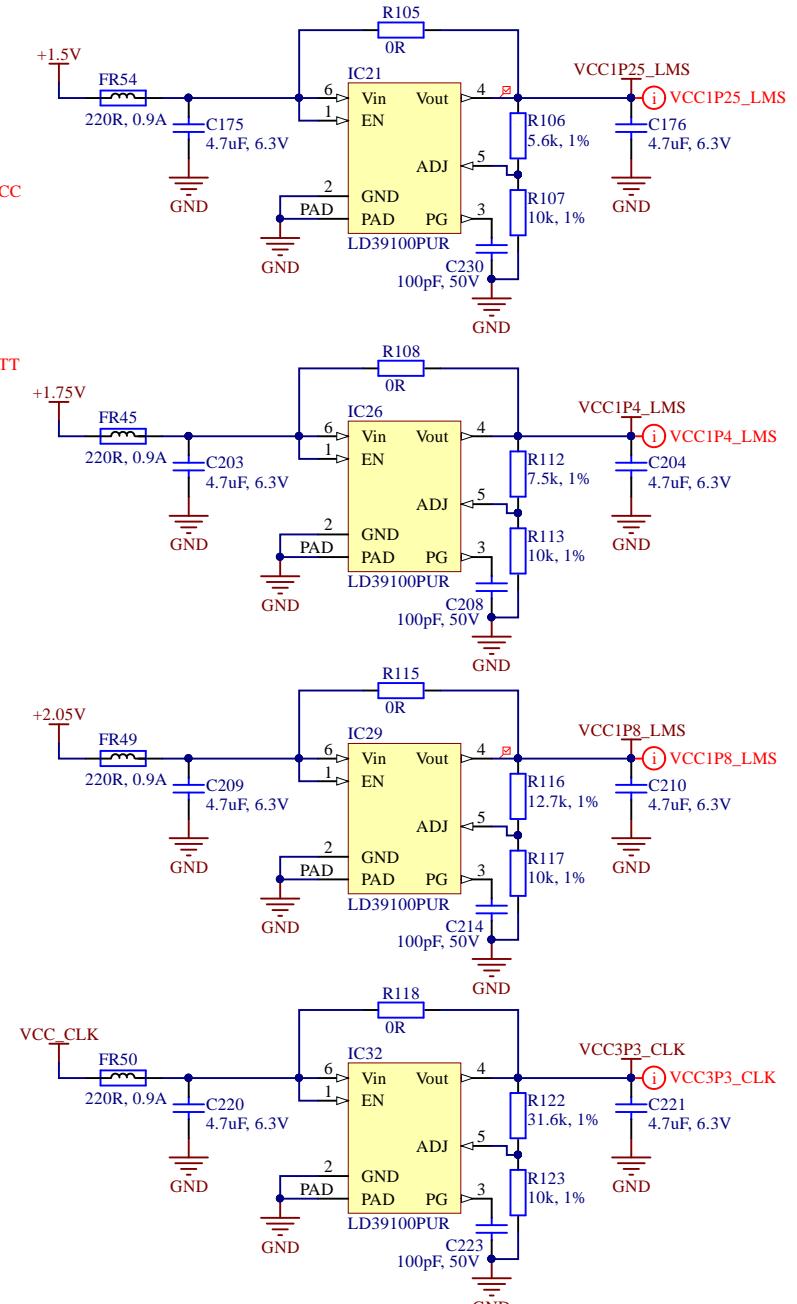
Power input



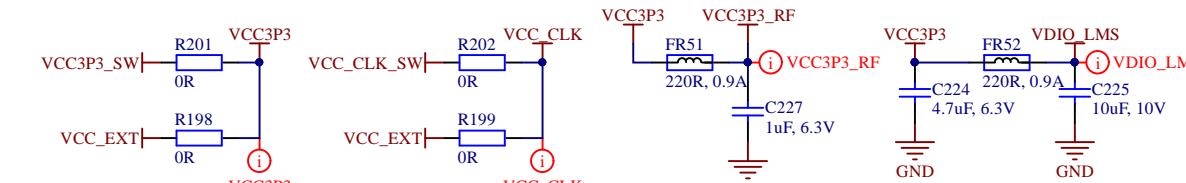
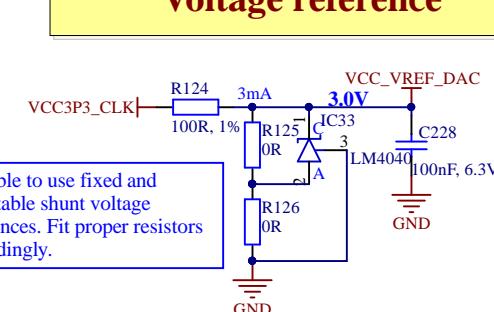
Switching regulators



Linear regulators



Voltage reference



Filters, voltage selection

Project name: LimeSDR-XTRX_Iv3.PrjPcb	
Title: Power	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.3
Date: 2024-12-06	Time: 14:32:17
File: 11_Power.SchDoc	Sheet 11 of 11

