10. Selectable I/O Standards in Cyclone II Devices

CII51010-2.4

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential *(3)*	*(4)*	1.5 V	—	—	—	✓ *(6)*	—
		1.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential HSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—	—	✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
LVDS	Differential	2.5 V	2.5 V	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(7)*	Differential	*(4)*	2.5 V	—	✓	—	✓	✓
LVPECL *(8)*	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	*(4)*	✓	—	✓	—	—

Notes to Table 10–1:

(1) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(2) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(3) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(4) This I/O standard is not supported on these I/O pins.
(5) This I/O standard is only supported on the dedicated clock pins.
(6) `PLL_OUT` does not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(7) mini-LVDS and RSDS are only supported on output pins.
(8) LVPECL is only supported on clock inputs, not DQS and dual-purpose clock pins.

3.3-V LVTTL (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-/3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of $-0.3\ V \leq V_I \leq 3.9\ V$. Altera recommends an input voltage range of $-0.5\ V \leq V_I \leq 4.1\ V$.

3.3-V LVCMOS (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL ($-0.3\ V \leq V_I \leq 3.9\ V$). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels specified by the 3.3-V LVCMOS I/O standard.

3.3-V (PCI Special Interest Group [SIG] PCI Local Bus Specification Revision 3.0)

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 3.0 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires a 3.3-V V_{CCIO}. The 3.3-V PCI standard does not require input reference voltages or board terminations.

The side (left and right) I/O banks on all Cyclone II devices are fully compliant with the 3.3V PCI Local Bus Specification Revision 3.0 and meet 32-bit/66 MHz operating frequency and timing requirements.

Table 10–2 lists the specific Cyclone II devices that support 64- and 32-bit PCI at 66 MHz.

Table 10–2. Cyclone II 66-MHz PCI Support (Part 1 of 2)

Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLineBGA®		✓

Table 10–2. Cyclone II 66-MHz PCI Support (Part 2 of 2)

Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C8	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLine BGA		✓
EP2C15	256-pin FineLine BGA		✓
	484-pin FineLine BGA	✓	✓
EP2C20	240-pin PQFP		✓
	256-pin FineLine BGA		✓
	484-pin FineLine BGA	✓	✓
EP2C35	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C50	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C70	672-pin FineLine BGA	✓	✓
	896-pin FineLine BGA	✓	✓

Table 10–3 lists the specific Cyclone II devices that support 64-bit and 32-bit PCI at 33 MHz.

Table 10–3. Cyclone II 33-MHz PCI Support (Part 1 of 2)

Device	Package	–6, –7 and –8 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP	—	—
	208-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
EP2C8	144-pin TQFP	—	—
	208-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
EP2C15	256-pin FineLine BGA	—	✓
	484-pin FineLine BGA	✓	✓

Table 10–3. Cyclone II 33-MHz PCI Support (Part 2 of 2)

Device	Package	–6, –7 and –8 Speed Grades	
		64 Bits	32 Bits
EP2C20	240-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
	484-pin FineLine BGA	✓	✓
EP2C35	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C50	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C70	672-pin FineLine BGA	✓	✓
	896-pin FineLine BGA	✓	✓

3.3-V PCI-X

The 3.3-V PCI-X I/O standard is formulated under PCI-X Local Bus Specification Revision 1.0 developed by the PCI SIG.

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 gigabit per second (Gbps) for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, devices can be designed to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V V_{CCIO}. Cyclone II devices are fully compliant with the 3.3-V PCI-X Specification Revision 1.0a and meet the 133 MHz operating frequency and timing requirements. The 3.3-V PCI-X standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels operation for left and right I/O banks.

Easy-to-Use, Low-Cost PCI Express Solution

PCI Express is rapidly establishing itself as the successor to PCI, providing higher performance, increased flexibility, and scalability for next-generation systems without increasing costs, all while maintaining software compatibility with existing PCI applications. Now you can easily design high volume, low-cost PCI Express ×1 solutions today featuring:

- Cyclone II FPGA (EP2C15 or larger)
- Altera PCI Express Compiler ×1 MegaCore® function
- External PCI Express transceiver/PHY

2.5-V LVTTL (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVTTL.

2.5-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVCMOS.

SSTL-2 Class I and II (EIA/JEDEC Standard JESD8-9A)

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operations in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\ V \leq V_I \leq V_{CCIO} + 0.3\ V$. SSTL-2 requires a V_{REF} value of 1.25 V and a V_{TT} value of 1.25 V connected to the termination resistors (refer to Figures 10–1 and 10–2).

Figure 10–1. SSTL-2 Class I Termination

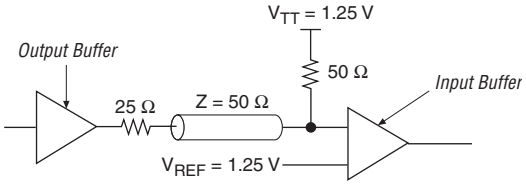
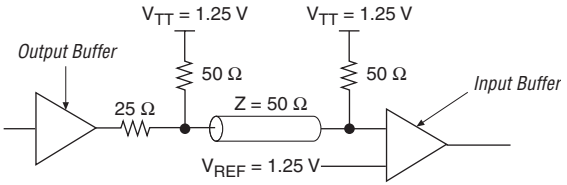


Figure 10–2. SSTL-2 Class II Termination



Cyclone II devices support both input and output SSTL-2 class I and II levels.

Pseudo-Differential SSTL-2

The differential SSTL-2 I/O standard (EIA/JEDEC standard JESD8-9A) is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of – 0.3 V ≤V_I ≤V_{CCIO} + 0.3 V. The differential SSTL-2 standard does not require an input reference voltage. Refer to Figures 10–3 and 10–4 for details on differential SSTL-2 terminations.

Cyclone II devices do not support true differential SSTL-2 standards. Cyclone II devices support pseudo-differential SSTL-2 outputs for `PLL_OUT` pins and pseudo-differential SSTL-2 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

Figure 10–3. SSTL-2 Class I Differential Termination

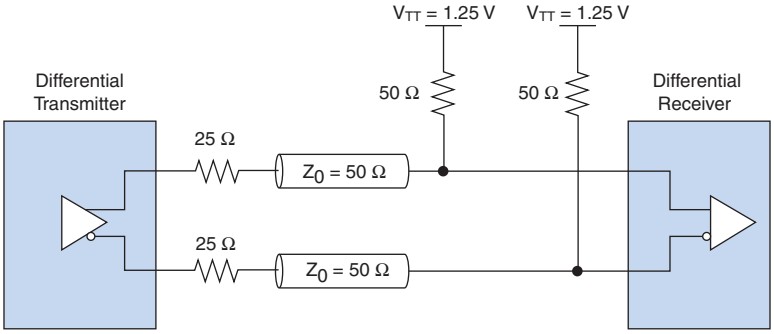
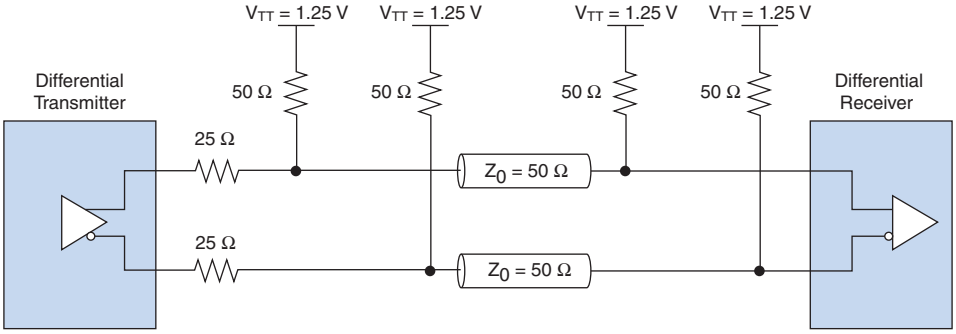


Figure 10–4. SSTL-2 Class II Differential Termination



1.8-V LVTTL (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVTTL.

1.8-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVCMOS.

SSTL-18 Class I and II

The 1.8-V SSTL-18 standard is formulated under JEDEC Standard, JESD815: Stub Series Terminated Logic for 1.8V (SSTL-18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT}, with the termination resistors connected to both. There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera provides solutions to two derived applications in JEDEC specification and names them class I and class II to be consistent with other SSTL standards. Figures 10–5 and 10–6 show SSTL-18 class I and II termination, respectively. Cyclone II devices support both input and output levels.

Figure 10–5. 1.8-V SSTL Class I Termination

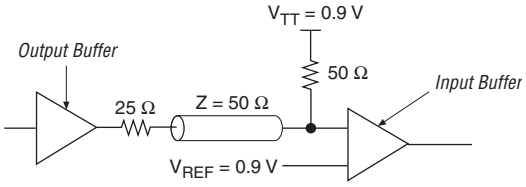
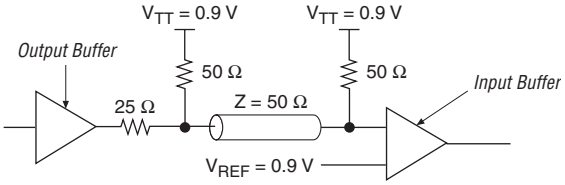


Figure 10–6. 1.8-V SSTL Class II Termination



1.8-V HSTL Class I and II

The HSTL standard is a technology independent I/O standard developed by JEDEC to provide voltage scalability. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces.

Although JEDEC specifies a maximum V_{CCIO} value of 1.6 V, there are various memory chip vendors with HSTL standards that require a V_{CCIO} of 1.8 V. Cyclone II devices support interfaces with V_{CCIO} of 1.8 V for HSTL. Figures 10–7 and 10–8 show the nominal V_{REF} and V_{TT} required to track the higher value of V_{CCIO}. The value of V_{REF} is selected to provide optimum noise margin in the system. Cyclone II devices support both input and output levels of operation.

Figure 10–7. 1.8-V HSTL Class I Termination

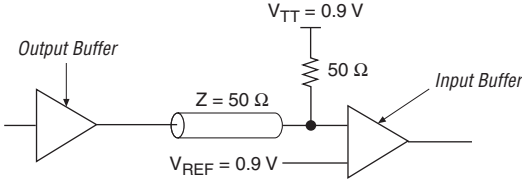
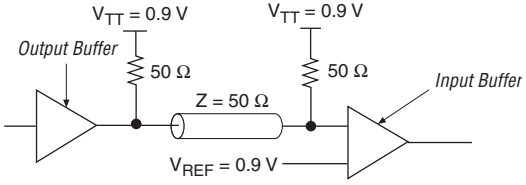


Figure 10–8. 1.8-V HSTL Class II Termination



Pseudo-Differential SSTL-18 Class I and Differential SSTL-18 Class II

The 1.8-V differential SSTL-18 standard is formulated under JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8V (SSTL-18).

The differential SSTL-18 I/O standard is a 1.8-V standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard supports differential signals in systems using the SSTL-18 standard and supplements the SSTL-18 standard for differential clocks. Refer to Figures 10–9 and 10–10 for details on differential SSTL-18 termination.

Cyclone II devices do not support true differential SSTL-18 standards. Cyclone II devices support pseudo-differential SSTL-18 outputs for `PLL_OUT` pins and pseudo-differential SSTL-18 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

Figure 10–9. Differential SSTL-18 Class I Termination

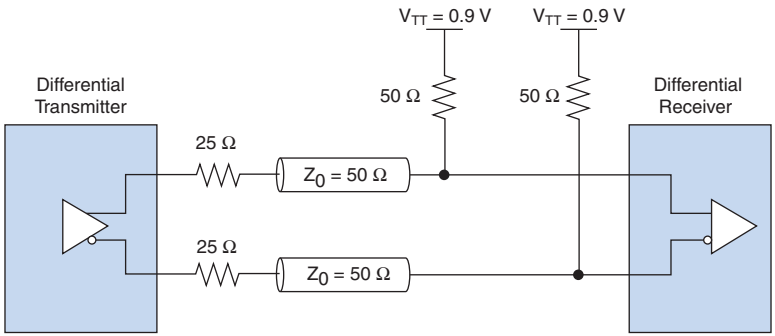
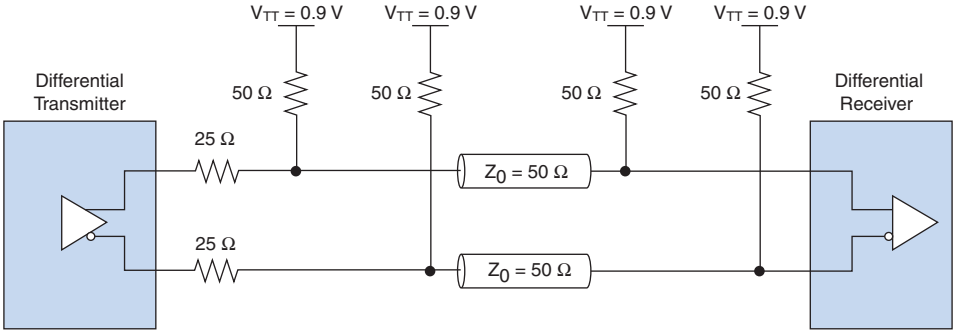


Figure 10–10. Differential SSTL-18 Class II Termination



1.8-V Pseudo-Differential HSTL Class I and II

The 1.8-V differential HSTL specification is the same as the 1.8-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0 to 1.8-V HSTL logic switching range such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–11 and 10–12 for details on 1.8-V differential HSTL termination.

Cyclone II devices do not support true 1.8-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

Figure 10–11. 1.8-V Differential HSTL Class I Termination

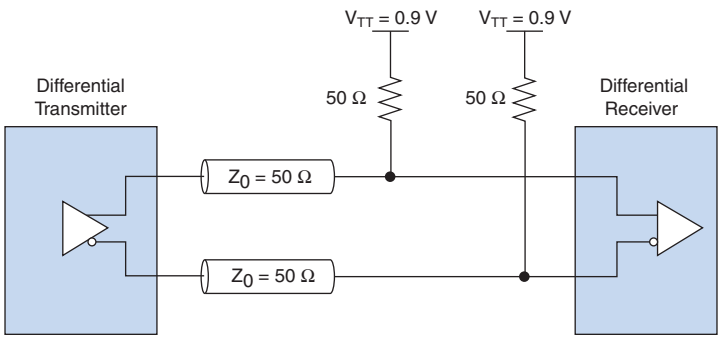
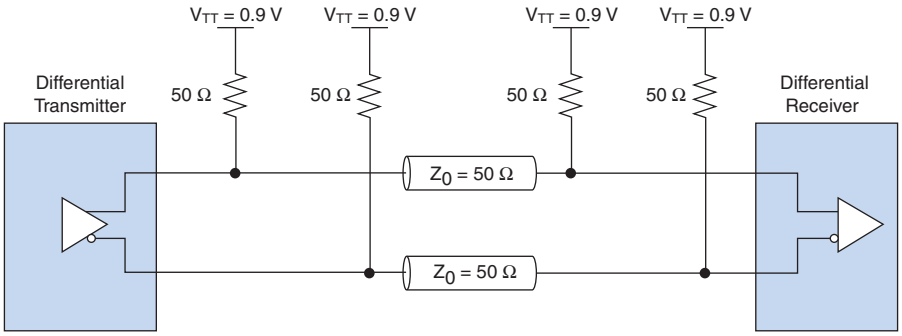


Figure 10–12. 1.8-V Differential HSTL Class II Termination



1.5-V LVCMOS (EIA/JEDEC Standard JESD8-11)

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices.

The 1.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.5-V LVCMOS.

1.5-V HSTL Class I and II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Cyclone II devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, Stratix® II, Stratix GX, Stratix, and in Cyclone II devices themselves because the input and output voltage thresholds are compatible. Refer to Figures 10–13 and 10–14. Cyclone II devices support both input and output levels with V_{REF} and V_{TT}.

Figure 10–13. 1.5-V HSTL Class I Termination

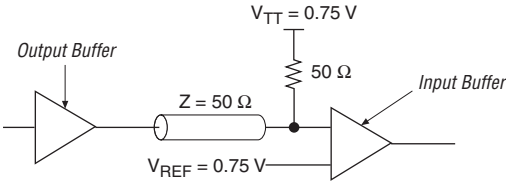
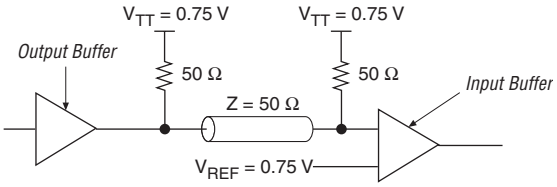


Figure 10–14. 1.5-V HSTL Class II Termination



1.5-V Pseudo-Differential HSTL Class I and II

The 1.5-V differential HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V differential HSTL specification is the same as the 1.5-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range, such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–15 and 10–16 for details on the 1.5-V differential HSTL termination.

Cyclone II devices do not support true 1.5-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

Figure 10–15. 1.5-V Differential HSTL Class I Termination

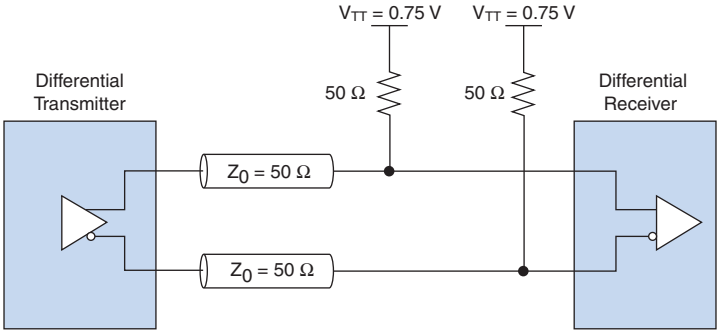
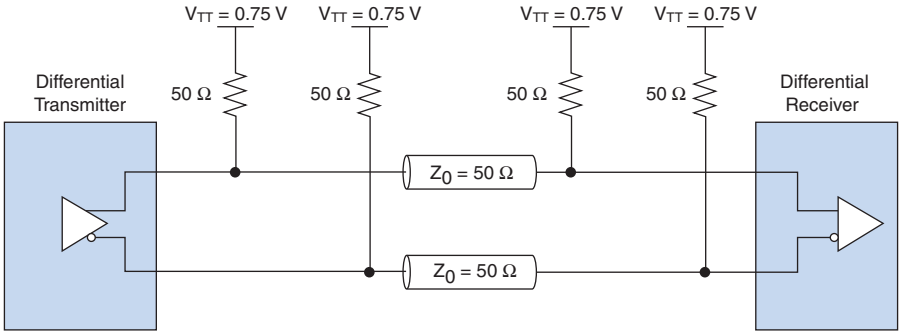


Figure 10–16. 1.5-V Differential HSTL Class II Termination



LVDS, RSDS and mini-LVDS

The LVDS standard is formulated under ANSI/TIA/EIA Standard, ANSI/TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits.

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. Cyclone II devices are capable of running at a maximum data rate of 805 Mbps for input and 640 Mbps for output and still meet the ANSI/TIA/EIA-644 standard.

Because of the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than complementary metal-oxide semiconductor (CMOS),

transistor-to-transistor logic (TTL), and positive (or pseudo) emitter coupled logic (PECL). This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage. However, it does require a termination resistor of 90 to 110 Ωbetween the two signals at the input buffer. Cyclone II devices support true differential LVDS inputs and outputs.

LVDS outputs on Cyclone II need external resistor network to work properly. Refer to the *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook* for more information.

For reduced swing differential signaling (RSDS), V_{OD} ranges from 100 to 600 mV. For mini-LVDS, V_{OD} ranges from 300 to 600 mV. The differential termination resistor value ranges from 95 to 105 Ωfor both RSDS and mini-LVDS. Cyclone II devices support RSDS/mini-LVDS outputs only.

Differential LVPECL

The low voltage positive (or pseudo) emitter coupled logic (LVPECL) standard is a differential interface standard recommending V_{CCIO} of 3.3 V. The LVPECL standard also supports V_{CCIO} of 2.5 V, 1.8 V and 1.5 V. The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require an external 100-Ωtermination resistor between the two signals at the input buffer. Figures 10–17 and 10–18 show two alternate termination schemes for LVPECL. LVPECL input standard is supported at the clock input pins on Cyclone II devices. LVPECL output standard is not supported.

Figure 10–17. LVPECL DC Coupled Termination

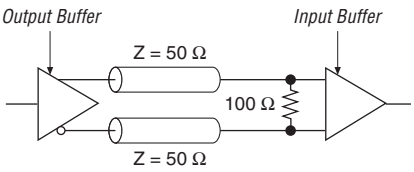
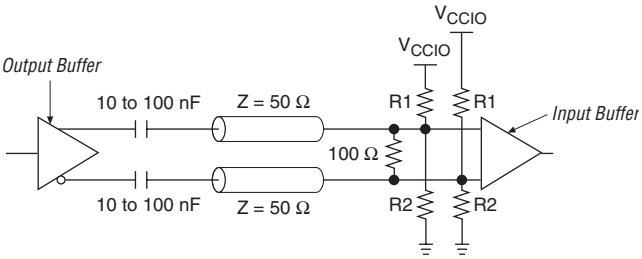


Figure 10–18. LVPECL AC Coupled Termination

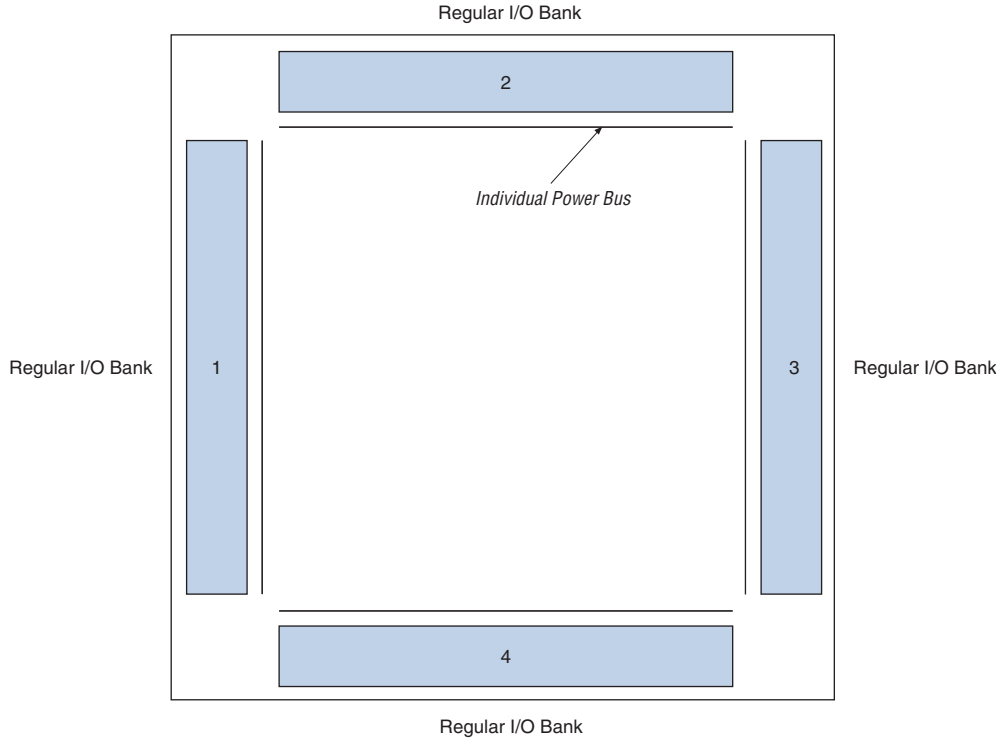


Cyclone II I/O Banks

The I/O pins on Cyclone II devices are grouped together into I/O banks, and each bank has a separate power bus. This allows you to select the preferred I/O standard for a given bank, enabling tremendous flexibility in the Cyclone II device's I/O support.

EP2C5 and EP2C8 devices support four I/O banks. EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices support eight I/O banks. Each device I/O pin is associated with one of these specific, numbered I/O banks (refer to Figures 10–19 and 10–20). To accommodate voltage-referenced I/O standards, each Cyclone II I/O bank has separate V_{REF} bus. Each bank in EP2C5, EP2C8, EP2C15, EP2C20, EP2C35, and EP2C50 devices supports two `VREF` pins and each bank in EP2C70 devices supports four `VREF` pins. In the event these pins are not used as `VREF` pins, they may be used as regular I/O pins. However, they are expected to have slightly higher pin capacitance than other user I/O pins when used with regular user I/O pins.

Figure 10–19. EP2C5 and EP2C8 Device I/O Banks *Notes (1), (2)*

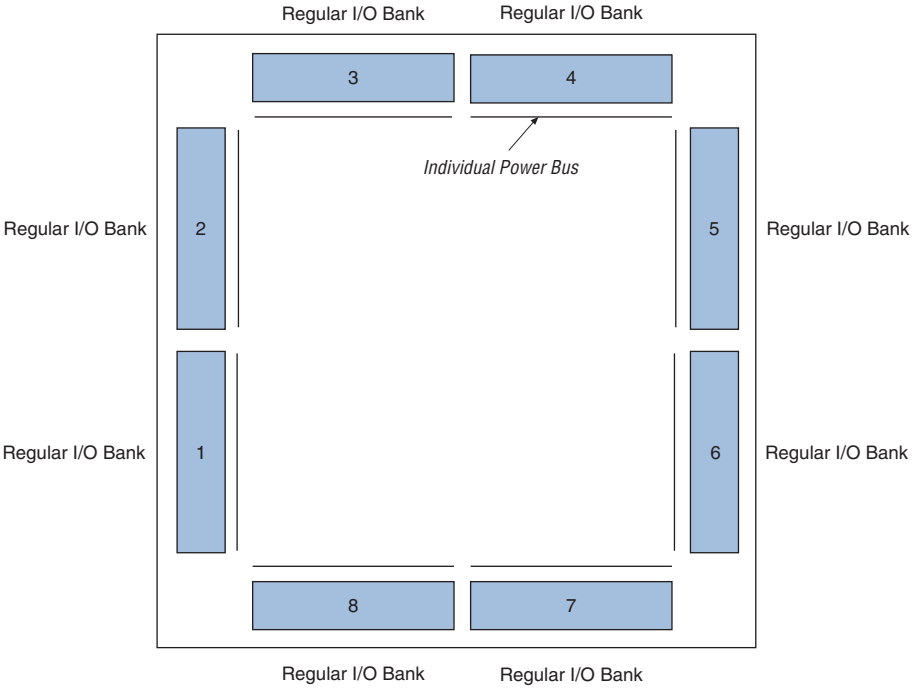


Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Figure 10–20. EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 Device I/O Banks *Notes (1), (2)*



Notes to Figure 10–20:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Additionally, each Cyclone II I/O bank has its own VCCIO pins. Any single I/O bank can only support one V_{CCIO} setting from among 1.5, 1.8, 2.5 or 3.3 V. Although there can only be one V_{CCIO} voltage per I/O bank, Cyclone II devices permit additional input signaling capabilities, as shown in Table 10–4.

Table 10–4. Acceptable Input Levels for LVTTL and LVCMOS

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
3.3	✓	✓ (1)		
2.5	✓	✓		
1.8	✓ (2)	✓ (2)	✓	✓ (1)
1.5	✓ (2)	✓ (2)	✓	✓

Notes to Table 10–4:

(1) Because the input level does not drive to the rail, the input buffer does not completely shut off, and the I/O current is slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** in Settings > Device > Device and Pin Options > Pin Placement tab. This setting allows input pins with LVTTL or LVCMOS I/O standards to be placed by the Quartus II software in an I/O bank with a lower V_{CCIO} voltage than the voltage specified by the pins.

Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank as long as they use compatible V_{CCIO} levels for input and output pins. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V LVTTL inputs and outputs, 2.5-V LVDS-compatible inputs and outputs, and 3.3-V LVCMOS inputs only.

Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone II device, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

Refer to "Pad Placement and DC Guidelines" on page 10–27 for more information.

Table 10–5 shows I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Cyclone II devices.

Table 10–5. Cyclone II Regular I/O Standards Support

I/O Standard	I/O Banks for EP2C15, EP2C20, EP2C35, EP2C50 and EP2C70 Devices								I/O Banks for EP2C5 and EP2C8 Devices			
	1	2	3	4	5	6	7	8	1	2	3	4
LVTTL	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
3.3-V PCI	✓	✓	—	—	✓	✓	—	—	✓	—	✓	—
3.3-V PCI-X	✓	✓	—	—	✓	✓	—	—	✓	—	✓	—
SSTL-2 class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
1.8-V HSTL class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V HSTL class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
1.5-V HSTL class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
Pseudo-differential SSTL-2	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
Pseudo-differential SSTL-18	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
1.8-V pseudo-differential HSTL	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
1.5-V pseudo-differential HSTL	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
LVDS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RSDS and mini-LVDS	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
Differential LVPECL	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*

Notes to Table 10–5:

(1) These I/O banks support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.

(2) Pseudo-differential I/O standards are only supported for clock inputs and dedicated `PLL_OUT` outputs. Refer to Table 10–1 for more information.

(3) This I/O standard is only supported for outputs.

(4) This I/O standard is only supported for the clock inputs.

Programmable Current Drive Strength

The Cyclone II device I/O standards support various output current drive settings as shown in Table 10–6. These programmable drive-strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for I_{OH} and I_{OL} of the corresponding I/O standard.

Table 10–6. Programmable Drive Strength (Part 1 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Side I/O Pins
LVTTL (3.3 V)	4	4
	8	8
	12	12
	16	16
	20	20
	24	24
LVCMOS (3.3 V)	4	4
	8	8
	12	12
	16	—
	20	—
	24	—
LVTTL and LVCMOS (2.5 V)	4	4
	8	8
	12	—
	16	—
LVTTL and LVCMOS (1.8 V)	2	2
	4	4
	6	6
	8	8
	10	10
	12	12
LVCMOS (1.5 V)	2	2
	4	4
	6	6
	8	—

Table 10–6. Programmable Drive Strength (Part 2 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Side I/O Pins
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	—
	24	—
SSTL-18 class I	6	6
	8	8
	10	10
	12	—
SSTL-18 class II	16	—
	18	—
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	N/A
	18	—
	20	—
HSTL-15 class I	8	8
	10	—
	12	—
HSTL-15 class II	16	N/A

These drive-strength settings are programmable on a per-pin basis using the Quartus II software.

I/O Termination

The majority of the Cyclone II I/O standards are single-ended, non-voltage-referenced I/O standards and, as such, the following I/O standards do not specify a recommended termination scheme:

- 3.3-V LVTTL and LVCMOS
- 2.5-V LVTTL and LVCMOS
- 1.8-V LVTTL and LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI and PCI-X

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

For more information on termination for voltage-referenced I/O standards, refer to "Supported I/O Standards" on page 10–1.

Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

Cyclone II devices support differential I/O standards LVDS, RSDS, and mini-LVDS, and differential LVPECL.

For more information on termination for differential I/O standards, refer to "Supported I/O Standards" on page 10–1.

I/O Driver Impedance Matching (R_S) and Series Termination (R_S)

Cyclone II devices support driver impedance matching to the impedance of the transmission line, typically 25 or 50 Ω When used with the output drivers, on-chip termination (OCT) sets the output driver impedance to 25 or 50 Ωby choosing the driver strength. Once matching impedance is selected, driver current can not be changed. Table 10–7 provides a list of output standards that support impedance matching. All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

Table 10–7. Selectable I/O Drivers with Impedance Matching and Series Termination

I/O Standard	Target R_S (Ω)
3.3-V LVTTL/CMOS	25 *(1)*
2.5-V LVTTL/CMOS	50 *(1)*
1.8-V LVTTL/CMOS	50 *(1)*
SSTL-2 class I	50 *(1)*
SSTL-18 class I	50 *(1)*

Note to Table 10–7:

(1) These RS values are nominal values. Actual impedance varies across process, voltage, and temperature conditions. Tolerance is specified in the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Handbook*.

Pad Placement and DC Guidelines

This section provides pad placement guidelines for the programmable I/O standards supported by Cyclone II devices and includes essential information for designing systems using the devices' selectable I/O capabilities. This section also discusses the DC limitations and guidelines.

Quartus II software provides user controlled restriction relaxation options for some placement constraints. When a default restriction is relaxed by a user, the Quartus II fitter generates warnings.

For more information about how Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads in the same I/O bank. Use the following guidelines for placing single-ended pads with respect to differential pads and for differential output pads placement in Cyclone II devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Maximum of four 155-MHz (or greater) LVDS output channels per VCCIO and ground pair.
- Maximum of three 311-MHz (or greater) LVDS output channels per VCCIO and ground pair.

For optimal signal integrity at the LVDS input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVDS input pad.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Maximum of three 85-MHz (or greater) RSDS and mini-LVDS output channels per VCCIO and ground pair.

The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.

For optimal signal integrity at the LVPECL input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVPECL input pad.

V_{REF} Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the V_{REF} rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to V_{REF} pads and VCCIO and ground pairs. Use the following guidelines for placing single-ended pads in Cyclone II devices.

The Quartus II software automatically does all the calculations in this section.

Input Pads

Each V_{REF} pad supports up to 15 input pads on each side of the V_{REF} pad for FineLine BGA devices. Each V_{REF} pad supports up to 10 input pads on each side of the V_{REF} pad for quad flat pack (QFP) devices. This is irrespective of VCCIO and ground pairs, and is guaranteed by the Cyclone II architecture.

Output Pads

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VCCIO and ground pair supports 9 output pins for Fineline BGA packages (not more than 9 output pins per 12 consecutive row I/O pins) or 5 output pins for QFP packages (not more than 5 output pins per 12 consecutive row I/O pins or 8 consecutive column I/O pins). Any non-SSTL and non-HSTL output can be no closer than two pads away from a V_{REF} pad. Altera recommends that any SSTL or HSTL output, except for pintable defined DQ and DQS outputs, to be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels.

Quartus II software will not check for the SSTL and HSTL output pads placement rule.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

If the bidirectional pads are all controlled by the same output enable (OE) and there are no other outputs or voltage referenced inputs in the bank, then there is no case where there is a voltage referenced input is active at the same time as an output. Therefore, the output limitation does not apply. However, since the bidirectional pads are linked to the same OE, all the bidirectional pads act as inputs at the same time. Therefore, the input limitation of 30 input pads (15 on each side of the V_{REF} pad) for FineLine BGA packages and 20 input pads (10 on each side of the V_{REF} pad) for QFP packages applies.

If the bidirectional pads are all controlled by different OEs, and there are no other outputs or voltage referenced inputs in the bank, then there may be a case where one group of bidirectional pads is acting as inputs while another group is acting as outputs. In such cases, apply the formulas shown in Table 10–8.

Table 10–8. Input-Only Bidirectional Pad Limitation Formulas

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤9 (per VCCIO and ground pair)
QFP	(Total number of bidirectional pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤5 (per VCCIO and ground pair).

Consider a FineLine BGA package with four bidirectional pads controlled by the first OE, four bidirectional pads controlled by the second OE, and two bidirectional pads controlled by the third OE. If the first and second OEs are active and the third OE is inactive, there are 10 bidirectional pads, but it is safely allowable because there would be 8 or fewer outputs per VCCIO/GND pair.

When at least one additional voltage referenced input and no other outputs exist in the same V_{REF} bank, the bidirectional pad limitation applies in addition to the input and output limitations. See the following equations:

Total number of bidirectional pads + total number of input pads ≤30 (15 on each side of your V_{REF} pad) for Fineline BGA packages

Total number of bidirectional pads + total number of input pads ≤20 (10 on each side of your V_{REF} pad) for QFP packages

After applying the equation above, apply one of the equations in Table 10–9, depending on the package type.

Table 10–9. Bidirectional Pad Limitation Formulas (Where V_{REF} Inputs Exist)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) ≤9 (per VCCIO and ground pair)
QFP	(Total number of bidirectional pads) ≤5 (per VCCIO and ground pair)

When at least one additional output exists but no voltage referenced inputs exist, apply the appropriate formula from Table 10–10.

Table 10–10. Bidirectional Pad Limitation Formulas (Where V_{REF} Outputs Exist)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of additional output pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤9 (per VCCIO and ground pair)
QFP	(Total number of bidirectional pads) + (Total number of additional output pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤5 (per VCCIO and ground pair)

When additional voltage referenced inputs and other outputs exist in the same V_{REF} bank, the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. As such, the following rules apply:

Total number of bidirectional pads + total number of input pads ≤30 (15 on each side of your V_{REF} pad) for Fineline BGA packages

Total number of bidirectional pads + total number of input pads ≤20 (10 on each side of your V_{REF} pad) for QFP packages

After applying the equation above, apply one of the equations in Table 10–11, depending on the package type.

Table 10–11. Bidirectional Pad Limitation Formulas (Multiple V_{REF} Inputs and Outputs)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of output pads) ≤9 (per VCCIO/GND pair)
QFP	Total number of bidirectional pads + Total number of output pads ≤5 (per VCCIO/GND pair)

Each I/O bank can only be set to a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values (refer to Table 10–4 for more details) and compatible V_{REF} voltage levels.

DDR and QDR Pads

For dedicated DQ and DQS pads on a DDR interface, DQ pads have to be on the same power bank as DQS pads. With the DDR and DDR2 memory interfaces, a VCCIO and ground pair can have a maximum of five DQ pads.

For a QDR interface, D is the QDR output and Q is the QDR input. D pads and Q pads have to be on the same power bank as CQ. With the QDR and QDRII memory interfaces, a VCCIO and ground pair can have a maximum of five D and Q pads.

By default, the Quartus II software assigns D and Q pads as regular I/O pins. If you do not specify the function of a D or Q pad in the Quartus II software, the software sets them as regular I/O pins. If this occurs, Cyclone II QDR and QDRII performance is not guaranteed.

DC Guidelines

There is a current limit of 240 mA per eight consecutive output top and bottom pins per power pair, as shown by the following equation:

$$\sum_{pin}^{pin+7} I_{PIN} < 240mA \text{ per power pair}$$

There is a current limit of 240 mA per 12 consecutive output side (left and right) pins per power pair, as shown by the following equation:

pin+11
$\Sigma I_{PIN} < 240mA$ per power pair
pin

In all cases listed above, the Quartus II software generates an error message for illegally placed pads.

Table 10–12 shows the I/O standard DC current specification.

Table 10–12. Cyclone II I/O Standard DC Current Specification (Preliminary) (Part 1 of 2)

I/O Standard	I_{PIN} (mA)	
	Top and Bottom Banks	Side Banks
LVTTL	*(1)*	*(1)*
LVCMOS	*(1)*	*(1)*
2.5 V	*(1)*	*(1)*
1.8 V	*(1)*	*(1)*
1.5 V	*(1)*	*(1)*
3.3-V PCI	Not supported	1.5
3.3-V PCI-X	Not supported	1.5
SSTL-2 class I	12 *(2)*	12 *(2)*
SSTL-2 class II	24 *(2)*	20 *(2)*
SSTL-18 class I	12 *(2)*	12 *(2)*
SSTL-18 class II	8 *(2)*	Not supported
1.8-V HSTL class I	12 *(2)*	12 *(2)*
1.8-V HSTL class II	20 *(2)*	Not supported
1.5-V HSTL class I	12 *(2)*	10 *(2)*
1.5-V HSTL class II	18 *(2)*	Not supported
Differential SSTL-2 class I *(3)*	8.1 *(4)*	
Differential SSTL-2 class II *(3)*	16.4 *(4)*	
Differential SSTL-18 class I *(3)*	6.7 *(4)*	
Differential SSTL-18 class II *(3)*	13.4 *(4)*	
1.8-V differential HSTL class I *(3)*	8 *(4)*	
1.8-V differential HSTL class II *(3)*	16 *(4)*	
1.5-V differential HSTL class I *(3)*	8 *(4)*	

Table 10–12. Cyclone II I/O Standard DC Current Specification (Preliminary) (Part 2 of 2)

I/O Standard	I_{PIN} (mA)	
	Top and Bottom Banks	Side Banks
1.5-V differential HSTL class II *(3)*	16 *(4)*	
LVDS, RSDS and mini-LVDS	12	12

Notes to Table 10–12:

(1) The DC power specification of each I/O standard depends on the current sourcing and sinking capabilities of the I/O buffer programmed with that standard, as well as the load being driven. LVTTL and LVCMOS, and 2.5-, 1.8-, and 1.5-V outputs are not included in the static power calculations because they normally do not have resistor loads in real applications. The voltage swing is rail-to-rail with capacitive load only. There is no DC current in the system.

(2) This I_{PIN} value represents the DC current specification for the default current strength of the I/O standard. The I_{PIN} varies with programmable drive strength and is the same as the drive strength as set in Quartus II software. Refer to the *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook* for more information on the programmable drive strength feature of voltage referenced I/O standards.

(3) The current value obtained for differential HSTL and differential SSTL standards is per pin and not per differential pair, as opposed to the per-pair current value of LVDS standard.

(4) This I/O standard is only supported for clock input pins and `PLL_OUT` pins.

Table 10–12 only shows the limit on the static power consumed by an I/O standard. The amount of total power used at any moment could be much higher, and is based on the switching activities.

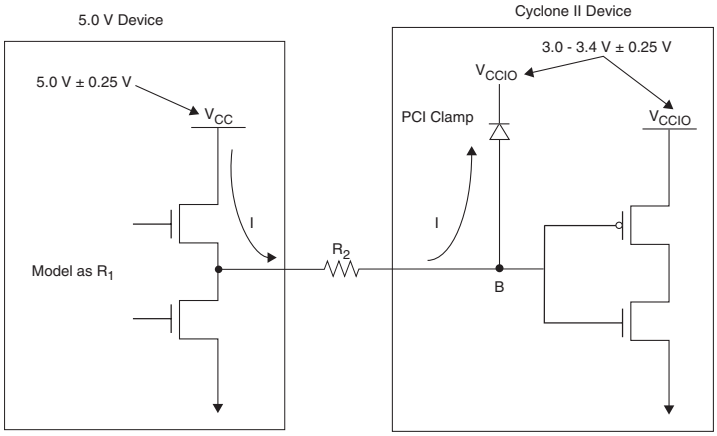
5.0-V Device Compatibility

A Cyclone II device may not correctly interoperate with a 5.0-V device if the output of the Cyclone II device is connected directly to the input of the 5.0-V device. If V_{OUT} of the Cyclone II device is greater than V_{CCIO}, the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0-V.

A Cyclone II device can drive a 5.0-V LVTTL device by connecting the V_{CCIO} pins of the Cyclone II device to 3.3 V. This is because the output high voltage (V_{OH}) of a 3.3-V interface meets the minimum high-level voltage of 2.4-V of a 5.0-V LVTTL device. (A Cyclone II device cannot drive a 5.0-V LVCMOS device.)

Because the Cyclone II devices are 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI and 64-bit 133-MHz PCI-X compliant, the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.1-V. To drive a Cyclone II device with a 5.0-V device, you must connect a resistor (R_2) between the Cyclone II device and the 5.0-V device. Refer to Figure 10–21.

Figure 10–21. Driving a Cyclone II Device with a 5.0-Volt Device

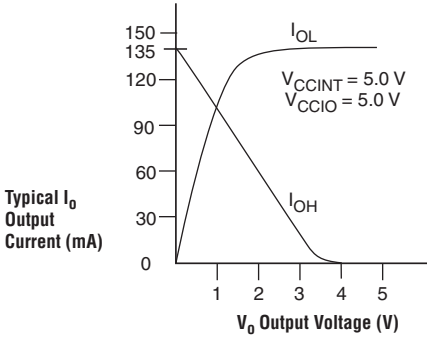


If V_{CCIO} is between 3.0 V and 3.6 V and the PCI clamping diode is enabled, the voltage at point B in Figure 10–21 is 4.3 V or less. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace. The PCI clamping diode in the Cyclone II device can support 25 mA of current.

To compute the required value of R_2, first calculate the model of the pull-up transistors on the 5.0-V device. This output resistor (R_1) can be modeled by dividing the 5.0-V device supply voltage (V_{CC}) by the I_{OH}: $R_1 = V_{CC}/I_{OH}$.

Figure 10–22 shows an example of typical output drive characteristics of a 5.0-V device.

Figure 10–22. Output Drive Characteristics of a 5.0-V Device



As shown above, R_1 = 5.0-V/135 mA.

The values shown in data sheets usually reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction when applied in the example in Figure 10–22 gives R_1 a value of 30 Ω

R_2 should be selected so that it does not violate the driving device's I_{OH} specification. For example, if the device has a maximum I_{OH} of 8 mA, given that the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{-V} = 3.7\text{-V}$, and the maximum supply load of a 5.0-V device (V_{CC}) is 5.25-V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.25\ V - 3.7\ V) - (8\ mA \times 30\ \Omega)}{8\ mA} = 164\ \Omega$$

This analysis assumes worst case conditions. If your system does not have a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in Cyclone II devices requires use of the PCI clamp, and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured.

Conclusion

Cyclone II device I/O capabilities enable you to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for I/O standards including SSTL and LVDS compatibility allow Cyclone II devices to fit into a wide variety of applications. The Quartus II

software makes it easy to use these I/O standards in Cyclone II device designs. After design compilation, the software also provides clear, visual representations of pads and pins and the selected I/O standards. Taking advantage of the support of these I/O standards in Cyclone II devices allows you to lower your design costs without compromising design flexibility or complexity.

References

For more information on the I/O standards referred to in this document, refer to the following sources:

- Stub Series Terminated Logic for 2.5-V (SSTL-2), JESD8-9A, Electronic Industries Association, December 2000.
- 1.5-V +/- 0.1-V (Normal Range) and 0.9-V - 1.6-V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.
- 1.8-V +/- 0.15-V (Normal Range) and 1.2-V - 1.95-V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.
- 2.5-V +/- 0.2-V (Normal Range) and 1.8-V to 2.7-V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
- Interface Standard for Nominal 3-V/ 3.3-V Supply Digital Integrated Circuits, JESD8-B, Electronic Industries Association, September 1999.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, December 1998.
- Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunications Industry/Electronic Industries Association, October 1995.

Referenced Documents

This chapter references the following documents:

- *Altera Reliability Report*
- *AN 75: High-Speed Board Designs*
- *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Cyclone II Device Family Data Sheet*, *section 1* of the *Cyclone II Device Handbook*
- *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*
- *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*
- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 10–13 shows the revision history for this document.

Table 10–13. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v2.4	• Added "Referenced Documents" section. • Updated "Differential Pad Placement Guidelines" section.	—
February 2007 v2.3	• Added document revision history. • Updated "Introduction" and its feetpara note. • Updated *Note (2)* in Table 10–4. • Updated "Differential LVPECL" section. • Updated "Differential Pad Placement Guidelines" section. • Updated "Output Pads" section. • Added new section "5.0-V Device Compatibility" with two new figures.	• Added reference detail for ESD specifications. • Added information about differential placement restrictions applying only to pins in the same bank. • Added information that Cyclone II device supports LVDS on clock inputs at 3.3V V_{CCIO}. • Added more information on DC placement guidelines. • Added information stating SSTL and HSTL outputs can be closer than 2 pads from V_{REF}. • Added 5.0 Device tolerence solution.

November 2005 v2.1	• Updated Tables 10–2 and 10–3. • Added PCI Express information. • Updated Table 10–6.	—
July 2005 v2.0	Updated Table 10–1.	—
November 2004 v1.1	Updated Table 10–7.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—