Thin Solid Films 704 (2020) 137991

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Solution-Processed Cupric Oxide P-type Channel Thin-Film Transistors

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ARTICLE INFO

Keywords:
Cupric oxide
p-type
Oxide semiconductor
Solution process
Thin film transistor

ABSTRACT

Thin films of cupric oxide (CuO) with various solution concentrations are deposited on the glass substrates via solution processing, as suggested for p-type semiconductors with non-toxic requirement. The effect of the solution concentration ranging from 0.15 M to 0.30 M was examined. We observed that the CuO thin films were single phase, polycrystalline with monoclinic crystal structure and were oriented along planes, such as (110), (-111), (111) and (-202). The micrographs of the scanning electron microscopy were observed to verify that the grain size of the CuO thin films increased with increases in the solution concentration. In addition, the CuO thin films showed a minimum resistivity of 0.0359 Ωcm, corresponding to the solution concentration of 0.30 M. Finally, the thin film transistors using the solution-processed CuO channel exhibited a p-type operation, with an on/off current ratio of approximately 10^2-10^3, and saturated field-effect mobility of approximately 10^{-4} $cm^2V^{-1}s^{-1}$.

1. Introduction

The oxide-semiconductor based thin film transistors (TFTs) have attracted significant attention for improving the traditional amorphous Si and organic-based TFTs, owing to their excellent performances in electrical applications such as in integrated circuits, sensors, and active matrix displays [1,2]. Generally, most studies have attempted to fabricate n-channel transistors using ZnO [3], In_2O_3 [4], zinc-tin oxide [5], indium zinc oxide [6] and indium-gallium-zinc oxide [7] thin films. In contrast, only a few studies have focused on the p-channel TFTs, due to the difficulties encountered in developing high-quality p-type thin films [8,9]. Moreover, the mobility of the p-type TFTs is often lower than that of the n-type TFTs. If this issue is resolved, a huge challenge may arise in the fabrication of low-power complementary logic circuits such as an inverter structure based on oxide-semiconductor transistors. Therefore, it is difficult to develop TFTs using the p-type metal oxide semiconductor as the conducting channel to fabricate complementary integrated circuits [2]. To address this, typical p-type semiconductors such as cupric oxide (CuO) [10], Cu_2O [11], NiO [12], and SnO [13] were developed as active material layers for application in p-channel TFTs. Among the various p-type semiconducting materials with non-toxic requirements, CuO is considered as one of the potential candidates for p-type TFTs, as it can be crystallized in a monoclinic structure via low-temperature fabrication and has a narrow bandgap energy, along with chemical and thermal stabilities. There are several techniques to synthesize CuO thin films, such as sputtering [14,15], pulsed laser deposition [16,17], chemical vapor deposition [18,19], thermal evaporation [20,21], and spin coating [22,23]. Among these, the spin coating method is the simplest and offers great advantages in the fabrication of thin films, as it requires low-power and low-material consumptions. Furthermore, it has a short processing time, and conformal formation on flexible substrates under atmospheric pressure can be

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https://doi.org/10.1016/j.tsf.2020.137991
Received 13 December 2019; Received in revised form 2 March 2020; Accepted 30 March 2020
Available online 13 April 2020
0040-6090/

easily achieved [24].

CuO TFTs are known to exhibit inferior electrical properties, as compared to other p-type semiconductors, as their valence band is mainly composed of anisotropic and local oxygen 2p orbitals; this leads to a large effective mass of holes and a low mobility [25]. Fabrication factors such as the annealing temperature and time can significantly influence the film features. In particular, the effect of annealing time on the electrical properties of CuO TFTs has been reported by Y. Yang et al. [2]. They found that the mobility and the on/off current ratio was improved by varying the annealing time. The optimal field-effect mobility and on/off current ratio obtained for the CuO TFTs were 1.2×10^{-2} $cm^2V^{-1}s^{-1}$ and 2×10^4, respectively, with an annealing time of 30 min. The effect of annealing temperature was also reported by J. Yu et al., and their results emphasized that the performance of CuO TFTs was improved if the annealing temperature was increased from 400 °C to 600 °C [26]. As the effect of solution concentration on the CuO thin film quality was unexplored, it was necessary to investigate its influence on the performance of the CuO TFTs. Hence, the concentrations of precursor solutions were adjusted to identify the optimum condition for fabricating CuO TFTs. The crystal structure, surface morphology, and the electrical properties of CuO thin films were also investigated systematically, prior to the evaluation of the operation of CuO TFTs.

2. Experimental procedures

2.1. CuO precursors preparation

The CuO precursor solution was prepared according to the following procedure. First, the copper (II) acetate monohydrate was dissolved in pure ethanol and stirred at the room temperature for 15 min. After light-blue $Cu(OH)_2$ was formed, the mono-ethanolamine (MEA) was added to the reaction solution under steady stirring at the room temperature for 15 min. An optimum molar ratio of MEA to copper (II) acetate salt of 2 was maintained. The concentration of the precursor solution was varied from 0.15 to 0.30 M. The resulting solution was stirred at 75°C for 60 min, using a digital hot plate stirrer (PC-620D, Corning), to form a network of molecules linking the copper ions together. No suspended particles were observed in the obtained dark-blue solution after an hour. The precursor solution was compensated with a pure ethanol to regain its initial volume, before being stored in a bottle. All the precursor solutions were stored in bottles and preserved in a refrigerator for 24 h before spin coating the surfaces of the substrates. In our experiment, when the Cu^{2+} ions concentration was more than 0.30 M, the precipitate phenomenon occurred in the precursor solution, and when less than 0.15 M, the surface of the CuO thin film was found to be discontinuous.

2.2. Thin films deposition

2.2.1. Substrate treatment

The cleaning of glass substrates significantly affects the film quality, because the surface contaminants can lead to the phenomenon of open resistor or localized high resistance. Thus, prior to coating the CuO precursor solution, commercial 22×22 mm^2 Deckglaser cover glasses were cleaned in the following manner. The glass substrates were first sonicated in acetone and ethanol for 5 min to remove organic dust present on the surface of the substrates. Next, the substrates were washed with distilled water to remove traces of acetone and ethanol. Finally, the substrates were dried using nitrogen flow. As the solution poses polar property and the surface of the glass is hydrophobic in nature, the glass substrates were treated with 5 ml of 2% HF acid for 30 s to cause the surface to be hydrophilic. Consequently, the precursor solution could be well applied to the surface of the treated substrates.

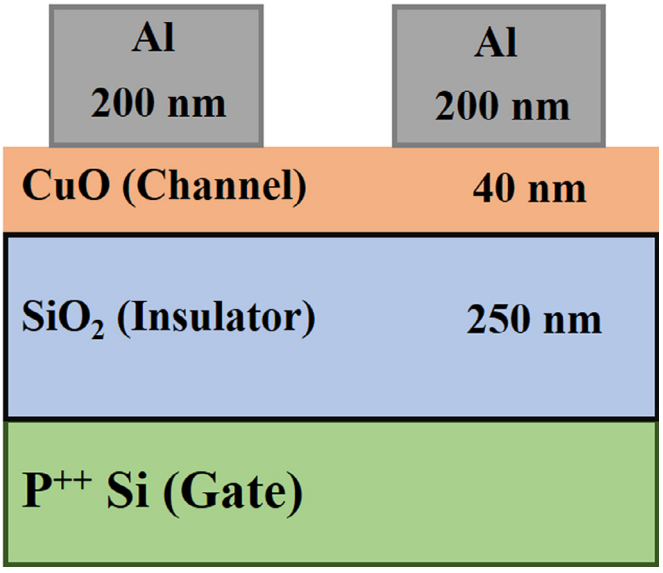

Figure 1. Schematic drawing of the CuO TFT structure.

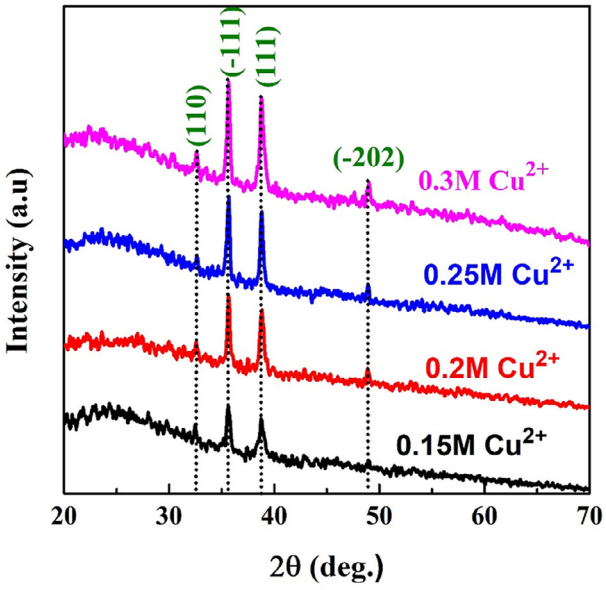

Figure 2. XRD patterns of the CuO thin films with various solution concentrations.

Table 1
Microstructural parameters of CuO films with various precursor concentrations.

Parameters	Diffraction peaks	0.15 M	0.20 M	0.25 M	0.30 M
D (nm)	(002)	28.86	34.32	41.86	47.50
	(111)	29.51	34.09	42.13	46.71
δ (10^{15} line/m^2)	(002)	1.20	0.85	0.57	0.44
	(111)	1.15	0.86	0.56	0.46
Strain (10^{-3})	(002)	1.20	1.01	0.83	0.73
	(111)	1.70	1.02	0.82	0.74

2.2.2. Spin coating process

After cleaning the surfaces of the substrates, the CuO thin films were deposited via a solution process. A glass substrate was first placed on the sample holder of a spin coater. The CuO solution was then spread on the surface of the substrate with a spin speed of 500 rpm for 10 s, and 1500 rpm for 40 s. Next, the CuO samples were pre-heated at 90°C for 3 min in air, and cooled for 3 min for each layer. To obtain the desired thickness of the CuO thin films, the spin-coating and drying steps were

Table 2
Lattice parameters (*a, b, c, β*) and unit cell volume (*V*) of CuO thin films.

Sample	*a* (Å)	*b* (Å)	*c* (Å)	*β* (°)	*V* (Å)^3
0.15 M	4.694	3.420	5.085	99.35	80.547
0.20 M	4.693	3.420	5.087	99.32	80.569
0.25 M	4.692	3.421	5.087	99.37	80.564
0.30 M	4.693	3.420	5.090	99.33	80.614

repeated four times. Lastly, after the spin-coating process was completed, the CuO samples were annealed at 550°C for 30 min under atmospheric pressure to change the deposited films from a gel state to a crystallized state.

2.3. Transistors fabrication

Figure 1 depicts the schematic drawing of the fabricated CuO TFT structure, in which a commercial Si substrate with heavy hole doping was used as the gate electrode, and a 250-nm-thick SiO_2 thin film formed by thermal oxidation technique was used as the gate insulator. The 40-nm-thick CuO thin film was deposited as a channel layer via a solution process with optimized conditions as mentioned in section 2.2. A 200 nm thick aluminum was patterned using the thermal evaporation technique for the source and drain electrodes of the CuO TFTs with stencil shadow masks of various sizes. In the TFTs structure, the channel width (*W*) was fixed at 1000 μm, and the channel length (*L*) was varied in a range 50–200 μm.

2.4. Characterizations

For evaluation of film quality, the structural, surface morphology, and electrical properties of the CuO thin film were analyzed. The crystal structure was analyzed using an X-ray diffractometer (XRD, Bruker, D5005) with Cu − *Ka* radiation (λ = 1.54056 Å), parallel beam, and a scanning speed of 0.03 °/s, from 10 ° to 70°. The morphological property was examined via scanning electron microscopy (SEM, Nova NANOSEM 450, FEI), with an operating voltage of 5 kV. The thickness of the CuO thin film was measured using a 3D High Resolution Stylus Surface Profilo-meter (NanoMap 500LS). The four-probe measurement system was used to determine electrical resistivity of the CuO thin films. The output characteristics (drain current I_D versus drain-source voltage V_{DS}) and transfer characteristics (I_D versus gate-source voltage V_{GS}) of the CuO TFTs were measured at room temperature using Keysight B2912A with a 3-probe station. The lower limit of the current measurement in this system was approximately 10^{-10} A.

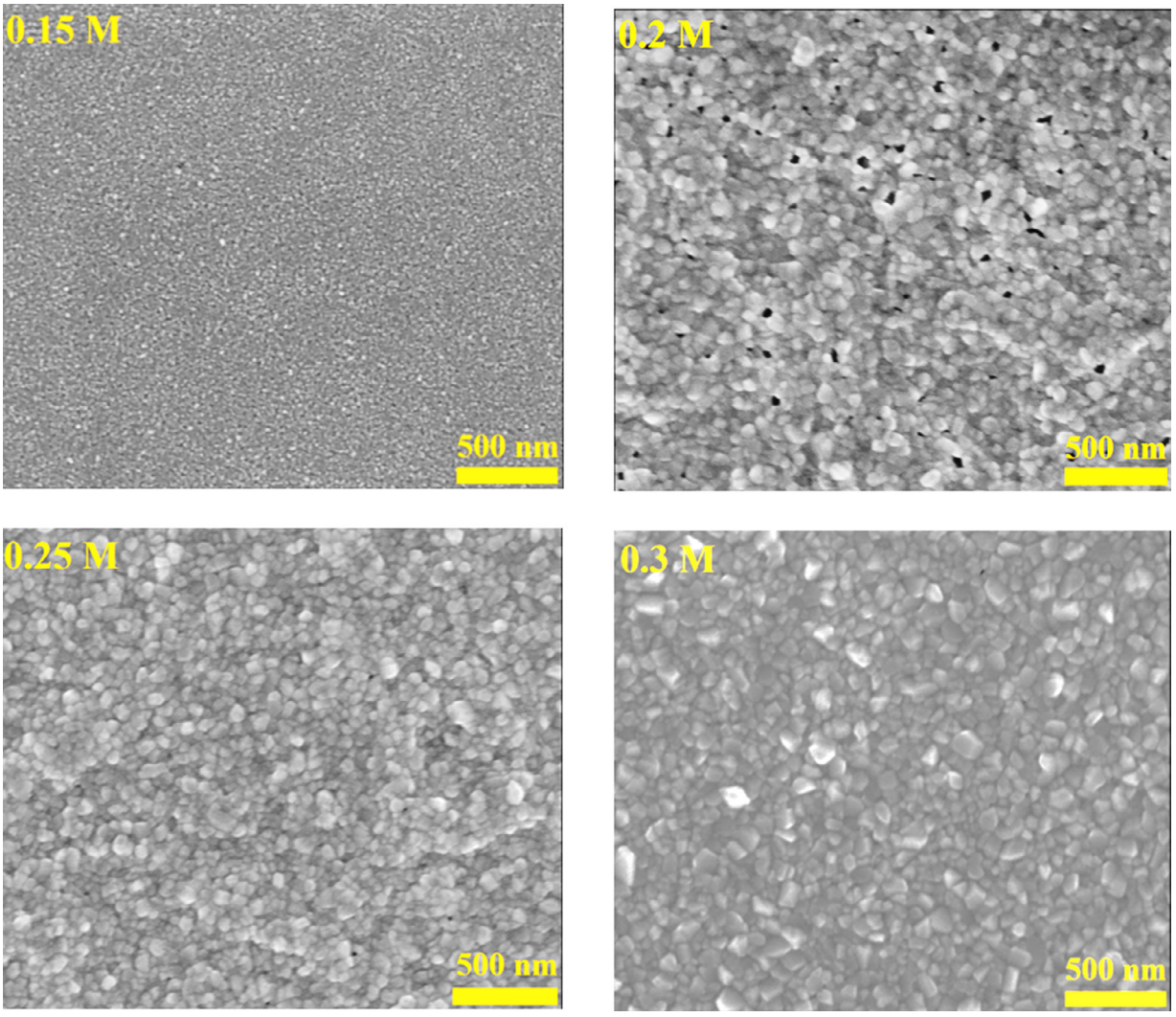

Figure 3. SEM micrographs of the CuO thin films with various solution concentrations.

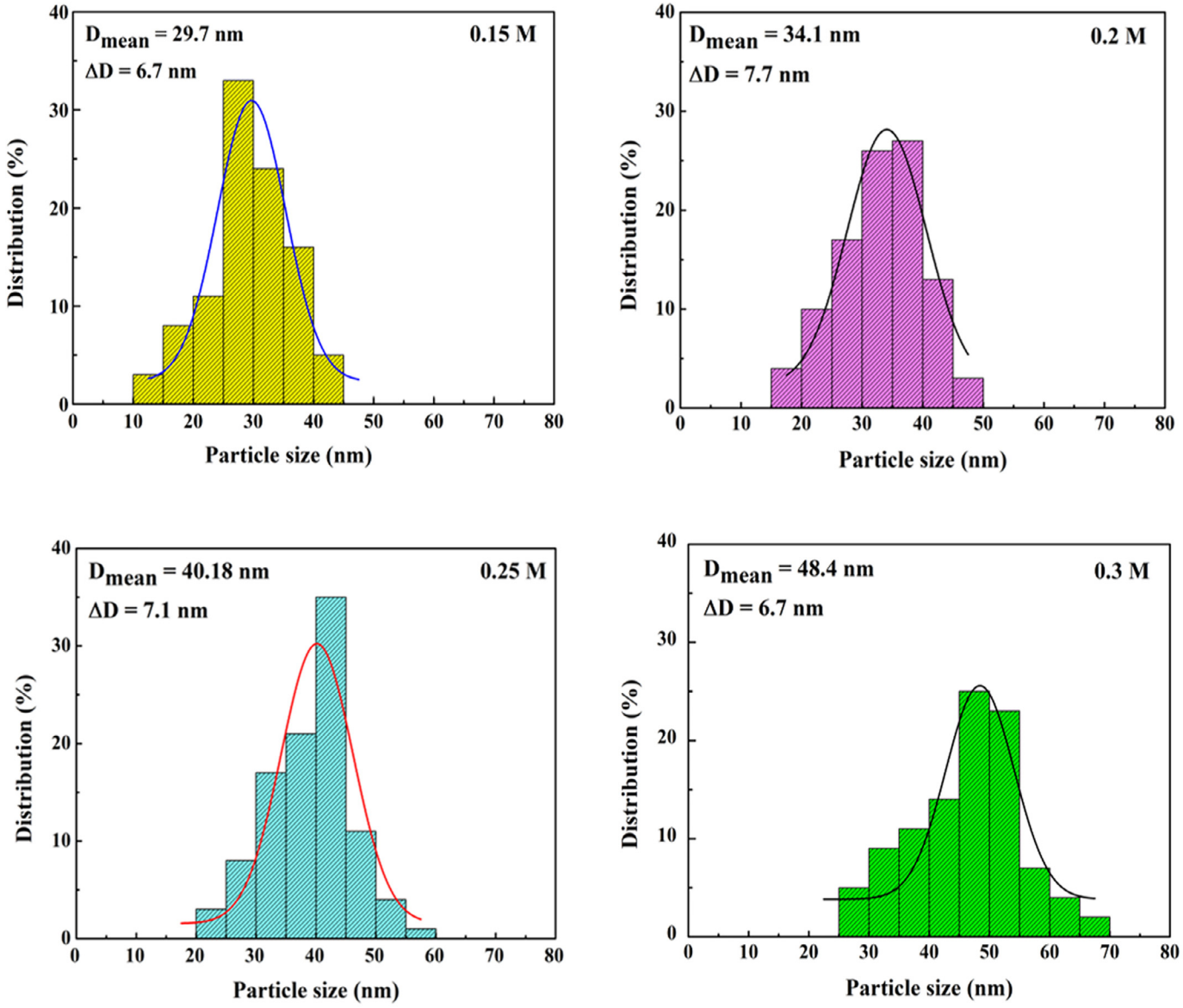

Figure 4. Particle size of the CuO calculated using ImageJ software and Gaussian fitting function.

Table 3
Electrical property of the CuO thin films as a function of precursor molar concentration.

Sample	Thickness (nm)	Resistivity (Ωcm)	Conductivity $(\Omega cm)^{-1}$
0.15 M	148	0.0838	11.9
0.20 M	164	0.0740	13.5
0.25 M	190	0.0568	17.6
0.30 M	240	0.0359	27.9

3. Results and discussion

3.1. Structural properties

The crystalline phases of the CuO thin films deposited on the glass substrates with various solution concentrations are identified in Figure 2. Regarding the XRD patterns of the CuO thin films, four peaks are observed at diffractive angles, 2θ, of 32.6°, 35.61°, 38.74°, and 48.9°, which are in complete agreement with the standard (110), (-111), (111) and (-202) orientations, respectively, and are referred in the monoclinic crystal structure of CuO (JCPDS 41-0254). Herein, the peak intensity of (-111) and (111) is higher than that of other peaks, which implies that the CuO thin films were grown mainly along the (-111) and (111) planes. This is consistent with the findings published in our previous work [23] and with the those reported by other researchers who prepared CuO thin films via the sol-gel method [22,27].

Based on the Debye-Scherer equation, it is possible to calculate the crystallite size (D) of the CuO thin films, using the following equation.

$$D = \frac{0.9\lambda}{\beta \cos\theta} \quad (1)$$

where, λ is the wavelength of X-ray radiation, β is the full width at haft maximum (FWHM) of the diffraction peak, and θ is the diffraction angle.

The strain (ε) of the CuO thin films is determined by the following formula [28].

$$\varepsilon = \frac{FWHM \cos\theta}{4} \quad (2)$$

The dislocation density (δ) of the CuO thin film is calculated by using the formula [29].

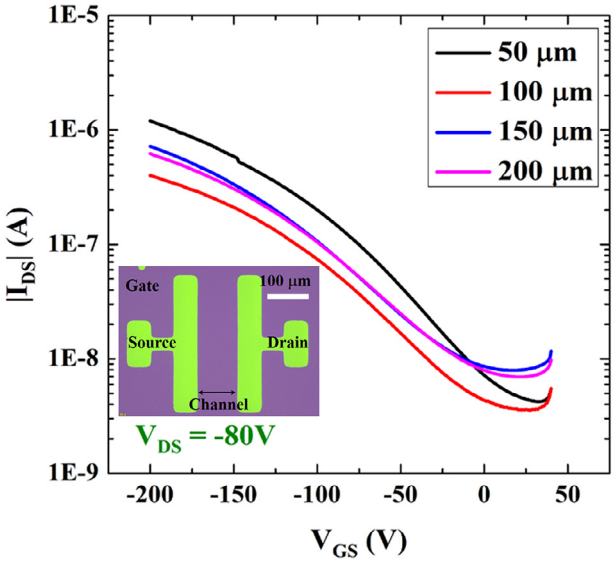

Figure 5. Transfer characteristics of the CuO TFTs with various channel lengths. The inset is a microscope image of the CuO TFT fabricated.

Table 4
Transistor performance of the CuO TFTs with different channel lengths.

Channel length (μm)	Threshold voltage V_T (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	Subthreshold Swing (V/dec)	On/off current ratio
50	-31.27	3×10^{-4}	65.83	1.66×10^2
100	-23.9	1.9×10^{-4}	77.04	1×10^2
150	-41.23	6.2×10^{-4}	85.11	8.35×10^1
200	-30.53	6.24×10^{-4}	84.25	7.81×10^2

$$\delta = \frac{1}{D^2} \tag{3}$$

Here, D is the crystallite size in the CuO thin films.

The values of D, ε and δ of the CuO thin films with different solution concentrations were calculated from the (002) and (111) preferential orientations using equations (1), (2) and (3) as listed in Table 1. Noticeably, the solution concentration varied from 0.15 to 0.30 M, and the microstructural parameters of the CuO thin films changed correspondingly. The crystalline size also increases with the increase in the precursor solution concentration. The decreasing dislocation density of the films indicated that the increasing solution concentration led to a reduction in the crystal lattice imperfections. In addition, the estimated strain decreased with increase in the solution concentration owing to the reduction of the grain boundary area [25,30]. These results indicate that the crystal quality of CuO thin film can be controlled by adjusting the initial solution concentration. It means that with an increase in the crystallite size, the dislocation density decreases, and the smaller strain values yield a better CuO thin film quality at higher solution concentrations.

Furthermore, the lattice parameters (a, b, c, $\alpha = \gamma = 90^o \neq \beta$) and unit cell volume ($V$) of the CuO thin films can be estimated by the following equations.

$$\frac{1}{d^2} = \frac{1}{\sin^2\beta}\left(\frac{1}{a^2} + \frac{k^2\sin^2\beta}{b^2} + \frac{1}{c^2} - \frac{2\cos\beta}{ac}\right) \tag{4}$$

$$V = abc\sin\beta \tag{5}$$

where, a, b and c are the lattice parameters of the monoclinic structure, (h, k, l) are the miller indices, and d is the interplanar distance [31]. The estimated lattice parameters and unit-cell volume of the CuO thin films are listed in Table 2. These values are in good agreement with those reported in the literature [32].

3.2. Surface morphology

The morphology of CuO thin films for various solution concentrations is illustrated in Figure 3. The ImageJ software was used to calculate the percentage distribution of particle sizes for determining the average particle size of CuO. Thereafter, the average particle size (D_{mean}) and standard deviation (ΔD) were estimated using the Gaussian fitting functions as shown in Figure 3. The average particle size was 29.70 ± 6.7 nm, 34.1 ± 7.7 nm, 40.2 ± 7.1 nm and 48.4 ± 6.7 nm for each corresponding concentration. It was confirmed that these sizes obtained by the ImageJ software and Gaussian fitting function are consistent with those calculated from the XRD patterns using the Debye-Scherrer formula. From Figure 4, we can infer that the grain size of the particles increases with the increase in the precursor solution concentration. Furthermore, an analysis of the SEM micrographs reveals that the CuO thin film becomes less porous when the solution concentration increases from 0.15 to 0.30 M. In the samples with 0.25 and 0.30 M concentrations, the surface of the CuO thin film was dense and non-porous. The SEM micrographs also show that the grain size of the thin film decreases as the precursor solution concentration reduces from 0.30 to 0.15 M. The expected surface morphology was achieved for the CuO thin film at a solution concentration more than 0.30 M, and a closed grain size. This can be explained as follows. During gel formation, the stabilizer (MEA) reacts with the Cu^{2+} ions present in the solution to generate the $Cu(CH_2CH_2OH)_2(H_2O)_2$ complex, which links the copper ions together [33]. Thus, a lower Cu^{2+} ions concentration will generate a lower amount of the $Cu(CH_2CH_2OH)_2(H_2O)_2$ complex for the same volume. This leads to the formation of smaller sized CuO particles with higher density after preheating at 90 °C and annealing at 550 °C. Therefore, these particles were not sufficient for occupying a proper equilibrium site, thereby leading to the formation of more porous thin films. In contrast, a higher concentration of Cu^{2+} ion generates a higher concentration of the complex, which leads to a higher condensation of Cu atoms and faster nucleation. Consequently, the CuO particles with bigger size were created with higher density. These particles can fill up whole spaces within the thin films, i.e., dense thin films were achieved for samples with 0.25 and 0.30 M concentration. Thus, at the same annealing temperature, these particles can combine together and form bigger crystallite sizes for higher precursor solution concentrations.

3.3. Electrical resistivity

The electrical property is a crucial parameter in the evaluation of the oxide-semiconductor thin film. In this work, the electrical resistivity for the fabricated CuO thin film was measured via the four-probe measurement technique, and the results are detailed in Table 3. Note that the thickness of the CuO thin film ranged from 148 nm to 240 nm. The electrical resistivity of the CuO thin film was found to decrease steadily from 0.0838 to 0.0359 Ωcm (i.e., the conductivity increased from 11.93 to 27.85 Ωcm^{-1}) when the Cu^{2+} ion concentration in the precursor solution was increased from 0.15 to 0.30 M. This is reasonable, as the grain size reduces with the reduction of the precursor molar concentration. When the grain size increases with the increase in the solution concentration, the grain boundaries decrease, which leads to the reduction in the subsequent scattering of carriers at the grain boundaries. Therefore, the resistivity decreases with the increase in the solution concentration, thereby resulting in the improvement of the conductivity of thin films [34].

Hence, the CuO thin film prepared from the precursor solution concentration of 0.30 M has a minimum electrical resistivity of 0.0359 Ωcm. This is found to be consistent with the results obtained from XRD and SEM analysis. More details toward the the interpretation of this result can be found in our previous work [23]. It is interesting that the

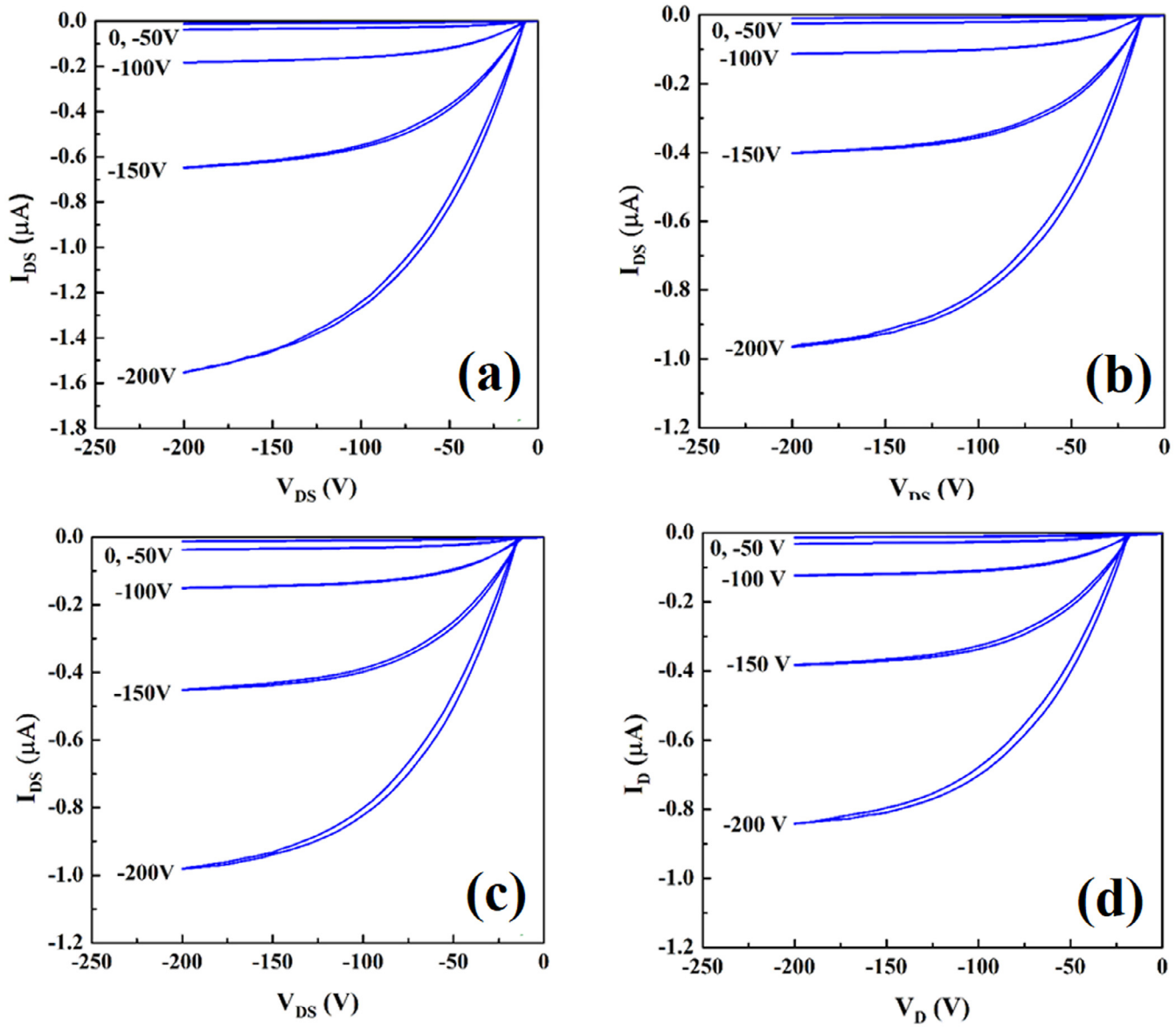

Figure 6. Output characteristics of the CuO TFTs with various channel lengths: a) 50 μm, b) 100 μm c) 150 μm, and d) 200 μm.

Table 5
Performance comparison of the p-type oxide-semiconductor TFTs.

Channel layer	μ_{sat} ($cm^2V^{-1}s^{-1}$)	On/off current ratio	Reference
Cu_2O	4.30	3.0×10^6	[40]
SnO	0.90	5.2×10^4	[13]
NiO	0.48	1.8×10^3	[12]
CuO (sputtering)	0.01	1.0×10^4	[39]
[a)]CuO (solution process)	0.26 - 0.78	$10^5 - 10^6$	[38]
[b)]CuO (solution process)	1.2×10^{-2}	2.0×10^4	[2]
[c)]CuO (solution process)	6.24×10^{-4}	7.81×10^2	This work

a: CuO prepared at the low annealing temperature of 300°C.
b: CuO optimized with the annealing time.
c: CuO optimized with the precursor concentration.

resistivity values found in this study are relatively lower than those of the previous reports [22,35,36], which suggested that the fabricated CuO thin films satisfied both the channel and the electrode requirement. Here, it should be noted that annealing at elevated temperatures can support the increase in grain size and improve the conductivity of CuO thin films. For channel application, a material with high mobility is more advantageous than the one with a high conductivity. Therefore, the temperature in the solution process is limited to 550 °C to avoid the deformation of glass substrates in flexible electronic applications of the non Si-based technology in the future.

3.4. Transistor performance

Figure 5 depicts the transfer characteristics of CuO TFTs for different L annealed at 550 °C in air, measured at a drain-source voltage of V_{DS} = -80 V. The inset of Figure 5 presents a typical microscopic image of the fabricated CuO TFTs. The CuO TFTs showed a clear p-type operation with an on/off current ratio of 10^2. In the saturation regime, I_D is determined as follows:

$$I_D = \frac{W.\mu.C_{SiO_2}}{2L}(V_{GS} - V_T)^2 \quad (6)$$

where, μ is the field-effect mobility, and V_T is the threshold voltage. C_{SiO_2} is the gate SiO_2 capacitance [37]. Additionally, the field-effect mobility of CuO TFTs can be estimated as follows.

$$\mu = \frac{2L}{WC_{SiO_2}}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_G}\right)^2 \quad (7)$$

In consequence, we can estimate μ and V_T from the slope and intercept of the fitting line, according to the $\sqrt{I_{DS}}$ versus V_G characteristics. The μ, V_T, and on/off current ratio obtained for the CuO TFTs with different channel lengths ranging from 50 to 200 μm with a step of 50 μm are listed in Table 4. The optimum values of μ and on/off current ratio for CuO TFTs were estimated to be 10^{-4} $cm^2V^{-1}s^{-1}$ and 10^{-2}, respectively. In another study, the μ of $0.012 \sim 1.6 \times 10^{-4}$ $cm^2V^{-1}s^{-1}$ and the on/off current ratio of 10^3 - 10^4 were reported for the CuO TFTs fabricated via the spin-coating method [2], which is quite similar to our work. For typical solution-processed CuO TFTs, the field-effect mobility and the on/off current ratio were found to be 0.26 $cm^2V^{-1}s^{-1}$ and 10^5, respectively. However, the best transistor performance with a μ of 0.78 $cm^2V^{-1}s^{-1}$ and on/off current ratio of 10^5 was reported by A. Liu et al., for the CuO TFTs based on the ScO_x dielectric [38]. Therefore, it is suggested that high-k materials should be potentially used to enhance the field-effect mobility and the on/off current ratio, in future studies.

In addition to the field-effect mobility and the on/off current ratio, the sub-threshold swing (*SS*) is also a key parameter of TFTs for the evaluation of switching ability, and it is determined as follows:

$$SS = \frac{\partial V_{GS}}{\partial \log I_{DS}} \quad (8)$$

The estimated values of *SS* for CuO TFTs with various channel lengths are listed in Table 4. As can be seen from the table, the *SS* values are 65.83, 77.04, 85.11 and 84.25 V/dec with different channel lengths ranging from 50 to 200 μm, with a step of 50 μm. CuO TFT with a channel length of 50 μm exhibits faster transition between the off state (low-leveled current) and on state (high-leveled current) as compared to other channel lengths.

Figure 6 describes the output characteristics of CuO TFTs for different channel lengths annealed at 550°C in air. In this measurement, the V_{GS} was scanned from 0 to -200 V with a step size of -50V. The V_{DS} was also scanned from 0 to -200V. The output-characteristic curves showed clear linear and saturation regions associated with the field-effect transistor, essentially belonging to the p-type semiconducting operation, which should be interesting considering the known nontoxic character of the CuO. At a low V_{DS}, the magnitude of I_D increases linearly, thereby indicating that the existence of an injection barrier between the source electrodes, and the channel of CuO thin film was in ohmic contact, which implies a well-switched on current originating from the hole carriers, as expected.

Table 5 presents a performance comparison of typical p-type oxide-semiconductor TFTs in the recent years. The performance of Cu_2O TFT appears to be more promising than that of SnO, NiO and CuO TFTs, because of higher field-effect mobility and on/off current ratio. Only few studies exist, in which the CuO TFTs were fabricated using a solution process. Although the performance of CuO TFT in this work is poorer than those reported by other studies [2,38], some possible routes can be considered to improve the transistor operation, for instance, optimization of the annealing time, annealing temperature, or the use of HfO_2 or ScO_x as a gate insulator, instead of SiO_2.

In this work, the thickness of the gate insulator layer was 250 nm. When the applied voltage was 200 V, the electric field was 800 kV/cm, which was relatively close to the breakdown electric field of 1000 kV/cm for SiO_2 material; however, this is not a serious problem. The surface of the SiO_2 should be well treated to avoid the presence of any interface layers between the SiO_2 and the CuO, although it was etched in 2% HF acid for 30 s. The presence of any interface layers may lead to the dropping of the applied voltage, and therefore, this leads to the application of a voltage smaller than the actual value to the SiO_2 layer. This causes the obtained subthreshold swing to be high. Therefore, the SiO_2 surface must be further processed by changing the dipping time or the acid concentration.

4. Conclusion

The solution processed CuO thin films were fabricated on glass substrates with various solution concentrations. The XRD results indicated that the CuO thin films were polycrystalline in nature with a monoclinic structure and were oriented along typical planes such as (110), (-111), (111) and (-202). The SEM micrographs showed that the grain size of thin film increased with the increase in solution concentration. A minimum electrical resistivity of 0.0359 Ωcm was achieved for the CuO thin film prepared from a 0.30 M solution. Interestingly, the CuO thin film, when stacked as a channel layer in the thin film transistor, exhibited a p-type operation with an on/off current ratio of 10^2 and a saturation mobility of $\sim 10^{-4}$ $cm^2V^{-1}s^{-1}$. It is expected that this achievement may widen the application of electrical devices such as thin film transistors, gas sensors or p-type absorption layers of solar cells.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

Funding: This work has been supported by the Vietnam National University, Hanoi (VNU), under Project No. QG.19.02.

References

[1] F.H. Alshammari, P.K. Nayak, Z. Wang, H.N. Alshareef, Enhanced ZnO Thin-Film Transistor Performance Using Bilayer Gate Dielectrics, ACS Appl. Mater. Inter 8 (2016) 22751–22755, https://doi.org/10.1021/acsami.6b06498.

[2] Y. Yang, J. Yang, W. Yin, F. Huang, A. Cui, D. Zhang, W. Li, Z. Hu, J. Chu, Annealing time modulated the film microstructures and electrical properties of P-type CuO field effect transistors, Appl. Surf. Sci 481 (2019) 632–636, https://doi.org/10.1016/j.apsusc.2019.03.130.

[3] B.Y. Oh, Y.H. Kim, H.J. Lee, B.Y. Kim, H.G. Park, J.W. Han, G.S. Heo, T.W. Kim, K.Y. Kim, D.S. Seo, High-performance ZnO thin-film transistor fabricated by atomic layer deposition, Semicond. Sci. Tech 26 (2011) 085007, , https://doi.org/10.1088/0268-1242/26/8/085007.

[4] P.K. Nayak, M.N. Hedhili, D. Cha, H.N. Alshareef, High performance In_2O_3 thin film transistors using chemically derived aluminum oxide dielectric, Appl. Phys. Lett. 103 (2013) 033518, , https://doi.org/10.1063/1.4816060.

[5] S. Sanctis, N. Koslowski, R. Hoffmann, C. Guhl, E. Erdem, S. Weber, J. r. J. Schneider, Toward an Understanding of Thin-Film Transistor Performance in Solution-Processed Amorphous Zinc Tin Oxide (ZTO) Thin Films, ACS Appl. Mater. Inter 9 (2017) 21328–21337, https://doi.org/10.1021/acsami.7b06203.

[6] H.C. Cheng, C.Y. Tsay, Flexible a-IZO thin film transistors fabricated by solution processes, J. Alloy. Compd. 507 (2010) L1–L3, https://doi.org/10.1016/j.jallcom.2010.06.166.

[7] P. Ma, L. Du, Y. Wang, R. Jiang, Q. Xin, Y. Li, A. Song, Low voltage operation of IGZO thin film transistors enabled by ultrathin Al_2O_3 gate dielectric, Appl. Phys. Lett 112 (2018) 023501, , https://doi.org/10.1063/1.5003662.

[8] Z. Yao, S. Liu, L. Zhang, B. He, A. Kumar, X. Jiang, W. Zhang, G. Shao, Room temperature fabrication of p-channel Cu_2O thin-film transistors on flexible polyethylene terephthalate substrates, Appl. Phys. Lett 101 (2012) 042114, , https://doi.org/10.1063/1.4739524.

[9] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, Epitaxial growth of high mobility Cu_2O thin films and application to p-channel thin film transistor, Appl. Phys. Lett 93 (2008) 202107, , https://doi.org/10.1063/1.3026539.

[10] S.Y. Sung, S.Y. Kim, K.M. Jo, J.H. Lee, J.J. Kim, S.G. Kim, K.H. Chai, S. Pearton, D. Norton, Y.W. Heo, Fabrication of p-channel thin-film transistors using CuO active layers deposited at low temperature, Appl. Phys. Lett 97 (2010) 222109, , https://doi.org/10.1063/1.3521310.

[11] Z. Wang, P.K. Nayak, J.A. Caraveo-Frescas, H.N. Alshareef, Recent developments in p-Type oxide semiconductor materials and devices, Adv. Mater 28 (2016) 3831–3892, https://doi.org/10.1002/adma.201503080.

[12] W Xu, J. Zhang, Y. Li, L. Zhang, L. Chen, D. Zhu, P. Cao, W. Liu, S. Han, X. Liu, P-type transparent amorphous oxide thin-film transistors using low-temperature solution-processed nickel oxide, J. Alloy. Compd 806 (2019) 40–51, https://doi.org/10.1016/j.jallcom.2019.07.108.

[13] Ha-Yun Jeong, Soo-Hun Kwon, Hyo-Jun Joo, Min-Gyu Shin, Hwan-Seok Jeong, Dae-Hwan Kim, and Hyuck-In Kwon, Radiation-Tolerant p-Type SnO Thin-Film Transistors, IEEE Electron Device Lett. 40 (2019) 1124-1127, doi: 10.1109/LED.

2019.2914252.
[14] S. Dolai, R. Dey, S. Das, S. Hussain, R. Bhar, A. Pal, Cupric oxide (CuO) thin films prepared by reactive dc magnetron sputtering technique for photovoltaic application, J. Alloy. Compd. 724 (2017) 456–464, https://doi.org/10.1016/j.jallcom.2017.07.061.
[15] A.S. Reddy, H.H. Park, V.S. Reddy, K. Reddy, N. Sarma, S. Kaleemulla, S. Uthanna, P.S. Reddy, Effect of sputtering power on the physical properties of dc magnetron sputtered copper oxide thin films, Mater. Chem. Phys 110 (2008) 397–401, https://doi.org/10.1016/j.matchemphys.2008.02.031.
[16] X. Hu, F. Gao, Y. Xiang, H. Wu, X. Zheng, J. Jiang, J. Li, H. Yang, S. Liu, Influence of oxygen pressure on the structural and electrical properties of CuO thin films prepared by pulsed laser deposition, Mater. Lett 176 (2016) 282–284, https://doi.org/10.1016/j.matlet.2016.04.055.
[17] K. Osako, K. Matsuzaki, H. Hosono, G. Yin, D. Atarashi, E. Sakai, T. Susaki, M. Miyauchi, Examination of interfacial charge transfer in photocatalysis using patterned CuO thin film deposited on TiO_2, APL Mater 3 (2015) 104409, , https://doi.org/10.1063/1.4926934.
[18] D. Barreca, E. Comini, A. Gasparotto, C. Maccato, C. Sada, G. Sberveglieri, E. Tondello, Chemical vapor deposition of copper oxide films and entangled quasi-1D nanoarchitectures as innovative gas sensors, Sensors Actuat. B: Chem 141 (2009) 270–275, https://doi.org/10.1016/j.snb.2009.05.038.
[19] T. Maruyama, Copper oxide thin films prepared by chemical vapor deposition from copper dipivaloylmethanate, Sol. Energ. Mater. Sol. C 56 (1998) 85–92, https://doi.org/10.1016/S0927-0248(98)00128-7.
[20] X. Jiang, T. Herricks, Y. Xia, CuO nanowires can be synthesized by heating copper substrates in air, Nano Lett 2 (2002) 1333–1338, https://doi.org/10.1021/nl0257519.
[21] D. Tahir, S. Tougaard, Electronic and optical properties of Cu, CuO and Cu_2O studied by electron spectroscopy, J. Phys.: Condens. Mat. 24 (2012) 175002, , https://doi.org/10.1088/0953-8984/24/17/175002.
[22] Y. Lim, C.S. Chua, C.J.J. Lee, D. Chi, Sol–gel deposited Cu_2O and CuO thin films for photocatalytic water splitting, Phys. Chem. Chem. Phys 16 (2014) 25928–25934, https://doi.org/10.1039/C4CP03241A.
[23] H.Q. Nguyen, D. Van Nguyen, A. Fujiwara, B.N.Q. Trinh, Solution-processed CuO thin films with various Cu^{2+} ion concentrations, Thin Solid Films 660 (2018) 819–823, https://doi.org/10.1016/j.tsf.2018.03.036.
[24] W. Li, W. Yu, Y. Jiang, C. Jing, J. Zhu, M. Zhu, Z. Hu, X. Tang, J. Chu, optical Structure, and room-temperature ferromagnetic properties of pure and transition-metal-(Cr, Mn, and Ni)-doped ZnO nanocrystalline films grown by the sol− gel method, J. Phys. Chem. C 114 (2010) 11951–11957, https://doi.org/10.1021/jp103183v.
[25] A. Liu, S. Nie, G. Liu, H. Zhu, C. Zhu, B. Shin, E. Fortunato, R. Martins, F. Shan, In situ one-step synthesis of p-type copper oxide for low-temperature, solution-processed thin-film transistors, J. Phys. Chem. C 5 (2017) 2524–2530, https://doi.org/10.1039/C7TC00574A.
[26] J. Yu, G. Liu, A. Liu, Y. Meng, B. Shin, F. Shan, Solution-processed p-type copper oxide thin-film transistors fabricated by using a one-step vacuum annealing technique, J. Phys. Chem. C 3 (2015) 9509–9513, https://doi.org/10.1039/C5TC02384J.
[27] M. Dhaouadi, M. Jlassi, I. Sta, I.B. Miled, G. Mousdis, M. Kompitsas, W. Dimassi, Physical Properties of Copper Oxide Thin Films Prepared by Sol–Gel Spin–Coating Method, America Journal of Physics and Applications 6 (2018) 43–50, https://doi.org/10.11648/j.ajpa.20180602.13.
[28] Y. Zhao, J. Zhang, Microstrain and grain-size analysis from diffraction peak width and graphical derivation of high-pressure thermomechanics, J, Appl. Crystallogr. 41 (2008) 1095–1108, https://doi.org/10.1107/S0021889808031762.
[29] F. Szekely, I. Groma, J. Lendvai, Characterization of self-similar dislocation structures by X-ray diffraction, Mater. Sci. Eng.: A 324 (2002) 179–182, https://doi.org/10.1103/PhysRevB.62.3093.
[30] A. Begum, A. Hussain, A. Rahman, Effect of deposition temperature on the structural and optical properties of chemically prepared nanocrystalline lead selenide thin films, Beilstein J. Nanotech 3 (2012) 438–443, https://doi.org/10.3762/bjnano.3.50.
[31] I. Singh, R. Bedi, Studies and correlation among the structural, electrical and gas response properties of aerosol spray deposited self assembled nanocrystalline CuO, Appl. Surf. Sci 257 (2011) 7592–7599, https://doi.org/10.1016/j.apsusc.2011.03.133.
[32] H Zare Asl, S. Mohammad Rozati, Spray deposited nanostructured CuO thin films: influence of substrate temperature and annealing process, Mater. Res 21 (2018) e20170754, , https://doi.org/10.1590/1980-5373-MR-2017-0754.
[33] E. Casassas, R. Tauler, Spectrophotometric study of complex formation in copper (II) mono-, di-, and tri-ethanolamine systems, J. Chem. Soc. Dalton 4 (1989) 569–573, https://doi.org/10.1039/DT9890000569.
[34] D. Jundale, P. Joshi, S. Sen, V. Patil, Nanocrystalline CuO thin films: synthesis, microstructural and optoelectronic properties, J. Mater. Sci.: Mater. El. 23 (2012) 1492–1499, https://doi.org/10.1007/s10854-011-0616-2.
[35] T. Chtouki, S. Taboukhat, H. Kavak, A. Zawadzka, H. Erguig, B. Elidrissi, B. Sahraoui, Characterization and third harmonic generation calculations of undoped and doped spin-coated multilayered CuO thin films, J. Phys. Chem. Solids 124 (2019) 60–66, https://doi.org/10.1016/j.jpcs.2018.08.035.
[36] S. Shariffudin, S. Khalid, N. Sahat, M. Sarah, H. Hashim, Preparation and characterization of nanostructured CuO thin films using sol-gel dip coating, Proceedings of IOP Conference Series: Materials Science and Engineering 99 (2015) 012007, , https://doi.org/10.1088/1757-899X/99/1/012007.
[37] Y. Matsuoka, K. Uno, N. Takahashi, A. Maeda, N. Inami, E. Shikoh, Y. Yamamoto, H. Hori, A. Fujiwara, Intrinsic transport and contact resistance effect in C_{60} field-effect transistors, Appl. Phys. Lett 89 (2006) 173510, , https://doi.org/10.1063/1.2372596.
[38] A. Liu, G. Liu, H. Zhu, H. Song, B. Shin, E. Fortunato, R. Martins, F. Shan, Water-induced scandium oxide dielectric for low-operating voltage n-and p-type metal-oxide thin-film transistors, Adv. Funct. Mater 25 (2015) 7180–7188, https://doi.org/10.1002/adfm.201502612.
[39] K.C. Sanala, L.S. Vikasa, M.K. Jayaraj, Room temperature deposited transparent p-channel CuO thin film transistors, Appl. Surf. Sci. 297 (2014) 153–157, https://doi.org/10.1016/j.apsusc.2014.01.109.
[40] X. Zou, G. Fang, L. Yuan, M. Li, G. Wenjie, X. Zhao, Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-κ HfON Gate Dielectric, IEEE Electron Device Lett 31 (2010) 827–829 doi: 0.1109/LED.2010.2050576.