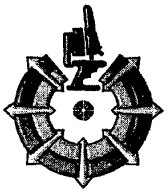

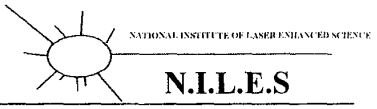

A GENERAL OVERVIEW OF SOLID STATES IMAGING SENSORS TYPES

by

S.Abdallah, B. Saleh, and A.K. Aboulsoud

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Abstract

There is a trend to replace thin film by Electronic Solid State image sensors in many application due to their outstanding performance and abilities in new fields of image capture applications such as digital still photography, video communications, as video conferencing cameras, and video phone. In addition to digital radiography, as medical radiography in which x-ray films are replaced. The results were superior. There is no need for film processing. It gives better resolution and the image can be restored digitally. The imaging system includes some essential and common elements, as an imaging lens, an image sensor, and a light source. The scope of this paper is to concentrate on two main types of the image sensor elements, namely the CCD's and the CMOS.

1. Introduction

The family of Electronic Solid State Image Sensors include about two main types and the rest is still under development. The market of image sensors witness a great competition between the eldest giant Charge Coupled Devices **(CCDs)** Image sensors and the new competitor Complementary Metal Oxide **(CMOS)** Image sensor. They are both implemented in silicon. Silicon properties dictate image sensor wavelength response and ultimate sensitivity. Fundamentally, CCDs and CMOS image sensors can have identical responses to light, since both depend on the absorption of light by silicon and the collection of photogenerated electrons (or holes). It is in the readout of these signals that the similarity ends. In addition to that there is a another powerful image sensor which is the Charge Injection Device **(CID)** introduced to the image sensor world yet used mainly in military applications due to its expensive costs in manufacture. Finally, there are two methods to illuminate the image sensor, the first is Front-illumination Technique , and the second is the Back-illuminated Technique. In which the last increases the efficiency of any image sensors in order of 99.99%.

2. Historical Background for image sensors

Before CMOS active pixel Sensors (APS's) and before CCD's, there were MOS image sensors. In the 1960's there were numerous groups working on solid-state image sensors with varying degrees of success using NMOS, PMOS, and bipolar processes. For example, in 1963, Morrison reported a structure, that is now referred to as computational sensor, that allowed determinations of a light spot's position using the photoconductivity effect. In 1966, Westinghouse reported a 50 × 50 element monolithic array of phototransistors. All of these sensors had an output signal proportional to the instantaneous local incident light intensity and did not perform any intentional integration of the optical signal. As a consequence, the sensitivity of these devices was low and they required gain within the pixel to enhance their performance. In 1967, Weckler at Fairchild suggested operating p-n junctions in a photon flux integration mode. The photocurrent from the junction is integrated on a reverse-biased p-n junction capacitance. Readout of the integrated charge using PMOS switch was suggested. The signal charge, appearing as a current pulse, could be converted to a voltage pulse using a series resistor. A 100 × 100 element array of photodiodes was reported in 1968. Weckler latter called the device Reticon

* *Faculty of Engineering-Arab Academy For Science & Technology, Alex-Egypt..*
** *Faculty of Engineering-University of Alexandria, Egypt.*

Also in 1967, RCA reported a thin-film transistor (TFT) solid-state image sensor using CdS/CdSe TFT's and photoconductors. More development have been further made but it was not until Fixed Pattern Noise (FPN) has been considered as the primary problem with MOS and CMOS image sensors. In 1970, when the CCD was first reported, its relative freedom from FPN was one of the major reasons for it to dominate other forms of Solid-State Image sensors.[5]

3. CCD's Background.

Like many technologies, the Charge-Coupled Device (CCD) started out as one kind of creature and wound up as something completely different. Imagine 30 years of development that was not meant for it to be as CCD was actually born for the wrong reason. The story started in the 1960s were computers needed an efficient way to store data, and at that time inexpensive mass-produced memory they needed to operate did not yet exist. Instead there were lots of strange and unusual ways being explored to store data while it was being manipulated. However at that time the most commonly used technology was the Bubble Memory. And it was not until the year 1969 when the researchers at Bell Labs (where Bubble Memory had been invented) then came up with the CCD, which was initially conceived of as a new type of computer memory circuit. Two Bell Labs scientists, Willard Boyle and George Smith, "started batting ideas around," in Smith's words, "and invented charge-coupled devices in an hour. Yes, it was unusual—like a light bulb going on." Since then, that "light bulb" has reached far and wide. Briefly speaking the journey for the CCD then continued as follows [9][6]:

- In 1974, the first imaging CCD was produced by Fairchild Electronics with a format of 100x100 pixels. *(i.e., first astronomical image)*
- In 1975, the first CCD TV cameras were ready for use in commercial broadcasts.
- In 1975, the first CCD flatbed scanner was introduced by Kurzweil Computer Products using the first CCD integrated chip, a 500 sensor linear array from Fairchild.
- In the 80's it slowly started replacing the photomultipliers, and photographic plates especially in the year 1982, the first solid state camera was introduced for video-laparoscopy.
- Nowadays, CCDs larger than **2048 x 2048** are currently under development , Pixels can now be made as small as 5 microns, Charge Transfer Efficiency **(CTE)** of 99.99 % are now possible *(although not common)*. In addition, Back-side illumination and various coatings have made 90% Quantum efficiency **(QE)** *(over a limited wavelength range)* possible ,and Amateur grade CCDs are now available for ~ **$500.** See figure(1). [9][10]

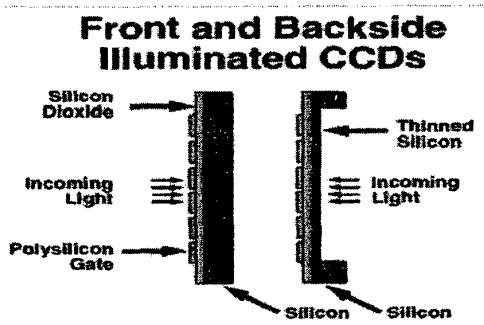


Fig 1. *Front and Backside illuminated Methods for a CCD Imager.* [2]

3.a.i. CCD's Image Sensor Fundamentals

Obviously from those previously mentioned facts the CCD early promise as a memory element has since disappeared. However, it has many potential applications, including signal processing and imaging. Its superb ability to detect light has turned it into a very important image sensor device, in the industry-standard image sensor technology, as a result of the silicon's light

sensitivity, which responds to wavelengths <1.1 mm, keeping in mind the visible spectrum falls between 0.4 mm and 0.7 mm. Like integrated circuits (IC), CCD's begin on thin wafers of silicon which are processed with a series of elaborate steps which define the various functions within the circuit. On each wafer lies several identical devices **(die),** each capable of yielding a functional device. Selected die, based on a variety of preliminary screening tests, are then cut from the wafer and packaged into a carrier for use in a system. A CCD allows individual charge packets to be transferred over a physical distance while maintaining the original charge packet integrity. Charge coupled devices are ideally suited for use in solid state imagers as a means of transferring integrated photogenerated charge. The CCD may be used to collect the photogenerated charge, or it may be placed adjacent to a array of photodiodes or photocapacitors. A CCD used to directly collect photogenerated charge will have reduced photoresponse at shorter optical wavelengths due to the presence of polysilicon electrodes. As Shown in figure(2). [1][2].

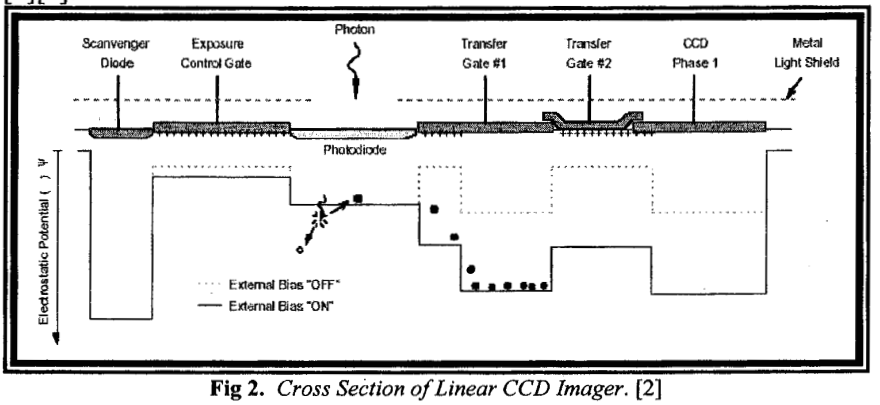


Fig 2. *Cross Section of Linear CCD Imager.* [2]

Three approaches to rapidly moving the charge under a light shield exist. The first, frame transfer (FT), shifts the entire CCD image vertically, in a column-parallel way. FT CCDs have large smears because the entire image takes a millisecond to be transferred. The second, is Interline Transfer (ILT) as figure(3). It has a fill factor of roughly 20% or less but can be improved over two times with microlenses, and still has some residual smear due to light leaking under the light shield. Finally, there is frame interline transfer (FIT), a combination of both FT and ILT approaches, representing a sort of one-two punch to reduce smear.

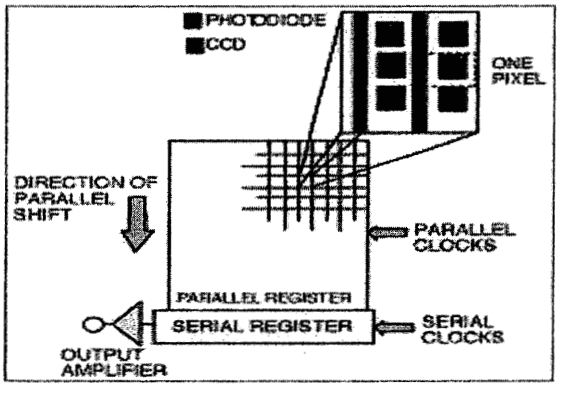


Fig 3. *In an interline CCD, each pixel is composed of a photodiode and an associated light-shielded CCD. After exposure, the charges in each photodiode are immediately transferred to the adjacent CCD, where the readout process is conducted. Frame rates increase because the transfer rate is even faster than a frame-transfer device. [4]*

The unique CCD fabrication process precludes cost-efficient integration of on-chip ancillary circuits such as timing generators, clock drivers, signal processors, and analog-to-digital converters (ADCs), so that implementation of a CCD-based camera system requires an actual set of chips. This increases system power and retards miniaturization of cameras. Due to the shift-

style readout of the CCD shows lower resolution readout without risking charge overflow. Despite these functional limitations, CCDs have achieved an extraordinarily high level of performance with low readout noise, high dynamic range, and excellent responsively. See figure(4).

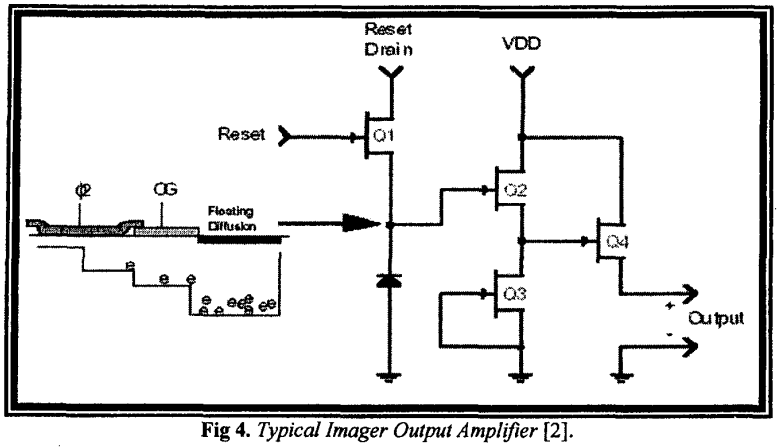


Fig 4. *Typical Imager Output Amplifier* [2].

4. CMOS Image Sensor Background

CMOS are a second-generation solid-state imaging technology [3]. It has been illustrated before that image sensors are manufactured in wafer foundries or fabs. Where the tiny circuits and devices are etched onto silicon chips. However, the biggest problem with CCDs for example, is that there isn't enough economy of scale as we have mentioned previously. They are created in foundries using specialized and expensive processes that can only be used to make CCDs. " Meanwhile, more and larger foundries across the world are using a different process called Complementary Metal Oxide Semiconductor **(CMOS)** to make millions of chips for computer processors and memory. Thus we can say that CMOS refers to how a sensor is manufactured, and not to a specific sensor technology This is by far the most common and highest yielding process in the world " [5]. " Vendors of CMOS sensors also benefit from the large investments which are made continually to improve the quality and capacity of CMOS foundries." [4]. See figure(5)

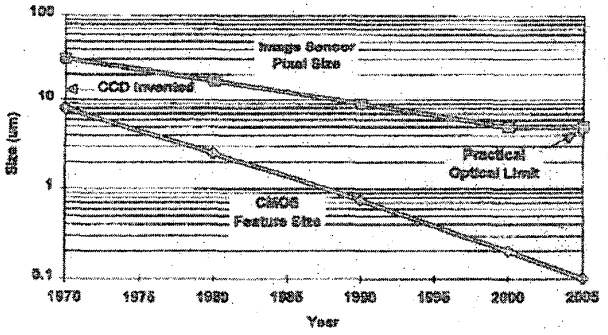


Fig 5. *Steadily increasing Ratio between Image sensor pixel size and minimum feature size permits the use of CMOS circuitry within each pixel.* [8]

They sense light in the same way as CCD, but from the point of sensing onwards everything is different. The charge packets are not transferred, but they are instead detected as early as possible by charge sensing amplifier, which are made from CMOS transistors. [4]

4.a. CMOS Image Sensor general Architecture

The general architecture of a CMOS image sensor is shown in figure(6). The image sensor consists of an array of pixels that are typically selected a row at a time by row select logic This can be either a shift register or a decoder. The pixels are read out vertical column busses that

connect the selected row of pixels to a bank of analog signal processors (APSs). These APSs perform functions such as **charge integration, sample and hold, Correlated Double Sampling technique (CDS)** and **FPN suppression.**

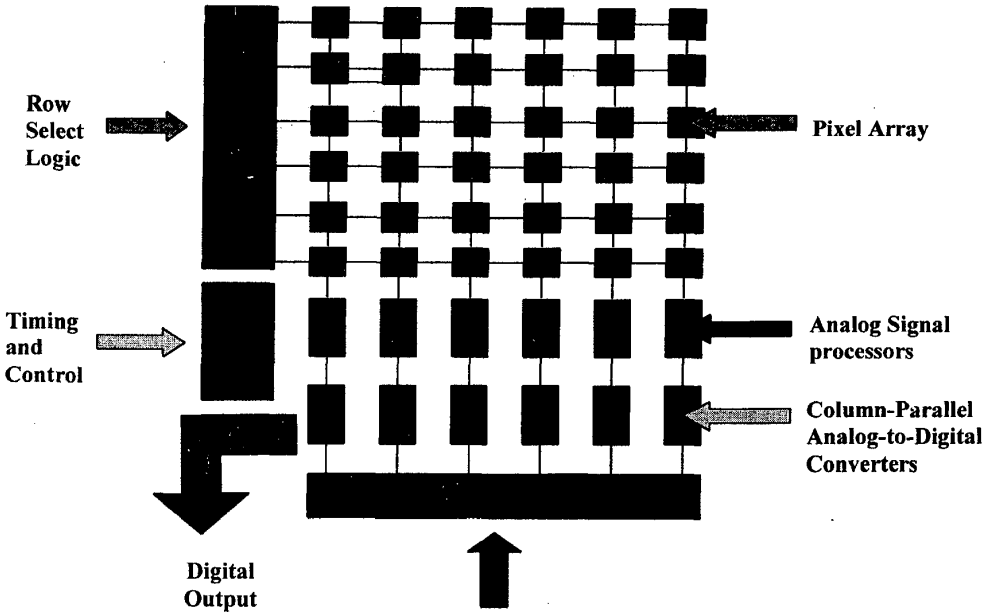


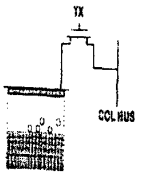
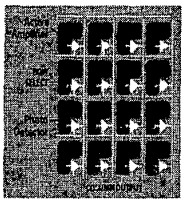
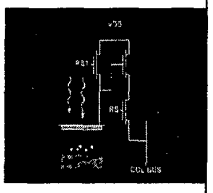
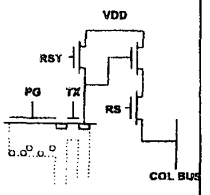
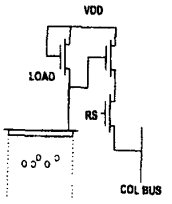
Fig 6. *CMOS APS integrates timing and control, ADC and other circuitry on the same chip.*[3]

More advanced CMOS image sensors contain analog-to-digital converters (ADC) . In Figure(6), the ADCs are shown as column-parallel ADCs; that is each column of pixels has its own ADC. The digital output of the ADCs or analog output of the APSs are selected for readout by column select logic that can be either a shift register or decoder. Also integrated on-chip is a timing and control logic block is readily defined at a high level using tools such as VHDL and inserted on-chip.

The CMOS image sensor architecture of Figure(6) permits several modes of image readout. Progressive-scan readout of the entire array is the common readout mode. A window readout mode readily implemented where only a smaller region of pixels is selected for read out. This increases access rates to windows of interest. A skip mode is also possible where every second (or third, etc.) pixel is readout. This mode allows for subsampling of the image to increase readout speed at the cost of resolution. Combination of skip and window mode allows electronic pan, tilt and zoom to be implemented. [3]

4.b. CMOS Image Sensor Types.

We can classify CMOS Image Sensors according to their Pixel Circuit Structures. Thus there are two main types. They are named the passive pixel image sensors **(PPSs),** and the active pixel sensors **(APSs),** in which the later includes an active amplifier. There are three predominant approaches to pixel implementation in CMOS: photodiode-type passive pixel, photodiode-type active pixel, and photogate-type active pixel. . Each has various advantages and disadvantages with respect to sensitivity, noise, pixel size, and linearity, and the choice often depends on the application. These are discussed below.[4][8].

Points of comparison	Passive Pixel (PPS)	Active Pixel (APS)	Photodiode-Type APS	Photogate-Type APS	Logarithmic Pixels
Circuit Schematic Structure					
Approach	• *It* consists of a photodiode and a pass (access) transistor • When the access transistor is activated, the photodiode is connected to a vertical column bus. • A charge integrating amplifier **(CIA)** readout circuit at the bottom of the column bus keeps the voltage on the column bus constant *and* reduces **kTC** noise • When the photodiode is accessed, the voltage on the photodiode is reset to the column bus voltage, and the charge, proportional to the photosignal, is converted to a voltage by the CIA. • In below figure notice the Potential well, and Transfer gate (TX).	• A sensor with an active amplifier within each pixel is referred to as an active pixel sensor or APS, and each amplifier is only activated during readout. • Power dissipation is minimal and is generally less than a CCD. Typically providing a charge gain between the photodetector, and an analog signal processor at the bottom of each column. • Moreover, they contain at least three transistors per pixel. • The in-pixel amplifier (transistor) is typically implemented as a single source follower because of simplicity and excellent gain uniformity. • Circuitry at each pixel determines what its noise level is and cancels it out. • Sampling of the pixel output occurs twice, once after the readout node resets, and the second sample after the signal is transferred to the readout node ***(i.e., after integrating the signal charge).***	• It is an improved sensor that uses a transfer gate between the photodiode and the source follower gate. • The transfer gate keeps the photodiode at constant potential and increases output conversion gain by reducing capacitance but introduces lag. • It permits random access and electronic shuttering with a significant increase in pixel size. • There is no overlying polysilicon. • APS uses three transistors per pixel and has a typical pixel pitch of 15x the minimum feature size. • In below figure notice RS-row select, and RST reset for the transistor.	• Signal charge is integrated under a photogate. • For Readout, an output floating diffusion is reset and its resultant voltage measured by the source follower. • The charge is then transferred to the output diffusion by pulsing the photogate. • The new voltage is then sensed after applying a CDS • The photogate and transfer gate ideally overlap using a double poly process. • However, the insertion of a bridging diffusion between PG and TX has minimal effect on circuit performance and permits the use of single poly processes. *(Approx. $100e^{UU}$ of lag resulted)* • Variable integration time and window of interest readout is commanded asynchronously. • It uses five transistors per pixel and has a pitch typically equal to 20x the minimum feature size. • The floating diffusion capacitance is typically of the order of 10 fF yielding a conversion gain of 10-20 $\mu V/e^-$	• Uses logarithmic transformation, where the output signal from the pixel is proportional to the logarithm of the photosignal. • The photodiode voltage self-adjusts to a level such that load transistor current is equal to the photocurrent collected by the photodiode. This results in a logarithmic transformation of the photosignal for typical light levels and wide intrascene dynamic range. • It permits true random access in both space and time since it is a non-integrating pixel.

Points of comparison	Passive Pixel (PPS)	Active Pixel (APS)	Photodiode-Type APS	Photogate-Type APS	Logarithmic Pixels
Advantages	• It allows the highest design fill factor for a given pixel size or the smallest pixel size for a given design fill factor for a particular CMOS process. • When adding a second selection transistor it permits a true *X-Y* addressing. Similar to analog **DRAMs** operation. • Its quantum efficiency can be quite high due to the large fill factor and absence of an overlaying layer of polysilicon such as that found in many CCD's.	• Its main advantage is that it can reduce the noise associated with PPSs. • They trade pixel fill factor (e.g., 20-30%, similar to ILT CCDs),for improved performance compared to PPSs. Thus an effective improvement in sensitivity using microlense may be two-fold. • Loss in optical signal is more than compensated by reduction in read noise for a net increase in signal-to-noise (S/N) ratio and dynamic range. • The pixel pitch is typically between 10-20 times minimum. feature size *L*. • They have recorded noise as low as 5 electrons rms, readout speeds of 8,000 frames per second, and arrays as large as 2,000 x 2,000 elements (i.e., large-format megapixel arrays. • Their performance is comparable to many forms of CCDs	• Improved FPN using a feedback technique. • Increase in pixel size. • High quantum efficiency • They are suitable for most mid to low-performance applications. • The output signal remains constant for the same optical flux, to first order, since a decrease in detector area is compensated by an increase in conversion gain. • A tradeoff can be made in designed pixel fill-factor (photodiode area), dynamic range (full well) and conversion gain ($\mu V/e^-$). • Lateral carrier collection permits high responsively even for small fill-factor at the possible expense of pixel-to-pixel crosstalk.	• CDS sampling process suppresses reset noise, 1/f noise, and FPN due to threshold voltage variations. • Subsequent circuit noise is of the order of 150-250 μV r.m.s., resulting in a readout noise of 10-20 electrons r.m.s., with the lowest noise reported to date of 5 electrons r.m.s.	• Ability to cover over six order of magnitude in incident light level, • It operates in a non-integrating current mode with logarithmic response. • FPN is corrected by means of hot-carrier-induced threshold voltage shift.
Dis-advantages	• Its readout noise level appearing as a background pattern in the image, arises after a charge collected by the pixel flows out into a column readout wire. Due to large capacitance column wire collects a small amount of charge, noise becomes a critical factor. *(e.g., the readout noise with a PPS falls typically in the range of 250 electrons rms, which can be compared to commercial CCDs that achieve less than 20 electrons rms of*	• They are susceptible to residual FPN and has less maturity than CCD's. Thus the idea of using Sampled twice known as **Correlated Double Sampling (CDS)** to remove fixed-pattern noise and correlated temporal noise, was applied . • In a spatially varying dc offset leads to a fixed pattern in the image, referred to as **Fixed-Pattern Noise**	• Its S/N performance decreases for smaller pixel sizes since the reset voltage noise scales as $1/C^{1/2}$, where C is the photodiode capacitance.	• Read noise for the photogate pixel is offset by a reduction in quantum efficiency, particularly in the blue, due to overlying polysilicon.	It has a small S/N ratio 45 dB due to temporal noise and small voltage swings. Drawbacks to this non-integrating approach include slow response time for low light levels, large FPN (e.g., 60 mV).

Points of comparison	Passive Pixel (PPS)	Active Pixel (APS)	Photodiode-Type APS	Photogate-Type APS	Logarithmic Pixels
[cont..] Dis-advantages	*read noise).* To cancel out this noise, sensors often use additional processing steps. As for scalability noise, it also does not scale well to larger array sizes and/or faster pixel readout rates. This is because both increased bus capacitance and faster readout speeds result in higher readout noise	(FPN). Depending on its source, FPN can lead to unacceptable image artifacts such as stripes. Usually they have lower noise but poorer packing density than passive pixel CMOS. Thus inexpensive CMOS chips are being used in low-end digital cameras.	----------	----------	----------

Table 1. Various Types of Pixel Circuitry architectures in CMOS image sensors.

- **Other Pixels**

  Finally, The pinned photodiode, developed for interline transfer CCD's, features high quantum efficiency (especially in the blue), low dark current, and low noise readout. The pinned photodiode has been combined with CMOS APS readout by JPL/Kodak to achieve high-performance pixel response. A photogate CMOS APS with a floating-gate sense amplifier that allows multiple nondestructive, doubly sampled reads of the same signal was developed by JPL for use with oversampled column-parallel ADC's. A floating gate sensor with a simple structure was reported by JPL/Olympus. This sensor used a floating gate to collect and sense the photosignal and features a compact pixel layout with complete reset. There has been significant work on retina-like CMOS sensors with nonlinear, adaptive response, While their utility for the electronic image capture has not yet been demonstrated, their very large dynamic range and similarity to the response of the human eye offer intriguing possibilities for on-chip intelligent imaging.

5.CMOS Eclipsing CCD 's.

CMOS can be used for image sensors in a rapidly expanding sphere of applications .Several important factors have contributed to the emergence of CMOS image sensors at this time rather than 10 to 20 years ago. The primary factor consists of recent demand for portable, low-power, miniaturized digital imaging systems. A second important factor is that present-day CMOS offers submicron feature sizes and low defect and contamination levels, permitting cost-effective pixel sizes and low junction leakage (or *dark*) current. In addition, threshold voltage control and uniformity is stable and reproducible. The third important factor, new circuit techniques that have been invented or adopted from CCD signal processing, permits both low noise and high dynamic-range imaging that is competitive with the best CCDs. This includes the development of active pixel sensor technology and column-parallel, signal-processing circuits for temporal and fixed-pattern noise reduction.

6. Conclusion

Thus it seems it is a tough competition for any competitor such as CMOS or CIDs. As they must achieve similar levels of performance to displace CCD technology, or have other overwhelming advantages such as very low power or new functions. Yet the CMOS is going ahead very strongly and might be able to dominate the market of the Imaging Sensors.

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