UNIVERSITY of SOUTH FLORIDA

Hardware Accelerators for Machine Learning Department Of Computer Science and Engineering

Course Instructor: Dr.Dayane A.Reis

Project Title

Accelerating Kernel SVM-based Pedestrian Detection with FPGA-GPU Architecture

FPGA(TEAM A)

Mythreye Pasula (U88527486)

Yaswanth Sai Ram Pavan Jami (U22367338)

Chaitanya Sai Dangeti (U77695453)

Vineeth Reddy Betham (U36652271)

GPU(TEAM B)

Sree Vardhani Iragavarapu (U13255029)

Lakshmi Venkata Chaitanya Raju Gedela(U42289643)

Kumar Ganesh Chowdary Naidu(U05647359)

Akshay Reddy Sudini(U44174638)

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Literature Review

When it comes to human detection, it is an innately complex problem as there is a variability in the appearance for example body articulation, clothing, occlusions and also environmental conditions. Also it is an important part of many applications such as surveillance, robotics and autonomous vehicles. In fact, a number of techniques pertaining to system architecture, image descriptors, and classification systems have been proposed in this field throughout the past ten years. among which are Afifi et al., (2015) and Berberich & Doll, (2014). Appearance-based approaches are more promising, according to recent comparison research like the one done by Kyrkou et al. (2018). The best descriptors for classification performance, according to empirical study, are histograms of oriented gradients (HOG) descriptors. To prove this, Zhou et al. (2015) benchmarked sliding-window based pedestrian detectors, whereas Wasala & Kryjak (2022) compared appearance-based algorithms with their shape-texture recognition system. HOG performs better than other features in the majority of ADAS-related circumstances, according to both author groups' conclusions and results from their research. Additionally, Weimer et al. (2011) states that fundamental descriptor elicits minimal computing costs as compared to other features surveyed in the benchmarks. Various hardware accelerated HOG implementations have been developed in response to real-time requirements.

Support Vector Machines (SVMs) for HOG Classification

Berberich & Doll (2014) suggest support vector machines as a classifier for HOG classification. Their research demonstrates that, at the expense of a somewhat longer run time, the performance of a Gaussian kernel SVM outperforms a linear one. Because of this, authors who have suggested real-time HOG detection systems have opted for other classifiers

like AdaBoost or linear SVMs on FPGA or GPU hardware. Nevertheless, an early rejection by one of the weak classifiers is often followed by a reduction in classification performance. Intersection kernel support vector machines (SVMs) have been shown to outperform linear SVMs in terms of classification performance at the same order of computational cost when assessing the similarity between the histograms describing the features (Maggiani et al., 2018). It is usually assumed that real-world application requirements can only be satisfied by a combination of complimentary sensors. The best results can be achieved by combining the best characteristics and classifier with the best sensors available.

Combining FPGA and GPU for Pedestrian Detection (Proposed Research)

In this section, the research outlines the development and key components of a real-time pedestrian identification system leveraging a multisensor platform.

Multisensor Integration for Pedestrian Detection

The system utilizes far-infrared and visible light sensors, strategically combined to enhance pedestrian identification accuracy, particularly at junctions.

SVM-Based Pedestrian Detection

A Support Vector Machine (SVM) classifier, in conjunction with the Histograms of Oriented Gradients (HOG) descriptor, is employed for detecting potential pedestrians in the given environment.

Gaussian Kernel SVM for Enhanced Performance

The focus of the study is on the implementation of a Gaussian kernel SVM, emphasizing its ability to provide high classification accuracy and adaptability with various descriptor types. This choice deviates from earlier systems that heavily relied on hardware acceleration.

Hardware Architecture: GPU and FPGA Integration

The system's hardware architecture is designed to seamlessly combine Graphics Processing Unit (GPU) and Field-Programmable Gate Array (FPGA) technologies. This integration aims to deliver accelerated processing speed without compromising the accuracy of pedestrian detection.

Parallel Hardware Architecture for Real-Time Processing

These parts are set up in a pipeline: the CPU controls overall processing, the GPU does classification, the FPGA handles feature extraction, and so on. With this configuration, real-time processing is possible without sacrificing good classification performance. We anticipate that this system design, based on parallel hardware architectures, can be extended beyond pedestrian detection to other computer vision and pattern recognition tasks. Researchers can select the right hardware and implementation method based on the particular task. Our framework is perfect for rapid prototyping and for academics who are new to embedded computer vision, since all the components are common PC hardware and software tools are accessible for FPGA design.

References

Afifi, S. M., GholamHosseini, H., & Poopak, S. (2015). Hardware implementations of SVM on FPGA: A state-of-the-art review of current practice.

Berberich, M., & Doll, K. (2014). Highly flexible FPGA-architecture of a support vector machine. In *MPC workshop* (pp. 25-32).

Kyrkou, C., Theocharides, T., Bouganis, C. S., & Polycarpou, M. (2018). Boosting the hardware-efficiency of cascade support vector machines for embedded classification

applications. *International Journal of parallel programming*, *46*(6), 1220-1246.

Maggiani, L., Bourrasset, C., Quinton, J. C., Berry, F., & Sérot, J. (2018). Bio-inspired heterogeneous architecture for real-time pedestrian detection applications. *Journal of Real-Time Image Processing*, *14*, 535-548.

Weimer, D., Köhler, S., Hellert, C., Doll, K., Brunsmann, U., & Krzikalla, R. (2011, June). Gpu architecture for stationary multisensor pedestrian detection at smart intersections. In *2011 IEEE Intelligent Vehicles Symposium (IV)* (pp. 89-94). IEEE.

Wasala, M., & Kryjak, T. (2022, June). Real-time HOG+ SVM based object detection using SoC FPGA for a UHD video stream. In *2022 11th Mediterranean Conference on Embedded Computing (MECO)* (pp. 1-6). IEEE.

Zhou, Y., Chen, Z., & Huang, X. (2015, May). A pipeline architecture for traffic sign classification on an FPGA. In *2015 IEEE international symposium on circuits and systems (ISCAS)* (pp. 950-953). IEEE.