Design Compiler Tutorial

This is a simple tutorial for getting the text based Design Compiler (DC) running on the Linux ECI computers. Before you do anything check what shell you are using by running, `echo $SHELL`.

Cshell

Edit your .cshrc file to contain the following license and path information. Make sure that you save the .cshrc file and run "source .cshrc" to load the new path and license.

You must have the following two lines in your .cshrc file:

```
setenv LM_LICENSE_FILE 1717@license.ece.ucsb.edu:1781@license.ece.ucsb.edu
set path = (/ece/synopsys/synthesis/bin/ $path)
```

Here is a complete .cshrc file in case you are totally lost:

```
if (-f /eci/share/skel/.cshrc_sys) then
    source /eci/share/skel/.cshrc_sys
endif
# Add your personal configurations after this line.

set path = (/ece/mentor/modeltech/bin $path)
setenv LM_LICENSE_FILE 1717@license.ece.ucsb.edu:1781@license.ece.ucsb.edu
set path = (/ece/mentor/modelsim_6.2/modeltech/linux $path)
set path = (/ece/synopsys/synthesis/bin/ $path)
```

Bash

Edit your .bashrc file to contain the following license and path information. Make sure that you save the .bashrc file and run "source .bashrc" to load the new path and license.

You must have the following two lines in your .cshrc file:

```
export LM_LICENSE_FILE=1717@license.ece.ucsb.edu:1781@license.ece.ucsb.edu
PATH=$PATH:/ece/synopsys/synthesis/bin/
```

Here is an example .bashrc file in case you are totally lost:

```
if [ -f /etc/bashrc ]; then
        . /etc/bashrc
fi

# User specific aliases and functions
PATH=$PATH:/eci/bin:/ece/mentor/modeltech/bin:/ece/mentor/modelsim_6.2/modeltec
h/linux:/ece/synopsys/synthesis/bin/

PATH=$PATH:./:~/bin/

export LM_LICENSE_FILE=1717@license.ece.ucsb.edu:1781@license.ece.ucsb.edu
```

1. Now that you have the path and license information, create a folder where you will do your design compiler work. Eg. ~/HW5_DC/. Place your behavioral Verilog code in the ~/HW5_DC/

directory, as well as the “.synopsys_DC.setup” file (synopsys_dc.setup). **When you download synopsys_DC.setup make sure that it is saved with a leading dot (ie .synopsys_DC.setup). It should be a hidden file.** Navigate to ~/HW5_DC/ and launch the text based design compiler by typing the following command: `dc_shell`

If everything worked correctly you should see a welcome screen Initializing… and then get this prompt: `dc_shell>`

To exit the Design Compiler type: `exit`

2. From this point on you will need to execute a series of commands. How the commands are suppose to be issued, and in what order is going to be up to you to decide. You need to look at this PDF (http://cadlab.ece.ucsb.edu/ece156B_04/dctut.pdf) to determine how to issue these commands.

   Some of the commands you need are:
   ```
   compile
   read_file
   write
   ```
   Also research other commands to print output area summary and whatever else is asked for in the project description.

3. With the Design Compiler you should be able to generate the gate level netlist of your behavioral code. From there you will need to take your gate level code (generated by DC), and your behavioral code (that you created), use the “class.v” library and construct a miter to prove that the two circuits are equivalent using Modelsim.