SOC Design Report

Lab-3 Fir

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1.Design Overview

Key Specifications：

Taps: 11 coefficients (parameter Tape_Num).

Data Width: 32 bits for all interfaces.

BRAM Organization:

Coefficient BRAM: Base address 0xFF for 11 coefficients (4-byte aligned).

Data BRAM: Circular buffer with wrap-around at address 0x28 (10 samples).

2. Block Diagram

Key Components:

AXI-Lite Controller: Handles register reads/writes for coefficients, data length, and control signals (ap_start, ap_done, ap_idle).

AXI-Stream Flow Controller: Manages input/output data flow using tvalid and tready handshakes.

BRAM Manager: Implements dual-port SRAM for coefficients (11x32b) and circular buffer for input data (10x32b).

FIR Core: Computes y[t] = Σ(h[i] * x[t-i]) using a single multiplier-accumulator (MAC) pipeline.

Control Signals：

Signal	**Function**	**Implementation**
ap_start	Start filter operation	Set via AXI-Lite write to 0x00[0], auto-cleared when operation starts
ap_done	Completion status	Set when last output sent, cleared by write-1-to-clear
ap_idle	Idle status indicator	High when reset or after ap_done, low during computation
tvalid	Data validity	Synchronized with BRAM read latency and MAC pipeline
tready	Flow control	Backpressure handling for input/output streams

3. Interface Description

AXI4-Lite Interface

Signals:

awready, wready, arready: Handshake signals for write/read channels.

awaddr, araddr: Address buses for write/read operations.

wdata, rdata: Data buses for write/read operations.

Register Map:

ADDR_AP_CTRL (0x00): Control register (start bit, idle/done status).
ADDR_datalength (0x10): Data length register.
ADDR_tapparameters (0xFF): Base address for coefficients.

AXI-Stream Interface

Slave Stream (Input):

ss_tvalid, ss_tdata, ss_tlast: Input data stream.
ss_tready: Asserted when the filter is ready to accept data.

Master Stream (Output):

sm_tvalid, sm_tdata, sm_tlast: Filtered output data stream.

BRAM Interfaces

Coefficient BRAM:

Write enable (tap_WE) triggered by AXI-Lite writes to 0xFF.
Read address (tap_A) selected based on read/write operations.

Data BRAM:

Circular buffer implementation with automatic address wrapping at 0x28.
Write enable (data_WE) controlled by stream input validity.

Core FIR Computation：Multiply-Accumulate (MAC) Engine

Pipeline Stages:

Coefficient Fetch: Read coefficient from tap_Do and data sample from data_Do.
Multiplication: Compute ymult = tap_Do * data_Do.
Accumulation: Update yout = ymult + yout.

State Machine:

Initial State: Load first coefficient and data sample.
Intermediate States: Iterate through all 11 taps.
Final State: Output result via sm_tdata and reset addresses.

```
// MAC operation for FIR computation
always @(posedge axis_clk) begin
    if (firstate) begin
        case (tapa)
            12'h00: begin
                ymult <= tap_Do * data_Do;
                yout <= ymult + yout;
                tapa <= tapa + 4;
            end
            // ...
            12'h28: begin
                ymult <= tap_Do * data_Do;
                yout <= ymult + yout;
                tapa <= 12'h00;
            end
        endcase
    end
end
```

4. Datapath

Data Input Flow:

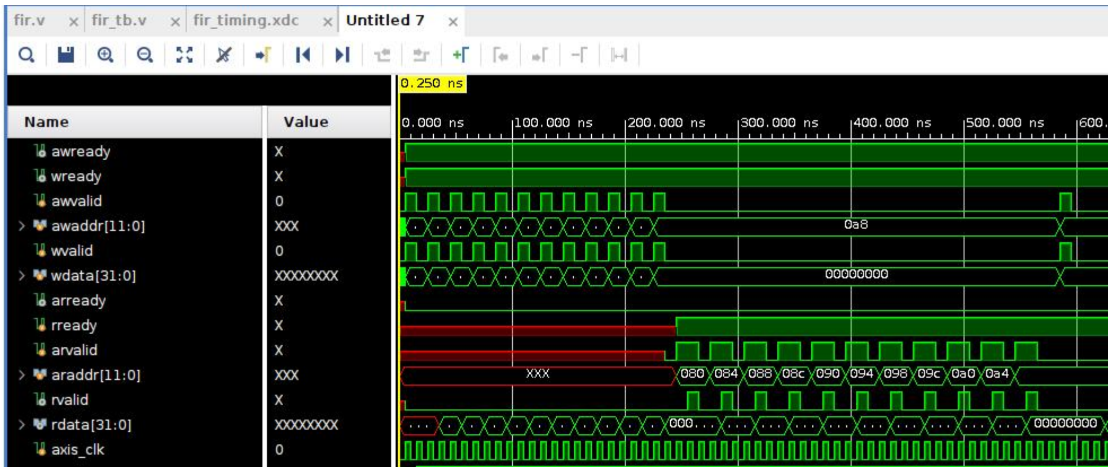
ss_tready deasserted during computation to prevent overflow.

AXI-Stream Slave receives data via ss_tdata

Data stored in circular buffer (Data BRAM)

Address wrapping at 0x28 (40 bytes = 10 samples)

```
always @(posedge axis_clk) begin
    ymult <= tap_Do * data_Do;
    yout <= ymult + yout;end
```



Computation Flow:

Parallel MAC operations with pipeline registers

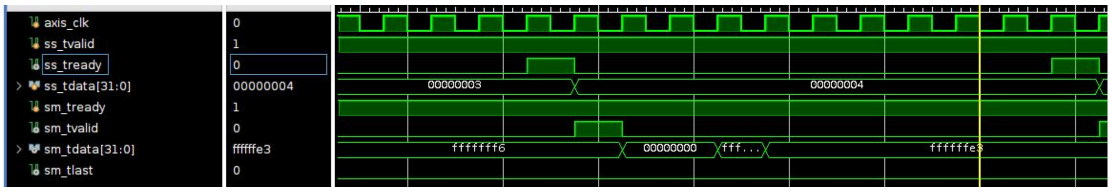
Coefficient addressing: 0x00-0x28 (11 taps)

Output Flow:

Results stored in yout register

AXI-Stream Master controls sm_tvalid/sm_tready handshake

tlast generation synchronized with data length



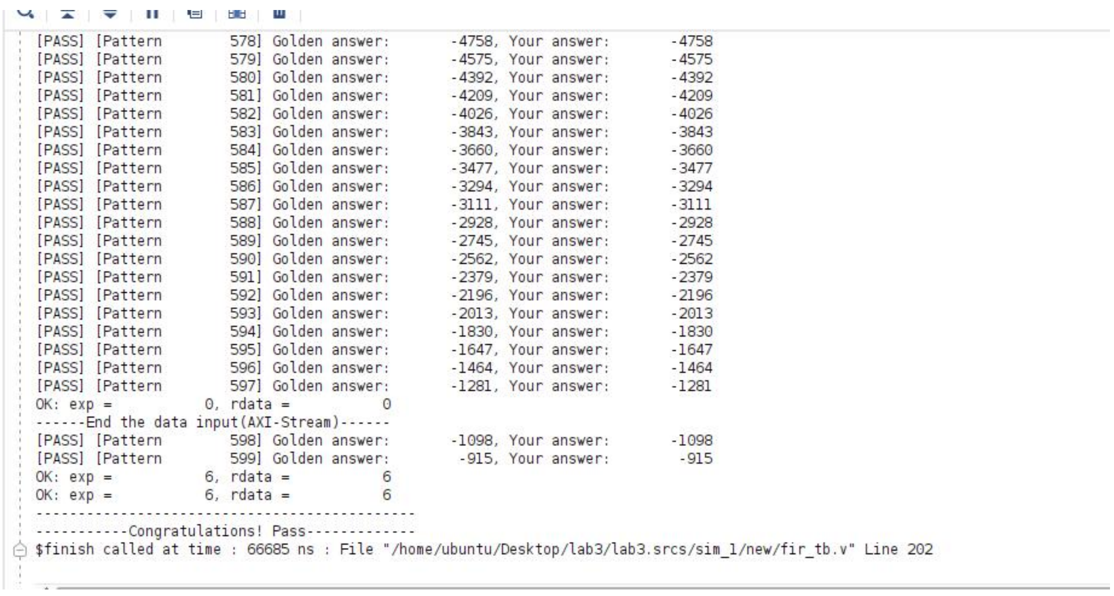
5. Simulation result

The verification used 600 input data points. The final checks validated the control register with masking.

AXI-Lite writes to ap_start and coefficient registers.

AXI-Stream data input with tlast assertion.

Output Yn matching golden reference.



```
[PASS] [Pattern       578] Golden answer:      -4758, Your answer:      -4758
[PASS] [Pattern       579] Golden answer:      -4575, Your answer:      -4575
[PASS] [Pattern       580] Golden answer:      -4392, Your answer:      -4392
[PASS] [Pattern       581] Golden answer:      -4209, Your answer:      -4209
[PASS] [Pattern       582] Golden answer:      -4026, Your answer:      -4026
[PASS] [Pattern       583] Golden answer:      -3843, Your answer:      -3843
[PASS] [Pattern       584] Golden answer:      -3660, Your answer:      -3660
[PASS] [Pattern       585] Golden answer:      -3477, Your answer:      -3477
[PASS] [Pattern       586] Golden answer:      -3294, Your answer:      -3294
[PASS] [Pattern       587] Golden answer:      -3111, Your answer:      -3111
[PASS] [Pattern       588] Golden answer:      -2928, Your answer:      -2928
[PASS] [Pattern       589] Golden answer:      -2745, Your answer:      -2745
[PASS] [Pattern       590] Golden answer:      -2562, Your answer:      -2562
[PASS] [Pattern       591] Golden answer:      -2379, Your answer:      -2379
[PASS] [Pattern       592] Golden answer:      -2196, Your answer:      -2196
[PASS] [Pattern       593] Golden answer:      -2013, Your answer:      -2013
[PASS] [Pattern       594] Golden answer:      -1830, Your answer:      -1830
[PASS] [Pattern       595] Golden answer:      -1647, Your answer:      -1647
[PASS] [Pattern       596] Golden answer:      -1464, Your answer:      -1464
[PASS] [Pattern       597] Golden answer:      -1281, Your answer:      -1281
OK: exp =          0, rdata =          0
------End the data input(AXI-Stream)------
[PASS] [Pattern       598] Golden answer:      -1098, Your answer:      -1098
[PASS] [Pattern       599] Golden answer:       -915, Your answer:       -915
OK: exp =          6, rdata =          6
OK: exp =          6, rdata =          6
-----------------------------------------------
----------Congratulations! Pass-------------
$finish called at time : 66685 ns : File "/home/ubuntu/Desktop/lab3/lab3.srcs/sim_1/new/fir_tb.v" Line 202
```

6.Implementation Challenges

AXI Protocol Compliance:

Strict timing requirements for signal assertions

Handshake synchronization between channels

Memory Timing:

BRAM read latency compensation

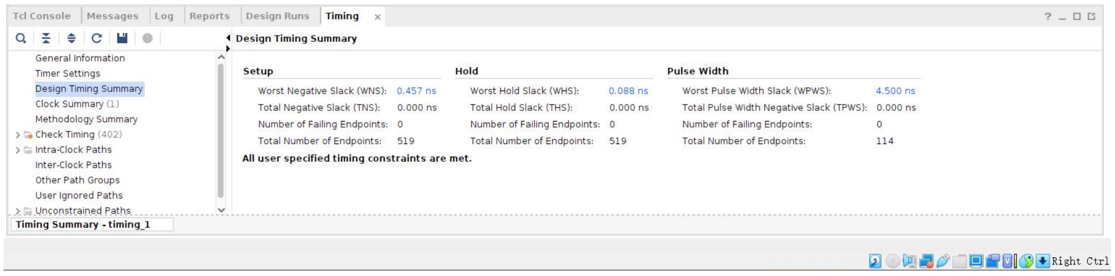
Address wrapping management

Concurrent Access Handling:

Arbitration between configuration and operation phases

Invalid access detection during computation

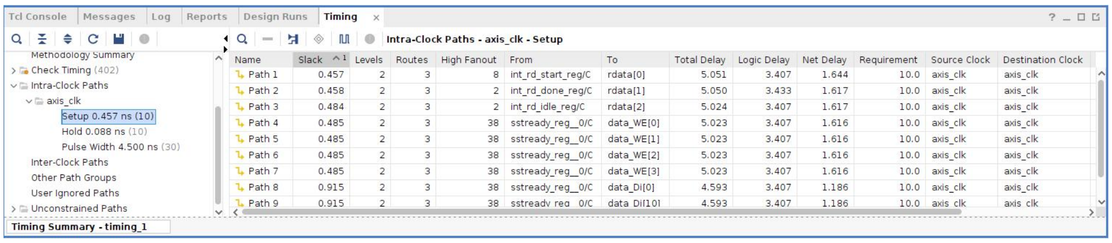
To further optimize the design's timing performance and scalability, I plan to enhance the pipeline architecture by increasing the number of pipeline stages. This improvement aims to reduce critical path delays and boost the maximum achievable clock frequency.



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.457 ns	Worst Hold Slack (WHS):	0.088 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	519	Total Number of Endpoints:	519	Total Number of Endpoints:	114

All user specified timing constraints are met.



Intra-Clock Paths - axis_clk - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	0.457	2	3	8	int_rd_start_reg/C	rdata[0]	5.051	3.407	1.644	10.0	axis_clk	axis_clk
Path 2	0.458	2	3	2	int_rd_done_reg/C	rdata[1]	5.050	3.433	1.617	10.0	axis_clk	axis_clk
Path 3	0.484	2	3	2	int_rd_idle_reg/C	rdata[2]	5.024	3.407	1.617	10.0	axis_clk	axis_clk
Path 4	0.485	2	3	38	sstready_reg__0/C	data_WE[0]	5.023	3.407	1.616	10.0	axis_clk	axis_clk
Path 5	0.485	2	3	38	sstready_reg__0/C	data_WE[1]	5.023	3.407	1.616	10.0	axis_clk	axis_clk
Path 6	0.485	2	3	38	sstready_reg__0/C	data_WE[2]	5.023	3.407	1.616	10.0	axis_clk	axis_clk
Path 7	0.485	2	3	38	sstready_reg__0/C	data_WE[3]	5.023	3.407	1.616	10.0	axis_clk	axis_clk
Path 8	0.915	2	3	38	sstready_reg__0/C	data_Di[0]	4.593	3.407	1.186	10.0	axis_clk	axis_clk
Path 9	0.915	2	3	38	sstready_reg__0/C	data_Di[10]	4.593	3.407	1.186	10.0	axis_clk	axis_clk