

CSM151B HW 5
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4.13.1

```
add r5,r2,r1
lw  r3,4(r5)
lw  r2,0(r2)
or   r3,r5,r3
sw  r3,0(r5)
```

Insert nops to ensure correct execution :

add	IF	ID	EX	ME	WB									
nop		IF	ID	EX	ME	WB								
nop			IF	ID	EX	ME	WB							
lw				IF	ID	EX	ME	WB						
lw					IF	ID	EX	ME	WB					
nop						IF	ID	EX	ME	WB				
or							IF	ID	EX	ME	WB			
nop								IF	ID	EX	ME	WB		
nop									IF	ID	EX	ME	WB	
sw										IF	ID	EX	ME	WB

4.14.1

```
lw r2,0(r1)
label1: beq r2,r0,label2 # not taken once, then taken
lw r3,0(r2)
beq r3,r0,label1 # taken
add r1,r3,r1
label2: sw r1,0(r2)
```

Draw the pipeline execution diagram for this code, assuming there are no delay slots and that branches execute in the EX stage:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
I1	IF	ID	EX	ME	WB									
I2		IF	ID	*	EX	ME	WB							
I3			IF	*	ID	EX	ME	WB						
I4					IF	ID	*	EX	ME	WB				
I5								IF	ID	EX	ME	WB		
I6									IF	ID	EX	ME	WB	

For the code sequence in 4.13, how many cycles would it take to execute this code on the 5-stage pipelined data path with forwarding logic?

Ans: There will be 14 cycles.

add	IF	ID	EX	ME	WB									
nop		IF	ID	EX	ME	WB								
nop			IF	ID	EX	ME	WB							
lw				IF	ID	EX	ME	WB						
lw					IF	ID	EX	ME	WB					
nop						IF	ID	EX	ME	WB				
or							IF	ID	EX	ME	WB			
nop								IF	ID	EX	ME	WB		
nop									IF	ID	EX	ME	WB	
sw										IF	ID	EX	ME	WB

For the code sequence in 4.14, show the pipeline diagram (e.g. as we did in class) for the following cases:

a) full forwarding, branches resolved in EX

	1	2	3	4	5	6	7	8	9	10	11
lw r2,0(r1)	IF	ID	EX	ME	WB						
beq r2,r0,label2		IF	ID	EX	ME	WB					
lw r3,0(r2)			IF	ID	EX	ME	WB				
beq r3,r0,label1				IF	ID	EX	ME	WB			
add r1,r3,r1					IF	ID	-	-	EX	ME	WB

b) full forwarding, branches resolved in ID

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
lw r2,0(r1)	IF	ID	EX	ME	WB									
beq r2,r0,label 2		IF	ID	EX	ME	WB								
lw r3,0(r2)			IF	ID	EX	ME	WB							
beq r3,r0,label 1				IF	ID	-	-	-	EX	ME	WB			
add r1,r3,r1					IF	ID	-	-	-	EX	ME	WB		
sw r1,0(r2)						IF	ID	-	-	-	-	EX	ME	WB