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CSM151B HW4
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4.7 1.

Opcode = (101011)2 = (43)10This is a load/store function

Rs = (00011)2 = 3Rt = (00010)2 = 2Address = (000000000010100)2 = 20

Thus, the instruction is sw \$s2, 20(\$s3).

The output of the shift left is: (XXXX 1000 1000 0000 0000 1010 0000)2, where XXXX is the most significant 4 bits of PC+4

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ALU control input is: Function field of instruction: (010100)2 = (43)10 It's a SW instruction ALUop is 00

3.

The new PC is PC+4 The data path is shown in the diagram attached below.

4.

Two muxes at branch: PC+4

Mux before the registers: Can be either 00010 or 00000

Mux before the ALU: 0000 0000 0000 0000 0000 0000 0001 0100

Mux after data memory: Random bits from "read data" port

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ALU input 1: (-3)10 ALU input 2: (20)10

Top left adder: current PC and 4 add(ALU result): pc + 4 and (80)10

6.

Read register 1: 00011 Read register 2: 00010

Write register: 00010 or 00000 (don't care)

Write data: don't care RegWrite:0