Chapter 5

Large and Fast: Exploiting Memory Hierarchy



Cache Memory

- Cache memory
 - The level of the memory hierarchy closest to the CPU
- Given accesses X₁, ..., X_{n-1}, X_n

X ₄
X ₁
X _{n-2}
X _{n-1}
X ₂
X ₃

X ₄
X ₄ X ₁
X _{n-2}
X _{n-1}
X ₂
X_n
X ₃

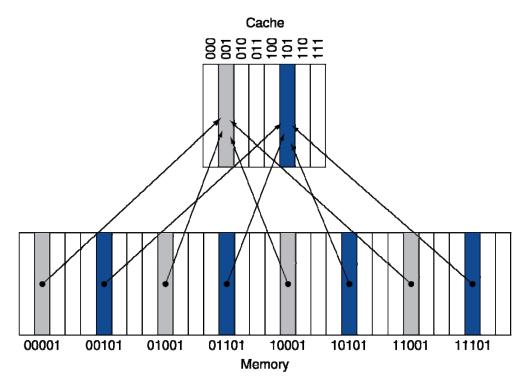
- How do we know if the data is present?
- Where do we look?

b. After the reference to X_n

a. Before the reference to X_n

Direct Mapped Cache

- Location determined by address
- Direct mapped: only one choice
 - (Block address) modulo (#Blocks in cache)



- #Blocks is a power of 2
- Use low-order address bits

Tags and Valid Bits

- How do we know which particular block is stored in a cache location?
 - Store block address as well as the data
 - Actually, only need the high-order bits
 - Called the tag
- What if there is no data in a location?
 - Valid bit: 1 = present, 0 = not present
 - Initially 0

- 8-blocks, 1 word/block, direct mapped
- Initial state

Index	V	Tag	Data
000	N		
001	N		
010	N		
011	N		
100	N		
101	N		
110	N		
111	N		

Word addr	Binary addr	Hit/miss	Cache block
22	10 110	Miss	110

Index	V	Tag	Data
000	N		
001	N		
010	N		
011	N		
100	N		
101	N		
110	Υ	10	Mem[10110]
111	N		

Word addr	Binary addr	Hit/miss	Cache block
26	11 010	Miss	010

Index	V	Tag	Data
000	N		
001	N		
010	Υ	11	Mem[11010]
011	N		
100	N		
101	N		
110	Y	10	Mem[10110]
111	N		

Word addr	Binary addr	Hit/miss	Cache block
22	10 110	Hit	110
26	11 010	Hit	010

Index	V	Tag	Data
000	N		
001	N		
010	Υ	11	Mem[11010]
011	N		
100	N		
101	N		
110	Υ	10	Mem[10110]
111	N		

Word addr	Binary addr	Hit/miss	Cache block
16	10 000	Miss	000
3	00 011	Miss	011
16	10 000	Hit	000

Index	V	Tag	Data
000	Y	10	Mem[10000]
001	N		
010	Υ	11	Mem[11010]
011	Υ	00	Mem[00011]
100	N		
101	N		
110	Υ	10	Mem[10110]
111	N		

Word addr	Binary addr	Hit/miss	Cache block
18	10 010	Miss	010

Index	V	Tag	Data
000	Υ	10	Mem[10000]
001	N		
010	Y	10	Mem[10010]
011	Υ	00	Mem[00011]
100	N		
101	N		
110	Υ	10	Mem[10110]
111	N		

Address Subdivision

