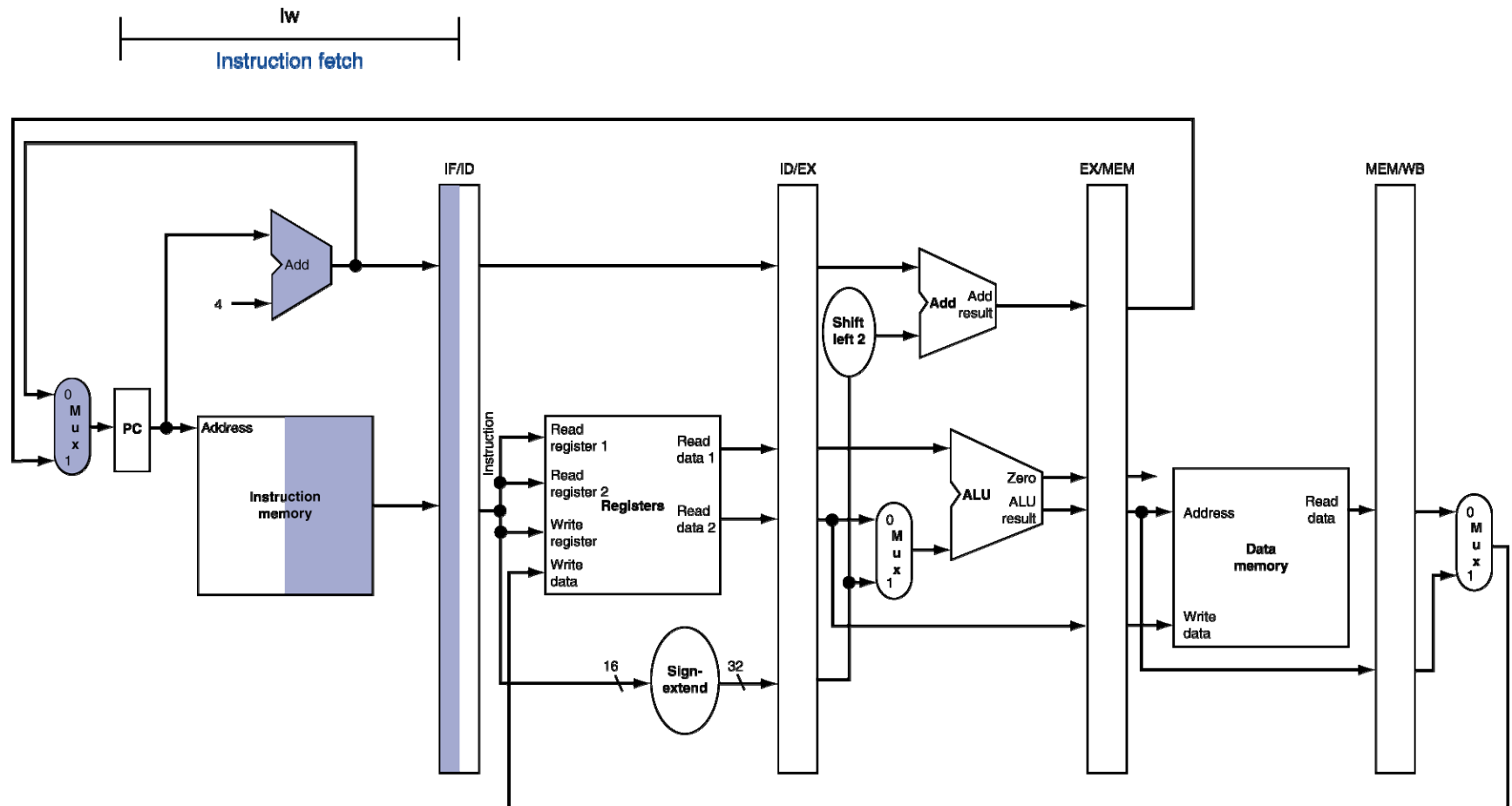# Chapter 4

The Processor

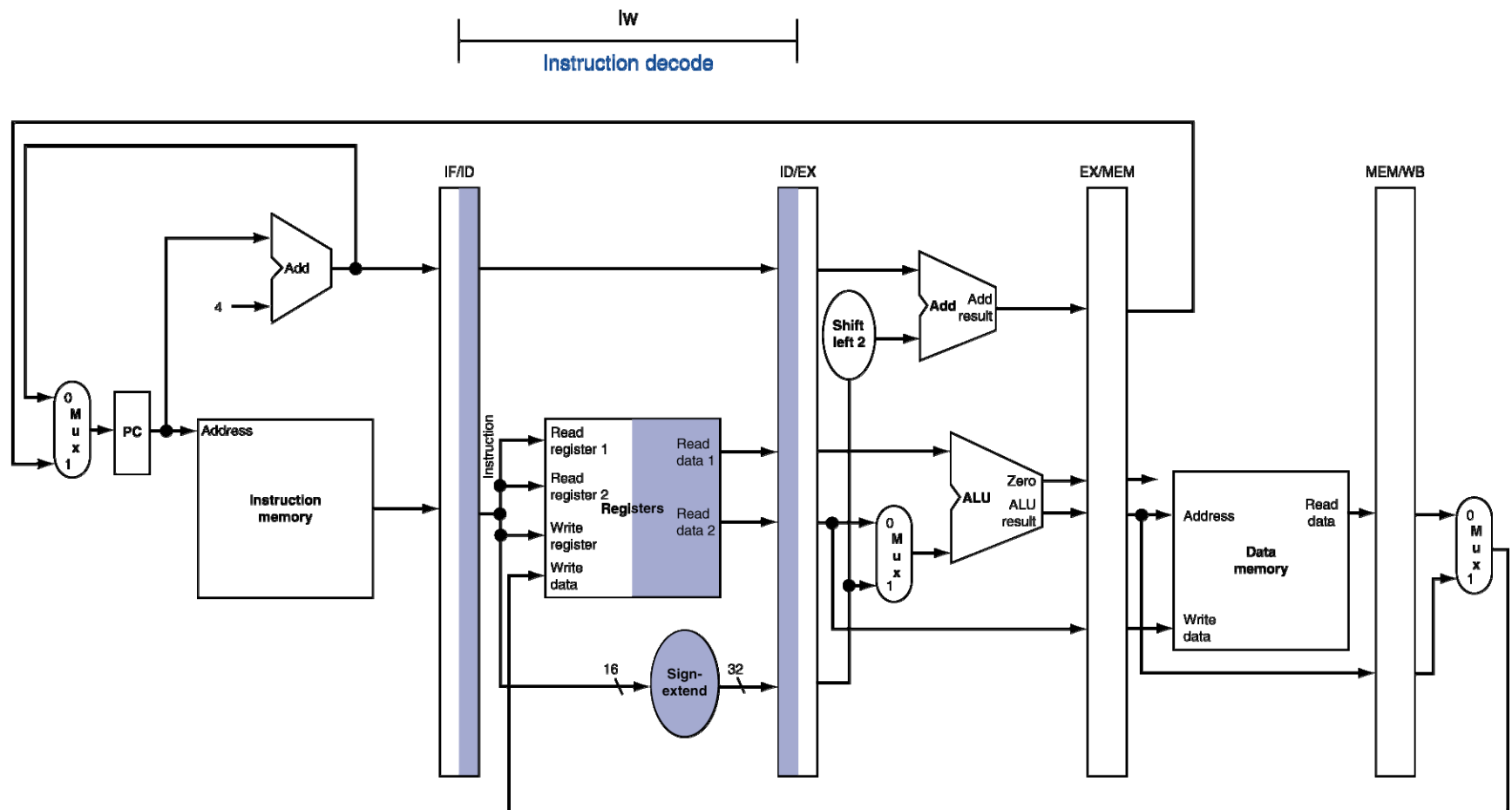# Pipeline Operation

- Cycle-by-cycle flow of instructions through the pipelined datapath
    - "Single-clock-cycle" pipeline diagram
        - Shows pipeline usage in a single cycle
        - Highlight resources used
    - c.f. "multi-clock-cycle" diagram
        - Graph of operation over time

- We'll look at "single-clock-cycle" diagrams for load & store
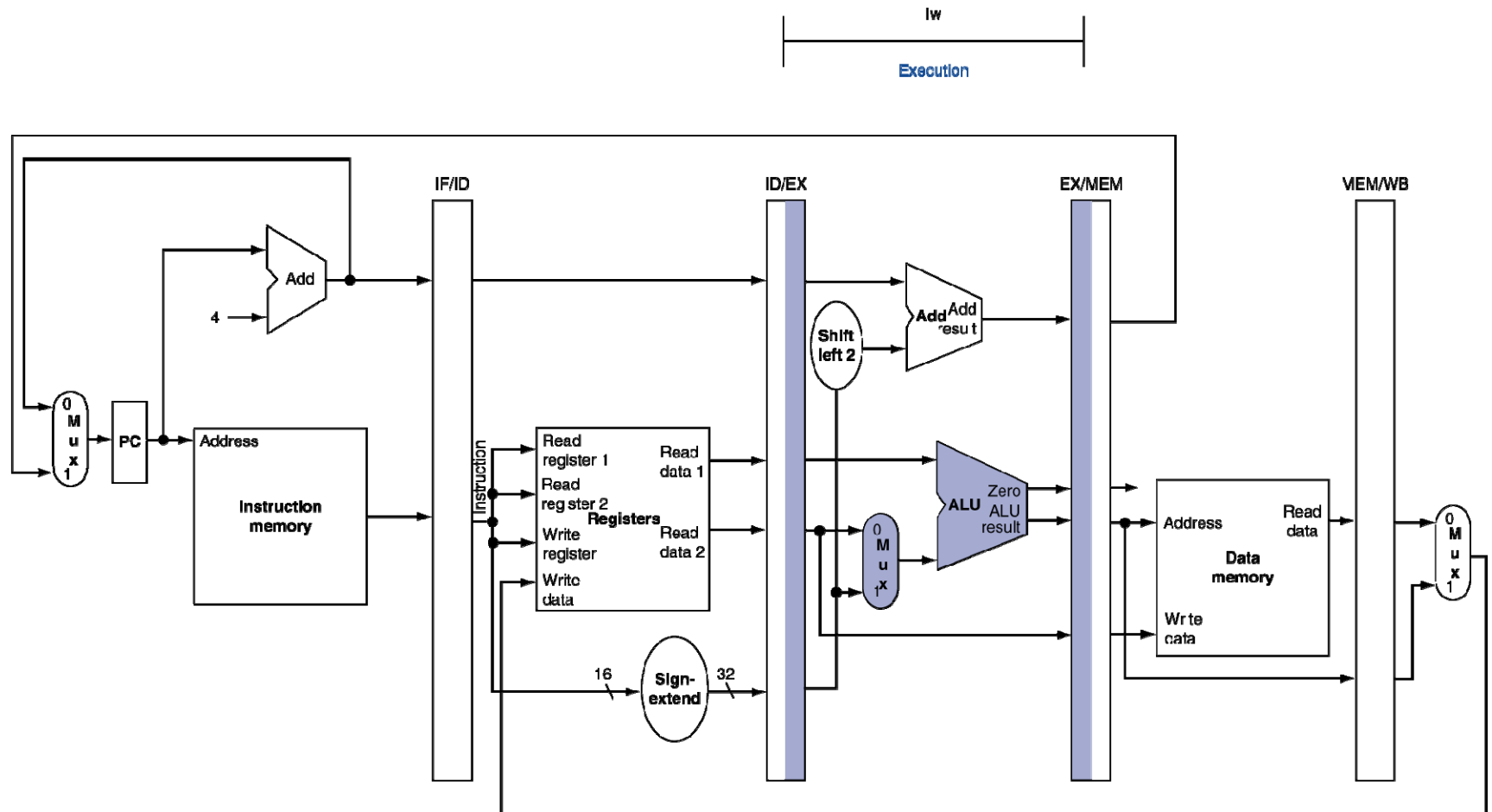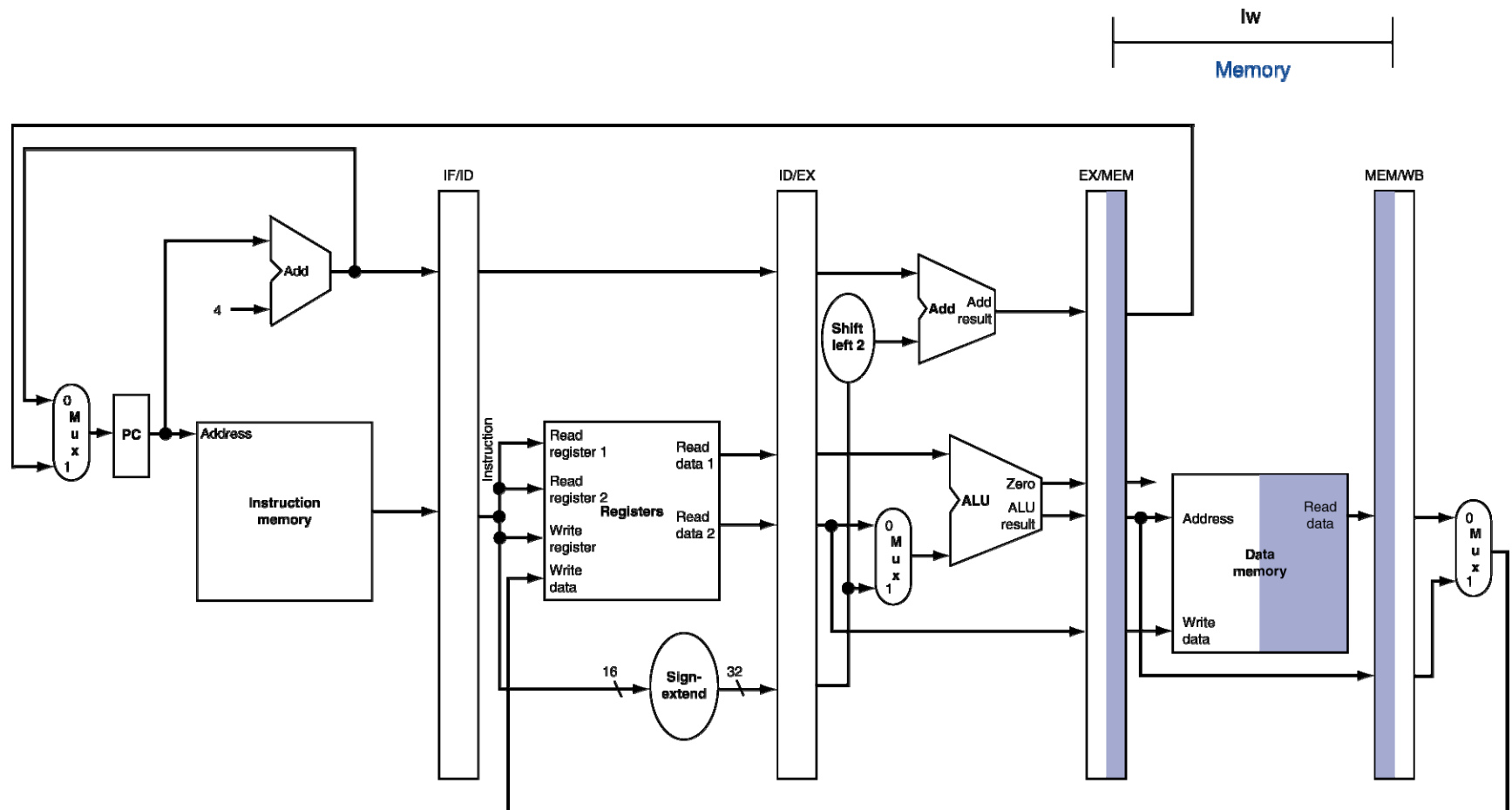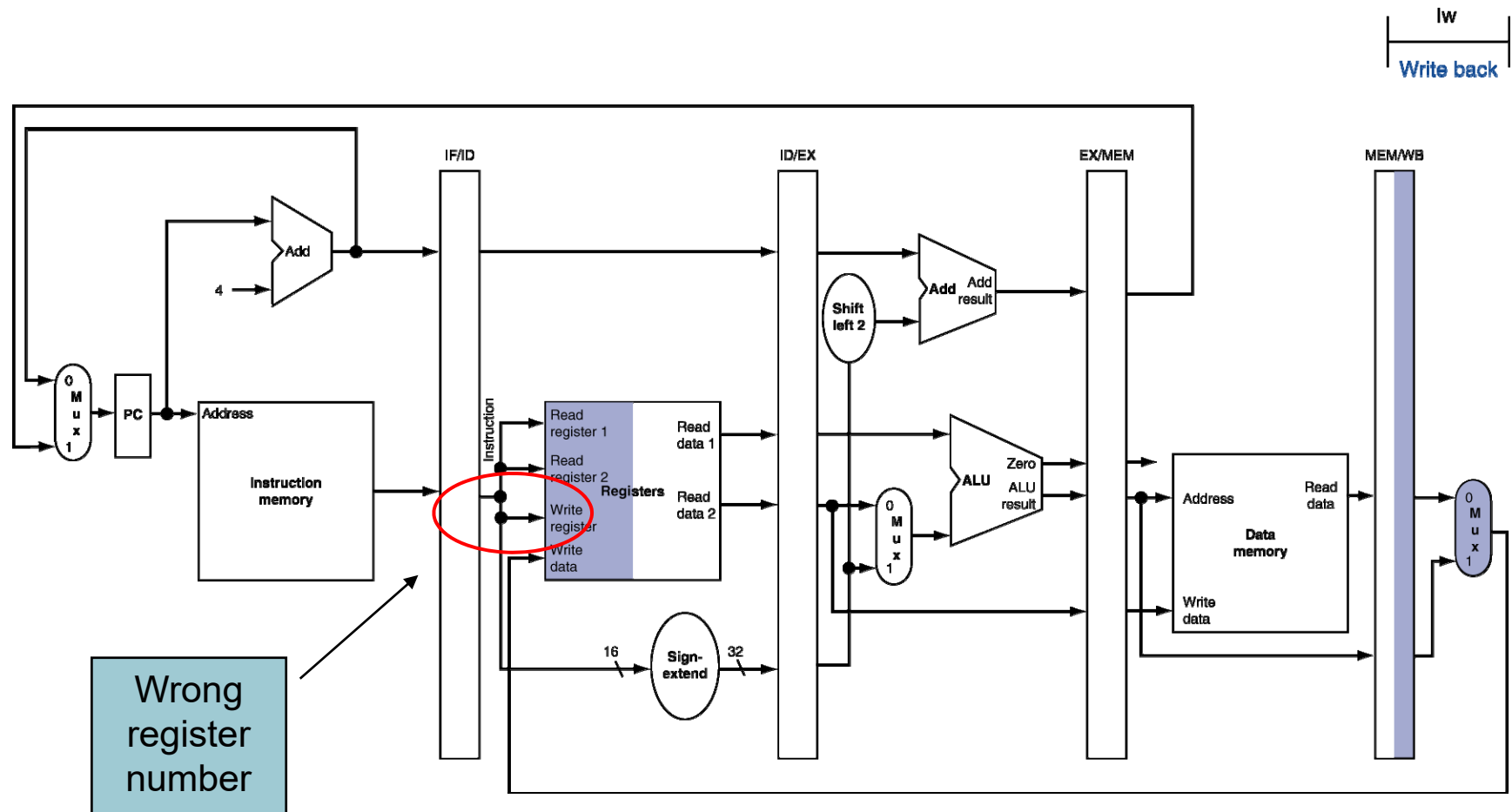
IF for Load, Store, …
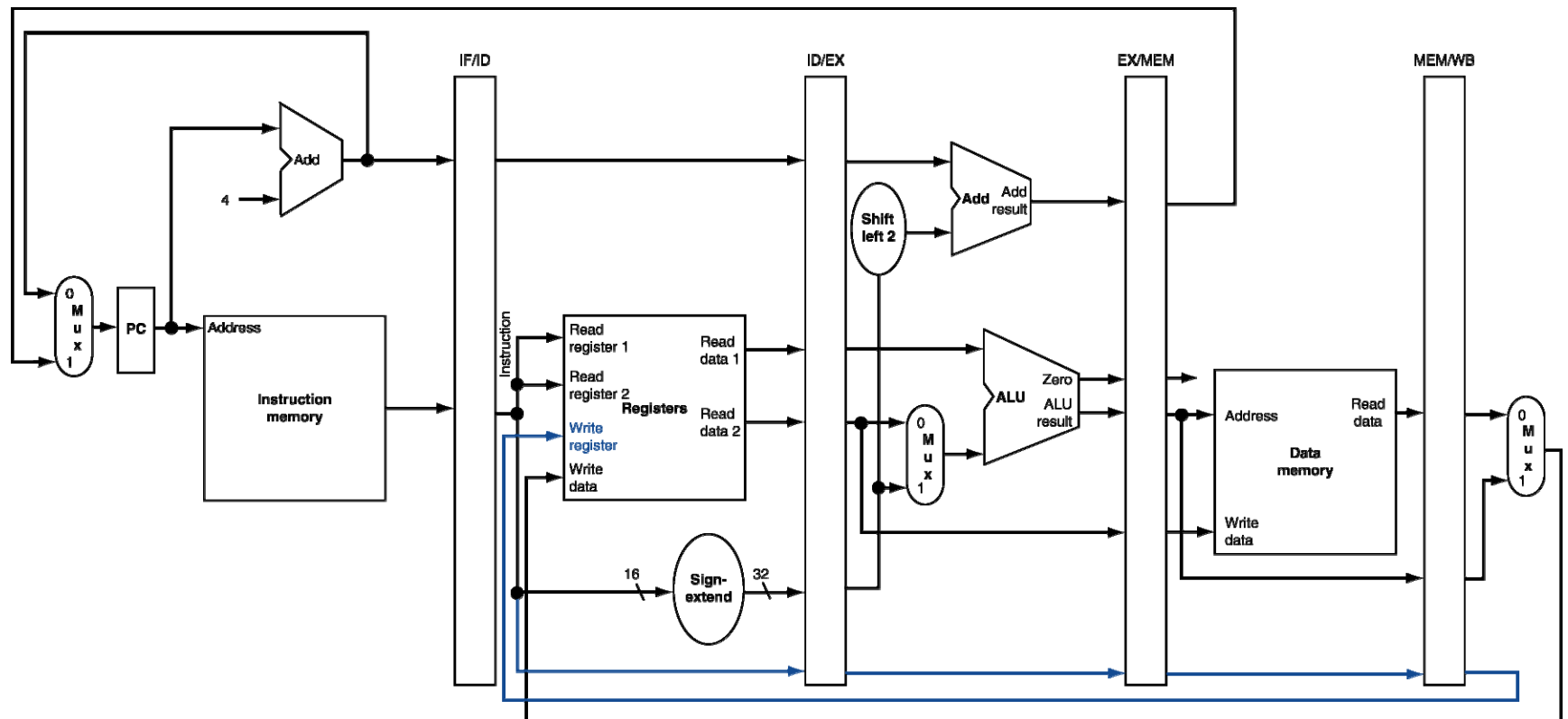
ID for Load, Store, …

EX for Load

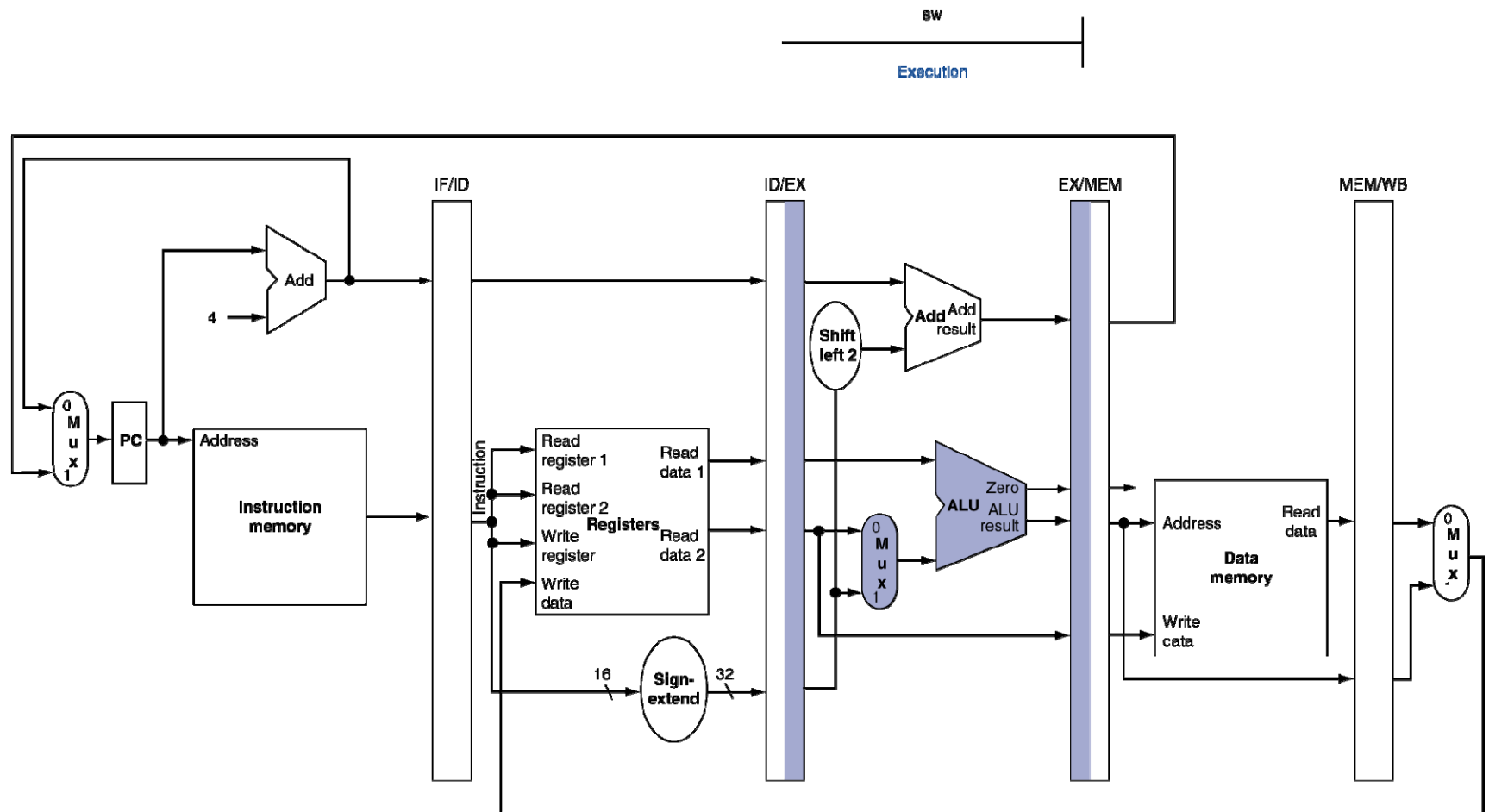# MEM for Load

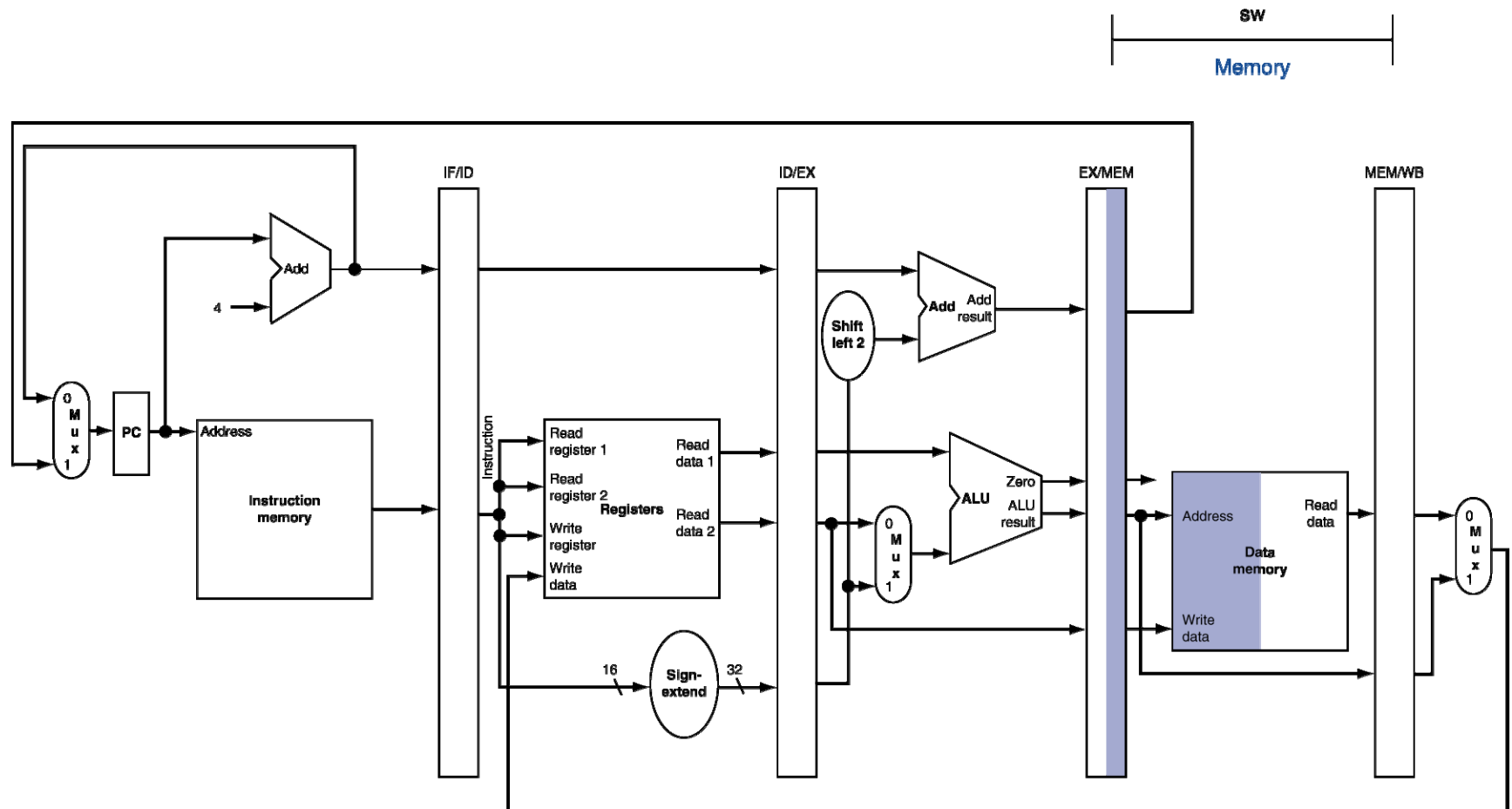# WB for Load

Wrong register number

Corrected Datapath for Load

EX for Store

MEM for Store

WB for Store