Three stage cmos ring oscillator

Mohamed Irfan

***Abstract*—The design and simulation of a three-stage CMOS ring oscillator using the SkyWater PDK. The oscillator, consisting of three interconnected inverters, demonstrates stable oscillation characteristics, including tunable frequency and appropriate duty cycle. Simulation results highlight the impact of transistor sizing and load capacitance on performance. This work emphasizes the significance of ring oscillators in integrated circuit applications.**

I. INTRODUCTION

A ring oscillator is a key component in digital electronics, primarily used for generating clock signals. It consists of an odd number of inverters connected in a feedback loop, enabling continuous oscillation through signal inversion and propagation delay. With advancements in complementary metal-oxide-semiconductor (CMOS) technology, ring oscillators have become essential for applications such as phase-locked loops and frequency synthesizers due to their efficiency and low power consumption. This paper explores the design and simulation of a three-stage CMOS ring oscillator using the SkyWater PDK, highlighting its operational principles and performance characteristics.

II. PRINCIPLE OF GENERATION:

A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false. A schematic diagram of a simple three inverter ring oscillator is shown in Fig.1.

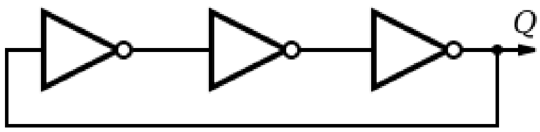


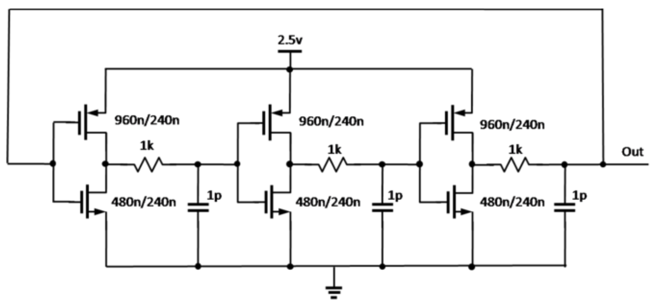
Fig.1: A 3-inverter ring oscillator.

The NOT gates, or inverters, are attached in a chain; the output of the last inverter is fed back into the first. Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. This final output is asserted a finite amount of time after the first input is asserted; the feedback of this last output to the input causes oscillation.

A real oscillator only requires power to operate; above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of oscillation, two methods may be used. Firstly, the applied voltage may be increased; this increases both the frequency of the oscillation, and the power consumed, which is dissipated as heat.

III. IMPLEMENTATION

A three-stage CMOS ring oscillator operates on the principles of feedback and propagation delay to generate oscillating signals. This circuit consists of three inverters arranged in a circular configuration, allowing for continuous signal inversion and propagation. The key to its operation is the feedback loop that connects the output of the last inverter back to the input of the first. In this configuration, each inverter inverts the logic state of its input, creating a cascading effect that leads to oscillation. The initial state can be influenced by noise or fluctuations, prompting the inverters to change states. As the signal propagates through the inverters, it produces a square wave output.



The frequency of oscillation is determined by the cumulative propagation delay of the inverters. This delay is the time it takes for a change at the input to be reflected at the output. Using complementary metal-oxide-semiconductor (CMOS) technology enhances the efficiency of the ring oscillator. NMOS transistors pull the output low, while PMOS transistors pull it high, ensuring low static power consumption and fast switching speeds. At power-up, the oscillator requires a small disturbance to initiate oscillation. Once triggered, the system stabilizes and produces a consistent output waveform. The resulting square wave signal oscillates between high and low voltage levels, characterized by its frequency, duty cycle, and voltage levels, which are critical for digital circuit applications. In summary, the three-stage CMOS ring oscillator exemplifies the fundamental principles of digital circuit design, effectively generating clock signals essential for various applications in integrated systems. Its reliance on feedback and propagation delay underpins its functionality, making it a crucial component in modern electronics.

IV. CONCLUSION

The three-stage CMOS ring oscillator effectively generates stable clock signals essential for various digital applications. Its design leverages feedback and propagation delay, utilizing CMOS technology for low power consumption and high-speed performance. This oscillator's reliability and versatility make it a crucial component in modern integrated circuits and digital systems.

References

[1] B. Razavi. (2001). "Design of Analog CMOS Integrated Circuits." *McGraw-Hill*.

[2] https://en.wikipedia.org/wiki/Ring_oscillator#:~:text=The%20ring%20oscillator%20is%20a,at%20the%20intended%20oscillation%20frequency.

[3] https://www.researchgate.net/figure/Schematic-diagram-of-three-stage-CMOS-ring-oscillator-The-schematic-diagram-of-three_fig2_324106283

[4] https://vlsi-iitg.vlabs.ac.in/RingOscillator_theory.html