Computer and Communication Engineering Program
Faculty of Engineering
Alexandria University

Course Title: Digital Logic Circuits - I

Course Code: CSE 136

4-bit Full Adder

with output on 7 segment display

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Problem Statement

In the project it is required to implement a logic circuit that functionally aims to add 2 binary 4-bit numbers and displaying the result as a 2-digit decimal number on two 7 segment displays.

However, first we must illustrate how the full adder works when dealing with 2 binary 1-bit numbers then using 4 cascaded full adders.

Truth Table

The truth table for the single full adder is shown as follows:

C_{in}	A	B	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map

- For the sum (S):

	A'		A	
C_{in}'		1		1
C_{in}	1		1	
	B'	B		B'

$$S = C_{in}\, A'\, B' + C_{in}'\, A'\, B + C_{in}\, A\, B + C_{in}'\, A\, B'$$

$$S = A' (C_{in}\, B' + C_{in}'\, B) + A (C_{in}\, B + C_{in}'\, B')$$

$$S = A' (C_{in}\, B' + C_{in}'\, B) + A (C_{in}\, B' + C_{in}'\, B)'$$

$$S = A' (C_{in} \oplus B) + A (C_{in} \oplus B)'$$

$$\boxed{S = A \oplus B \oplus C_{in}}$$

- For the carry out (C_{out}):

	A'		A	
C_{in}'			1	
C_{in}		1	1	1
	B'	B		B'

$$C_{out} = C_{in}' A B + C_{in} A' B + C_{in} A B + C_{in} A B'$$
$$C_{out} = A B (C_{in}' + C_{in}) + C_{in} (A' B + A B')$$
$$\boxed{C_{out} = A B + C_{in} (A \oplus B)}$$

Simulations

- ## Full Adder
  1. ### Circuit Diagram

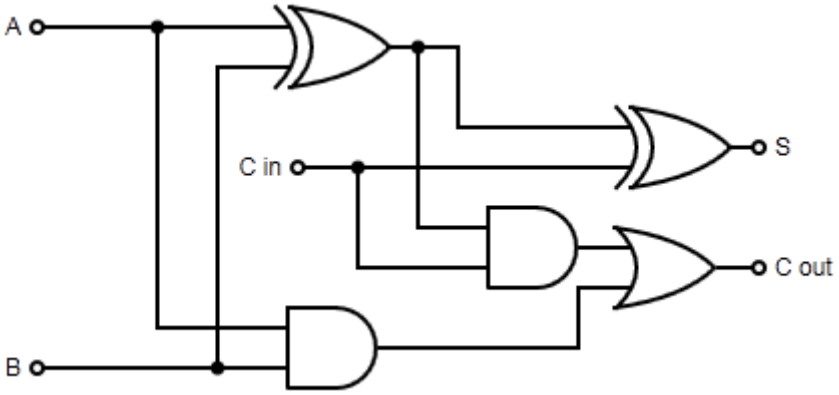

Fig. I: 1-bit Full Adder Circuit Diagram

  2. ### Circuit Simulation

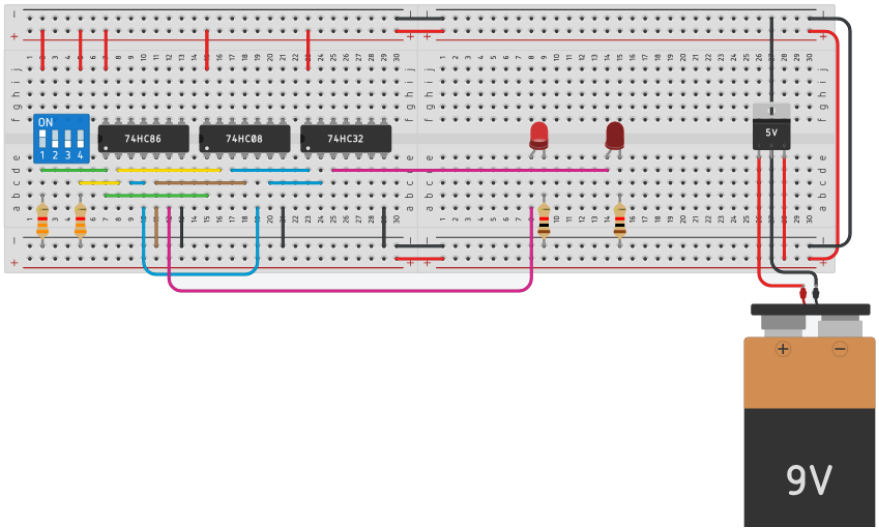

Fig. II: 1-bit Full Adder Circuit Simulation with conditions (A=1, B=0 and C_{in} is grounded thus S=1 and C_{out}=0)

- 4-bit Full Adder
    1. Circuit Diagram

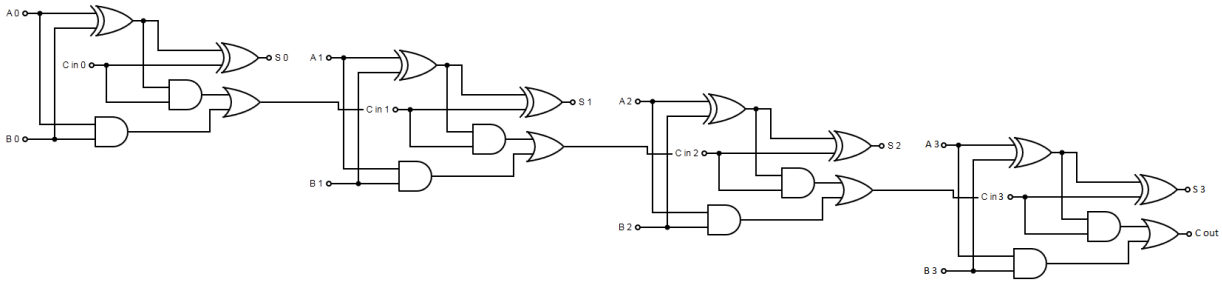

Fig. III: 4-bit Full Adder Circuit Diagram

2. Circuit Simulation

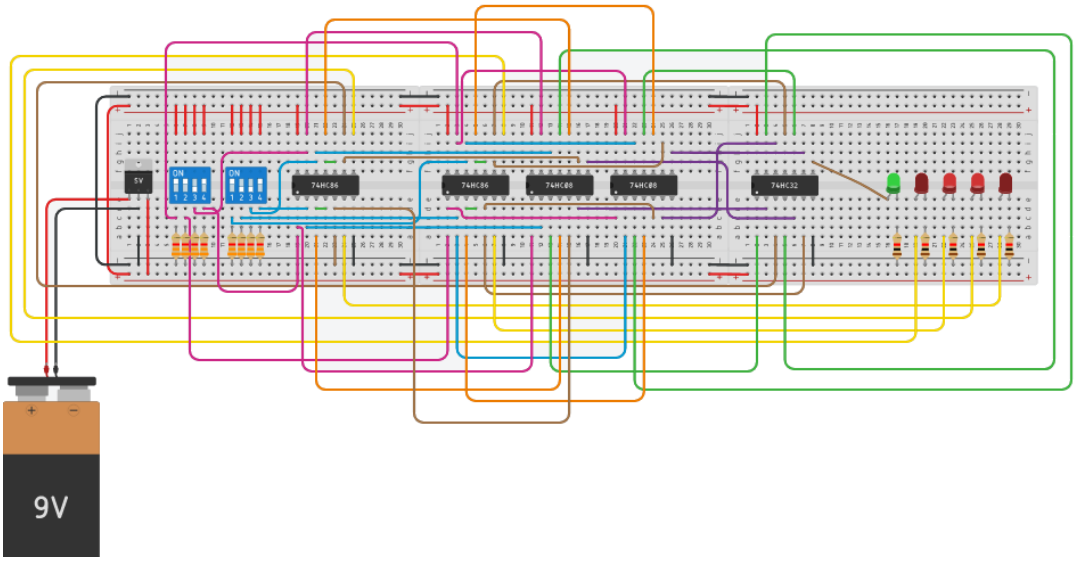

Fig. IV: 4-bit Full Adder Circuit Simulation with conditions (A = $(1101)_2$ = 13 and B = $(1001)_2$ = 9 and C_{in} is grounded thus S = $(0110)_2$ = 6 and C_{out} = 1 thus the result is $(10110)_2$ = 22)

Assigned Circuit

- ### Truth Table

Since we are dealing with adding 2 numbers with the output as a decimal number on 7 segment display thus the following truth table represents the inputs and outputs of the operation in the form of decimal numbers and with removing cases of redundancies such as (24 = 11 + 13 = 13 + 11) so, only one of the two cases is illustrated as the addition operation has commutative property. In addition, the C_{in} isn't illustrated because it is grounded in all cases.

$A_{decimal}$	$B_{decimal}$	$S_{decimal}$
0	0	0
0	1	1
0	2	2
1	1	2
0	3	3
1	2	3
0	4	4
1	3	4
2	2	4
0	5	5
1	4	5
2	3	5
0	6	6
1	5	6
2	4	6
3	3	6
0	7	7
1	6	7
2	5	7
3	4	7
0	8	8
1	7	8
2	6	8
3	5	8
4	4	8
0	9	9
1	8	9
2	7	9
3	6	9
4	5	9

$A_{decimal}$	$B_{decimal}$	$S_{decimal}$
0	10	10
1	9	10
2	8	10
3	7	10
4	6	10
5	5	10
0	11	11
1	10	11
2	9	11
3	8	11
4	7	11
5	6	11
0	12	12
1	11	12
2	10	12
3	9	12
4	8	12
5	7	12
6	6	12
0	13	13
1	12	13
2	11	13
3	10	13
4	9	13
5	8	13
6	7	13
0	14	14
1	13	14
2	12	14
3	11	14

$A_{decimal}$	$B_{decimal}$	$S_{decimal}$
4	10	14
5	9	14
6	8	14
7	7	14
0	15	15
1	14	15
2	13	15
3	12	15
4	11	15
5	10	15
6	9	15
7	8	15
1	15	16
2	14	16
3	13	16
4	12	16
5	11	16
6	10	16
7	9	16
8	8	16
2	15	17
3	14	17
4	13	17
5	12	17
6	11	17
7	10	17
8	9	17
3	15	18
4	14	18
5	13	18
6	12	18
7	11	18
8	10	18
9	9	18
4	15	19
5	14	19
6	13	19
7	12	19
8	11	19
9	10	19

$A_{decimal}$	$B_{decimal}$	$S_{decimal}$
5	15	20
6	14	20
7	13	20
8	12	20
9	11	20
10	10	20
6	15	21
7	14	21
8	13	21
9	12	21
10	11	21
7	15	22
8	14	22
9	13	22
10	12	22
11	11	22
8	15	23
9	14	23
10	13	23
11	12	23
9	15	24
10	14	24
11	13	24
12	12	24
10	15	25
11	14	25
12	13	25
11	15	26
12	14	26
13	13	26
12	15	27
13	14	27
13	15	28
14	14	28
14	15	29
15	15	30

The following table illustrates the equivalent binary numbers for all possible inputs:

$N_{decimal}$	N_3	N_2	N_1	N_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

- Circuit Simulation

  The following figure shows an example of simulating the addition operation processed for the two inputs A = 10 = $(1010)_2$ and B = 15 = $(1111)_2$ giving the output S = 25 = $(11001)_2$.

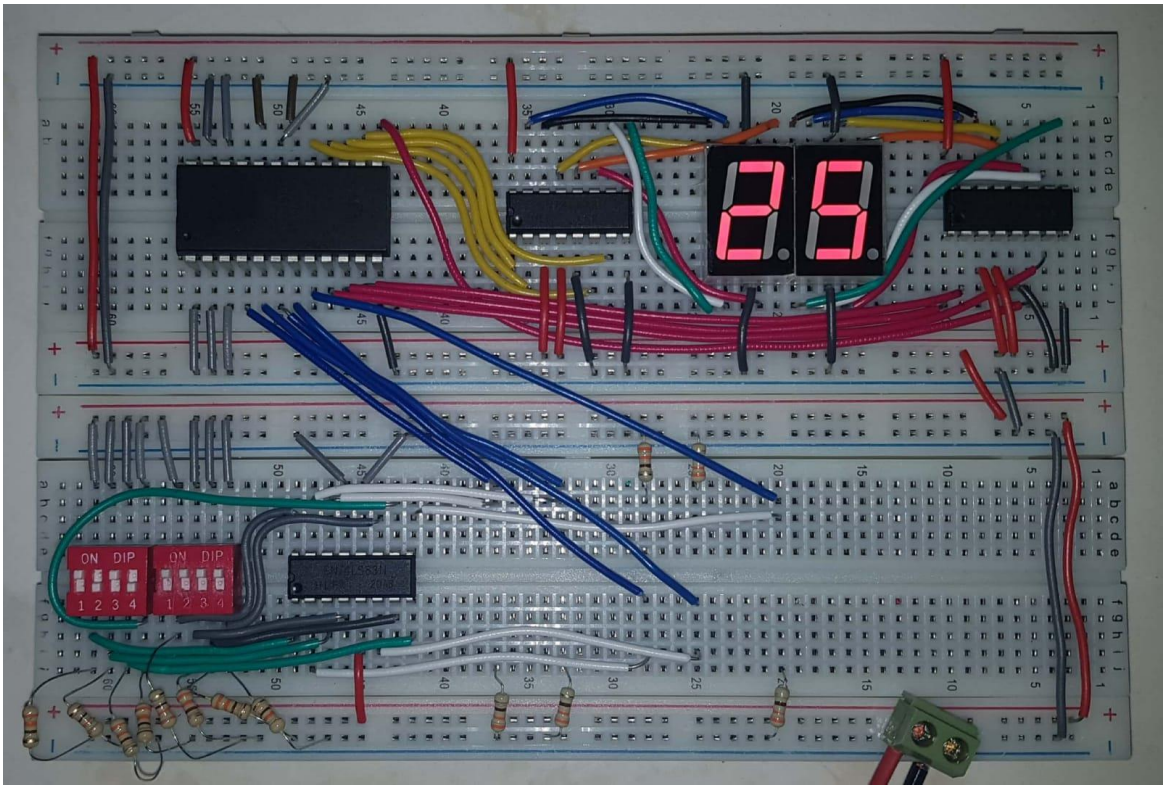

Fig. V: Sample simulation for the assigned circuit

- Data Sheets

The circuit operates using four ICs in addition to two seven segment displays as shown in the following:

- 4-bit Full Adder (7483 (1 IC))

A 16 pin IC that accepts two binary 4-bit numbers as well as an initial carry (which is grounded in our project to keep its value Zero) and outputs a 5-bit binary number represented as (C_{out}, $\sum_4$, $\sum_3$, $\sum_2$ and $\sum_1$).

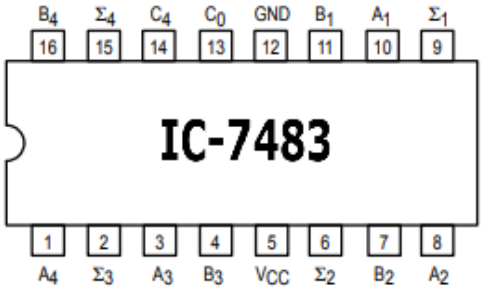

Fig. VI: Pin Diagram of IC 7483 4-bit Full Adder

- Parallel EEPROM (2816 (1 IC))

A 24 pin programmable IC that is used to assign certain values to certain addresses by the aid of a push button, 1 nF capacitor and two 1 kΩ resistors and as the chip is set to write mode (connecting pin 20 to V_{CC} as it is active low and pin 21 to the other end of the capacitor) and the input/output pins are connected to the V_{CC} or the ground as needed then by pressing the button, the change occurred by the RC circuit causes what is called a save operation for the input value to be assigned to the address set at this time as long as this operation is not repeated for the same address with different code.

In our project, this EEPROM was used in order to convert the output of the Full Adder from 5-bit binary number into 8-bit BCD number thus we programmed it starting from 0 until 31 as the output is 5-bit binary number that can't take values higher than 31.

The following table shows the conversions of the binary numbers into BCD numbers:

Binary Number					BCD Number							
					Tens in Binary				Units in Binary			
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	0	0	1	1
0	0	1	0	0	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	0	0	1	0	1
0	0	1	1	0	0	0	0	0	0	1	1	0
0	0	1	1	1	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	1	0	0	0
0	1	0	0	1	0	0	0	0	1	0	0	1
0	1	0	1	0	0	0	0	1	0	0	0	0
0	1	0	1	1	0	0	0	1	0	0	0	1
0	1	1	0	0	0	0	0	1	0	0	1	0
0	1	1	0	1	0	0	0	1	0	0	1	1
0	1	1	1	0	0	0	0	1	0	1	0	0
0	1	1	1	1	0	0	0	1	0	1	0	1
1	0	0	0	0	0	0	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	1	1	1
1	0	0	1	0	0	0	0	1	1	0	0	0
1	0	0	1	1	0	0	0	1	1	0	0	1
1	0	1	0	0	0	0	1	0	0	0	0	0
1	0	1	0	1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1	0	0	0	1	0
1	0	1	1	1	0	0	1	0	0	0	1	1
1	1	0	0	0	0	0	1	0	0	1	0	0
1	1	0	0	1	0	0	1	0	0	1	0	1
1	1	0	1	0	0	0	1	0	0	1	1	0
1	1	0	1	1	0	0	1	0	0	1	1	1
1	1	1	0	0	0	0	1	0	1	0	0	0
1	1	1	0	1	0	0	1	0	1	0	0	1
1	1	1	1	0	0	0	1	1	0	0	0	0
1	1	1	1	1	0	0	1	1	0	0	0	1

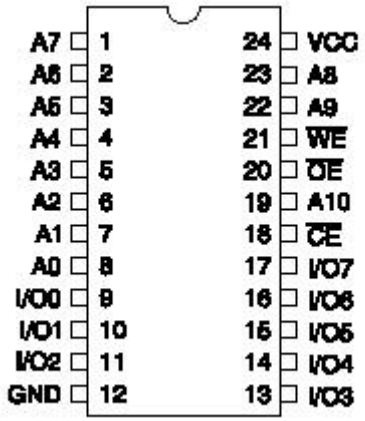

Fig. VII: Pin Diagram of IC 2816 Parallel EEPROM

- BCD to 7 segment Decoder (7448 (2 ICs))

A 16 pin IC that accepts a BCD digit (from 0 to 9) and outputs the seven components (a, b, c, d, e, f and g) corresponding to the seven lines in the 7 segment display. Pin 4 is connected to the V_{CC} to activate the output functionality while the pin 5 is connected to the ground.

The following table shows the truth table of the seven output corresponding to the ten possible incomes:

$N_{decimal}$	Outputs						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	0	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	0	0	1	1

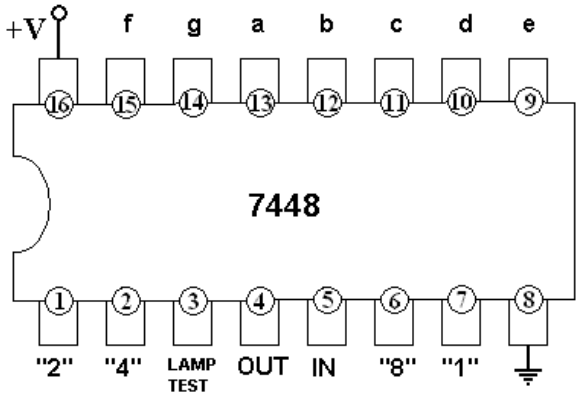

Fig. VIII: Pin Diagram of IC 7448 BCD to 7 segment Decoder

- 7 segment Display (2 Displays)

  A 10 pin output display that accepts 8 inputs representing the 7 lines as well as the decimal point (which is neglected in the project as we deal with adding two integers thus the result is an integer as well). Pins “Com” are connected to the ground as we deal with common cathode 7 segment which is functionally active high.

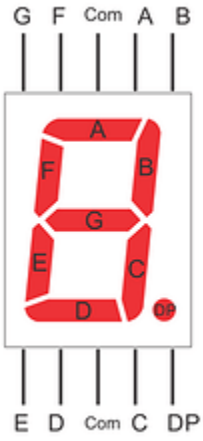

Fig. IX: Pin Diagram of 7 segment Display

- Wiring List

A total number of 81 wires are used in addition to 5 green LED lamps that represent the sum of the two 4-bit binary inputs as a 5-bit binary number as well as 13 resistors of value 330 Ω as 8 of them are connecting the switches (used in entering the inputs) to the ground and the remaining 5 connects the LED lamps to the ground. The value of the resistors' resistance is slightly low as the full adder consumes a lot of current produced by the supply.

The following table illustrates in detail the wires used in the circuit:

Color	Total Number	Amount	Usage
Grey	32	8	connecting the switches with V_{CC}
		8	connecting the ICs and the 7 segment displays to the ground
		6	connecting the 6 unused address input of the EEPROM to the ground to remain zero all the time
		4	connecting the inputs of the switch "B" to the Full Adder
		2	connecting the IN pins of the BCD to 7 segment Decoders to the ground
		2	connecting the negative poles of each of the two breadboards
		1	connecting the negative pole of the two breadboards together
		1	connecting the C_{in} pin of the Full Adder to the ground
Red	11	4	connecting the ICs to the V_{CC}
		2	connecting the OUT pins of the BCD to 7 segment Decoders to the V_{CC}
		2	connecting the LIGHT TEST pins of the BCD to 7 segment Decoders to the V_{CC}
		2	connecting the positive poles of each of the two breadboards
		1	connecting the positive pole of the two breadboards together
White	7	5	connecting the outputs of the Full Adder to the green LED lamps
		2	connecting the D pins from the BCD to 7 segment Decoders to the 7 segment Displays
Blue	7	5	connecting the outputs of the Full Adder to the inputs (addresses) of the EEPROM
		2	connecting the G pins from the BCD to 7 segment Decoders to the 7 segment Displays
Magenta	6	4	connecting the second 4 outputs of the EEPROM (Units Digit) to the second BCD to 7 segment Decoder
		2	connecting the C pins from the BCD to 7 segment Decoders to the 7 segment Displays
Yellow	6	4	connecting the first 4 outputs of the EEPROM (Tens Digit) to the second BCD to 7 segment Decoder
		2	connecting the A pins from the BCD to 7 segment Decoders to the 7 segment Displays
Green	6	4	connecting the inputs of the switch "A" to the Full Adder
		2	connecting the E pins from the BCD to 7 segment Decoders to the 7 segment Displays
Orange	2	2	connecting the B pins from the BCD to 7 segment Decoders to the 7 segment Displays
Black	2	2	connecting the F pins from the BCD to 7 segment Decoders to the 7 segment Displays
Brown	2	2	connecting the OUTPUT ENABLE and CHIP ENABLE pins of the EEPROM to the ground