USER MANUAL

BCM91125PCIX

Evaluation Board

16215 Alton Parkway • P.O. Box 57013 • Irvine, CA 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

91125PCIX-UM100-R
07/02/04

REVISION HISTORY

Revision	*Date*	*Change Description*
91125PCIX-UM100-R	07/02/04	Initial release.

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, CA 92619-7013

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Section 1: Product Overview

INTRODUCTION

The BCM91125PCIX evaluation board is an evaluation platform intended to support the needs of prospective users of the BCM1125H processor. This user manual provides information on how to get the BCM91125PCIX evaluation board up and running quickly. This manual also describes how to locate, configure, and observe the various connectors, switches, jumpers, and LEDs on the BCM91125PCIX, allowing software development and evaluation of the BCM1125H processor to begin.

For additional information on this board and the BCM1125H processor, go to: http://sibyte.broadcom.com/public.

ITEMS INCLUDED WITH THE SHIPMENT

The following items are included with the BCM91125PCIX evaluation board shipment:

- BCM91125PCIX evaluation board in ATX case with power supply and power cable
- OCDemon Macraigor Systems Wiggler parallel port JTAG probe
- Viosoft ARRIBA® Embedded Edition CD
- This document

FEATURES

This section describes the BCM91125PCIX's features.

HARDWARE

- BCM1125H processor
- microATX form factor board mounted in ATX case with a power supply (AC Input: 115V/230V, 10A/5A, 60 Hz/50 Hz; DC Output: 230W)
- Two DDR SDRAM DIMM slots
  - Ships with two 256MB PC2100 (266 MHz) w/ ECC DIMM
- Two 10/100/1000 Mbps Ethernet interfaces with RJ45 connectors
- Two UARTs with RS232 interface
- One 32-bit, 33/66-MHz, 3.3V PCI connector
- Two 64-bit, 33/66-MHz, 3.3V PCI-X connectors
- 2 MB Flash ROM
- Two SMBus channels with the following devices connected:
  - RTC
  - EEPROM
  - Temperature sensor
  - DIMMs SPD EEPROMs
- Two USB connectors

- EJTAG connector
- Four-character LED display
- Compact flash (CF) slot

FIRMWARE

The Common Firmware Environment (CFE) is designed to be easily portable to designs incorporating current and future Broadcom MIPS64-compatible broadband processors. Supported platforms include Broadcom's SiByte processor family (BCM1250, BCM1125H, and so forth), 32-bit and 64-bit memory models, and big and little-endian operation. There are many parameters configurable at build time that can be used to customize CFE to suit diverse customer requirements.

On the BCM91125PCIX, CFE can load programs (such as S-records, raw binary, or ELF formatted) from bootstrap devices in a variety of ways, including:

- Via either Ethernet port or from a TFTP server
- Via a CF card in the CF slot
- Via the serial port (S-records only)

For additional information on CFE, refer to the *Common Firmware Environment (CFE) Specification* document that can be found in the CFE source code distribution at: http://sibyte.broadcom.com/public.

BCM91125PCIX Front Panel

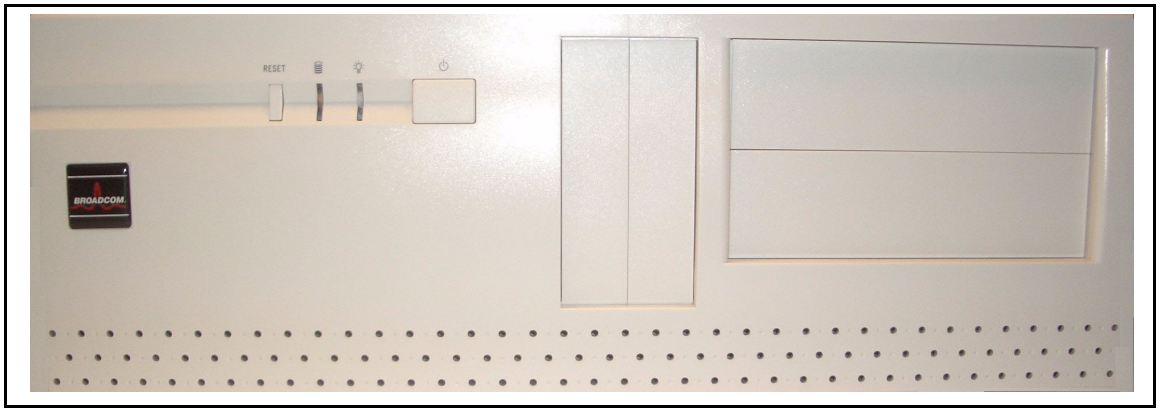

Figure 1: BCM91125PCIX Front Panel

BCM91125PCIX Rear Panel

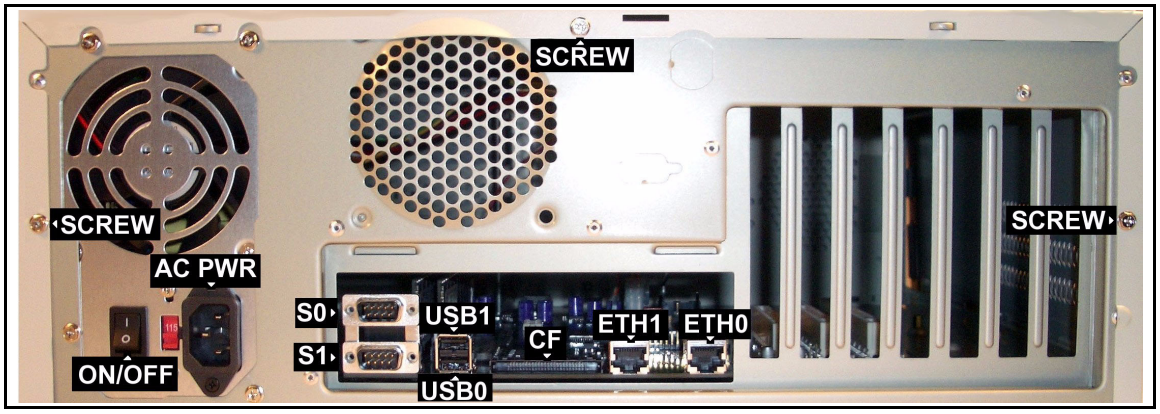

Figure 2: BCM91125PCIX Rear Panel

Section 2: Getting Started

Complete the following steps to get to a BCM91125PCIX CFE (firmware) prompt.

1. Connect a 9-pin null modem cable to the serial port of the BCM91125PCIX and a serial port on a workstation/PC.
2. Use a terminal program and set it to 115200 bps, 8-bit data, 1-stop bit, no parity, and no flow control.
3. Power up the BCM91125PCIX by plugging in the provided cable to the power supply socket on the back of the box and into a wall socket. Then hit the power button on the front panel.

   After a short delay, the CFE initialization output and serial console prompt should display. The following is an example of the output:

```
CFE version 1.0.41 for BCM91125PCIX (64bit,SP,BE,MIPS)
Build Date: Mon May  3 20:13:58 PDT 2004 (mpl@lc-sj1-091)
Copyright (C) 2000,2001,2002,2003 Broadcom Corporation.

Initializing Arena.
Initializing PCI. [normal]
PCI bus 0 slot 0/0: SiByte, Inc. BCM1250 PCI Host Bridge
PCI bus 1 slot 1/0: Advanced Micro Devices (PLX) HT7520 PCI-X Tunnel
PCI bus 1 slot 1/1: Advanced Micro Devices (PLX) HT7520 PCI-X IOAPIC
PCI bus 1 slot 2/0: Advanced Micro Devices (PLX) HT7520 PCI-X Tunnel
PCI bus 1 slot 2/1: Advanced Micro Devices (PLX) HT7520 PCI-X IOAPIC
Initializing Devices.
BCM91125PCIX board revision 1
PCIIDE: 0 controllers found
Config switch: 2
CPU: 1125H A2
L2 Cache: 256KB
SysCfg: 0080000020DB0860 [PLL_DIV: 16, IOB0_DIV: CPUCLK/3, IOB1_DIV: CPUCLK/2]
CPU type 0x40103: 800MHz
Total memory: 0x20000000 bytes (512MB)

Total memory used by CFE:  0x8FE84280 - 0x90000000 (1555840)
Initialized Data:          0x8FE84280 - 0x8FE8DE70 (39920)
BSS Area:                  0x8FE8DE70 - 0x8FE8E5E0 (1904)
Local Heap:                0x8FE8E5E0 - 0x8FF8E5E0 (1048576)
Stack Area:                0x8FF8E5E0 - 0x8FF905E0 (8192)
Text (code) segment:       0x8FF905E0 - 0x8FFFFFB0 (457168)
Boot area (physical):      0x0FE43000 - 0x0FE83000
Relocation Factor:         I:F03905E0 - D:0DF84280

CFE>
```

4. At the prompt, a program can be run via the network from a TFTP server by doing the following:
   a. Connect the BCM91125PCIX Ethernet port E0 with an Ethernet cable to a switch, repeater, or directly to the Ethernet port of the file server.

      Note: Because the Broadcom PHYs handle direct connects automatically, a crossover cable for direct connects is not needed.

   b. To initialize Ethernet port E0, type the following:

```
ifconfig eth0 -auto
```

Note: The *ifconfig eth0 -auto* command can only be used with a DHCP server.

c. To run a program, type the following:

```
boot -elf tftp_server:/path_to_software/program
```

Section 3: Physical Description

The BCM91125PCIX is implemented in the standard microATX form factor. Figure 3 shows a top view of the BCM91125PCIX.

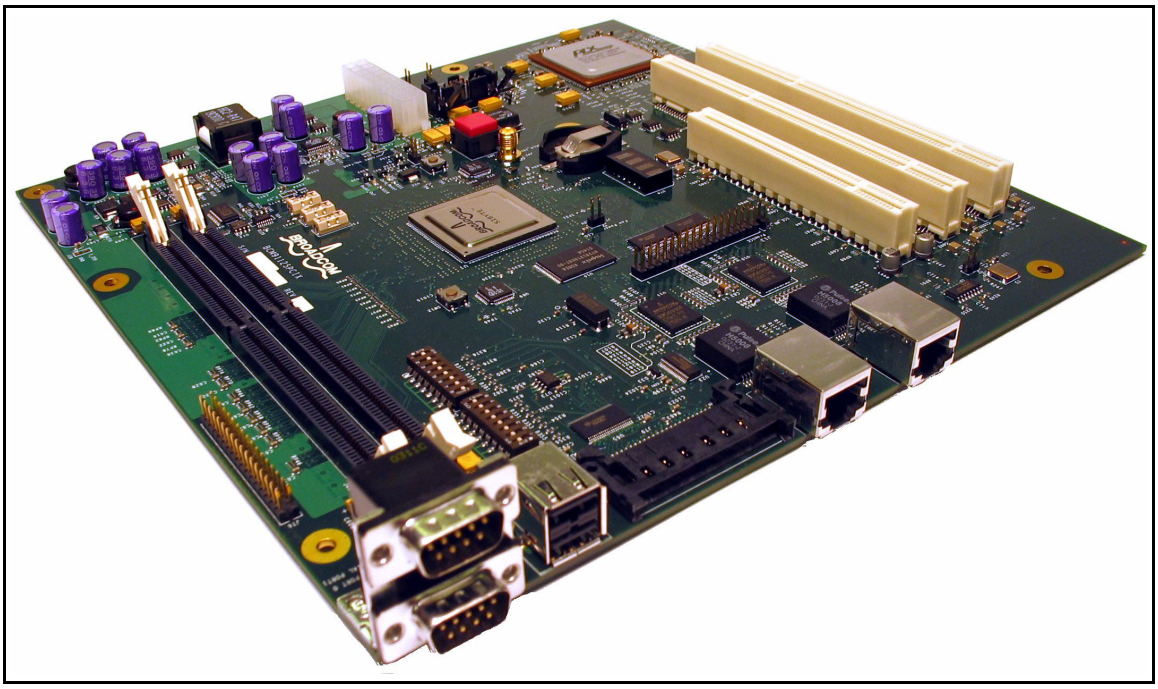

Figure 3: BCM91125PCIX Top View

BLOCK DIAGRAM

Figure 4 shows a block diagram of the BCM91125PCIX.

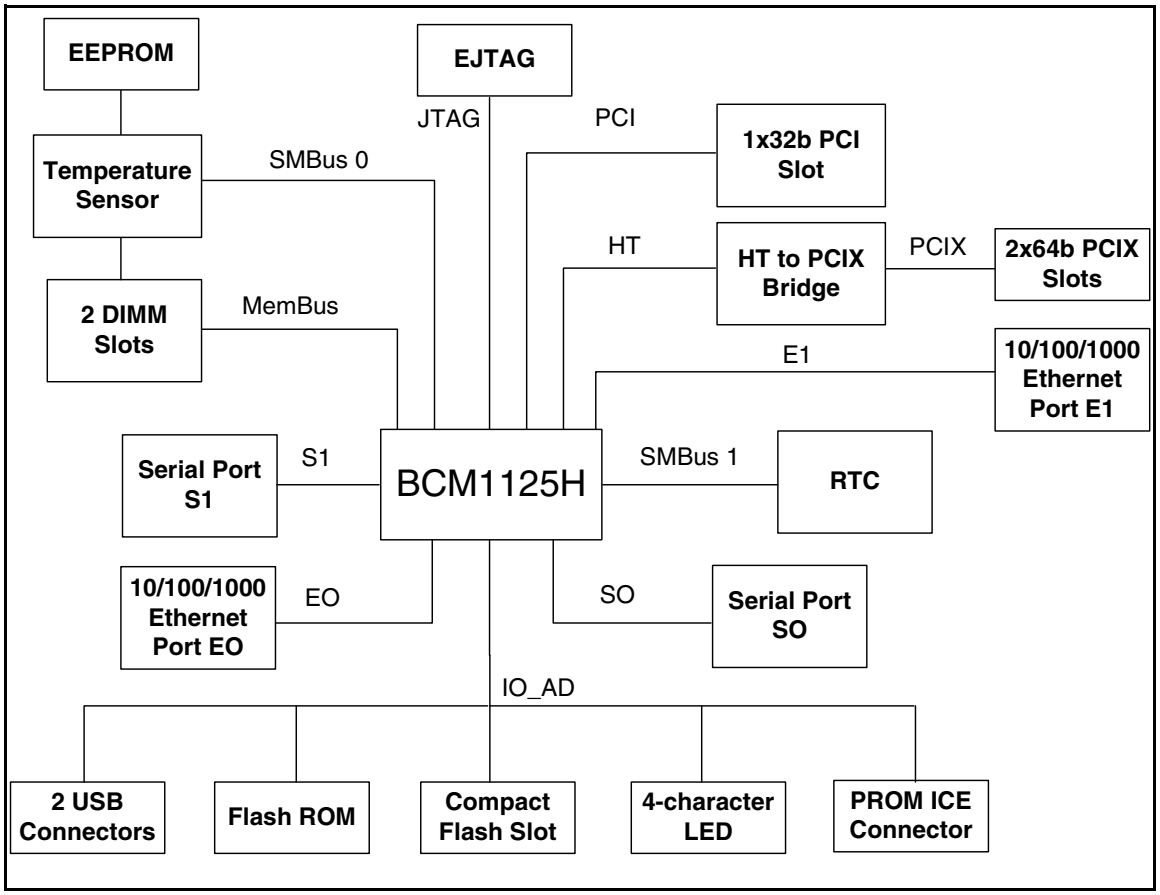

Figure 4: BCM91125PCIX Block Diagram

CONNECTORS

Figure 5 shows the board and identifies connectors numerically. For a description of each connector callout, compare Figure 5's number callouts with Table 1.

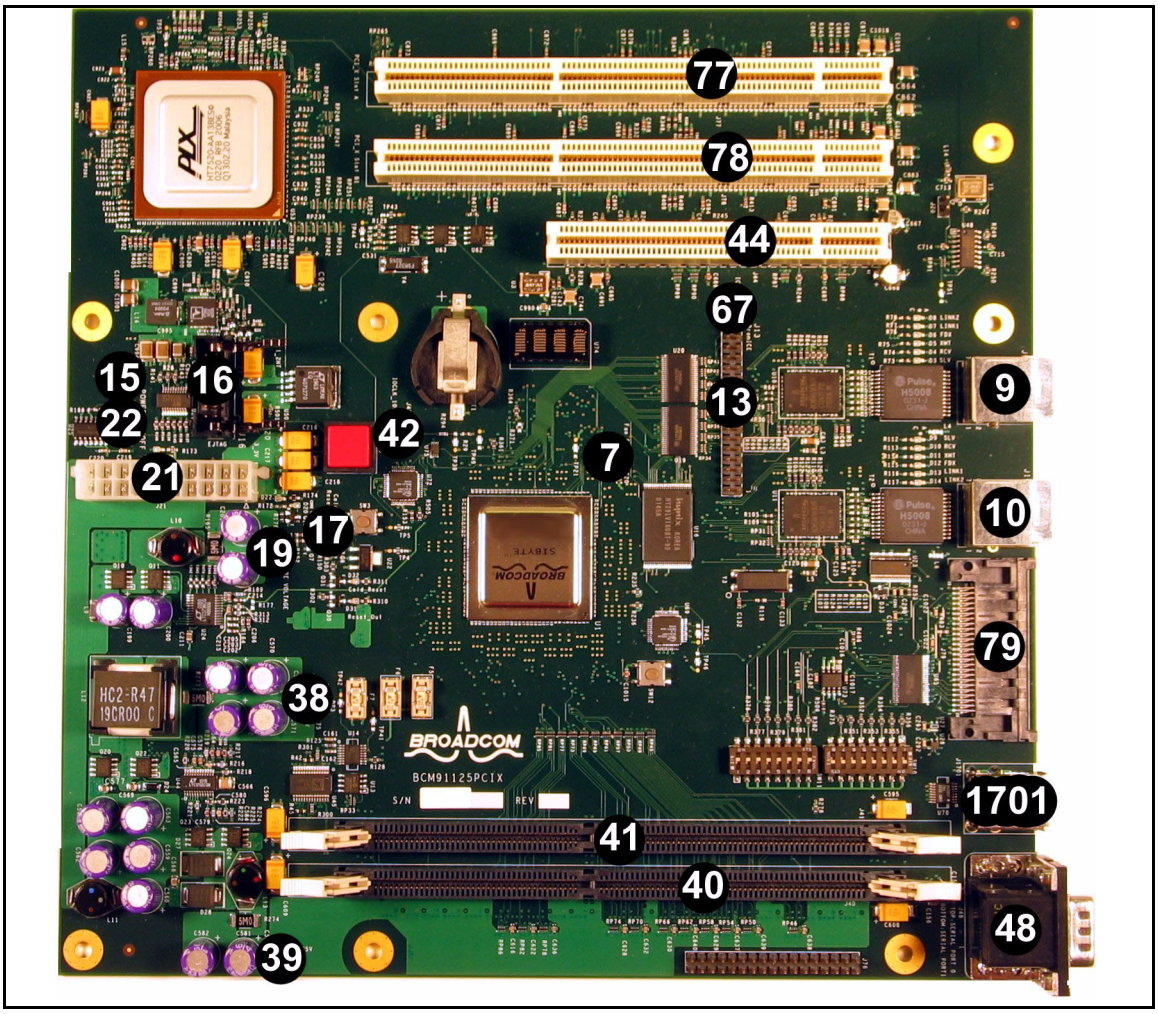

Figure 5: Connector Callouts

The following table shows the BCM91125PCIX connectors.

Table 1: *Connector Descriptions*

Board ID	***Description***
J7	Fan power connector (pin 1 = GND, pin 2 = 12VDC)
J9	10/100/1000 Mbps Ethernet Port E0
J10	10/100/1000 Mbps Ethernet Port E1
J13	ROM Emulator connector (see Table 2 on page 10)
J15	DEBUG_L trigger for scope (pin1 * = GND, pin2 = DEBUG_L)
J16	EJTAG connector
J17	External Cold Reset switch connector (pin 1 = GND, pin 2 = COLDRES_L)
J19	1.2V core supply sense (pin1 ** = GND, pin2 = 1.2V)
J21	ATX power connector
J22	ATX case power switch connector
J38	2.5V supply sense (pin1 ** = GND, pin2 = 2.5V)
J39	1.25V supply sense (pin1 ** = GND, pin2 = 1.25V)
J40	DDR SDRAM DIMM slot 1 (CS 2/3)
J41	DDR SDRAM DIMM slot 0 (CS 0/1)
J42	IO_CLK100 connector
J44	3.3V, 33/66 MHz, 32b PCI slot, BCM1125 PCI device 5
J48	Dual stack RS-232 serial port connectors (top = serial port S0, bottom = serial port S1)
J67	ROM emulator write line (pin 1 * = IO_WR_L, pin 2 = no connect)
J77	3.3V, 66/100/133 MHz, 64b PCI-X slot A, PLX HT7520 device 0
J78	3.3V, 66/100/133 MHz, 64b PCI-X slot B, PLX HT7520 device 1
J79	3.3/5V Compact Flash slot
J1701	Dual stack USB ports

* = Pin 1 located on the board by finding the arrow that points to it on the PCB silkscreen.
** = Pin 1 located by viewing the front of the board for the square solder pad.

ROM EMULATOR PINOUT

Note: The table layout reflects the physical location of the pins on the connector. Also all I/O signals are 3.3V outputs that are tolerant of 5V inputs.

Table 2: ***ROM Emulator Pinout***

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
GND	1	2	AD20
3.3 V PWR	3	4	AD19
AD18	5	6	AD16
AD17	7	8	AD15
AD14	9	10	AD12
AD13	11	12	AD7
AD8	13	14	AD6
AD9	15	16	AD5
AD11	17	18	AD4
OE_L	19	20	AD3
AD10	21	22	AD2
ROMEMUCS_L	23	24	AD1
AD31	25	26	AD0
AD30	27	28	AD24
AD29	29	30	AD25
AD28	31	32	AD26
AD27	33	34	GND

LEDs

Figure 6 shows the positions of the LEDs numerically. Compare Figure 6's number callouts with a description of each LED in Table 3 on page 12.

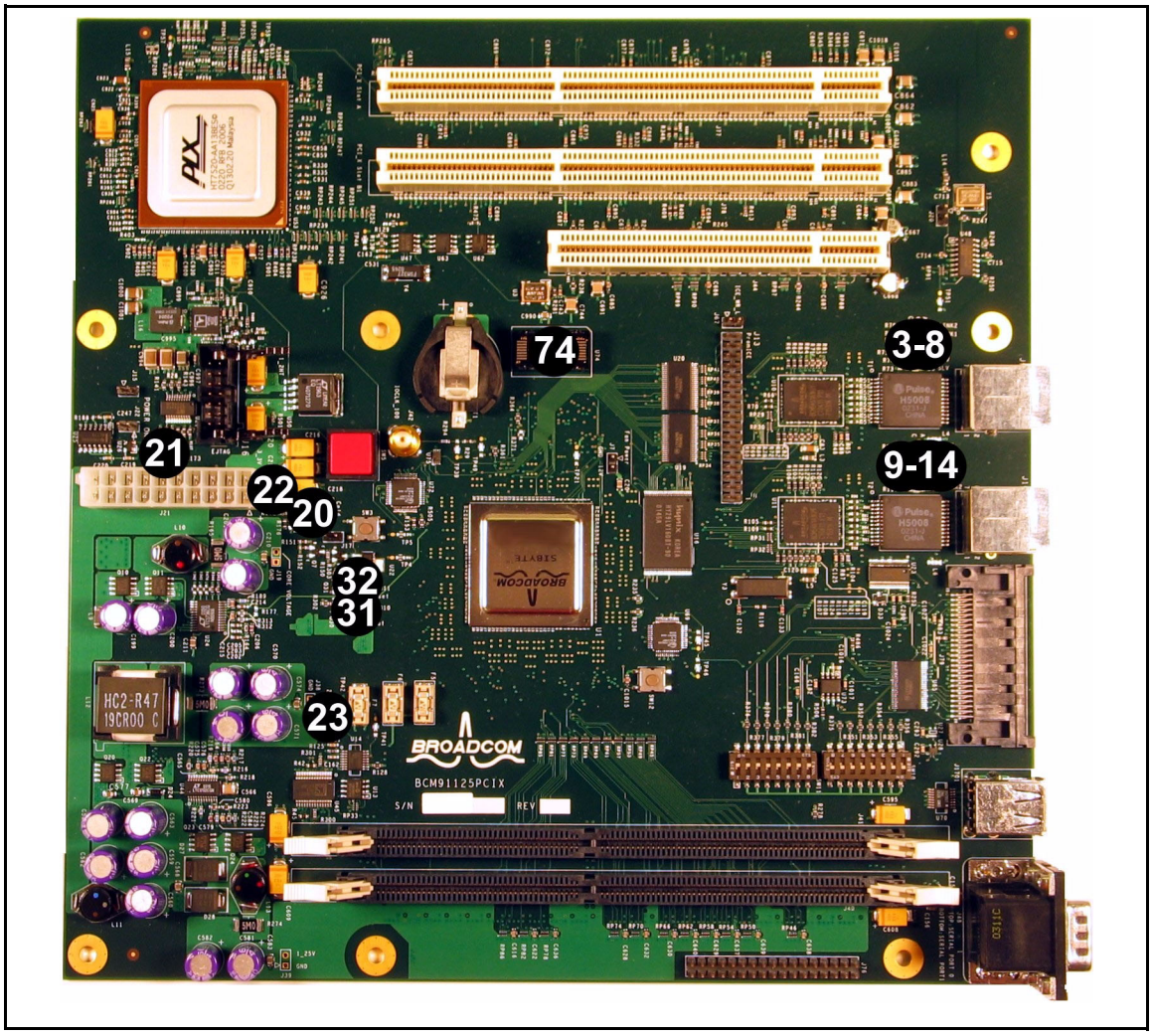

Figure 6: LED Callouts

Table 3: *LED Descriptions*

Board ID	*Color*	*Description*
D3	Green	PHY 0 Slave indicator
D4	Green	PHY 0 Receive indicator
D5	Green	PHY 0 Transmit indicator
D6	Green	PHY 0 Full-duplex indicator
D7	Green	PHY 0 Link 1 indicator
D8	Green	PHY 0 Link 2 indicator
D9	Green	PHY 1 Slave indicator
D10	Green	PHY 1 Receive indicator
D11	Green	PHY 1 Transmit indicator
D12	Green	PHY 1 Full-duplex indicator
D13	Green	PHY 1 Link 1 indicator
D14	Green	PHY 1 Link 2 indicator
D20	Green	1.2V BCM1125 Core Power good indicator
D21	Green	5V Power good indicator
D22	Green	3.3V Power good indicator
D23	Green	2.5V Power good indicator
D31	Red	RESET_OUT active indicator
D32	Red	COLD_RESET active indicator
U74	Green	Four-character LED display

JUMPERS, FUSES, AND BATTERY

Figure 7 shows the positions of the jumpers, fuses, and battery alpha-numerically. Compare Figure 7's alpha-numeric callouts with a description of each jumper, fuse, or battery in Table 4.

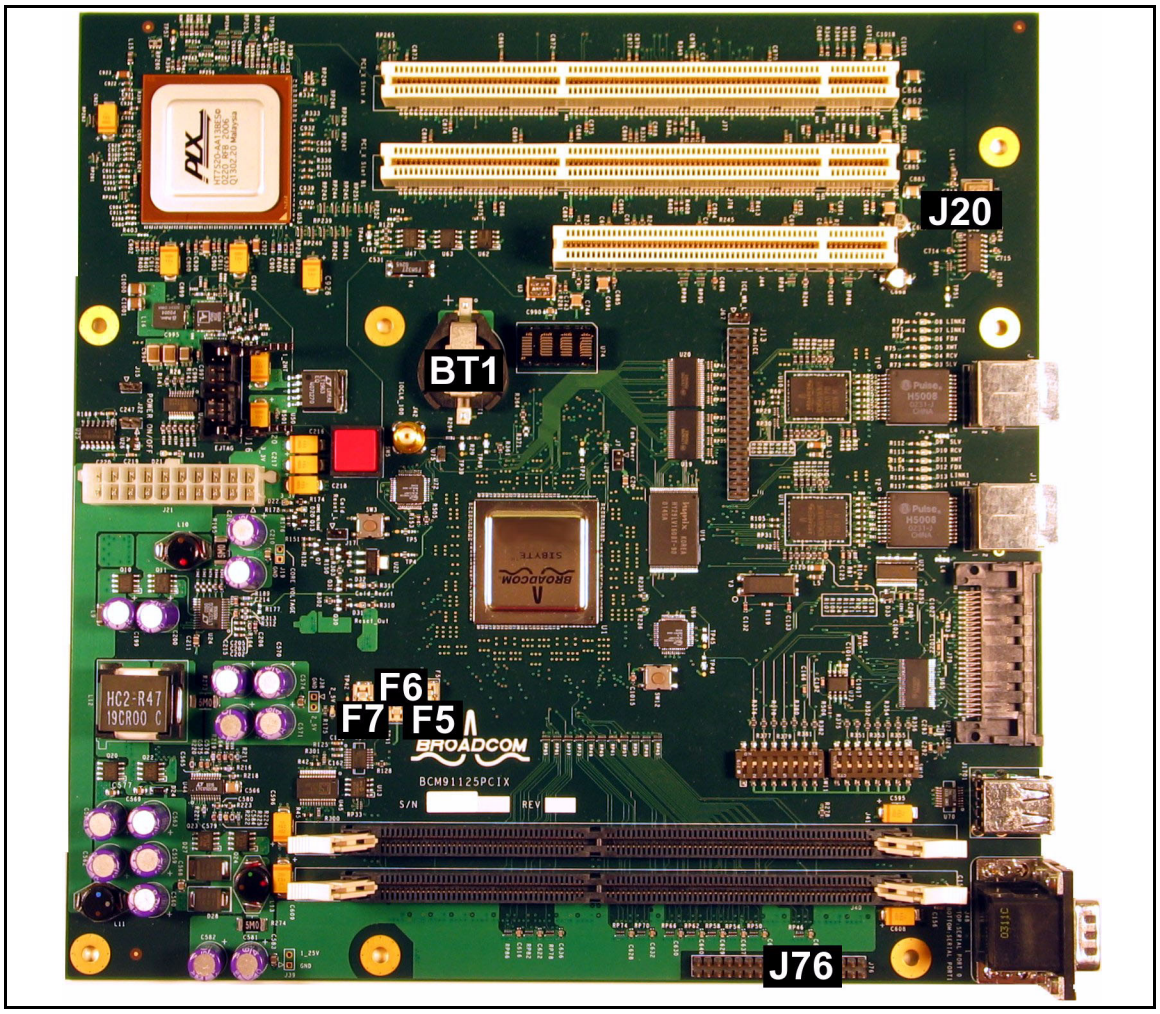

Figure 7: Jumper, Fuse, and Battery Callouts

Table 4: *Jumper, Fuse, and Battery Descriptions*

Board ID	*Function*
J20	32b PCI clock select (open * = run at slowest PCI agent; closed = force 33 MHz)
J76	Static configuration jumpers (See Table 5 for more details)
F5	USB slot0 5V, 1A current limit fuse
F6	USB slot1 5V, 1A current limit fuse
F7	EJTAG 3.3V, 1A current limit fuse
BT1	RTC battery
* = default	

Note: The table layout reflects the physical location of the pins on this header. The top of the header (where pin 1 exists) is where the “J76” designator is on the board silkscreen.

Note: Jumpers should only be used to connect the odd pin with the even pin directly across from it (for example, where pin 1 is connected to pin 2). Other connections could permanently damage the board.

Table 5: *Static Configuration Jumper (J76) Settings*

Odd Pin Name	*Odd Pin #*	*Even Pin #*	*Even Pin Name*	*Open Function*	*Closed Function*
3.3 V PWR	1	2	* CPU clock divider pll_div[0]	Open = Off (for switches SW11/ SW12)	Closed = On
3.3 V PWR	3	4	* CPU clock divider pll_div[1]	See Table 6 for configuration details	
3.3 V PWR	5	6	* CPU clock divider pll_div[2]		
3.3 V PWR	7	8	* CPU clock divider pll_div[4]		
GND	9	10	* CPU clock divider pll_div[3]		
RICE_IO_WR_L	11	12	reserved	N/A	N/A
3.3 V PWR	13	14	* BCM1125H software config[0]	Open = Off (for switches SW11/ SW12)	Closed = On
3.3 V PWR	15	16	* BCM1125H software config[1]	See Table 6 for configuration details.	
3.3 V PWR	17	18	* BCM1125H software config[2]		

* = Static configuration is also controlled by either switch SW11 or SW12. These signals are electrically OR’ed together, so if either is “On” in the case of the switches (SW11 or SW12), or “Closed” in the case of the jumper (J76), the “On”/“Closed” value is selected. Otherwise, both must be “Off” or “Open” to select the “Off”/”Closed” value.

Table 5: *Static Configuration Jumper (J76) Settings (Cont.)*

Odd Pin Name	*Odd Pin #*	*Even Pin #*	*Even Pin Name*	*Open Function*	*Closed Function*
3.3 V PWR	19	20	* BCM1125H software config[3]	See Table 6 for configuration details.	
3.3 V PWR	21	22	* BCM1125H software config[4]		
3.3 V PWR	23	24	* BCM1125H software config[5]		
GND	25	26	Boot ROM select	Boot from Flash.	Boot from PROMICE.
3.3 V PWR	27	28	* System byte order	Little Endian	Big Endian
GND	29	30	Cold Reset COLDRES_L	Cold Reset inactive	Cold Reset active
3.3 V PWR	31	32	* IOB0 clock divider iob0_div		
3.3 V PWR	33	34	* IOB1 clock divider iob1_div		

* = Static configuration is also controlled by either switch SW11 or SW12. These signals are electrically OR'ed together, so if either is "On" in the case of the switches (SW11 or SW12), or "Closed" in the case of the jumper (J76), the "On"/"Closed" value is selected. Otherwise, both must be "Off" or "Open" to select the "Off"/"Closed" value.

SWITCHES

Figure 8 shows the positions of switches numerically. Compare Figure 8's number callouts with a description of each switch in Table 6.

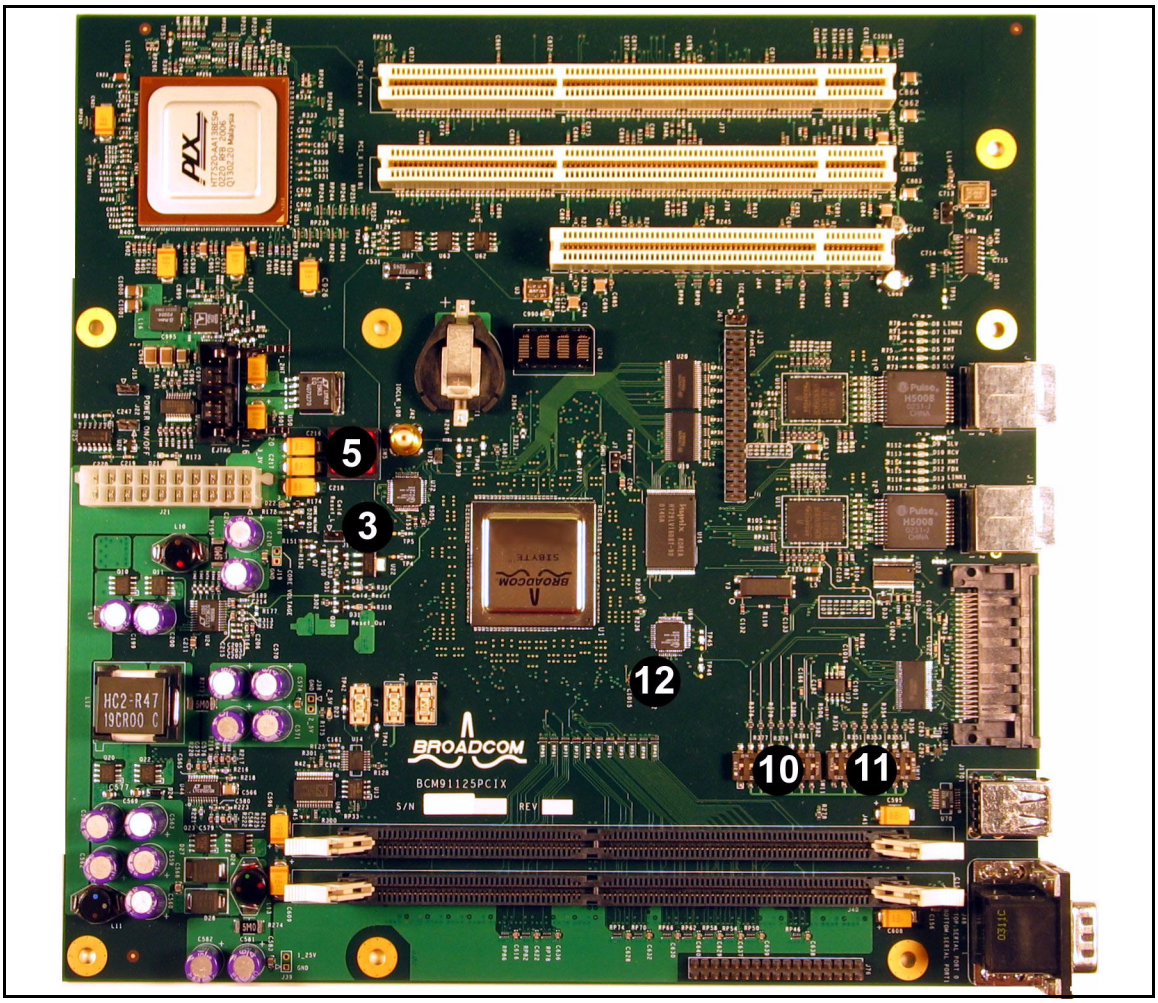

Figure 8: Switch Callouts

Table 6: *Switch Descriptions*

Board ID	*Function*	*Default*
SW3	Cold Reset asserted when the button is pressed	N/A
SW5	Power toggled on or off when pressed	N/A
SW10	8-position DIP switch, for board configuration dip[8:1]	
	dip[8] = reserved	off
	dip[7] = System byte order (on = big endian; off = little endian)	on

Table 6: *Switch Descriptions (Cont.)*

Board ID	*Function*	*Default*
	dip[6:1] = BCM1125H software config[5:0] bits. See Table 14 for more information.	off, off, off, off, on, off
SW11	8-position DIP switch, for BCM1125 clk configuration dip[1:8]	See specific bits below.
	dip[1] = reserved	off
	dip[2] = IOB1 clock divider iob1_div (off = /3; on = /2) dip[3] = IOB0 clock divider iob0_div (off = /4; on = /3)	Depends on BCM1125H speed bin. See Table 8 for acceptable settings.
	dip[4] = CPU clock divider pll_div[4] (off = 0; on = 1) dip[5] = CPU clock divider pll_div[[3] (off = 1; on = 0) dip[6:8] = CPU clock divider pll_div[2:0] (off = 0; on = 1)	Depends on BCM1125H speed bin. See Table 7 for acceptable settings.
SW12	NMI (GPIO 0) asserted when the button is pressed	N/A

ACCEPTABLE PLL SETTINGS

Table 7 shows acceptable PLL settings. Adjusting dip switch SW11 changes the multiplier of the CLK100.

Note: The default PLL settings are set according to the speed bin of the BCM1125H part. That setting is the maximum clock speed that the chip can attain without failure.

Table 7: *Acceptable PLL Settings*

SW11 dip[4:8] settings	*pll_div[4:0]*	*CLK100 MHz Multiplier*	*CPU clock (MHz)*
off,off,on,off,off	01100	6.0x	600
off,off,on,off,on	01101	6.5x	650
off,off,on,on,off	01110	7.0x	700
off,off,on,on,on	01111	7.5x	750
on,off,off,off,off	11000	8.0x	800
on,off,off,off,on	11001	8.5x	850
on,off,off,on,off	11010	9.0x	900
on,off,off,on,on	11011	9.5x	950
on,off,on,off,off	11100	10.0x	1000

SUPPORTED DRAM

Although this board ships with two 256MB DDR SDRAM DIMMs, it can support other DIMMs as well. This includes standard PC2100 and PC2700 DDR SDRAM DIMMs, either buffered or unbuffered and with or without ECC.

Note: Both DIMMs must operate at the same speed since there is only a single memory channel.

ACCEPTABLE I/O BRIDGE SETTINGS

The BCM1125H contains two bridges which isolate many of the chip's SOC components from the core, L2 cache, and other components. More details about these bridges can be found in the user manual for the specific chip. The clocking for these bridges is determined by dividing the CPU clock. The allowable divide ratios for a given bridge at a certain CPU frequency are provided below.

See Table 6 on page 16 for the details on setting these values.

Table 8: *Acceptable I/O Bridge Settings*

CPU Clock (MHz)	*IOB0 Divide Ratio*	*IOB1 Divide Ratio*
600-650	3 or 4	2 or 3
700-1000	3 or 4	3

BCM1125H PERIPHERAL DEVICES

Table 9: *SMBus Peripherals*

SMBus Channel	*SMBus Address*	*Description*
0	0x2A	Maxim MAX6654 temperature sensor
0	0x50	Microchip 28LC128C EEPROM
0	0x54	DDR SDRAM DIMM Slot 0 SPD
0	0x55	DDR SDRAM DIMM Slot 1 SPD
1	0x68	ST Microelectronics M41T81 RTC

Table 10: *Generic Bus Peripherals*

Chip Select #	*Description*
CS0	Hynix HY29LV160 boot flash memory or ROM Emulator (depending on J76 setting)
CS1	ROM Emulator or Hynix HY29LV160 boot flash memory (depending on J76 setting)
CS3	Infineon SLG2016 four character LED display
CS4	Cypress SL811HS USB Slot 0
CS5	Cypress SL811HS USB Slot 1
CS6	Compact Flash (CF) Slot

Table 11: *GPIO Map*

GPIO Pin #	*BCM1125H Pin Direction*	*Description*
0	Input	NMI_L (from switch SW12)
1	Input	OUT from RTC.
2	Input	PHY_INTERUPT_L (ORed PHY interrupt from both BCM5461 PHY chips)
3	Input	USB Slot 0 interrupt
4	Input	USB Slot 1 interrupt
5	Input	TEMP_ALERT_L from the temperature sensor
6	Output	Compact Flash Chip Enable 1 (CF_CE_L1)
7	Output	Compact Flash Chip Enable 2 (CF_CE_L2)
8	Output	Compact Flash Reset (CF_RESET)
9	Input	Compact Flash Ready Buffer (CF_READY_BUF)
10	Output	Compact Flash Reg (CF_REG)
11	Input	Compact Flash WP Buffer (CF_WP_BUF)
12	Input	Compact Flash CD 1 (CF_CD_L1)
13	Input	Compact Flash CD 2 (CF_CD_L2)
14	Input	Compact Flash VS 1 (CF_VS_L1)
15	Input	Compact Flash VS 2 (CF_VS_L2)

Table 12: *PCI/X Interrupt Map*

Description	*Interrupt Map*
32b PCI connector (J44).	BCM1125H PCI INTA = PCI Connector INTA. BCM1125H PCI INTB = PCI Connector INTB. BCM1125H PCI INTC = PCI Connector INTC. BCM1125H PCI INTD = PCI Connector INTD.
64b PCI-X Slot A (J77).	PLX HT7520 PCI-X Bus A INTA = PCI-X Slot A INTD. PLX HT7520 PCI-X Bus A INTB = PCI-X Slot A INTA. PLX HT7520 PCI-X Bus A INTC = PCI-X Slot A INTB. PLX HT7520 PCI-X Bus A INTD = PCI-X Slot A INTC.
64b PCI-X Slot B (J78).	PLX HT7520 PCI-X Bus B INTA = PCI-X Slot B INTD. PLX HT7520 PCI-X Bus B INTB = PCI-X Slot B INTA. PLX HT7520 PCI-X Bus B INTC = PCI-X Slot B INTB. PLX HT7520 PCI-X Bus B INTD = PCI-X Slot B INTC.

Section 4: Firmware Configuration

The firmware image in the flash is bi-endian, so it supports both big and little-endian operation. The following table describes where and how much physical memory the firmware maps to the chip selects on the generic bus.

Table 13: *Firmware Generic Bus Memory Mapping*

Chip Select	*Description*	*Physical Memory Address*	*Size*
CS0	Boot ROM	0x1FC0_0000	2 MB
CS1	Alternate Boot ROM	0x1F80_0000	2 MB
CS3	LED Display	0x100A_0000	64 KB
CS4	USB Slot 0	0x100B_0000	64 KB
CS5	USB Slot 1	0x100C_0000	64 KB
CS6	Compact Flash	0x1100_0000	64 MB

Table 14: *Firmware Configuration Bits Mapping*

SW10 dip #	*Software cfg bit #*	*Name*	*Action*
1	0	PROMICE Console	off * = UART0 console; on = PROMICE console.
3	2	Configure PCI	off = don't configure PCI; on * = configure PCI.
4	3	Autostartup	off * = ignore STARTUP env. variable; on = execute STARTUP env. variable command after init.
* = recommended/default setting. All other settings are reserved.			

Section 5: Troubleshooting

Corrective Procedures

1. When CFE is not able to initialize the system and reach the console prompt, the four-character alphanumeric LED display may be used to help debug the initialization sequence. When the Cer2 message appears, a cache error has occurred. This frequently occurs when the BCM1125H is either undercooled or is in a low-voltage situation. Ensure that the correct voltage and cooling is being provided. For other LED message descriptions, refer to the *Common Firmware Environment (CFE) Specification* document.
2. There is no output coming from the serial boot console, but the four-character LED displays *CFE*. Because CFE uses serial port 0 by default, ensure that a standard 9-pin RS232 null-modem cable connection is being used. Also ensure that the terminal program is set to a baud rate of 115200, 8-bit, no parity, no flow control.

Replacement Parts

Table 15: *Replacement Parts*

Board ID	*Description*	*Manufacturer*	*Manufacturer ID*	*Web Information*
F5, F6	USB 5V, 1A current limit fuse	Littelfuse®	154001	http://www.littelfuse.com/data/Data_Sheets/154.pdf
F7	EJTAG 3.3V, 1A current limit fuse			
BT1	3V Li RTC battery	various	CR2032	

Section 6: Web Resources

SiByte

Table 16: *SiByte Web Resources*

Resource	*Website*
BCM1250 and BCM1125H User Manual	http://sibyte.broadcom.com/public/resources/
SB-1 Core User Manual	
General information	http://sibyte.broadcom.com/public/

Peripherals

Table 17: *Peripheral Web Resources*

Resource	*Website*
Maxim MAX6654 temperature sensor	http://pdfserv.maxim-ic.com/en/ds/MAX6654.pdf
Microchip 24LC128C serial EEPROM	http://www.microchip.com/1010/pline/memory/memdvice/ic/64to512/devices/24lc128/index.htm
ST Microelectronics M41T81serial RTC	http://www.st.com/stonline/products/families/memories/rtc/nv_t81.htm
Infineon SLG2016 four-character alphanumeric display	http://www.infineon.com/cgi/ecrm.dll/jsp/home.do?lang=EN
Micron MT9VDDT1672AG-265 128 MB 266 MHz DDR SDRAM ECC	http://micron.com/products/modules/ddrsdram/part.aspx?part=MT9VDDT1672AG-265
Hynix HY29LV160 2 MB flash memory	http://www.hynix.com/datasheet/kor/flash/detail11.jsp?PartNo=HY29LV160
Cypress SL811HS dual-speed USB Embedded Host controller	http://www.cypress.com/products/datasheet.cfm?partnum=SL811HS
Broadcom BCM5461 10/100/1000BASE-T Gigabit Copper Transceiver	http://www.broadcom.com/products/product.php?product_id=BCM5421

BUS INTERFACE

Table 18: *Bus Interface Web Resources*

Resource	*Website*
HyperTransport specification	http://www.hypertransport.org/doc_specifications.htm
PCMCIA specification	http://www.pcmcia.org/pccardstandard.htm
EJTAG specification	http://www.mips.com/content/Documentation/MIPSDocumentation/EJTAG/doclibrary/
PCI specification	http://www.pcisig.com/specifications/conventional/
PCI-X specification	http://www.pcisig.com/specifications/pcix_20/
USB specification	http://www.usb.org/developers/docs/

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, CA 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710