USER MANUAL

BCM91250A

Evaluation Board

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91250A-UM100-R
05/18/04

REVISION HISTORY

Revision	*Date*	*Change Description*
91250A-UM100-R	05/18/04	Initial release.

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Section 1: Product Overview

INTRODUCTION

The BCM91250A Evaluation Board is an evaluation platform intended to support the needs of prospective users of the BCM1250 processor.

This manual describes how to locate, configure, and observe the various connectors, switches, jumpers, and LEDs on the BCM91250A. This fundamental background allows software development and evaluation of the BCM1250 processor to begin.

For additional information on this board and the BCM1250 processor, go to:

http://sibyte.broadcom.com/public/

ITEMS INCLUDED WITH YOUR SHIPMENT

- BCM91250A evaluation board in ATX case with power supply and power cable
- Corelis PIO-1149.1/E parallel port boundary scan (JTAG) controller board
- This document

FEATURES

This section describes BCM91250A features.

HARDWARE

- BCM1250 processor
- ATX form factor board mounted in case with a power supply (AC Input: 115V/230V, 10A/5A, 60Hz/50Hz; DC Output: 230W)
- Four DDR SDRAM DIMM slots
  - Ships with two 128MB PC2100 (266 Mhz) w/ ECC DIMMs
- Two 10/100/1000 Mbps Ethernet with RJ-45 interface
- NTSC/PAL video decoder
- Two serial ports
  - port 0 configured as standard asynchronous UART with RS232 interface
  - port 1 multiplexed between asynchronous UART with RS232 interface or synchronous Crystal CS4297A Audio codec
- HT to PCI bridge
- Two 3.3 V only, 66 MHz 32b and two 3.3V only, 66 MHz 64b PCI connectors
- Two HyperTransport (HT) connectors
- 2MB Flash ROM
- ROM emulator connector
- Two SMBus channels with the following devices connected:

  - real-time clock (RTC)
  - EEPROMs
  - Temperature sensor
  - DIMMs' SPDs
- IDE interface for ATA/ATAPI PIO mode 3 compliant devices
- Two USB connectors
- EJTAG connector
- Four-character LED display
- PCMCIA interface for single memory or I/O card

FIRMWARE

The Common Firmware Environment (CFE) is designed to be easily portable to designs incorporating current and future Broadcom MIPS64-compatible broadband processors. Supported platforms include Broadcom's SiByte processor family (BCM1250, BCM1125H, and so forth) 32-bit and 64-bit memory models, and big and little-endian operation. There are many parameters configurable at build time that may be used to customize CFE to suit diverse customer requirements.

On the BCM91250A, CFE can load programs (such as S-records, raw binary, or ELF formatted) from bootstrap devices in a variety of ways, including:

- Via either Ethernet port, from a TFTP server
- Via the serial port (S-records only)
- Via an IDE disk connected to the BCM1250's generic bus
- Via an IDE CD-ROM drive connected to the BCM1250's generic bus
- Via a PCMCIA flash card in the PCMCIA slot

For additional information on CFE, refer to the Common Firmware Environment (CFE) Specification document that can be found in the CFE source code distribution at:

http://sibyte.broadcom.com/public/

BCM91250A Front Panel

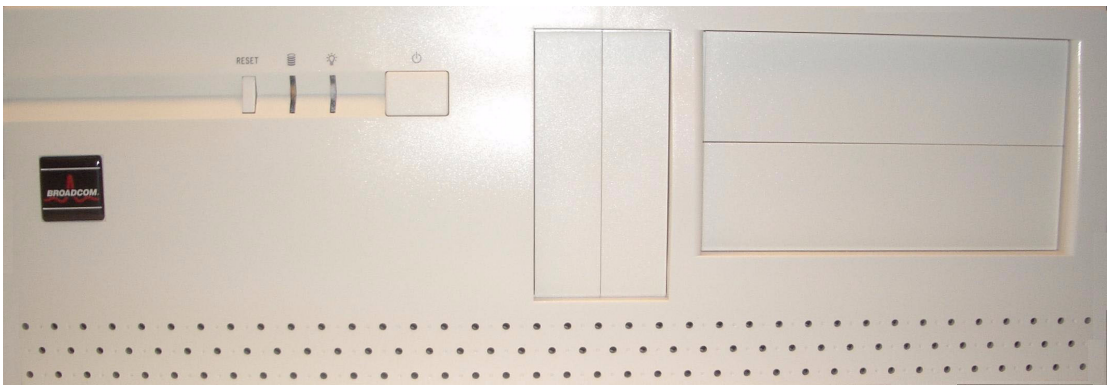

Figure 1: BCM91250A Front Panel

BCM91250A Rear Panel

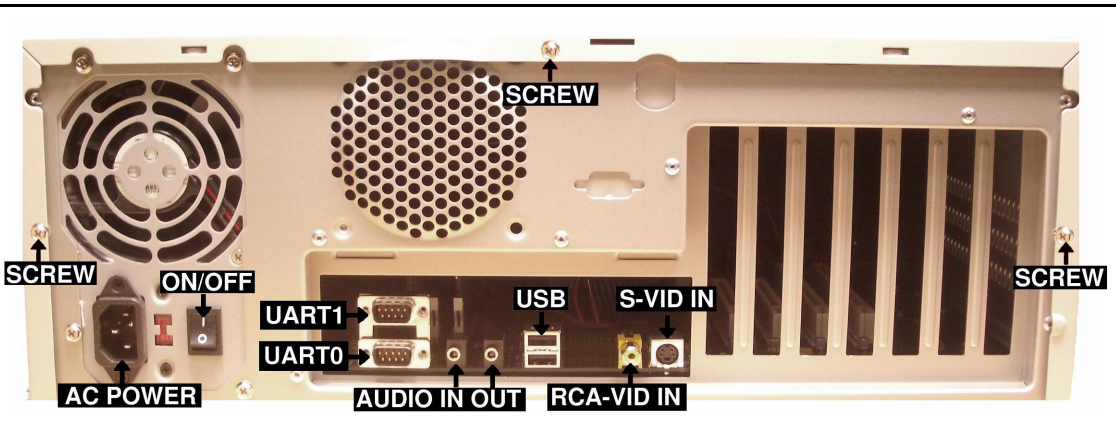

Figure 2: BCM91250A Rear Panel

Section 2: Getting Started

Complete the following steps to get to a BCM91250A CFE (firmware) prompt.

1. In order to connect to the Ethernet ports, the case cover must be removed. This requires removing three screws on the back of the case. Refer to the picture below for the location of the screws (labeled "SCREW"). Once the screws are removed, the cover should easily slide off in the direction of the rear panel. Now a standard CAT 5 cable with RJ45 connector can be inserted into an Ethernet port.
2. Connect a 9-pin null modem cable to the serial port of the BCM91250A and to a serial port on a workstation/PC.
3. Use a terminal program and set it to 115200 bps, 8-bit data, 1-stop bit, no parity, and no flow control.
4. Power up the BCM91250A by plugging in the provided cable to the power supply socket on the back of the box and into a wall socket. Then hit the power button on the front panel."

   After a short delay, the CFE initialization output and serial console prompt should display. The following is an example of the output:

```
CFE version 1.0.36 for SWARM (64bit,MP,BE)
Build Date: Thu Jan 16 14:41:34 PST 2003
Copyright (C) 2000,2001,2002 Broadcom Corporation.

Initializing Arena.
Initializing PCI. [normal]
HyperTransport: 400 MHz
PCI bus 0 slot 0/0: SiByte, Inc. BCM1250 PCI Host Bridge (host bridge, revision
0x02)
PCI bus 0 slot 1/0: SiByte, Inc. BCM1250 HyperTransport Host Bridge (host bridge,
revision 0x02)
PCI bus 0 slot 7/0: Opti RM861HA (USB serial bus, interface 0x10, revision 0x10)
PCI bus 1 slot 1/0: API Networks SP1011 HyperTransport-PCI Bridge (PCI bridge)
Initializing Devices.
SWARM board revision 3
PCIIDE: 0 controllers found
Config switch: 2
CPU: BCM1250 B2
L2 Cache Status: OK
Wafer ID: Not set
SysCfg: 0000000028DB0700 [PLL_DIV: 14, IOB0_DIV: CPUCLK/4, IOB1_DIV: CPUCLK/3]
CPU type 0x1040102: 700MHz
Total memory: 0x10000000 bytes (256MB)

Total memory used by CFE: 0x8FE85160 - 0x90000000 (1552032)
Initialized Data: 0x8FE85160 - 0x8FE8F040 (40672)
BSS Area: 0x8FE8F040 - 0x8FE8F6F0 (1712)
Local Heap: 0x8FE8F6F0 - 0x8FF8F6F0 (1048576)
Stack Area: 0x8FF8F6F0 - 0x8FF916F0 (8192)
Text (code) segment: 0x8FF91700 - 0x8FFFFFBC (452796)
Boot area (physical): 0x0FE44000 - 0x0FE84000
Relocation Factor: I:F0391700 - D:0FE84160

CFE>
```

5. At the prompt, a program can be run via the network from a TFTP server by doing the following:
   a. Connect the BCM91250A Ethernet port E0 with an Ethernet cable to a switch, repeater, or directly to the Ethernet port of the file server.

Note: Because the Broadcom PHYs handle direct connects automatically, a crossover cable for direct connects is not needed.

b. To initialize Ethernet port E0, type the following:

```
ifconfig eth0 -auto
```

Note: The ifconfig eth0 -auto command can only be used with a DHCP server.

c. To run a program, type the following:

```
boot -elf tftp_server:/path_to_software/program
```

Section 3: Physical Description

The BCM91250A is implemented in the standard ATX form factor. It is housed in an ATX 2.0 compliant enclosure and ships with a power supply. Figure 3 shows a top view of the BCM91250A.

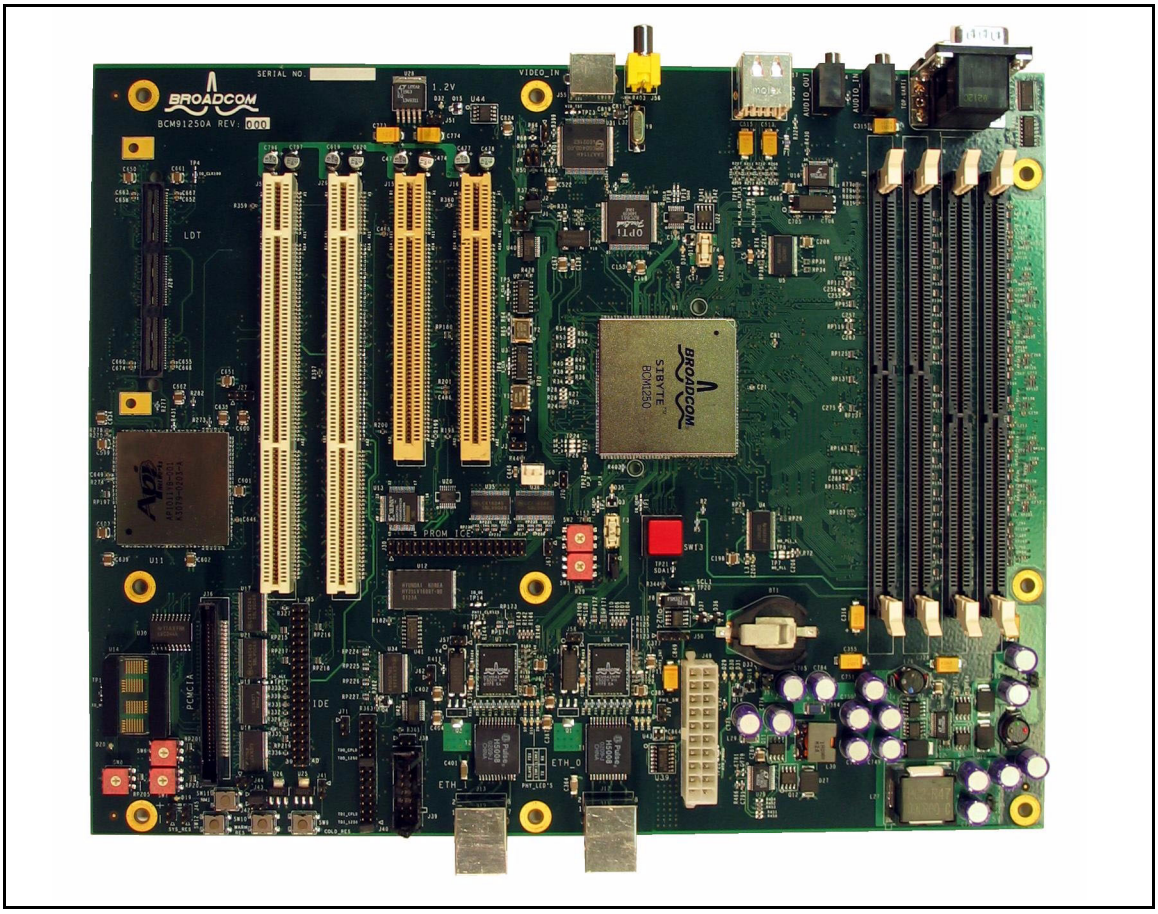

Figure 3: BCM91250A Top View

BLOCK DIAGRAM

Figure 4 shows a block diagram of the BCM91250A.

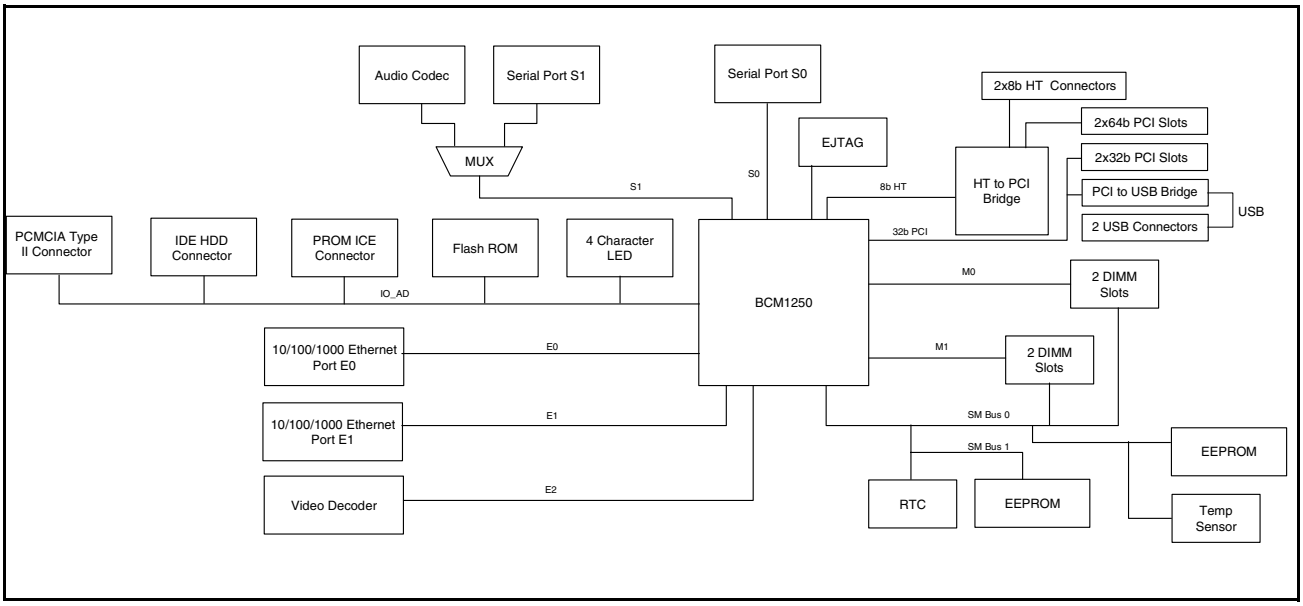

Figure 4: BCM91250A Block Diagram

CONNECTORS

BOARD CONNECTORS

Figure 5 shows the board and identifies connectors numerically. Compare Figure 5 number callouts with Table 1 for a description of each connector callout.

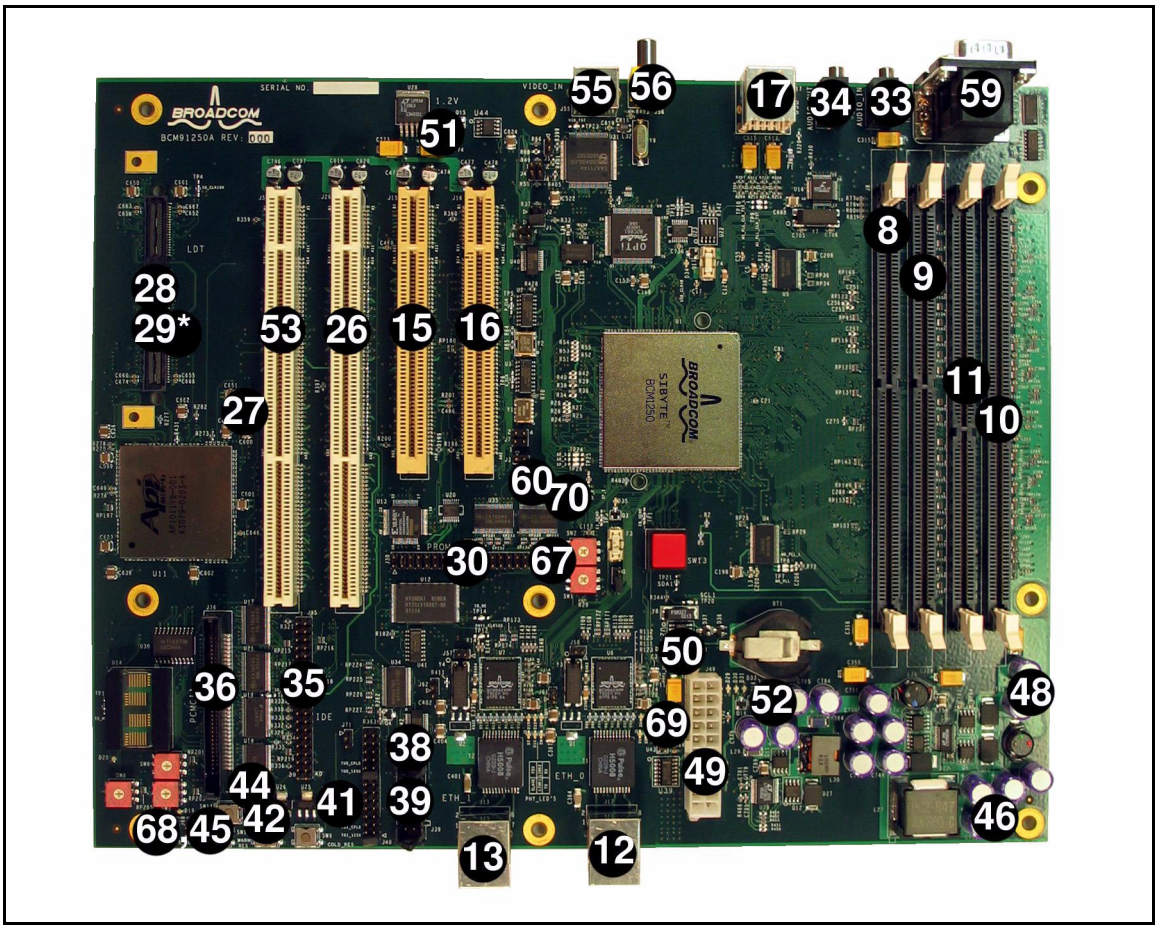

Figure 5: Connector Callouts

Table 1 shows BCM91250A connectors.

Note: For the nonstandard connectors which have their pins described below you can locate pin 1 on the board by finding the arrow that points to it on the PCB silkscreen. In some cases for connectors with multiple rows and columns of pins, the pin numbers at the corners of the connector are written on the PCB silkscreen.

Table 1: *Connector Descriptions*

Board ID	*Description*
J8	DDR SDRAM DIMM slot, MC channel 0, slot 0 (CS 0/1)
J9	DDR SDRAM DIMM slot, MC channel 0, slot 1 (CS 2/3)
J10	DDR SDRAM DIMM slot, MC channel 1, slot 0 (CS 0/1)
J11	DDR SDRAM DIMM slot, MC channel 1, slot 1 (CS 2/3)
J12	10/100/1000 Ethernet MAC0
J13	10/100/1000 Ethernet MAC1
J15	3.3V, 32b PCI slot, BCM1250 PCI device 5
J16	3.3V, 32b PCI slot, BCM1250 PCI device 6
J17	Dual stack USB ports
J26	3.3V, 64b PCI slot, SP1011 PCI device 0
J27	SP1011 SMBus (pin 1 = GND, pin 2 = SROM_SDA, pin 3 = SROM_SCL)
J28	HyperTransport socket for motherboards (see Table 2 on page 10)
J29*	HyperTransport header for daughtercards (see Table 2 on page 10)
J30	ROM Emulator connector (see Table 3 on page 12)
J33	Audio codec line in
J34	Audio codec line out
J35	IDE hard disk connector. Please see “IDE Connector (J35) Pin 20 Rework” on page 13 for more details.
J36	PCMCIA card connector
J38	DEBUG_L trigger for scope (pin 1= GND, pin 2 = DEBUG_L)
J39	BCM1250 EJTAG connector
J41	External Cold Reset switch connector (pin 1 = GND, pin 2 = COLDRES_L)
J42	External Warm Reset switch connector (pin 1 = GND, pin 2 = WARM_RESET_L)
J44	External NMI (GPIO 3) switch connector (pin 1 = GND, pin 2= NMI_L)
J45	External System Reset switch connector (pin 1 = GND, pin 2 = SYS_RESET_L)
J46	2.5V supply sense (pin 1 = GND, pin 2 = 2.5V)
J48	1.25V supply sense (pin 1 = GND, pin 2 = 1.25V)
J49	ATX power connector
J50	Bench supply connector (pin 1 = GND, pin 2 = 3.3V, pin 3 = 5V, pin 4 = ATX 5V Standby)
J51	1.2V supply sense (pin 1 = GND, pin 2 = 1.2V)
J52	1.2V core supply sense (pin 1 = GND, pin 2 = 1.2V)
J53	3.3V, 64b PCI slot, SP1011 PCI device 1
J55	S-Video input
J56	RCA video input
* = a connector located on the bottom of the board.	

Table 1: *Connector Descriptions (Cont.)*

Board ID	*Description*
J59	Dual DB-9 used by UARTs (top = UART 0, bottom = UART 1)
J60	Fan (pin 1 = no connect, pin 2 = 12VDC, pin 3 = GND)
J67	ROM emulator write line (pin 1 = IO_WR_L, pin 2 = no connect)
J68	External HDD activity LED connector (pin 1 = HD_ACTIVE_L, pin 2 = 5V)
J69	External Power switch connector (pin 1 = IN, pin 2 = GND)
J70	Alternate Fan (pin 1 = GND, pin 2 = 12VDC).
* = a connector located on the bottom of the board.	

PINOUT FOR HYPERTRANSPORT SOCKETS (J28 AND J29)

Note: The table layout reflects the physical location of the pins on the connector. The middle pins (121-132) are not shown though since they are all connected to ground (GND).

More information about these connectors can be found in "Web Resources" on page 26.

Table 2: *Pinout For Hypertransport Sockets (J28 and J29)*

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
VDD33	1	2	VDD33
VDD33	3	4	VDD33
VDDLDT	5	6	VDDLDT
GND	7	8	GND
TCK	9	10	CLK100
TMS	11	12	GND
TDI	13	14	RDY
TDO	15	16	OE_L
TRST_L	17	18	WR_L
SCL	19	20	CS_L0
SDA	21	22	CS_L1
LDT_RESET_L	23	24	INT
LDT_PWROK	25	26	RESET_L
GND	27	28	GND
LDT_RX_CTLn	29	30	LDT_TX_CADp0
LDT_RX_CTLp	31	32	LDT_TX_CADn0
GND	33	34	GND
LDT_RX_CADn7	35	36	LDT_TX_CADp1
LDT_RX_CADp7	37	38	LDT_TX_CADn1
GND	39	40	GND
GND	41	42	GND

Table 2: *Pinout For Hypertransport Sockets (J28 and J29) (Cont.)*

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
LDT_RX_CADn6	43	44	LDT_TX_CADp2
LDT_RX_CADp6	45	46	LDT_TX_CADn2
GND	47	48	GND
LDT_RX_CADn5	49	50	LDT_TX_CADp3
LDT_RX_CADp5	51	52	LDT_TX_CADn3
GND	53	54	GND
LDT_RX_CADn4	55	56	LDT_TX_CLKp
LDT_RX_CADp4	57	58	LDT_TX_CLKn
GND	59	60	GND
GND	61	62	GND
LDT_RX_CLKn	63	64	LDT_TX_CADp4
LDT_RX_CLKp	65	66	LDT_TX_CADn4
GND	67	68	GND
LDT_RX_CADn3	69	70	LDT_TX_CADp5
LDT_RX_CADp3	71	72	LDT_TX_CADn5
GND	73	74	GND
LDT_RX_CADn2	75	76	LDT_TX_CADp6
LDT_RX_CADp2	77	78	LDT_TX_CADn6
GND	79	80	GND
GND	81	82	GND
LDT_RX_CADn1	83	84	LDT_TX_CADp7
LDT_RX_CADp1	85	86	LDT_TX_CADn7
GND	87	88	GND
LDT_RX_CADn0	89	90	LDT_TX_CTLp
LDT_RX_CADp0	91	92	LDT_TX_CTLn
GND	93	94	GND
AD0	95	96	AD9
AD1	97	98	AD24
AD2	99	100	AD25
AD3	101	102	AD26
AD4	103	104	AD27
AD5	105	106	AD28
AD6	107	108	AD29
AD7	109	110	AD30
AD8	111	112	AD31
GND	113	114	GND
VDDLDT	115	116	VDDLDT
VDD33	117	118	VDD33
VDD33	119	120	VDD33

ROM EMULATOR PINOUT

Note: The table layout reflects the physical location of the pins on the connector. Also all I/O signals are 3.3 V outputs that are tolerant of 5V inputs.

Table 3: ***ROM Emulator Pinout***

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
GND	1	2	AD20
P3300 (3.3 V PWR)	3	4	AD19
AD18	5	6	AD16
AD17	7	8	AD15
AD14	9	10	AD12
AD13	11	12	AD7
AD8	13	14	AD6
AD9	15	16	AD5
AD11	17	18	AD4
OE_L	19	20	AD3
AD10	21	22	AD2
ROMEMUCS_L	23	24	AD1
AD31	25	26	AD0
AD30	27	28	AD24
AD29	29	30	AD25
AD28	31	32	AD26
AD27	33	34	GND

IDE Connector (J35) Pin 20 Rework

To use a keyed IDE cable (a cable with pin 20 blocked to prevent incorrect insertion) with the BCM91250A board, you'll need to bend down pin 20. This is easily done with a small flat-head screwdriver after you have located the pin. To find pin 20, count down the 2nd column (even column) in twos from pin 2 till you arrive at pin 20.

This pin is approximately halfway down the connector on the right-hand side (see Figure 3). By bending the pin down to the right until it is parallel to the board plane (in Figure 6 that is near the text labeled "<-pin 20"), this allows the IDE cable to properly seat on the connector while preventing the risk of shorting other connectors on the board.

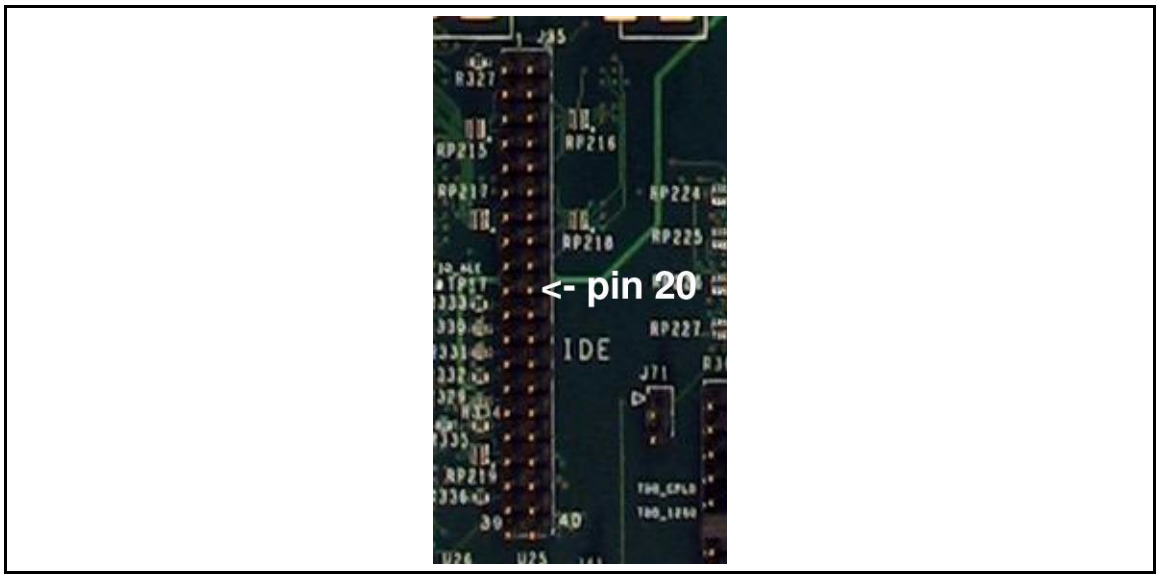

Figure 6: IDE Connector (J35) Pin 20 Rework

LEDs

Figure 7 shows the positions of the LEDs numerically. Compare Figure 7 number callouts with a description of each LED in Table 4.

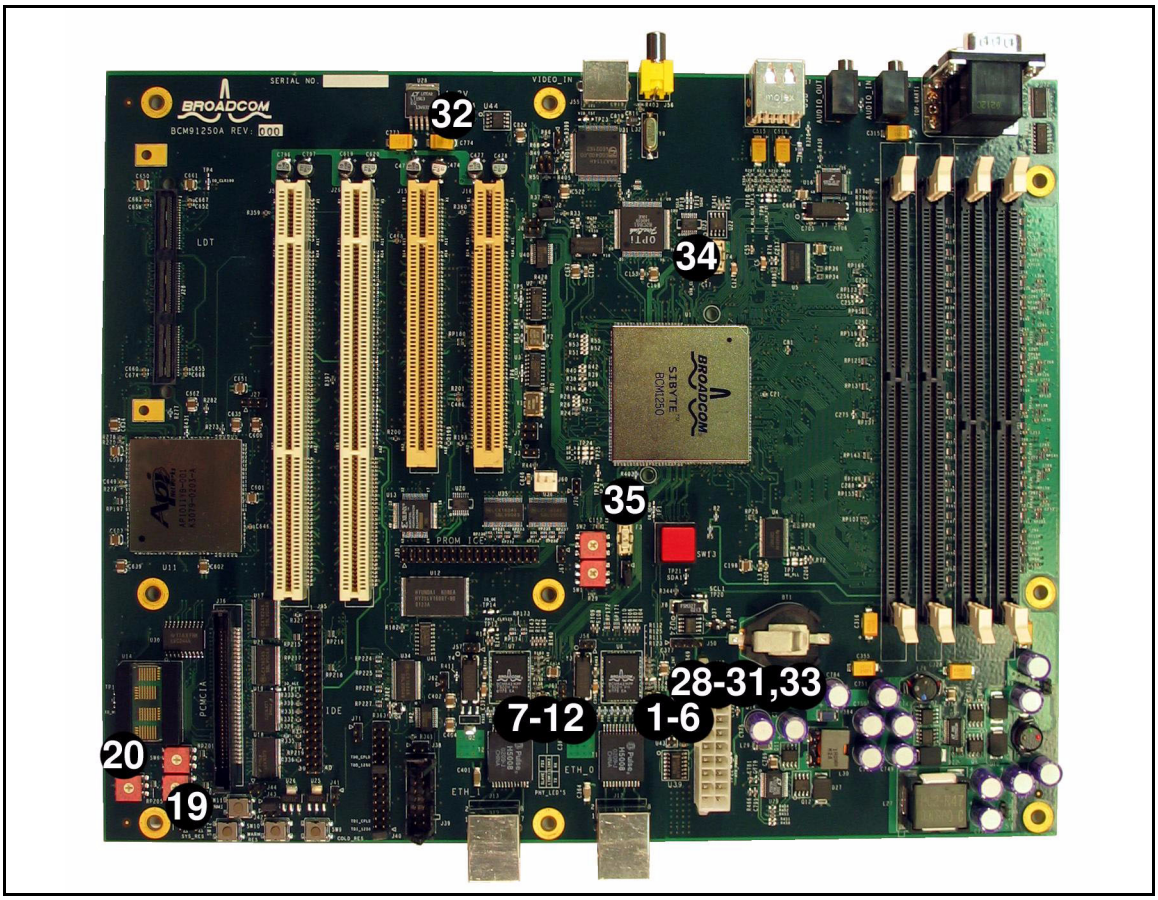

Figure 7: LED Callouts

Table 4: *LED Descriptions*

Board ID	*Color*	*Description*
D1	Green	PHY 0 Slave indicator
D2	Green	PHY 0 Receive indicator
D3	Green	PHY 0 Transmit indicator
D4	Green	PHY 0 Full Duplex indicator
D5	Green	PHY 0 Link 1 indicator
D6	Green	PHY 0 Link 2 indicator
D7	Green	PHY 1 Slave indicator
D8	Green	PHY 1 Receive indicator

Table 4: *LED Descriptions (Cont.)*

Board ID	*Color*	*Description*
D9	Green	PHY 1 Transmit indicator
D10	Green	PHY 1 Full Duplex indicator
D11	Green	PHY 1 Link 1 indicator
D12	Green	PHY 1 Link 2 indicator
D19	Green	IDE HDD active indicator
D20	Green	Debug LED
D28	Green	5V Power good indicator
D29	Green	3.3V Power good indicator
D30	Green	2.5V Power good indicator
D31	Green	1.25V Power good indicator
D32	Green	1.2V Power good indicator
D33	Green	1.2V BCM1250 Core Power good indicator
D34	Red	2.5V Fuse blown indicator
D35	Red	3.3V Fuse blown indicator

FUSES AND BATTERY

Figure 8 shows the positions of fuses and the battery alpha-numerically. Compare Figure 8's alpha-numeric callouts with a description of each component in Table 5.

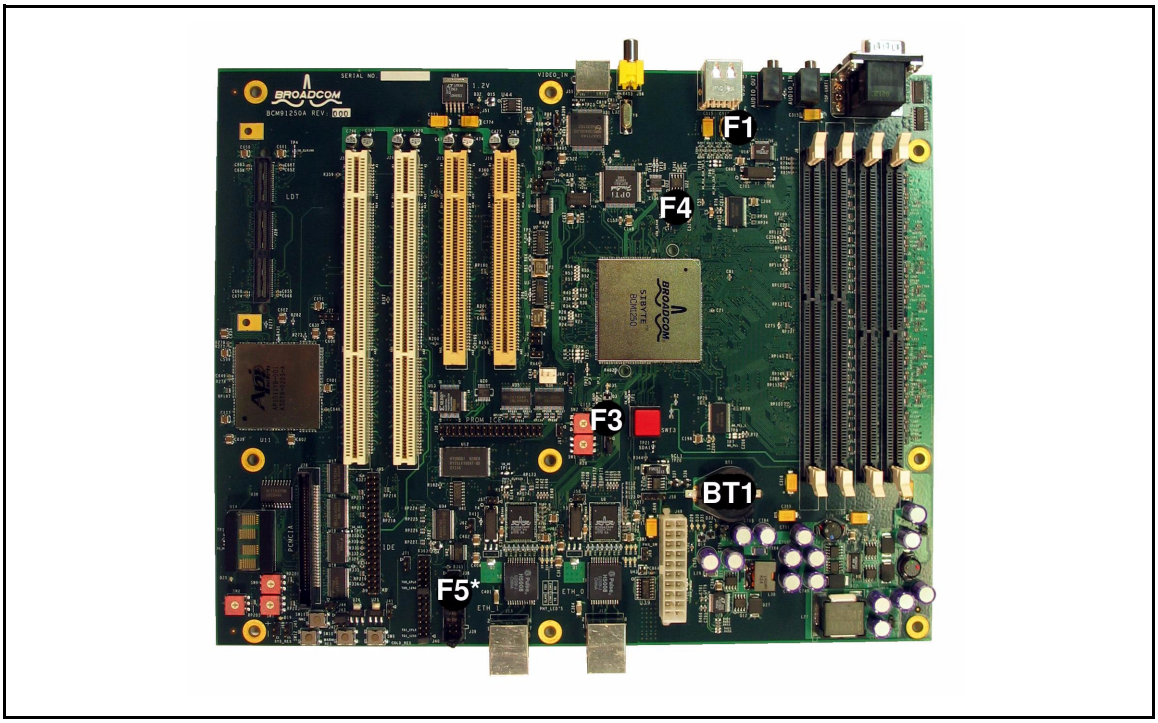

Figure 8: Fuses and Battery Callouts

Table 5: *Fuses and Battery Descriptions*

Board ID	*Function*
F1	USB 5V current limit, 1.1A
F3	BCM1250 3.3V current limit, 1A
F4	BCM1250 2.5V current limit, 5A
F5*	EJTAG 3.3V current limit, 500mA
BT1	RTC battery
* = fuse located on back side of the board	

JUMPERS

Figure 9 shows the positions of jumpers numerically. Compare Figure 9 number callouts with a description of each jumper in Table 6.

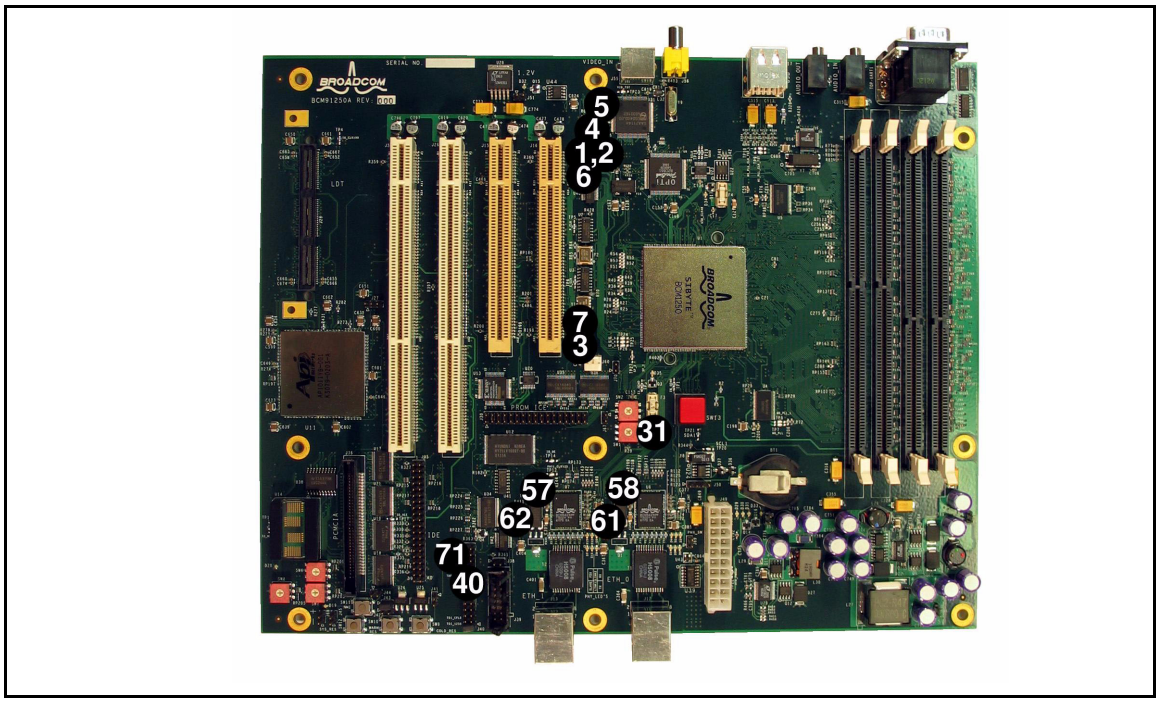

Figure 9: Jumper Callouts

Table 6: *Jumper Descriptions*

Board ID	*Function*	*Settings*	*Default*
J1	System Byte Order	open = little endian 1-2 = big endian	big endian
J2	BCM1250 BootMode[1] bit	open = 0 (generic bus boot ROM) 1-2 = 1 (SMBus boot ROM)	generic bus boot ROM
J3	BCM1250 plldiv[3]	1-2 = 0 open = 1 Please see "Acceptable PLL Settings" on page 21 for more information.	set to speed bin of BCM1250
J4	IOB0, IOB1 divide ratios	open = IOB0 div4, IOB1 div3 1-2 = IOB0 div4, IOB1 div2 3-4 = IOB0 div3, IOB1 div3 1-2, 3-4 = IOB0 div3, IOB1 div2	dependent on speed bin of BCM1250
J5	PLL bypass	open = normal PLL operation	normal PLL operation

Table 6: *Jumper Descriptions (Cont.)*

Board ID	*Function*	*Settings*	*Default*
J6	32-bit PCI clock select	open = run at slowest PCI agent 1-2 = force 33 MHz 2-4 = force 66 MHz 1-2, 3-4 = disable clock generator	run at slowest PCI agent
J7	64-bit PCI clock select	open = run at slowest PCI agent 1-2 = force 33 MHz 2-4 = force 66 MHz 1-2, 3-4 = disable clock generator	run at slowest PCI agent
J31	ROM/Emulator select	open = CS0 is Flash, CS1 is ROM Emulator 1-2 = CS0 is ROM Emulator, CS1 is ROM	CS0 is Flash, CS1 is ROM Emulator
J40	JTAG chain config	1-2, 17-18 = BCM1250 only 3-4, 19-20 = CPLD only (other settings are unsupported)	BCM1250 only
J43	Manual warm reset switch enable	open = disabled 1-2 = enabled	enabled
J61	MAC 0 PHY JTAG select	open = normal 1-2 = enable JTAG	normal (JTAG disabled)
J62	MAC 1 PHY JTAG select	open = normal 1-2 = enable JTAG	normal (JTAG disabled)
J71	JTAG chain config	open = enable BCM1250 and PHY JTAG rings 1-2 = enable all other JTAG rings (NOTE: Other jumpers (J40, J61, J62) must be set as well to enable the desired JTAG functionality)	enable BCM1250 and PHY JTAG rings

SWITCHES

Figure 10 shows the positions of switches numerically. Compare Figure 10 number callouts with a description of each switch in Table 7.

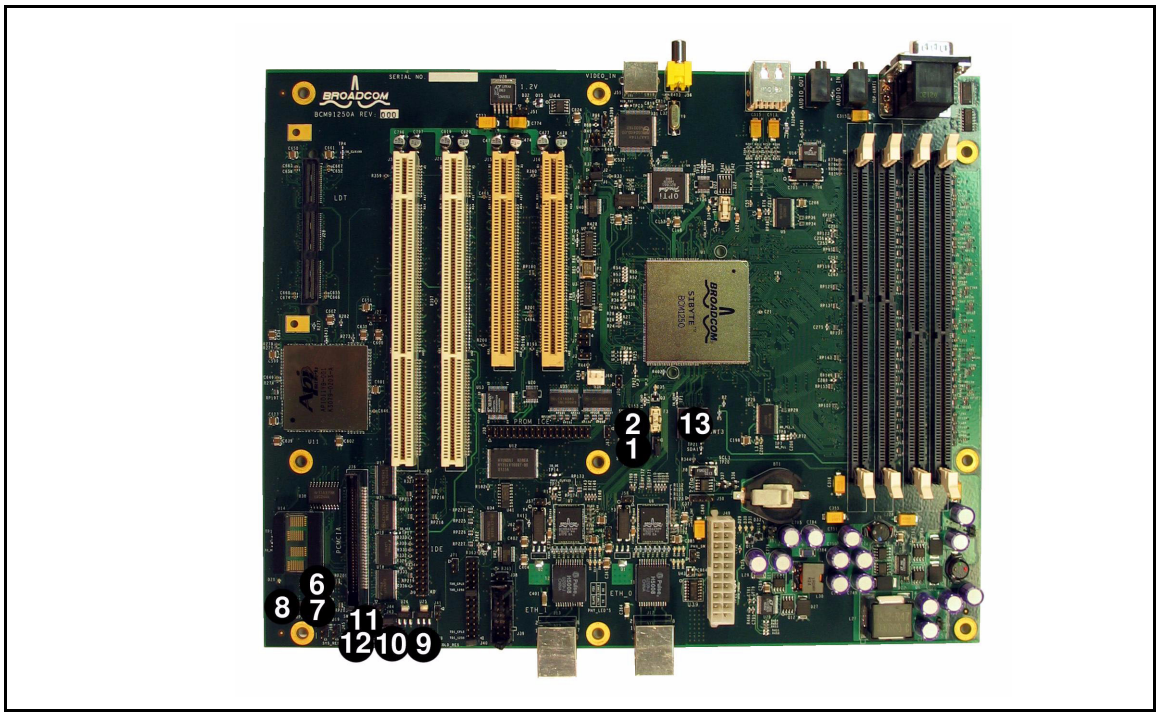

Figure 10: Switch Callouts

Table 7: *Switch Descriptions*

Board ID	*Function*	*Default*
SW1	16 position rotary switch to set config[5:2] for interpretation by software. See "Firmware Configuration" on page 24 for more details.	0x2
SW2	16 position rotary switch to set PLL ratio. Please see "Acceptable PLL Settings" on page 21 for the settings. Note: Your board should have shipped with the correct PLL settings so no adjustments should be needed. (* set to speed bin of BCM1250).	set to speed bin of BCM1250
SW6	SP1011 L0 Clock Divider select	0x0
SW7	SP1011 L1 Clock Divider select	0x0
SW8	SP1011 Core 33 Clock select	0x0
SW9	Cold Reset asserted when the button is pressed	N/A
SW10	Warm Reset asserted when the button is pressed	N/A
SW11	NMI (GPIO 3) asserted when the button is pressed	N/A
SW12	System Reset asserted when the button is pressed	N/A

Table 7: *Switch Descriptions (Cont.)*

Board ID	*Function*	*Default*
SW13	Power toggled on or off when pressed	N/A

ACCEPTABLE PLL SETTINGS

Table 8 shows acceptable PLL settings. These settings require a combination of a jumper (J3) and a switch (SW2).

Note: The default PLL settings are set according to the speed bin of the BCM1250 part. That setting is the maximum clock speed that the chip can attain without failure.

Table 8: *Acceptable PLL Settings*

J3 setting pll_div[3] open = 1 1-2 = 0	*SW2 setting pll_div[4,2:0]*	*pll_div[4:0]*	*CLK100 MHz Multipler*	*CPU clock (MHz)*
open	0x4	01100	6x	600
open	0x5	01101	6.5x	650
open	0x6	01110	7x	700
open	0x7	01111	7.5x	750
open	0x8	11000	8x	800
open	0x9	11001	8.5x	850
open	0xA	11010	9x	900
open	0xB	11011	9.5x	950
open	0xC	11100	10x	1000

ACCEPTABLE I/O BRIDGE SETTINGS

The BCM1250 contains two bridges which isolate many of the chip's SOC components from the core, L2 cache, and other components. More details about these bridges can be found in the user manual for the specific chip. The clocking for these bridges is determined by dividing the CPU clock. The allowable divide ratios for a given bridge at a certain CPU frequency are provided below.

Table 9: *Acceptable I/O Bridge Settings*

CPU clock (MHz)	*IOB0 divide ratio*	*IOB1 divide ratio*
600-650	3 or 4	2 or 3
700-1000	3 or 4	3

PERIPHERAL DEVICES

Table 10: *SMBus Peripherals*

SMBus Channel	*SMBus Address*	*Description*
0	0x2A	Maxim MAX6654 temperature sensor
0	0x54	DDR SDRAM DIMM SPD EEPROM, MC channel 0, slot 0
0	0x55	DDR SDRAM DIMM SPD EEPROM, MC channel 0, slot 1
0	0x56	DDR SDRAM DIMM SPD EEPROM, MC channel 1, slot 0
0	0x57	DDR SDRAM DIMM SPD EEPROM, MC channel 1, slot 1
0	0x50	Microchip 28LC128C EEPROM
1	0x51	Microchip 28LC128C EEPROM
1	0x57	ST Microelectronics M41T81 RTC

Table 11: *Generic Bus Peripherals*

Chip Select #	*Description*
CS0	Hynix HY29LV160 boot flash memory or ROM Emulator (depending on J31 setting)
CS1	ROM Emulator or Hynix HY29LV160 boot flash memory (depending on J31 setting)
CS3	HP HDLO-2416 LED display
CS4	IDE Hard disk connector (more information can be found in the application note referenced in Table 17 on page 26).
CS6	PCMCIA slot

Table 12: *GPIO Map*

GPIO Pin #	*Direction*	*Description*
0	Output	Debug LED
1	Output	Alliance Semiconductor (SiPackets) SP1011 nonmaskable interrupt (NMI)
2	Input	PHY interrupt
3	Input	BCM1250 NMI
4	Input	IDE disk interrupt
5	Input	Temperature sensor alert
6-15	N/A	PCMCIA interface

Table 13: *PCI Interrupt Map*

Interrupt Map	*Description*
BCM1250 PCI INTA = PCI connector (J15) INTA BCM1250 PCI INTB = PCI connector (J15) INTB BCM1250 PCI INTC = PCI connector (J15) INTC BCM1250 PCI INTD = PCI connector (J15) INTD	32-bit PCI connector (J15)
BCM1250 PCI INTA = PCI connector (J16) INTD BCM1250 PCI INTB = PCI connector (J16) INTA BCM1250 PCI INTC = PCI connector (J16) INTB BCM1250 PCI INTD = PCI connector (J16) INTC	32-bit PCI connector (J16)
BCM1250 PCI INTC = Firelink 82C861 INTA	Firelink 82C861 PCI to USB bridge
SiPackets SP1011 INTA = PCI connector (J26) INTA SiPackets SP1011 INTB = PCI connector (J26) INTB SiPackets SP1011 INTC = PCI connector (J26) INTC SiPackets SP1011 INTD = PCI connector (J26) INTD	64-bit PCI connector (J26)
SiPackets SP1011 INTA = PCI connector (J53) INTD SiPackets SP1011 INTB = PCI connector (J53) INTA SiPackets SP1011 INTC = PCI connector (J53) INTB SiPackets SP1011 INTD = PCI connector (J53) INTC	64-bit PCI connector (J53)

SUPPORTED DRAM

Although this board ships with two 128MB DDR SDRAM DIMMs, it can support other DIMMs as well. This includes standard PC2100 and PC2700 DDR SDRAM DIMMs, either buffered or unbuffered and with or without ECC.

The two provided DIMMs are placed in MC channel 0 slot 0 and MC channel 1 slot 0 by default. This provides the best memory utilization for two DIMMs because channel interleaving can be used.

Other available configurations for installing more or different DIMMs are as follows:

- Two identical DIMMs can be inserted in slot 1 of both channels to provide the best possible memory utilization.
- If you choose to put two DIMMs on a single channel, then the DIMM timing/characteristics must be identical. The firmware then uses chip select interleaving when configuring the memory controller.
- Finally, populating all four slots with identical DIMMs provides the best possible memory utilization for this board. This will allow both chip select and channel interleaving to be configured.

SERIAL PORT S1 MULTIPLEXER CONTROL

This serial port can be configured as either a standard asynchronous UART with an RS232 interface or a synchronous Crystal CS4297A audio codec. The mux control for this port is controlled by setting the BCM1250's E2_GENO signal. When that signal is low, the UART is active and when it is high the audio codec is active.

Section 4: Firmware Configuration

The firmware image in the flash is bi-endian, so it supports both big and little-endian operation. Table 14 describes the physical address and how much physical memory the firmware maps to the chip selects on the generic bus.

Table 14: *Firmware Generic Bus Memory Mapping*

Chip Select	*Description*	*Physical Memory Address*	*Size*
CS0	Boot ROM	0x1FC0_0000	2 MB
CS1	Alternate Boot ROM	0x1F80_0000	2 MB
CS3	LED Display	0x100A_0000	64 KB
CS4	IDE	0x100B_0000	64 KB
CS6	PCMCIA	0x1100_0000	64 MB

Table 15 defines how the firmware (CFE) interprets the setting of switch SW1 at startup.

Table 15: *Firmware Configuration Bits Mapping*

SW1 Setting	*Action*
0x0	UART console, no PCI initialization
0x1	PromICE console, no PCI initialization
0x2*	UART console, PCI initialization
0x3	PromICE console, PCI initialization
0x6	UART console, PCI initialization, Hypertransport (HT) slave mode
0x7	UART console, no PCI initialization, CFE safe mode
0xA	VGA console, PCI initialization
* = recommended/default setting. All other settings are reserved.	

Serial Port S1 Configuration

The firmware by default sets the BCM1250's E2_GENO signal (this is the mux select for the port) low. This setting selects the asynchronous UART as the default.

Section 5: Troubleshooting

Corrective Procedures

- When CFE is not able to initialize the system and reach the console prompt, the four-character alphanumeric LED display may be used to help debug the initialization sequence. When the Cer2 message appears, a cache error has occurred. This frequently occurs when the BCM1250 is either undercooled, overclocked, or is in a low-voltage situation. Ensure that the correct voltage and cooling is being provided. This error may also occur if a DIMM is not properly seated in the slot. Check the DIMMs to make sure they are properly seated. For other LED message descriptions, refer to the Common Firmware Environment (CFE) Specification document.
- When red LEDs D34 or D35 are lighted, this indicates that either fuses F4 or F3 have blown and must be replaced. Replacement part information can be found in Table 16.

  A blown fuse can be easily extracted from the fuse socket by pulling it out with a small pair of pliers.The new fuse can then be pressed into place.
- There is no output coming from the serial boot console, but the four-character LED displays CFE. Because CFE uses serial port 0 (UART0) by default, ensure that a standard 9-pin RS232 null-modem cable connection is being used. Also ensure that the terminal program is set to a baud rate of 115200, 8-bit, no parity, no flow control.

Replacement Parts

Table 16: *Replacement Parts*

Board ID	*Description*	*Manufacturer*	*Manufacturer ID*	*Web Information*
F3	BCM1250 3.3V power 1A current limit	Littelfuse®	154001	http://www.littelfuse.com/data/Data_Sheets/154.pdf
F4	BCM1250 2.5V power 5A current limit	Littelfuse®	154005	http://www.littelfuse.com/data/Data_Sheets/154.pdf
F5	EJTAG connector 0.5A 32V surface mounted fuse.	Littelfuse®	434.500	http://www.littelfuse.com/PDFs/Products/434.pdf
BT1	3V Li RTC battery	various	CR2032	
N/A	BCM1250 fan/heat sink	Avvid Thermalloy	031659	http://www.aavidthermalloy.com/bin/BGADisp.pl?partnum=031659

Section 6: Web Resources

SiByte

Table 17: *SiByte Web Resources*

Resource	*Website*
BCM1250 and BCM1125H User Manual	http://sibyte.broadcom.com/public/resources/
SB-1 Core User Manual	http://sibyte.broadcom.com/public/resources/
General information	http://sibyte.broadcom.com/public/
BCM1250 Generic Bus Interface to ATA/ATAPI PIO Mode 3 (IDE) Hard Disk Product Application Note	http://sibyte.broadcom.com/public/resources/

Peripherals

Table 18: *Peripheral Web Resources*

Resource	*Website*
Philips SA7114 video decoder	http://www.semiconductors.philips.com/pip/SAA7114.html
Cirrus (Crystal) CS4297A audio codec	http://www.cirrus.com/en/products/pro/detail/P23.html
Alliance Semiconductor (SiPackets) SP1011 HT to HT/PCI bridge	http://www.alsc.com/products/sipackets.htm#SP1011
Maxim MAX6654 temperature sensor	http://pdfserv.maxim-ic.com/en/ds/MAX6654.pdf
Microchip 24LC128C serial EEPROM	http://www.microchip.com/1010/pline/memory/memdvice/ic/64to512/devices/24lc128/index.htm
ST Microelectronic M41T81serial real-time clock (RTC)	http://www.st.com/stonline/products/families/memories/rtc/nv_t81.htm
HP HDLO-2416 four character alphanumeric display	http://literature.agilent.com/litweb/pdf/5988-3269EN.pdf
Micron MT9VDDT1672AG-265 128MB 266Mhz DDR SDRAM ECC	http://micron.com/products/modules/ddrsdram/part.aspx?part=MT9VDDT1672AG-265
Xilinx XC9572XL CPLD	http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=-18744
Hynix HY29LV160 2MB flash memory	http://www.hynix.com/datasheet/kor/flash/detail11.jsp?PartNo=HY29LV160
OPTi Firelink 82C861 USB controller	http://www.opti.com/html/usb1394.html
Broadcom BCM5421 10/100/1000BASE-T Gigabit Copper Transceiver	http://www.broadcom.com/products/product.php?product_id=BCM5421&cookiecheck=1
Samtec connector QSE-060-01-FDA (J28 callout)	http://www.samtec.com/signal_integrity/technical_specifications/overview.asp?series=QSE
Samtec connector QTE-060-01-FDA (J29 callout)	http://www.samtec.com/signal_integrity/technical_specifications/overview.asp?series=QTE

BUS INTERFACE

Table 19: *Bus Interface Web Resources*

Resource	*Website*
HyperTransport specification	http://www.hypertransport.org/doc_specifications.htm
PCMCIA specification	http://www.pcmcia.org/pccardstandard.htm
JTAG specification	http://www.mips.com/content/Documentation/MIPSDocumentation/EJTAG/doclibrary/
PCI specification	http://www.pcisig.com/specifications/conventional/
USB specification	http://www.usb.org/developers/docs/

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