Evaluation Board

REVISION HISTORY

Revision	Date	Change Description
91250E-UM100-R	01/07/05	Initial release.

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, CA 92619-7013

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Section 1: Product Overview

INTRODUCTION

The BCM91250E evaluation board is an evaluation platform intended to support the needs of prospective users of the BCM1250 processor. This user manual provides information on how to get the BCM91250E evaluation board up and running quickly. This manual also describes how to locate, configure, and observe the various connectors, switches, jumpers, and LEDs on the BCM91250E, allowing software development and evaluation of the BCM1250 processor to begin.

For additional information on this board and the BCM1250 processor, go to:
http://sibyte.broadcom.com/public.

ITEMS INCLUDED WITH THE SHIPMENT

The following items are included with the BCM91250E evaluation board shipment:

- BCM91250E evaluation board
- This document

FEATURES

This section describes the BCM91250E's features.

HARDWARE

- BCM1250 processor
- Full length PCI card form factor
- 256 MB DDR SDRAM
- Two 10/100/1000 Mbps Ethernet interfaces with RJ45 connectors
- One UART with RS232 interface
- Universal 32-bit, 33/66-MHz capable PCI connector
- 2 MB Flash ROM
- Two SMBus channels with the following devices connected:
  - RTC
  - EEPROM
  - Temperature sensor
- EJTAG connector
- PROMICE connector

FIRMWARE

The Common Firmware Environment (CFE) is designed to be easily portable to designs incorporating current and future Broadcom MIPS64-compatible broadband processors. Supported platforms include Broadcom's

SiByte processor family (containing the BCM1250, BCM1125H, and other processors), 32-bit and 64-bit memory models, and big and little-endian operation. There are many parameters configurable at build time that can be used to customize CFE to suit diverse customer requirements.

On the BCM91250E, CFE can load programs (such as S-records, raw binary, or ELF formatted) from bootstrap devices in a variety of ways, including:

- Via either Ethernet port, from a TFTP server
- Via the serial port (S-records only)

For additional information on CFE, refer to the *Common Firmware Environment (CFE) Specification* document that can be found in the CFE source code distribution at: http://sibyte.broadcom.com/public.

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Section 2: Getting Started

Complete the following steps to get to a BCM91250E CFE (firmware) prompt.

1 Connect a 9-pin null modem cable to the serial port of the BCM91250E and to a serial port on a workstation/PC.

2 Use a terminal program and set it to 115200 bps, 8-bit data, 1-stop bit, no parity, and no flow control.

3 Power up the BCM91250E by plugging in a standard hard drive power connector.

After a short delay, the CFE initialization output and serial console prompt should display. The following is an example of the output:

```
CFE version 1.0.37 for SENTOSA (64bit,MP,BE)
Build Date: Fri Jul 11 10:40:26 PDT 2003
Copyright (C) 2000,2001,2002,2003 Broadcom Corporation.

Initializing Arena.
Initializing PCI. [normal]
HyperTransport not initialized: InitDone not set
Initializing Devices.
SENTOSA board revision 1
PCIIDE: 0 controllers found
Config switch: 2
CPU: BCM1250 B2
L2 Cache Status: OK
Wafer ID:   0x2164E019  [Lot 2137, Wafer 7]
Manuf Test: Bin A [2CPU_FI_FD_F2 (OK)]
SysCfg: 0000000020C20800 [PLL_DIV: 16, IOB0_DIV: CPUCLK/4, IOB1_DIV: CPUCLK/3]
CPU type 0x1040102: 800MHz
Total memory: 0x10000000 bytes (256MB)

Total memory used by CFE:  0x8FE8C880 - 0x90000000 (1521536)
Initialized Data:          0x8FE8C880 - 0x8FE964A0 (39968)
BSS Area:                  0x8FE964A0 - 0x8FE96B90 (1776)
Local Heap:                0x8FE96B90 - 0x8FF96B90 (1048576)
Stack Area:                0x8FF96B90 - 0x8FF98B90 (8192)
Text (code) segment:       0x8FF98BA0 - 0x8FFFFFB0 (422928)
Boot area (physical):      0x0FE4B000 - 0x0FE8B000
Relocation Factor:         I:F0398BA0 - D:0DF8C880

CFE>
```

4 At the prompt, a program can be run via the network from a TFTP server by doing the following:

a. Connect the BCM91250E Ethernet port E0 with an Ethernet cable to a switch, repeater, or directly to the Ethernet port of the file server.

> **Note:** Because the Broadcom PHYs handle direct connects automatically, a crossover cable for direct connects is not needed.

b. To initialize Ethernet port E0, type the following:

```
ifconfig eth0 -auto
```

> **Note:** The ifconfig eth0 -auto command can only be used with a DHCP server.

c. To run a program, type the following:

```
boot -elf tftp_server:/path_to_software/program
```

Section 3: Physical Description

The BCM91250E is implemented in the standard full length PCI card form factor. Figure 1 shows a front view of the BCM91250E.
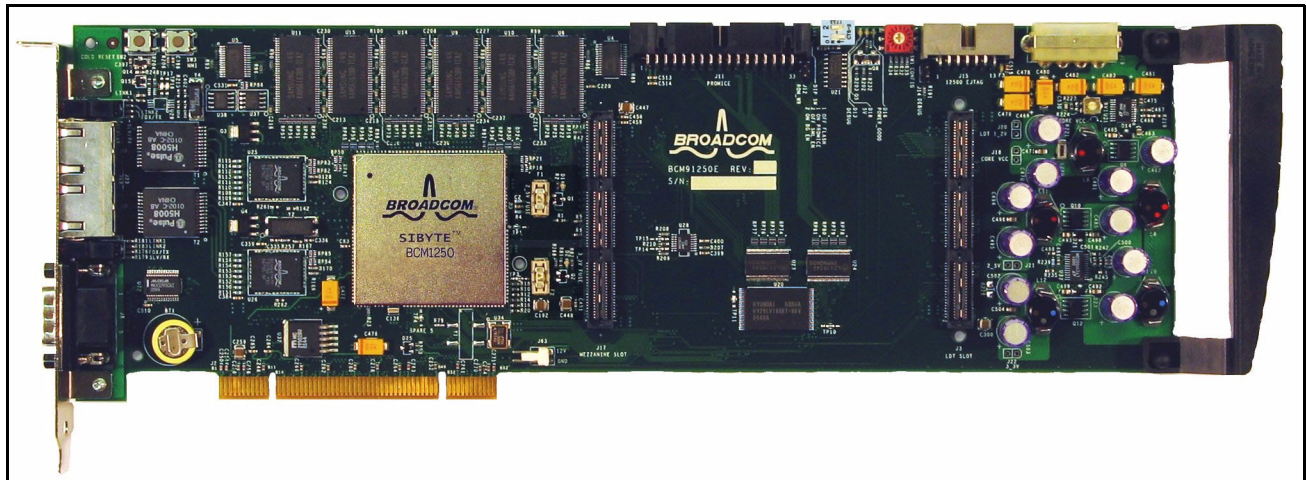

Figure 1: BCM91250E Front View

BLOCK DIAGRAM

Figure 2 shows a block diagram of the BCM91250E.
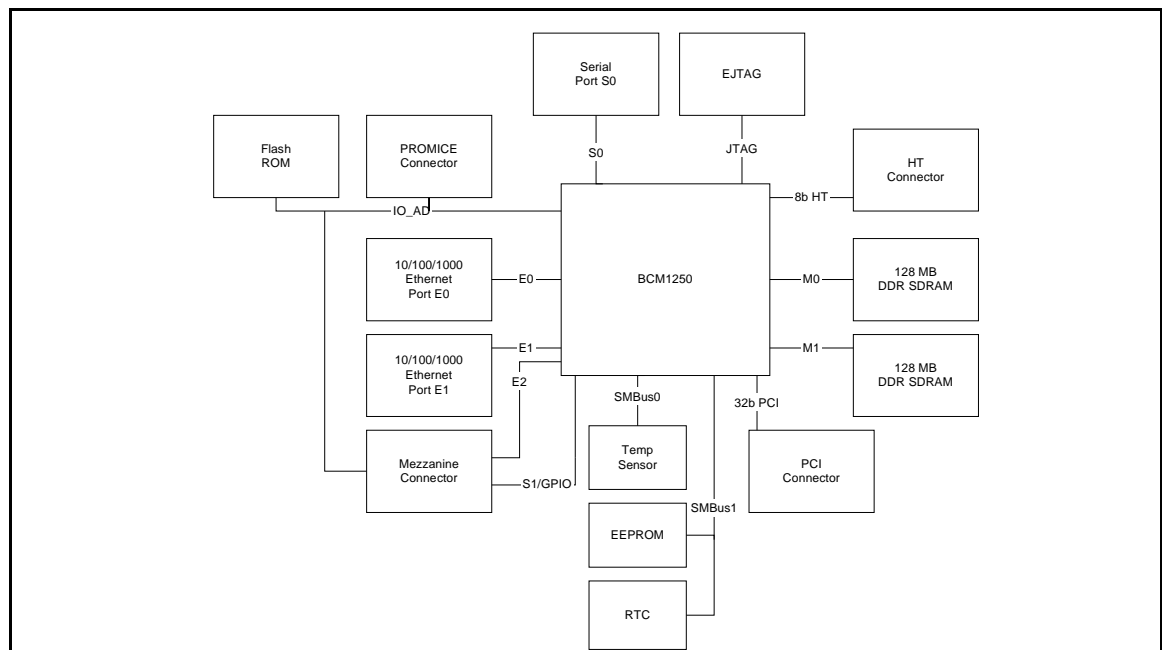
Figure 2: BCM91250E Block Diagram

CONNECTORS

Figure 3 shows the board and identifies connectors numerically. For a description of each connector callout, compare Figure 3's number callouts with Table 1.
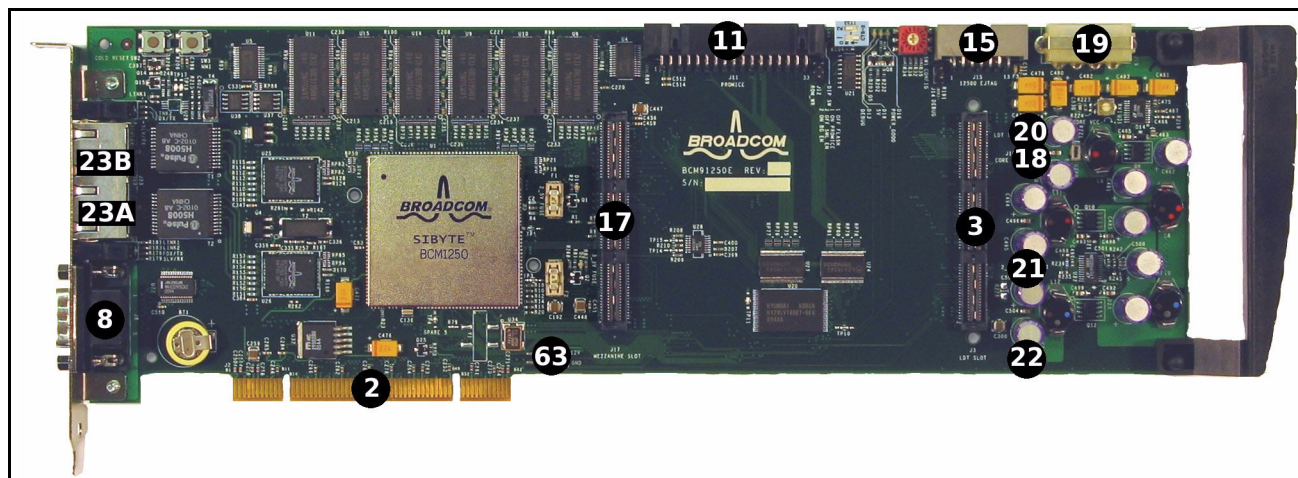
Figure 3: Connector Callouts

The following table shows the BCM91250E connectors.

Table 1: Connector Descriptions

Board ID	Description
J2	Dual-sided 62-pin edge finger PCI connector.
J3	HyperTransport socket for motherboards (see Table 2 on page 7).
J8	Serial port 0 RS-232 connector.
J11	ROM emulator connector (see Table 4 on page 11).
J12	ROM emulator write line (pin1* = IO_WR_L, pin2 = no connect).
J14	DEBUG_L trigger for scope (pin1* = GND, pin2 = DEBUG_L).
J15	EJTAG connector.
J17	Mezzanine connector (see Table 3 on page 9).
J18	1.2V core supply sense (pin1* = GND, pin2 = 1.2V).
J19	Standard hard drive power supply connector.
J20	1.2V HyperTransport supply sense (pin1 = GND, pin2 = 1.2V).
J21	2.5V supply sense (pin1* = GND, pin2 = 2.5V).
J22	3.3V supply sense (pin1* = GND, pin2 = 3.3V).
J23A	10/100/1000 Mbps Ethernet Port E1.
J23B	10/100/1000 Mbps Ethernet Port E0.
J63	12V Heatsink/Fan Power (pin1* = 12V, pin2 = GND).
* = Pin1 located by viewing the back of the board for the square solder pad.	

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PINOUT FOR HYPERTRANSPORT SOCKET (J3)

Note: The table layout reflects the physical location of the pins on the connector. The middle pins (121-132) are not shown though since they are all connected to ground (GND).

More information about these connectors can be found in "Web Resources" on page 19.

Table 2: Pinout For Hypertransport Socket (J3)

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
VDD33	1	2	VDD33
VDD33	3	4	VDD33
VDDLDT	5	6	VDDLDT
GND	7	8	GND
TCK	9	10	CLK100
TMS	11	12	GND
TDI	13	14	RDY
TDO	15	16	OE_L
TRST_L	17	18	WR_L
SCL	19	20	CS_L0
SDA	21	22	CS_L1
LDT_RESET_L	23	24	INT
LDT_PWROK	25	26	RESET_L
GND	27	28	GND
LDT_RX_CTLn	29	30	LDT_TX_CADp0
LDT_RX_CTLp	31	32	LDT_TX_CADn0
GND	33	34	GND
LDT_RX_CADn7	35	36	LDT_TX_CADp1
LDT_RX_CADp7	37	38	LDT_TX_CADn1
GND	39	40	GND
GND	41	42	GND
LDT_RX_CADn6	43	44	LDT_TX_CADp2
LDT_RX_CADp6	45	46	LDT_TX_CADn2
GND	47	48	GND
LDT_RX_CADn5	49	50	LDT_TX_CADp3
LDT_RX_CADp5	51	52	LDT_TX_CADn3
GND	53	54	GND
LDT_RX_CADn4	55	56	LDT_TX_CLKp
LDT_RX_CADp4	57	58	LDT_TX_CLKn
GND	59	60	GND

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Table 2: Pinout For Hypertransport Socket (J3) (Cont.)

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
GND	61	62	GND
LDT_RX_CLKn	63	64	LDT_TX_CADp4
LDT_RX_CLKp	65	66	LDT_TX_CADn4
GND	67	68	GND
LDT_RX_CADn3	69	70	LDT_TX_CADp5
LDT_RX_CADp3	71	72	LDT_TX_CADn5
GND	73	74	GND
LDT_RX_CADn2	75	76	LDT_TX_CADp6
LDT_RX_CADp2	77	78	LDT_TX_CADn6
GND	79	80	GND
GND	81	82	GND
LDT_RX_CADn1	83	84	LDT_TX_CADp7
LDT_RX_CADp1	85	86	LDT_TX_CADn7
GND	87	88	GND
LDT_RX_CADn0	89	90	LDT_TX_CTLp
LDT_RX_CADp0	91	92	LDT_TX_CTLn
GND	93	94	GND
AD0	95	96	AD9
AD1	97	98	AD24
AD2	99	100	AD25
AD3	101	102	AD26
AD4	103	104	AD27
AD5	105	106	AD28
AD6	107	108	AD29
AD7	109	110	AD30
AD8	111	112	AD31
GND	113	114	GND
VDDLDT	115	116	VDDLDT
VDD33	117	118	VDD33
VDD33	119	120	VDD33

PINOUT FOR MEZZANINE CONNECTOR (J17)

Note: The table layout reflects the physical location of the pins on the connector. The middle pins (121-132) are not shown though since they are all connected to ground (GND).

More information about these connectors can be found in "Web Resources" on page 19.

Table 3: Pinout For Mezzanine Connector (J17)

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
VDD33	1	2	VDD33
VDD33	3	4	VDD33
VDD50	5	6	VDD50
GND	7	8	GND
E2_RCLK	9	10	E2_TCLKI
GND	11	12	GND
E2_RXD7	13	14	E2_TCLKO
GND	15	16	GND
E2_RXD6	17	18	E2_TXD7
GND	19	20	GND
E2_RXD5	21	22	E2_TXD6
GND	23	24	GND
E2_RXD4	25	26	E2_TXD5
GND	27	28	GND
E2_RXD3	29	30	E2_TXD4
GND	31	32	GND
E2_RXD2	33	34	E2_TXD3
GND	35	36	GND
E2_RXD1	37	38	E2_TXD2
GND	39	40	GND
E2_RXD0	41	42	E2_TXD1
GND	43	44	GND
E2_RXDV	45	46	E2_TXD0
GND	47	48	GND
E2_RXER	49	50	E2_TXEN
GND	51	52	MEZ_MAC_PRSNT_L
E2_COL	53	54	E2_TXER
GND	55	56	GND
E2_CRS	57	58	E2_MDC
GND	59	60	GND

Table 3: Pinout For Mezzanine Connector (J17) (Cont.)

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
E2_MDIO	61	62	REFCLK02
GND	63	64	GND
IO_RD_WR	65	66	GPIO15
IO_CS_L3	67	68	GPIO14
IO_CS_L4	69	70	GPIO13
IO_ALE	71	72	GPIO12
GND	73	74	GPIO11
S1_DIN	75	76	GPIO10
S1_DIN_RCLKIN	77	78	GPIO9
S1_CTS_TCLKIN	79	80	GPIO8
S1_RIN	81	82	GND
GND	83	84	GPIO7
S1_TIN	85	86	GPIO6
S1_DOUT	87	88	GPIO5
S1_COUT	89	90	GPIO4
S1_RTS_TSTROBE	91	92	GPIO3
GND	93	94	GPIO2
IO_AD10	95	96	GPIO1
IO_AD11	97	98	GPIO0
IO_AD12	99	100	GND
IO_AD13	101	102	IO_AD14
GND	103	104	IO_AD16
IO_AD15	105	106	IO_AD18
IO_AD17	107	108	IO_AD20
IO_AD19	109	110	IO_AD22
IO_AD21	111	112	IO_AD23
GND	113	114	VDDN120
VDD50	115	116	VDD50
VDD33	117	118	VDD120
VDD33	119	120	VDD120

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ROM EMULATOR PINOUT

Note: The table layout reflects the physical location of the pins on the connector. Also all I/O signals are 3.3 V outputs that are tolerant of 5V inputs.

Table 4: ROM Emulator Pinout

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
GND	1	2	AD20
3.3 V PWR	3	4	AD19
AD18	5	6	AD16
AD17	7	8	AD15
AD14	9	10	AD12
AD13	11	12	AD7
AD8	13	14	AD6
AD9	15	16	AD5
AD11	17	18	AD4
OE_L	19	20	AD3
AD10	21	22	AD2
ROMEMUCS_L	23	24	AD1
AD31	25	26	AD0
AD30	27	28	AD24
AD29	29	30	AD25
AD28	31	32	AD26
AD27	33	34	GND

LEDs

Figure 4 shows the positions of the LEDs numerically. Compare Figure 4's number callouts with a description of each LED in Table 5 on page 13.
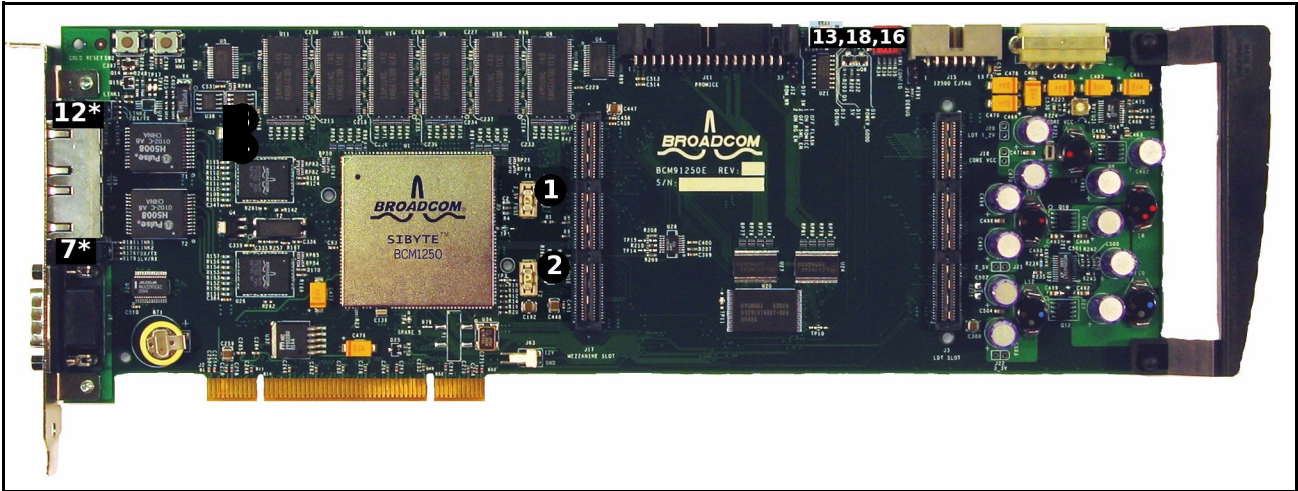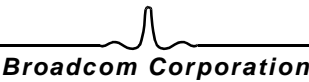

Figure 4: LED Callouts

Table 5: LED Descriptions

Board ID	Color	Description
D1	Red	2.5V Fuse blown indicator
D2	Red	3.3V Fuse blown indicator
D7 *		**Ethernet Port E1 PHY LEDs**
	Red	Link2 = Speed indicator.
	Green	Link1 = Speed indicator.
	Yellow	Fdx = Full-duplex indicator.
	Green	Slv = Slave indicator.
	Yellow	Act = Transmit and receive activity indicator.
	Green	Link = Link quality indicator.
D12 *		**Ethernet Port E0 PHY LEDs**
	Red	Link2 = Speed indicator.
	Green	Link1 = Speed indicator.
	Yellow	Fdx = Full-duplex indicator.
	Green	Slv = Slave indicator.
	Yellow	Act = Transmit and receive activity indicator.
	Green	Link = Link quality indicator.
D13	Green	Debug LED.
D16	Green	3.3V power good.
D18	Green	5V.
* = LEDs visible from the board's side panel.		

FUSES AND BATTERY

Figure 5 shows the positions of the fuses and battery alpha-numerically. Compare Figure 5's alpha-numeric callouts with a description of each fuse or battery in Table 6.
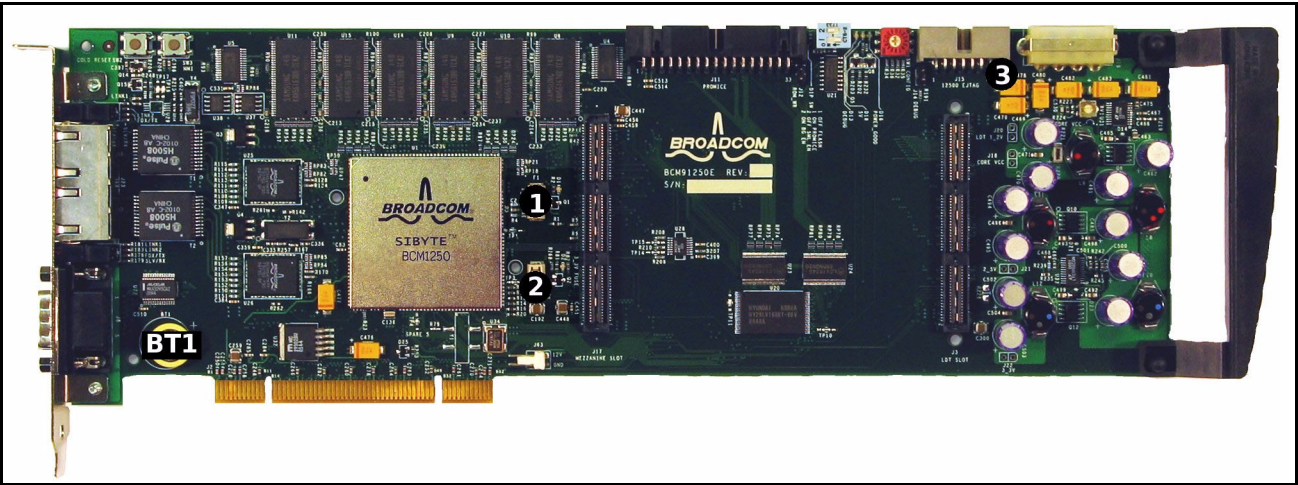

Figure 5: Fuses and Battery Callouts

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Table 6: Fuses and Battery Descriptions

Board ID	Function
F1	BCM1250 2.5V current limit, 5A.
F2	BCM1250 3.3V current limit, 1A.
F3	EJTAG 3.3V, 1A current limit fuse.
BT1	RTC battery.

SWITCHES

Figure 6 shows the positions of switches numerically. Compare Figure 6's number callouts with a description of each switch in Table 7.
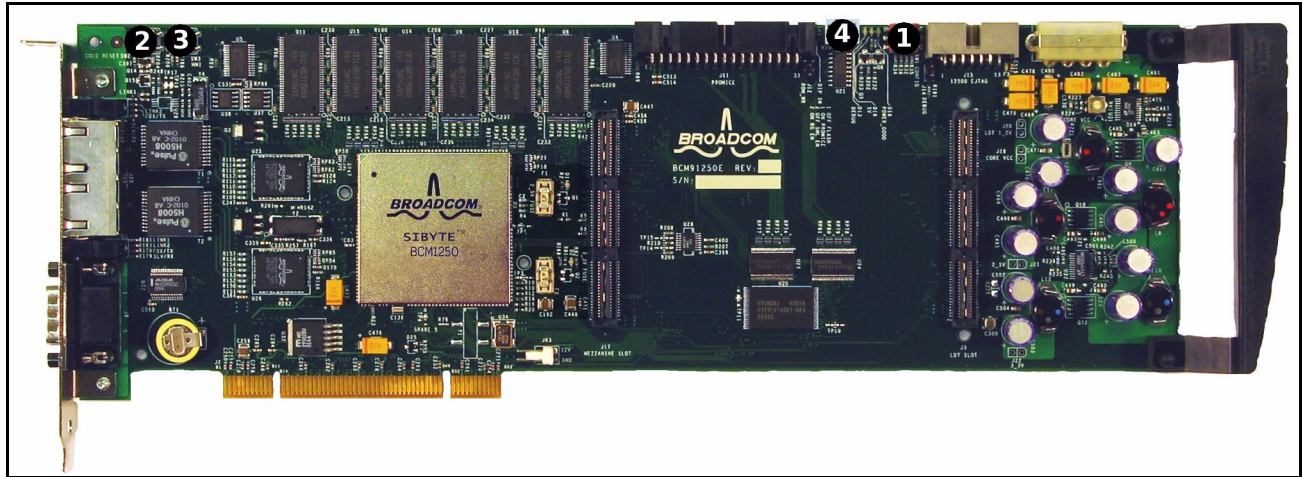

Figure 6: Switch Callouts

Table 7: Switch Descriptions

Board ID	Function	Default
SW1	16 position rotary switch to set config[5:2] for interpretation by software. See "Firmware Configuration" on page 17 for more details.	0x2
SW2	Cold Reset asserted when the button is pressed.	N/A
SW3	NMI (GPIO 8) asserted when the button is pressed.	N/A
SW4	2-position DIP switch, for board configuration dip[2:1]	See specific bits below.
	dip[2] = System byte order (on = big endian; off = little endian)	on
	dip[1] = generic bus CS0/1 mux (on = promice on CS0, flash on CS1; off = flash on CS0, promice on CS1)	off

PERIPHERAL DEVICES

Table 8: SMBus Peripherals

SMBus Channel	SMBus Address	Description
0	0x2A	Maxim MAX6654 temperature sensor.
1	0x50	Microchip 28LC128 EEPROM.
1	0x68	ST Microelectronics M41T81 RTC.

Table 9: Generic Bus Peripherals

Chip Select #	Description
CS0	Hynix HY29LV160 boot flash memory or ROM Emulator (depending on SW4 setting)
CS1	ROM Emulator or Hynix HY29LV160 boot flash memory (depending on SW4 setting)

Table 10: GPIO Map

GPIO Pin #	BCM1125H Pin Direction	Description
0	Output	Debug LED.
8	Input	NMI_L (from switch SW3).
9	Input	TEMP_ALERT_L from the temperature sensor.

Note: All GPIO[15:0] pins are routed to the mezzanine connector as well. See Table 3 for details.

Table 11: PCI Interrupt Map

Description	Interrupt Map
32-bit universal PCI connector.	BCM1250 PCI INTA = PCI Connector (J2) INTA
Ethernet PHY interrupts	BCM1250 PCI INTD = BCM5421 PHY0 INT || BCM5421 PHY1 INT

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Section 4: Firmware Configuration

The firmware image in the flash is bi-endian, so it supports both big and little-endian operation. The following table describes where and how much physical memory the firmware maps to the chip selects on the generic bus.

Table 12: Firmware Generic Bus Memory Mapping

Chip Select	Description	Physical Memory Address	Size
CS0	Boot ROM	0x1FC0_0000	2 MB
CS1	Alternate Boot ROM	0x1F80_0000	2 MB

Table 13: Firmware Configuration Bits Mapping

SW1 value	Action
0x0	UART console, no PCI initialization
0x1	PromICE console, no PCI initialization
0x2*	UART console, PCI initialization
0x3	PromICE console, PCI initialization
0x6	UART console, PCI initialization, Hypertransport (HT) slave mode
0x7	UART console, no PCI initialization, CFE safe mode
0x8	UART console, PCI initialization, device download mode
0x9	UART console, PCI initialization, device reboot mode
* = recommended/default setting. All other settings are reserved.	

Section 5: Troubleshooting

CORRECTIVE PROCEDURES

1   When CFE is not able to initialize the system and reach the console prompt, output on the serial boot console may be used to help debug the initialization sequence. When the Cer2 message appears, a cache error has occurred. This frequently occurs when the BCM1250 is either undercooled or is in a low-voltage situation. Ensure that the correct voltage and cooling is being provided. For other status/error message descriptions, refer to the *Common Firmware Environment (CFE) Specification* document.

2   There is no output coming from the serial boot console. Because CFE uses serial port 0 by default, ensure that a standard 9-pin RS232 null-modem cable connection is being used. Also ensure that the terminal program is set to a baud rate of 115200, 8-bit, no parity, no flow control. Finally make sure the output is not being routed to the PromICE console.

REPLACEMENT PARTS

Table 14: Replacement Parts

Board ID	Description	Manufacturer	Manufacturer ID	Web Information
F1	BCM1250 2.5V power 5A current limit	Littelfuse®	154005	http://www.littelfuse.com/data/Data_Sheets/154.pdf
F2	BCM1250 3.3V power 1A current limit	Littelfuse®	154001	http://www.littelfuse.com/data/Data_Sheets/154.pdf
F3	EJTAG connector 0.5A 32V surface mounted fuse.	Littelfuse®	434.500	http://www.littelfuse.com/PDFs/Products/434.pdf
BT1	RTC battery.	Panasonic	BR1225/1HC	http://www.panasonic.com/industrial/battery/oem/chem/lith/coin1.htm

Section 6: Web Resources

SIBYTE

Table 15: SiByte Web Resources

Resource	Website
BCM1250 and BCM1125H User Manual	http://sibyte.broadcom.com/public/resources/
SB-1 Core User Manual	
General information	http://sibyte.broadcom.com/public/

PERIPHERAL COMPONENTS

Table 16: Peripheral Component Web Resources

Board ID	Description	Manufacturer	Manufacturer ID	Web Information
U28	Temperature Sensor with SMBus Interface	Maxim	MAX6654	http://maxim-ic.com
U37	128K Serial EPROM	Microchip	24LC128	http://www.microchip.com
U38	Serial Real Time Clock	ST Microelectronics	M41T81	http://www.st.com
U6-U15	256Mbit 266MHz DDR SDRAM	Samsung	K4H561638D-TCA2	http://www.samsung.com/products/semiconductor
U25,U26	10/100/1000BASE-T Copper Transceiver	Broadcom	BCM5421	http://www.broadcom.com
J3, J17	128 Pin .8mm HT Mezzanine Socket	Samtec	QSE-060-01-FDA	http://www.samtec.com

BUS INTERFACE

Table 17: Bus Interface Web Resources

Resource	Website
HyperTransport specification	http://www.hypertransport.org
EJTAG specification	http://www.mips.com
PCI specification	http://www.pcisig.com

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