

EVALUATION BOARD FOR BCM1250

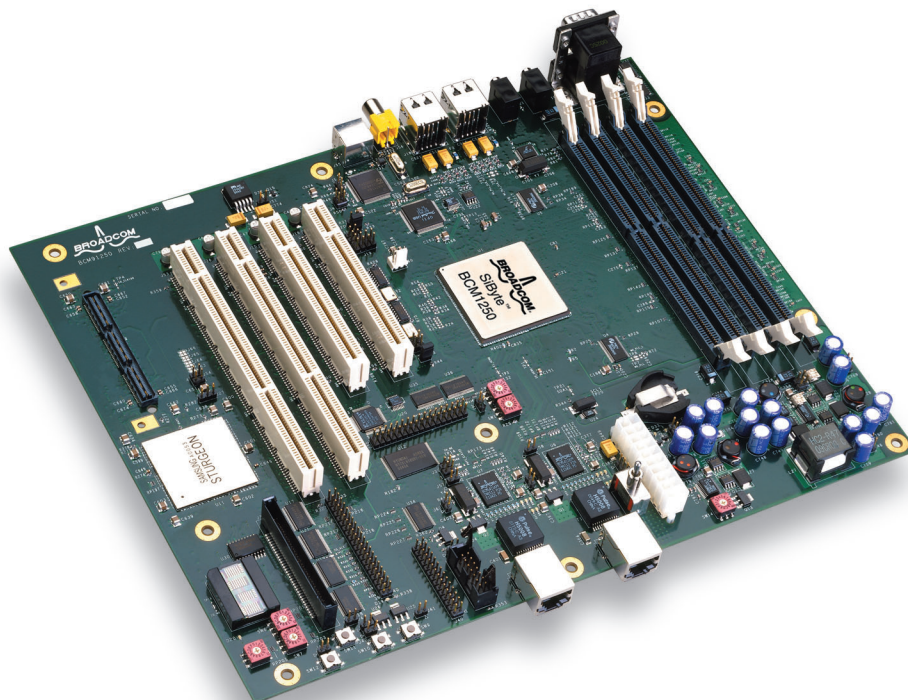
BCM91250A FEATURES

- Four DDR SDRAM slots
 - Each slot accepts a double-sided, 184-pin DDR DIMM with 64-bit data path and optional 8-bit ECC
 - Board comes populated with two 128-MB DIMMs
- Two Gigabit Ethernet ports
 - 10/100/1000BASE-T on standard CAT 5 UTP cable
- 66-MHz PCI local bus (rev. 2.2) compliant
 - Two 3.3V, 32-bit slots
 - Each slot can handle master or slave devices
- Two serial ports:
 - Serial Port 0: configured as a standard asynchronous UART with RS232 interface
 - Serial Port 1: Multiplexed to be either an additional UART with RS232, or audio CODEC
- HyperTransport™ (formerly LDT) to PCI bridge
 - Provides a bridge from the BCM1250 HyperTransport™ interface to two additional 64-bit, 66-MHz PCI slots and one HyperTransport™ connector

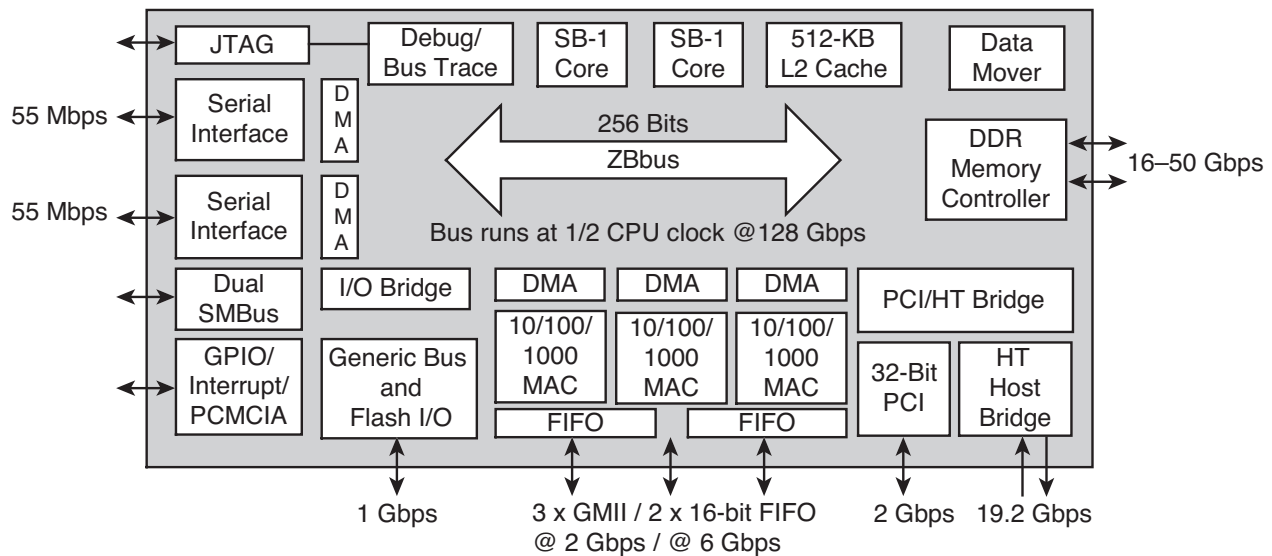
BCM91250A FEATURES

- Four USB ports
- NTSC/PAL video decoder
 - Demonstrates 8-bit packet FIFO option on BCM1250
- Two SMBus interfaces for two-wire devices
- JTAG, EJTAG headers for debugging and testing
- Four-character LED display and system boot error codes
- IDE interface for connection to IDE devices that are ATA/ATAPI PIO Mode 3 compliant
- PCMCIA interface supporting a single memory or I/O card
- BCM1250 running at current sampling speed
- For additional information on the BCM1250 processor, refer to the BCM1250 product brief.

BCM91250A Evaluation Board



BCM1250 Block Diagram



Product Overview

The BCM91250A is an evaluation board for the SiByte™ BCM1250 dual-processor SOC (System On a Chip) and is implemented in the standard ATX form factor. The board uses all the interfaces of the BCM1250. To provide examples for both hardware and software designers, configurable interfaces are used in all their modes wherever possible.

The board comes complete with an ATX 2.0 compliant case and power supply. Common off-the-shelf peripherals can be added, such as PCI graphics adapters, USB keyboards and mice, and ATA hard disks. In addition, the board has provisions for a few specialized applications including PCMCIA and HyperTransport™ (HT) peripherals.

Firmware

The BCM91250A is provided with Common Firmware Environment (CFE), which supports 32-bit and 64-bit operation. The CFE solution initializes the CPUs and the peripherals on the BCM1250, including the L2 cache, memory controller, Ethernet MACs, and UARTs. It also configures the HyperTransport™ fabric. CFE provides an environment for downloading and booting an Operating System using a disk, flash memory, the network, or the host as its boot device.

Operating System Support

Two operating systems are provided for the BCM91250A.

- VxWorks® version 5.4 with 64-bit support for data. VxMP™, a VxWorks® kernel running independently on each core, is an available option. Users will need to use the Tornado® tools version 2.1 for 64-bit or VxMP™ support. The BSP for the SWARM board is supported by Wind River Systems.

- Linux® version 2.4 running in 32-bit or 64-bit mode with full SMP support. Full source code is available.

Device drivers are provided as examples of how the many modes of the BCM1250 interfaces are used.

Development Tools

Broadcom supports the GNU toolchain. The toolchain is based on version 3.0 of the compiler, revision 2.11 of binutils, and supports cross compilation from x86/Linux® and SPARC/Solaris™ systems.

Broadcom has partnered with Corelis to provide debugging access through the BCM1250 JTAG port. There are two JTAG probe solutions:

- PICE-BCM1250 is a medium-performance probe that connects to the parallel port on a PC. This is provided with the BCM91250A.
- NetICE-BCM1250 is a high-performance probe that connects over the Ethernet. This probe can be directly purchased from Corelis.

Corelis provides a powerful source-level GUI debugger that works with both probes. This has been adapted for the BCM1250 and allows the registers of the internal peripherals to be examined easily. An evaluation copy of this debugger for Windows® 95/98/NT is provided with the BCM91250A.

Broadcom has enhanced the GNU debugger (GDB) to use the Corelis JTAG probes and enable multi-CPU debugging.

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