BCM52311

Hardware Design Guide

Design Guide

52311-DG105
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For a comprehensive list of changes to this document, see the Revision History.

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Chapter 1: System Overview

The 16 nm Knowledge-Based Processor (KBP) is designed to be used in conjunction with FPGAs, network processors, and other application-specific integrated circuits (ASICs). The 16 nm KBP interfaces with other devices through high-speed serial transceivers that can operate up to 28.125 Gb/s. Such a KBP requires careful PCB design of its supplies, clocks, and high speed-interfaces.

Block diagrams of the 16 nm KBP device in various modes are shown in Figure 1 and Figure 2 on page 6, and Figure 3 on page 6.

Figure 1: 16 nm KBP Single-Port Block Diagram

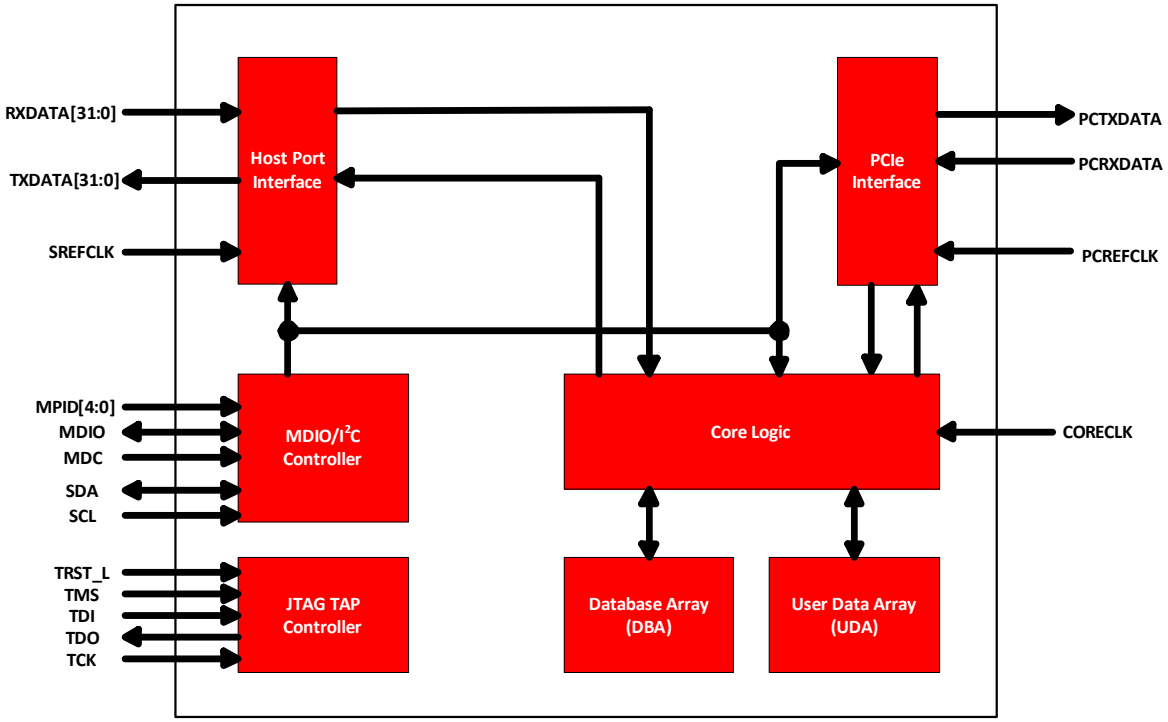


Figure 2: 16 nm KBP Dual-Port Block Diagram

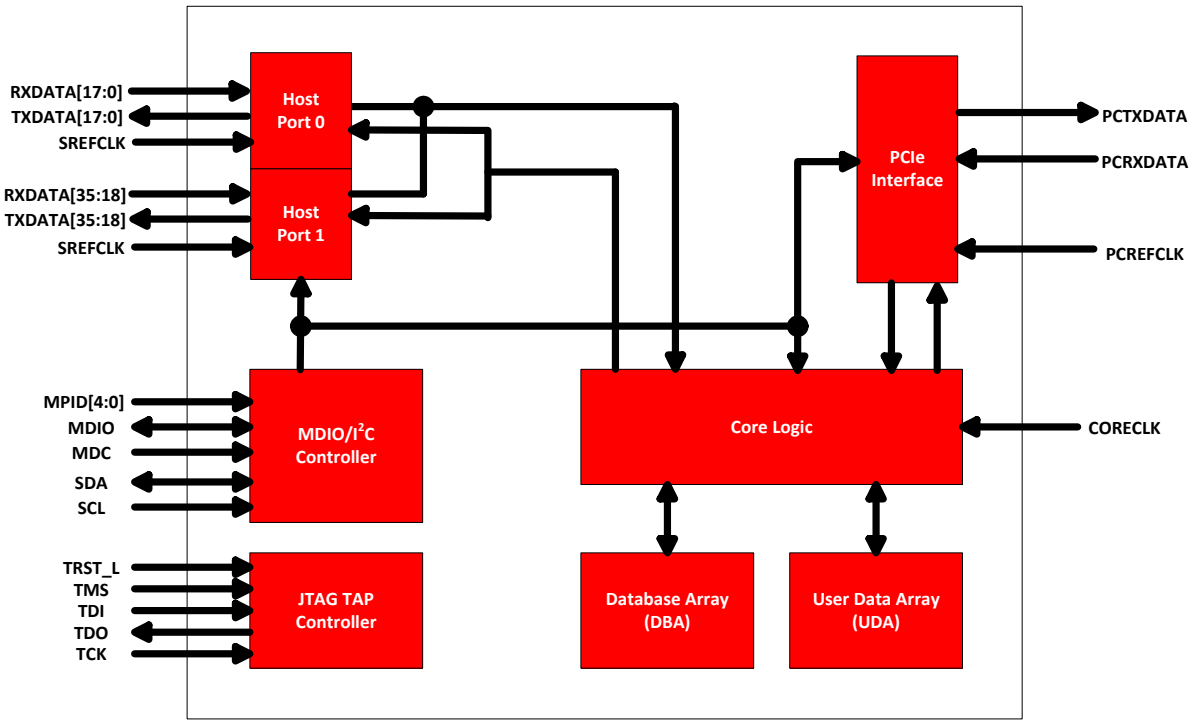
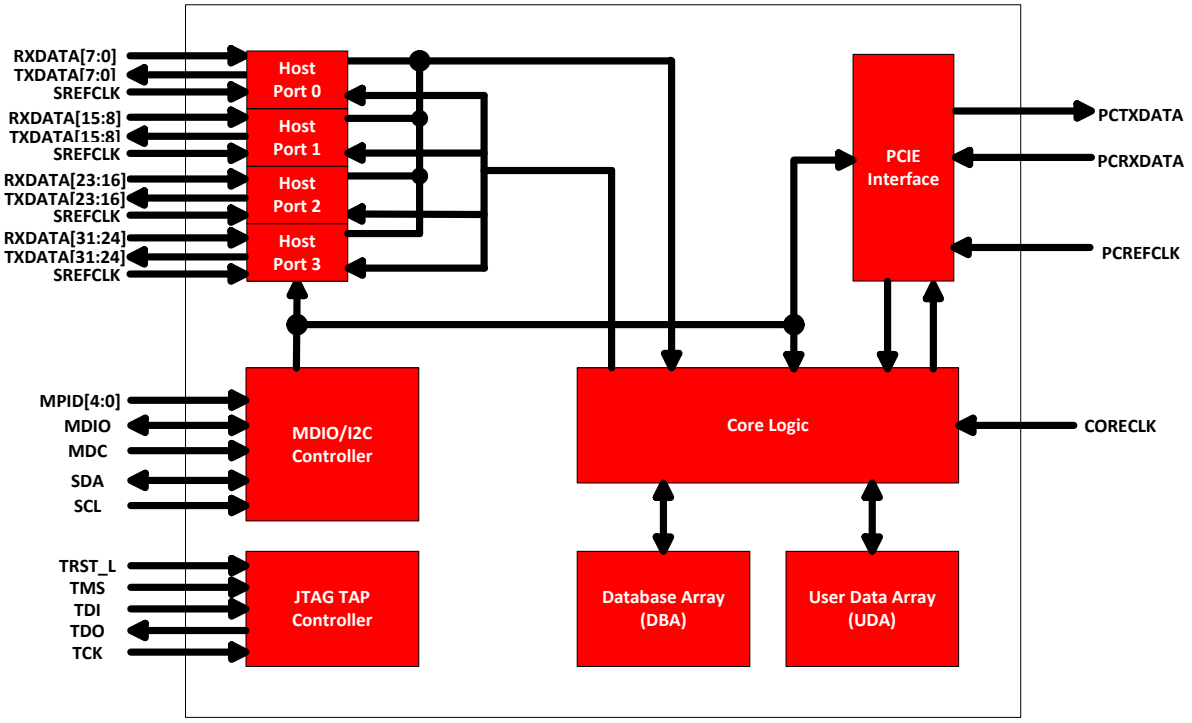


Figure 3: 16 nm KBP Quad-Port Block Diagram



The 16 nm KBP supports the interfaces listed below.

- Clock Inputs.
  - SREFCLKP, SREFCLKN – Differential input, reference clock for the 28.125 Gb/s SerDes interface.
  - CREFCLKP, CREFCLKN – Differential input, reference clock for the device core.
  - PCREFCLKP, PCREFCLKN – Differential input, reference clock for the 5 Gb/s PCIe Generation 2 interface.
- High Speed Interlaken-LA Interface.
  - Up to 36 receiving (RX) differential pairs and up to 36 transmitting (TX) differential pairs for the interface to the host device.
  - Up to 28.125 Gb/s data rate.
  - 1.8V Common Mode Logic (CML) signaling.
- PCIe Generation 2 Interface.
  - 1 lane receiver (RX) and 1 lane transmitter (TX).
  - 5 Gb/s data rate.
  - Meets PCIe Generation 2 specifications.
- Management Data Port (MDIO interface):
  - Single-ended clock input (management data clock), open drain. Pull-up through a 1 kΩ resistor to 1.8V supply.
  - Single-ended bidirectional I/O, open drain. Pull-up through a 1 kΩ resistor to 1.8V supply.
  - 1.8V signaling.
  - Per IEEE 802.3ae, Clause 45.
  - Used for serial interface and port configuration.
- Inter-Integrated Circuit (I^2C interface).
  - Single-ended clock input (SCL), open drain. Pull-up through a 1 kΩ resistor to 1.8V supply.
  - Single-ended bidirectional I/O, open drain. Pull-up through a 1 kΩ resistor to 1.8V supply.
  - 1.8V signaling. Not 3.3V tolerant.
  - The I^2C interface is currently not used.
- JTAG.
  - JTAG interface with AC capability (IEEE 1149.1 and 1149.6).
  - 1.8V signaling.
- Miscellaneous.
  - Static configuration pins, etc.
  - Test pins (for factory use only).
  - 1.8V signaling.

Chapter 2: Power Supplies

2.1 Overview

This device has the power supply inputs shown in Table 1.

NOTE: Power consumption is dependent on specific device usage and configuration. Values shown are for power supply planning only. Contact factory for estimation of power consumption under specific usage conditions.

Table 1: KBP Power Supply Inputs

Power Rail	Voltage [V_{out}] (mV)	Absolute Voltage Tolerance [$V_{out,max}$] (mV)	Max AC Ripple [R_C] (%)	Power Consumption (W)	Load Current Step [$\Delta I_{load,max}$] (A)	Comments
VDD	850 (AVS)	25	1.5	15 to 90	50	Powers core logic circuits. (Core)
VDDM	850	25	1.5	4.4	1.0	Powers SRAM circuits. (SRAM)
VDD12	1200	35	1.25	1.0	0.25	SerDes termination voltage supply. (HVA)
VDDS1	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS2	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS3	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS4	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS5	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS6	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS7	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS8	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDS9	800	25	1.25	0.74	0.18	Analog supply for SerDes circuits. (LVA)
VDDSPLL1	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL2	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL3	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL4	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL5	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)

Table 1: KBP Power Supply Inputs (Cont.)

Power Rail	Voltage [V_{out}] (mV)	Absolute Voltage Tolerance [$V_{out,max}$] (mV)	Max AC Ripple [R_c] (%)	Power Consumption (W)	Load Current Step [$\Delta I_{load,max}$] (A)	Comments
VDDSPLL6	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL7	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL8	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDSPLL9	800	25	0.375	0.10	0.02	PLL supply for SerDes circuits. (LVA)
VDDPC	800	25	1.5	0.05	0.01	Analog supply for PCIE circuits. (LVA)
VDDPCPLL	800	25	1.5	0.05	0.01	PLL supply for PCIE circuits. (LVA)
VDD18	1800	90	1.5	1.25	0.14	Supply for low-speed IOs and misc. circuits. (HVA)
VDDCPLL	1800	55	1.5	0.09	0.01	PLL supply for core logic circuits. (HVA)

Supply type is given in parenthesis in the Comments section. This is used in the power-on, power-off sequence.

Absolute voltage tolerance refers to the amount of deviation from the nominal (going both positive and negative) that the voltage can vary at the ball of the device, including DC variation and transient loads. For example, if the nominal voltage is 0.8V and the tolerance is 25 mV then the voltage at the device ball must be (under all conditions) between 0.775V and 0.825V.

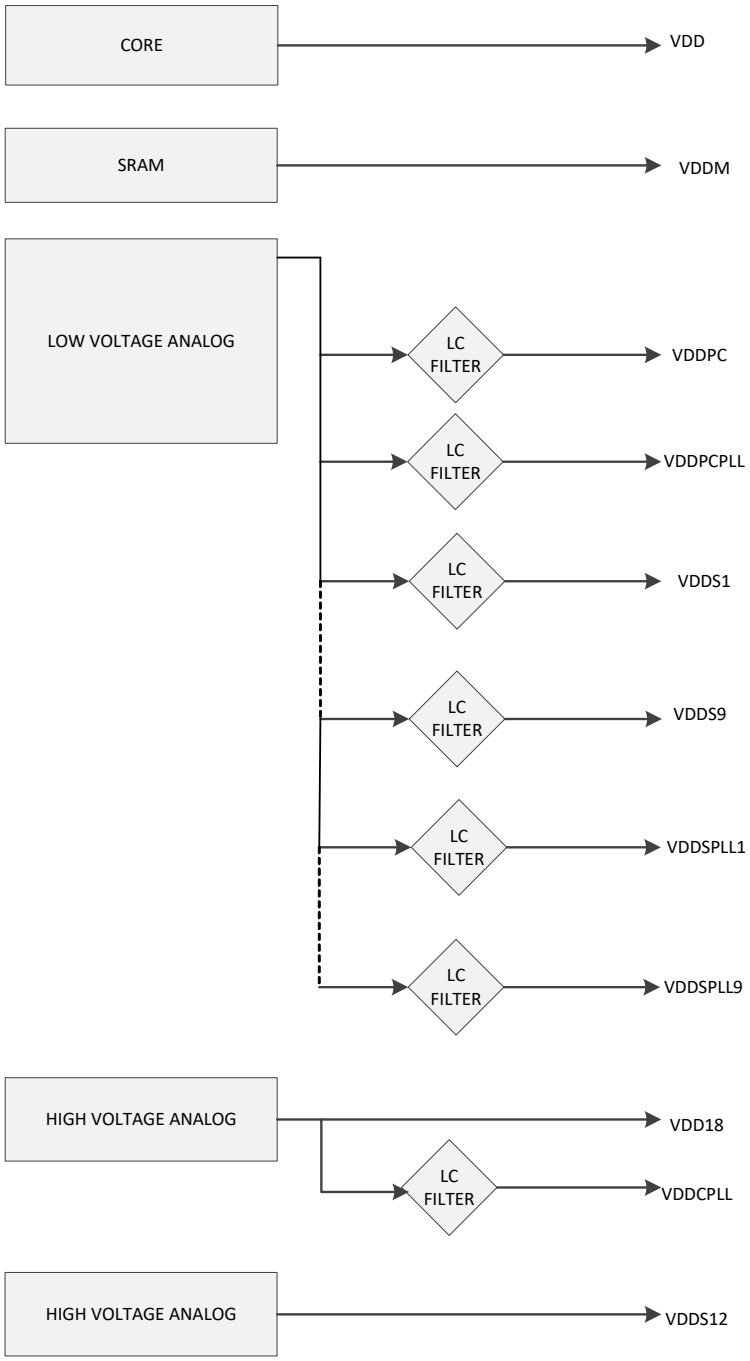
The AC ripple ratio (Rc) can be calculated as:

$$Rc = \frac{(\Delta Vout, pp)}{2Vout} \times 100\%$$

2.2 Power Supply Regulator Recommendations

A dedicated power supply is not required for all of the rails listed in Table 1, KBP Power Supply Inputs. In fact, the rails can be condensed into five power supplies.

Figure 4: Block Diagram of Recommended Power Supply Assignment



2.2.1 Core Regulator

A high-performance regulator designed for high power and fast-changing CPU-type loads is recommended for the core power supply. Except for very low device activity cases, a multiphase supply topology with 2–6 phases is required, depending on device utilization and activity factor. Desirable features for the core voltage regulator are fast transient response modes (non-linear control), dynamic phase shedding (improved light load efficiency), remote voltage sensing, and load-line regulation. Without non-linear control, it may be difficult for systems in the higher end of the power range to meet the absolute voltage tolerance specification under idle to full load step.

2.2.1.1 Adjustable DC Voltage and Dynamic Sense

2.2.1.1.1 System Design

NOTE: AVS connection and operation are required for proper device operation.

The KBP uses an automatic voltage scaling (AVS) technique to reduce the ill effects of a wide process variation. AVS involves adjusting the regulator voltage on the main VDD power supply level, as appropriate, for each silicon die. Slow silicon die use a higher voltage to ensure they run at the proper frequency. Fast silicon die use a lower voltage to reduce the power consumption. This ensures that the part runs at the desired frequency with minimal power consumption. AVS is required to be enabled and running to guarantee proper device operation. To implement AVS, the voltage regulator on the PCB must be programmed on a per-KBP basis. This happens once upon power-up, and the KBP determines which voltage it wants through the below scheme. Temperature is not adjusted since the KBP asks for static voltage from the regulator at all times.

AVS uses two chip pins (AVSA and AVSD), as shown in the AVS connectivity diagram in Figure 5 on page 12. Initially, both switches in the KBP are open and the regulator starts with a nominal V_{FB}, which is set by the R_{top} and R_{bot} voltage divider. After the initial start-up, the switches close and the AVSA pin outputs the desired voltage to set the external regulator. This value determines the steady-state DC value of the regulator and is governed by the silicon corner of the KBP, the temperature, and internal software settings. The regulator adjusts its output voltage in response to its V_{FB}. In steady state, $V_{REF} = V_{FB}$. The various components in Figure 5 on page 12 have constraints as depicted. R_{test} is to be used to test the AVS system as described in "Regulator Testing Procedure" on page 17. Add a test point at V_{ADC} where an external voltage supply can be connected. C_{ADC} ensures a slow varying output voltage and guarantees stability. It can be greater than the recommended value of 220 nF. C_{adc} acts to filter noise and maintain the feedback pin near its DC level. It can be less than the recommended value of 1 nF. The following equation governs the voltage relationship between V_{AVS}, V_{ADC}, and V_{FB}:

$$V_{AVS} = (1 + R_{top} / R_{bot}) \times V_{REF} + (R_{top} / R_{ADC}) \times (V_{REF} - V_{ADC}) \quad \text{(Equation 1)}$$

If is no AVS (so that $V_{REF} = V_{ADC}$), the second term of the equation drops out. R_{top} and R_{bot} are chosen using a nominal voltage for both V_{REF} and V_{AVS}. V_{REF} is determined by the given regulator and it is required to be in the range of 0.40V to 0.80V. The nominal start-up V_{AVS} is 0.85V, which implies that the first term of the equation is equal to 0.85V. This can be rewritten to determine the R_{top} to R_{bot} ratio.

$$R_{top}/R_{bot} = (0.85 / V_{REF}) - 1 \quad \text{(Equation 2)}$$

The regulator must be able to provide voltage in the range of 0.70V to 0.98V, but the actual AVS range will be on the order of 100 mV. The V_{ADC} voltage can range from 0 to 1.8V, but must be limited from 0.24V to 1.42V to maintain linearity in the DAC. To determine the R_{ADC} to R_{top} ratio, Equation 1 can be rewritten.

$$R_{ADC}/R_{top} = (V_{REF} - V_{ADC}) / (V_{AVS} - 0.85) \quad \text{(Equation 3)}$$

When V_{AVS} is at a maximum, V_{ADC} is at a minimum, and vice versa. An R_{ADC}/R_{top} ratio of 2.0 meets (equivalently R_{top} = 0.5 × R_{ADC}) the requirements for AVS and for V_{ADC} for all possible values of V_{REF}. It is required to use this specific ratio to control update times. The DAC can drive a maximum current of 100 µA. This limits R_{ADC} as per Equation 4.

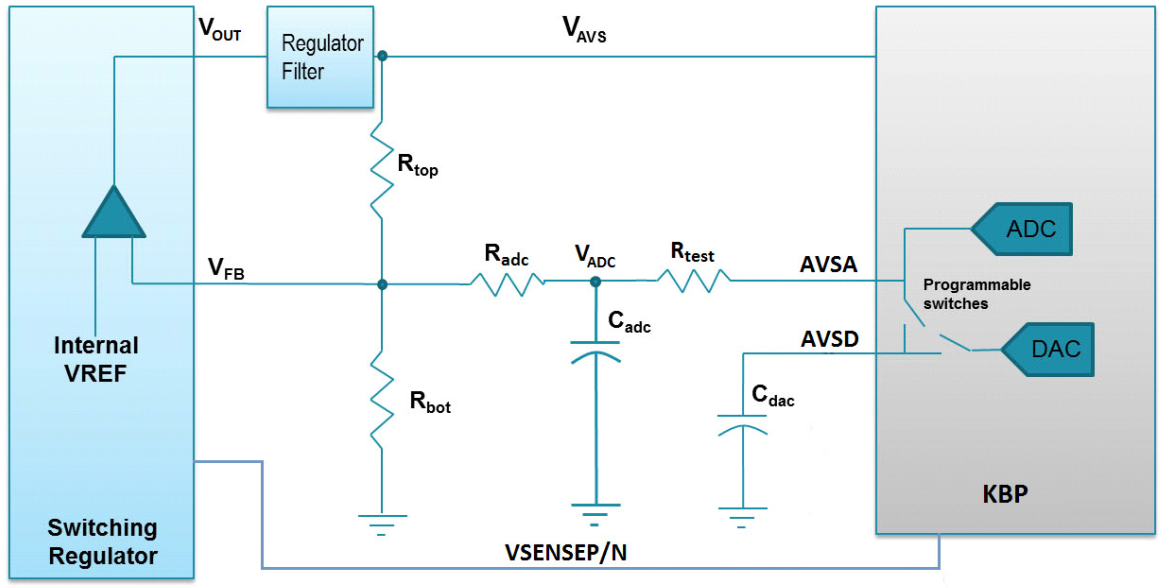
$$R_{ADC} >= (V_{ADC} - V_{REF}) / 100e^{-6} \quad \text{(Equation 4)}$$

Plugging in 1.42V as a maximum for V_{ADC} and 0.40V as a minimum for V_{REF} gives a value of greater than 10.2 kΩ. It is required that all resistor values be tightly controlled with a tolerance of 1% or less. Note that the regulator input impedance on V_{FB} may not be infinite and this should be taken into account when determining resistor values. Table 2 on page 13 shows the ideal voltage of V_{AVS} for a given V_{REF} and V_{ADC} voltage given an R_{top} of 6 kΩ, R_{ADC} value of 12 kΩ, and R_{bot} chosen for the appropriate V_{REF} (7.5 kΩ for V_{REF} = 0.5V). The yellow highlighted portion shows the full AVS range that the regulator could output to the device. The table is derived from Equation 1, above. It is required that the regulator V_{REF} allow for the full AVS range. The KBP changes V_{ADC} until it receives the desired V_{AVS} that it has determined. The KBP will set V_{ADC} and will expect the desired V_{AVS} that it has determined. The accuracy of the KBP DAC is around 2 mV.

The 16 nm KBP has two sense pins for the regulator called VSENSEP and VSENSEN. These pins are appropriate for dynamic feedback of the chip voltage to compensate for low-frequency noise. Some regulator remote voltage sense inputs are sensitive to high-frequency noise. It is recommended to filter VSENSEP/VSENSEN connections using an RC filter. The VSENSE pins take a sample of the voltage of the top metal layer in the die and route separately in the package to dedicated balls. They should be routed as a trace on the board to the regulator sense pins. The VSENSE pins should be able to work in conjunction with AVS.

CAUTION! Each of these VSENSE pins can source or sync a maximum of 35 mA. If this current is exceeded, the device will be damaged.

Figure 5: AVS System Configuration



V_{OUT}: Output of Switching Regulator
V_{AVS}: V_{DD} Supply of the SOC

Cdac >= 220nF
Cadc <= 1nF
Radc >= 10.2Kohm
Rtop = 0.5 * Radc
Rtest = 0ohm

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
1.33	0.435	0.460	0.485	0.510	0.535	0.560	0.585	0.610
1.32	0.440	0.465	0.490	0.515	0.540	0.565	0.590	0.615
1.31	0.445	0.470	0.495	0.520	0.545	0.570	0.595	0.620
1.3	0.450	0.475	0.500	0.525	0.550	0.575	0.600	0.625
1.29	0.455	0.480	0.505	0.530	0.555	0.580	0.605	0.630
1.28	0.460	0.485	0.510	0.535	0.560	0.585	0.610	0.635
1.27	0.465	0.490	0.515	0.540	0.565	0.590	0.615	0.640
1.26	0.470	0.495	0.520	0.545	0.570	0.595	0.620	0.645
1.25	0.475	0.500	0.525	0.550	0.575	0.600	0.625	0.650
1.24	0.480	0.505	0.530	0.555	0.580	0.605	0.630	0.655
1.23	0.485	0.510	0.535	0.560	0.585	0.610	0.635	0.660
1.22	0.490	0.515	0.540	0.565	0.590	0.615	0.640	0.665
1.21	0.495	0.520	0.545	0.570	0.595	0.620	0.645	0.670
1.2	0.500	0.525	0.550	0.575	0.600	0.625	0.650	0.675
1.19	0.505	0.530	0.555	0.580	0.605	0.630	0.655	0.680
1.18	0.510	0.535	0.560	0.585	0.610	0.635	0.660	0.685
1.17	0.515	0.540	0.565	0.590	0.615	0.640	0.665	0.690
1.16	0.520	0.545	0.570	0.595	0.620	0.645	0.670	0.695
1.15	0.525	0.550	0.575	0.600	0.625	0.650	0.675	0.700
1.14	0.530	0.555	0.580	0.605	0.630	0.655	0.680	0.705
1.13	0.535	0.560	0.585	0.610	0.635	0.660	0.685	0.710
1.12	0.540	0.565	0.590	0.615	0.640	0.665	0.690	0.715
1.11	0.545	0.570	0.595	0.620	0.645	0.670	0.695	0.720
1.1	0.550	0.575	0.600	0.625	0.650	0.675	0.700	0.725
1.09	0.555	0.580	0.605	0.630	0.655	0.680	0.705	0.730
1.08	0.560	0.585	0.610	0.635	0.660	0.685	0.710	0.735
1.07	0.565	0.590	0.615	0.640	0.665	0.690	0.715	0.740
1.06	0.570	0.595	0.620	0.645	0.670	0.695	0.720	0.745
1.05	0.575	0.600	0.625	0.650	0.675	0.700	0.725	0.750
1.04	0.580	0.605	0.630	0.655	0.680	0.705	0.730	0.755
1.03	0.585	0.610	0.635	0.660	0.685	0.710	0.735	0.760
1.02	0.590	0.615	0.640	0.665	0.690	0.715	0.740	0.765
1.01	0.595	0.620	0.645	0.670	0.695	0.720	0.745	0.770
1	0.600	0.625	0.650	0.675	0.700	0.725	0.750	0.775
0.99	0.605	0.630	0.655	0.680	0.705	0.730	0.755	0.780
0.98	0.610	0.635	0.660	0.685	0.710	0.735	0.760	0.785
0.97	0.615	0.640	0.665	0.690	0.715	0.740	0.765	0.790
0.96	0.620	0.645	0.670	0.695	0.720	0.745	0.770	0.795
0.95	0.625	0.650	0.675	0.700	0.725	0.750	0.775	0.800

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations (Cont.)

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
0.94	0.630	0.655	0.680	0.705	0.730	0.755	0.780	0.805
0.93	0.635	0.660	0.685	0.710	0.735	0.760	0.785	0.810
0.92	0.640	0.665	0.690	0.715	0.740	0.765	0.790	0.815
0.91	0.645	0.670	0.695	0.720	0.745	0.770	0.795	0.820
0.9	0.650	0.675	0.700	0.725	0.750	0.775	0.800	0.825
0.89	0.655	0.680	0.705	0.730	0.755	0.780	0.805	0.830
0.88	0.660	0.685	0.710	0.735	0.760	0.785	0.810	0.835
0.87	0.665	0.690	0.715	0.740	0.765	0.790	0.815	0.840
0.86	0.670	0.695	0.720	0.745	0.770	0.795	0.820	0.845
0.85	0.675	0.700	0.725	0.750	0.775	0.800	0.825	0.850
0.84	0.680	0.705	0.730	0.755	0.780	0.805	0.830	0.855
0.83	0.685	0.710	0.735	0.760	0.785	0.810	0.835	0.860
0.82	0.690	0.715	0.740	0.765	0.790	0.815	0.840	0.865
0.81	0.695	0.720	0.745	0.770	0.795	0.820	0.845	0.870
0.8	0.700	0.725	0.750	0.775	0.800	0.825	0.850	0.875
0.79	0.705	0.730	0.755	0.780	0.805	0.830	0.855	0.880
0.78	0.710	0.735	0.760	0.785	0.810	0.835	0.860	0.885
0.77	0.715	0.740	0.765	0.790	0.815	0.840	0.865	0.890
0.76	0.720	0.745	0.770	0.795	0.820	0.845	0.870	0.895
0.75	0.725	0.750	0.775	0.800	0.825	0.850	0.875	0.900
0.74	0.730	0.755	0.780	0.805	0.830	0.855	0.880	0.905
0.73	0.735	0.760	0.785	0.810	0.835	0.860	0.885	0.910
0.72	0.740	0.765	0.790	0.815	0.840	0.865	0.890	0.915
0.71	0.745	0.770	0.795	0.820	0.845	0.870	0.895	0.920
0.7	0.750	0.775	0.800	0.825	0.850	0.875	0.900	0.925
0.69	0.755	0.780	0.805	0.830	0.855	0.880	0.905	0.930
0.68	0.760	0.785	0.810	0.835	0.860	0.885	0.910	0.935
0.67	0.765	0.790	0.815	0.840	0.865	0.890	0.915	0.940
0.66	0.770	0.795	0.820	0.845	0.870	0.895	0.920	0.945
0.65	0.775	0.800	0.825	0.850	0.875	0.900	0.925	0.950
0.64	0.780	0.805	0.830	0.855	0.880	0.905	0.930	0.955
0.63	0.785	0.810	0.835	0.860	0.885	0.910	0.935	0.960
0.62	0.790	0.815	0.840	0.865	0.890	0.915	0.940	0.965
0.61	0.795	0.820	0.845	0.870	0.895	0.920	0.945	0.970
0.6	0.800	0.825	0.850	0.875	0.900	0.925	0.950	0.975
0.59	0.805	0.830	0.855	0.880	0.905	0.930	0.955	0.980
0.58	0.810	0.835	0.860	0.885	0.910	0.935	0.960	0.985
0.57	0.815	0.840	0.865	0.890	0.915	0.940	0.965	0.990
0.56	0.820	0.845	0.870	0.895	0.920	0.945	0.970	0.995
0.55	0.825	0.850	0.875	0.900	0.925	0.950	0.975	1.000

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations (Cont.)

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
0.54	0.830	0.855	0.880	0.905	0.930	0.955	0.980	1.005
0.53	0.835	0.860	0.885	0.910	0.935	0.960	0.985	1.010
0.52	0.840	0.865	0.890	0.915	0.940	0.965	0.990	1.015
0.51	0.845	0.870	0.895	0.920	0.945	0.970	0.995	1.020
0.5	0.850	0.875	0.900	0.925	0.950	0.975	1.000	1.025
0.49	0.855	0.880	0.905	0.930	0.955	0.980	1.005	1.030
0.48	0.860	0.885	0.910	0.935	0.960	0.985	1.010	1.035
0.47	0.865	0.890	0.915	0.940	0.965	0.990	1.015	1.040
0.46	0.870	0.895	0.920	0.945	0.970	0.995	1.020	1.045
0.45	0.875	0.900	0.925	0.950	0.975	1.000	1.025	1.050
0.44	0.880	0.905	0.930	0.955	0.980	1.005	1.030	1.055
0.43	0.885	0.910	0.935	0.960	0.985	1.010	1.035	1.060
0.42	0.890	0.915	0.940	0.965	0.990	1.015	1.040	1.065
0.41	0.895	0.920	0.945	0.970	0.995	1.020	1.045	1.070
0.4	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075
0.39	0.905	0.930	0.955	0.980	1.005	1.030	1.055	1.080
0.38	0.910	0.935	0.960	0.985	1.010	1.035	1.060	1.085
0.37	0.915	0.940	0.965	0.990	1.015	1.040	1.065	1.090
0.36	0.920	0.945	0.970	0.995	1.020	1.045	1.070	1.095
0.35	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
0.34	0.930	0.955	0.980	1.005	1.030	1.055	1.080	1.105
0.33	0.935	0.960	0.985	1.010	1.035	1.060	1.085	1.110
0.32	0.940	0.965	0.990	1.015	1.040	1.065	1.090	1.115
0.31	0.945	0.970	0.995	1.020	1.045	1.070	1.095	1.120
0.3	0.950	0.975	1.000	1.025	1.050	1.075	1.100	1.125
0.29	0.955	0.980	1.005	1.030	1.055	1.080	1.105	1.130
0.28	0.960	0.985	1.010	1.035	1.060	1.085	1.110	1.135
0.27	0.965	0.990	1.015	1.040	1.065	1.090	1.115	1.140
0.26	0.970	0.995	1.020	1.045	1.070	1.095	1.120	1.145
0.25	0.975	1.000	1.025	1.050	1.075	1.100	1.125	1.150
0.24	0.980	1.005	1.030	1.055	1.080	1.105	1.130	1.155
0.23	0.985	1.010	1.035	1.060	1.085	1.110	1.135	1.160

2.2.1.1.2 Alternate Regulator Configuration

Some regulators do not contain a V_{FB} pin and only have VSENSE pins. The VSENSE of the regulator responds to dynamic voltage changes and adjusts V_{AVS} quickly. The AVS system works with this regulator configuration. In this case, an alternate connection topology is used as illustrated in Figure 6. In this topology, the output of VSENSE on the SOC is very close to V_{AVS}, and all of the above equations to find the component values are still valid. The C_{adc} is half the value of the previous topology, as there are two capacitors to rails instead of just one.

The above analysis assumes large input impedance for the V_{FB} node of the regulator so that the effective resistance of R_{top} and R_{bot} is not changed. However, if the regulator has low input impedance the voltages created by the above equations do not hold as there is another parallel resistance path. To reduce this issue, decreased values of R_{adc}, R_{top}, and R_{bot} can be used but this can cause the DAC to source too much current. The solution is to use an operational amplifier, as depicted in Figure 7. The op-amp's high impedance limits the DAC current but allows for lower values of the resistor network. It is important that the values of the resistor network are not too low as the VSENSE pins can only source 35 mA of current. The added high-value resistors depicted in Figure 7 ensure a starting voltage on the op-amp. This configuration can be used for both implementations of AVS depicted in Figure 5 and Figure 6.

To choose the resistor values for R_{op1} and R_{op2} in Figure 7, the ratio can be found by taking a voltage divider with V_{AVS} and thus V_{SENSEP} is set to 0.85V, V_{FB} is set to the appropriate value based on the regulator, and V_{ADC} is set to the appropriate look-up value in Table 2 on page 13. The absolute value of R_{op} should be in the 100 kΩ range. For example, for a regulator with V_{FB} set to 0.55V, V_{ADC} should be set to 0.55V. With R_{op1} set to 100 kΩ, R_{op2} should be set to 185 kΩ.

Figure 6: Alternate AVS Configuration

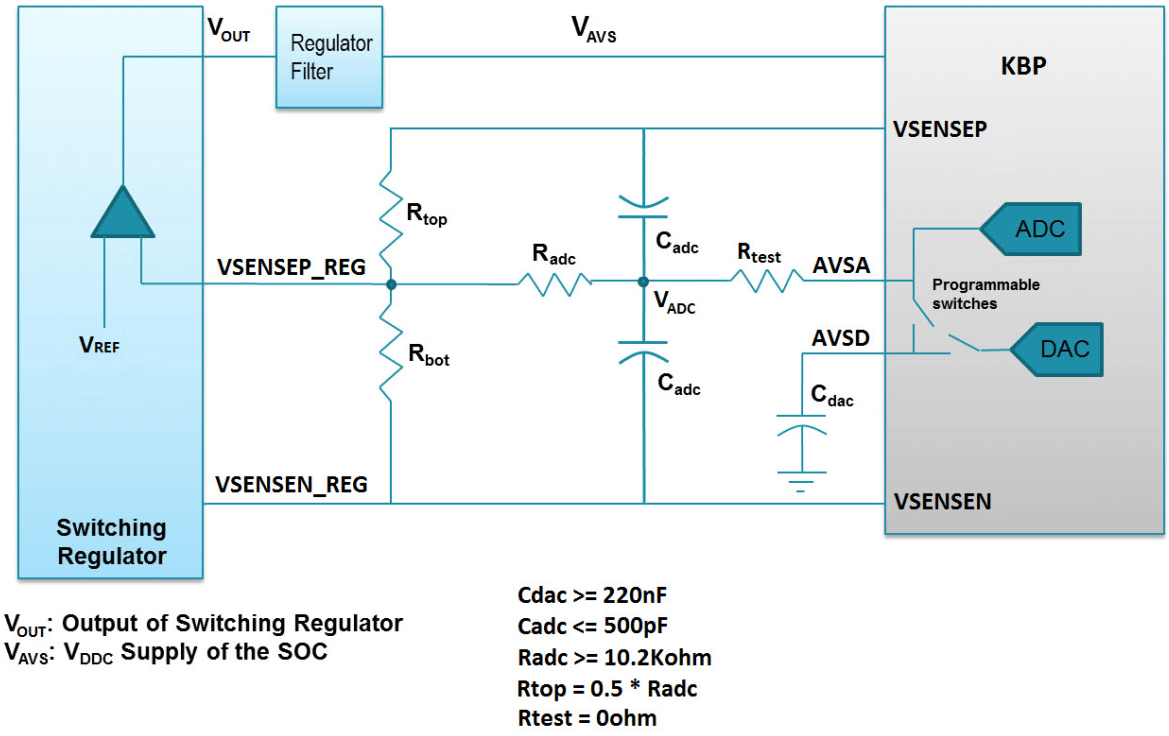
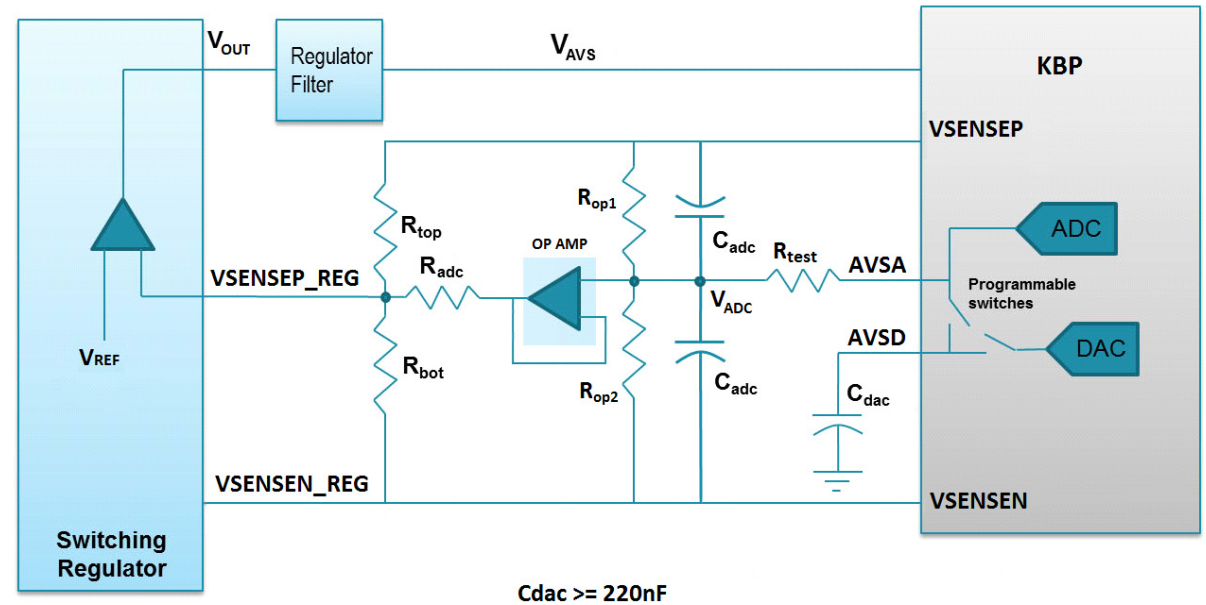


Figure 7: Alternate AVS Configuration with Op Amp

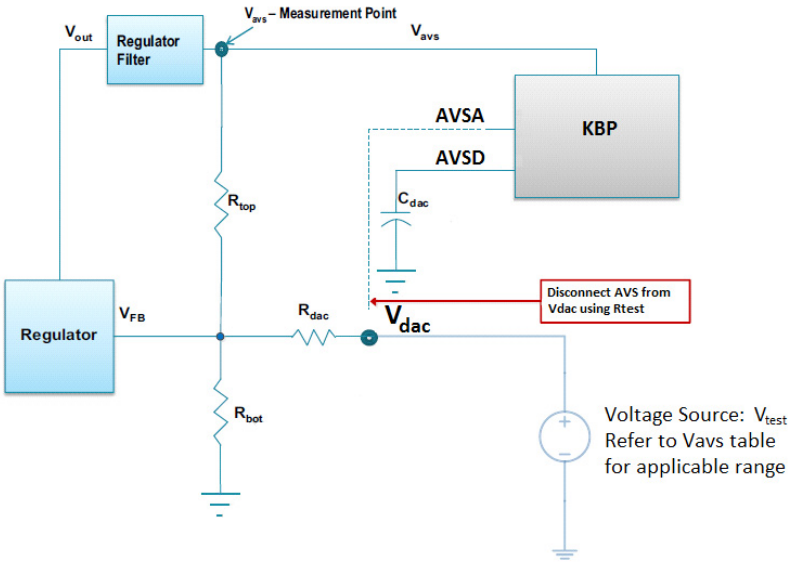


V_{OUT}: Output of Switching Regulator
V_{AVS}: V_{DDC} Supply of the SOC

Cdac >= 220nF
Cadc <= 500pF
Radc >= 10.2Kohm
Rtop = 0.5 * Radc
Rtest = 0ohm

2.2.1.1.3 Regulator Testing Procedure

Figure 8: Configuration to Test Switching Regulator



The applied voltage is not allowed by the chip hardware to drop below, or go above, a certain voltage. These levels depend on the silicon speed and temperature of an individual part. It is required that the switching regulator that supplies the AVS voltage be tested using the following procedure. See Figure 8.

CAUTION! There is a risk of damaging the KBP if the initial voltage level from the voltage source used in this test is not set in the safe 0.75V–0.80V voltage range.

1. Start with a system board with all the components installed, including the AVS components specified in these guidelines.
2. Disconnect the R_{test} resistor from the KBP by lifting its terminal on the R_{ADC} side from its connection pad. R_{test} is optional and can be shorted. In this case, the R_{ADC} terminal on the KBP side must be lifted from its connection pad. See Figure 8.
3. To protect the KBP against accidental damage, set the external voltage source V_{test} (connected to the test point at V_{ADC}) to an initial safe value in the range of 0.75V–0.80V.
4. Power up the board.
5. Attach the external voltage source to the added test point at V_{ADC}, which is now disconnected from the KBP. If the R_{test} resistor was not used, connect the external supply to the lifted R_{ADC} resistor terminal.
6. Slowly vary the voltage from the external voltage source (V_{test} connected at V_{ADC}) in the highlighted range indicated in Table 2 on page 13 for the specific regulator's V_{REF}. Since the safe starting voltage is somewhere in the middle of the range, it is necessary to vary the voltage in the upward and downward directions to cover the full range.
   - It is very important to stay within the allowed range in Table 2 on page 13. Going outside the allowed range in Table 2 on page 13 may damage the KBP.
   - In Table 2 on page 13, the yellowed text reflects the expected AVS voltage for each V_{REF} level.
   - As an example, if the regulator being used has a nominal V_{REF} value of 0.6V, the allowed V_{test} range is from 0.90V to 0.34V to cover the AVS operating range of 0.70V to 0.98V.
7. Measure the V_{AVS} voltage at the top terminal of R_{top} at each V_{test} input level using a voltmeter.

NOTE: Measuring the V_{AVS} voltage at any other location may show discrepancies relative to the expected voltage in the table due to board IR-voltage drop.

8. After the V_{test} sweep is completed and the data is collected from steps 6 and 7 above, return the voltage-source voltage to the initial safe zone (0.75V–0.80V) and disconnect from the board.

   Only after the voltage source is disconnected from the board can the V_{test} supply be turned off.
9. Safely power off the board once V_{test} is disconnected.
10. Plot the measured V_{AVS} and the corresponding expected voltages from Table 2 on page 13 (for the specific V_{REF} of the chosen regulator) against V_{ADC} and compare the results.
    - The KBP VDD voltage V_{AVS} as a function of the external voltage source should follow Equation 1 with V_{ADC} set to V_{test} values.
    - It is expected that the curves be within 2% of each other and the relationship to V_{ADC} is linear. If this condition is not met, the AVS system will not function as required. Choose a different regulator.

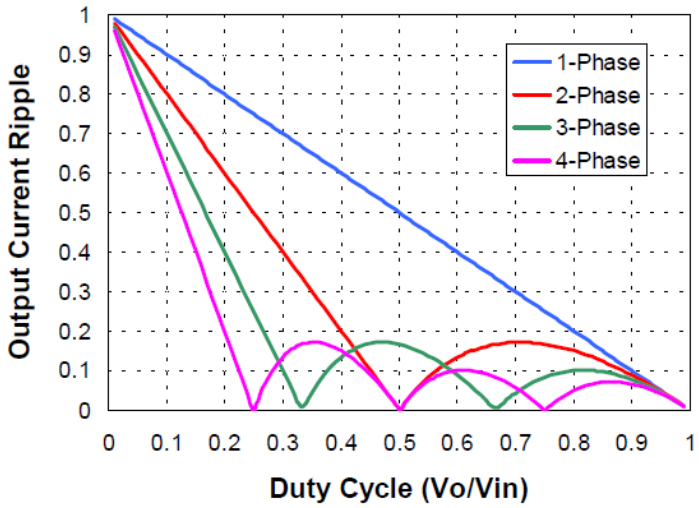
2.2.1.2 Multi-Phase Topologies

Use of a multi-phase topology has the following advantages:

- Reduced output voltage ripple as a result of inductor current ripple cancellation.
- Faster transient response as a result of smaller inductors.
- Possible to reduce overall solution size.
- Efficiency improvements.

It is recommended to use a multi-phase regulator for the core voltage.

Figure 9: Normalized Output Current Ripple vs. Duty Cycle



2.2.2 SRAM Memory Regulator

VDDM is used to power the SRAM on the chip. A separate power supply is required for VDDM as it is a different voltage from VDD or the analog supplies. Due to the high current requirement, a switching regulator is recommended.

2.2.3 Analog Regulator

There are many voltage islands that ultimately get their power from a low-voltage analog (LVA) supply. Either a low-dropout linear regulator or a switching regulator can be used for the LVA supply. The total current profile is at the upper end of what an LDO can handle. If desired, the LVA supply may be split into multiple regulator supplies. It is recommended to keep each VDDS grouped with its corresponding VDDSPLL supplies. VDDS1 goes with VDDSPLL1. VDDS2 goes with VDDSPLL2. VDDS3 goes with VDDSPLL3, and so on. The VDDS supplies may be combined with a maximum of three VDDS supplies being merged onto a filter. Also, it is desired to group consecutive supplies (for example, merge VDDS1, 2, 3 instead of VDDS1, 4, 8).

NOTE: If some SerDes lanes are to be powered down, the startup condition will have all of them powered. The regulator must be able to handle this startup condition.

The low-power and ripple specifications for the high-voltage analog (HVA) supplies make a low-dropout linear regulator attractive. It is recommended to power the LDO from 2V, 2.5V, or 3.3V. If powered from higher than 3.3V, the efficiency may not be acceptable and a switch-mode supply may need to be used for the HVA supply.

Additional filtering of the power supply ripple is recommended on VDDS, VDDSPLL, VDDCPLL, VDDPC, VDDPCPLL supplies, using a second order LC filter. A ferrite bead may be substituted for the inductor.

Table 3: Summary of Power Supply Regulator Recommendations

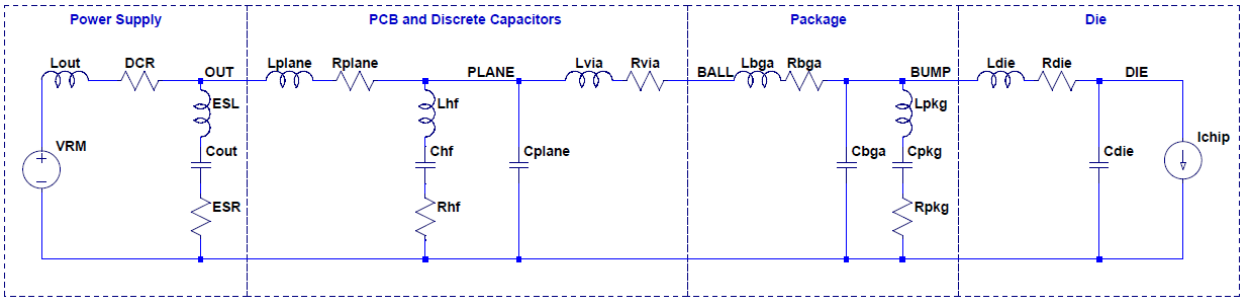
Power Supply	Regulator Recommendation	Desirable Features and Comments
Core	High-performance multiphase switch-mode buck regulator	■ Remote voltage sense ■ Dynamic phase shedding ■ Non-linear control mode for fast-load transient response ■ Load-line regulation ■ Enable/disable ■ Power good signal ■ Fault protection ■ Ability to set fine-grain voltage
SRAM	Switch-mode buck regulator	■ Remote voltage sense ■ Enable/disable ■ Power good signal ■ Fault protection
Low-Voltage Analog (LVA)	Switch-mode buck regulator or low-dropout regulator	■ Remote voltage sense ■ Low noise ■ Sufficient headroom to handle start-up power ■ High efficiency at nominal operating point ■ Enable/disable ■ Power good signal ■ Fault protection
High-Voltage Analog (HVA)	Low-dropout regulator	■ Low noise ■ Small solution size ■ Enable/disable ■ Power good signal ■ Fault protection

NOTE: Power supply pins are required to be fanned out to individual vias to connect with power supply planes. Sharing vias with multiple supply pins significantly increases the BGA loop inductance and is prohibited.

2.3 Core Power Delivery Network and Decoupling Scheme

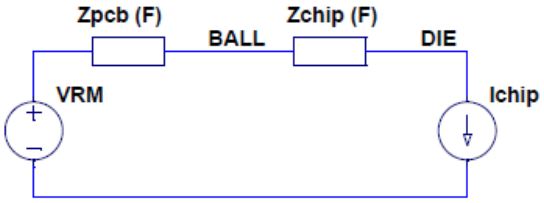
The output impedance of a perfect voltage source is zero, meaning the source can supply any current with no change in voltage. In a real system supplying power to an integrated circuit, the output impedance is composed of several components and many parasitic elements. A lumped element model of a typical system is shown in Figure 10.

Figure 10: Components and Parasitic Elements of a Typical Power Delivery Network



The power delivery network can be thought of as a voltage source with a frequency-dependent source impedance. Using Thevenin's Theorem, the source impedance can be found easily as a combination of the components in Figure 10. In Figure 11, it is split amongst PCB (controlled by the system designer) and chip components (controlled by the vendor).

Figure 11: Equivalent Circuit Split Into PCB and Chip Impedances



The voltage range for the core VDD supply is specified as ±3%. It is assumed that this will be split evenly amongst the regulator variation (AC + DC) and the AC ripple at the BGA caused by the chip noise. Thus the KBP device's specification for maximum AC ripple is 1.5% or 12 mV for an 800 mV supply.

The change in load current varies greatly depending on the application. The factors that affect this load current are the search rate, number of active blocks, and the operating frequency. The KBP can experience extremely high current spikes in the worst case. The maximum current change is TBD. It will be on the order of around 50 A/ns although it is unlikely to occur under practical applications. Active blocks should be limited as much as possible.

The impedance of the PDN is given by:

$$Zpdn,\ max(f) = \frac{Vn,\ chip}{Ichip\ (f)}$$

Thus, Zpdn, max (f) should be around 0.24 mΩ over the frequency range of the loop bandwidth of the regulator up to the effective frequency the board can decouple. The loop bandwidth of a typical buck converter switch regulator is in the 100 kHz range. The effective frequency the board can decouple is on the order of 20 MHz. These parameters are summarized in Table 4.

Table 4: Design Parameters for Core Supply PDN Analysis

Parameter	Symbol	Specification/Target
Chip noise budget	$V_{n, chip}$	12 mV
Maximum PCB impedance	$Z_{pcb, max}$	–0.24 mΩ
PCB impedance bandwidth	$f_{H, pcb}$	20 MHz

The inductance (ESL) of the decoupling capacitors is dominated by the component dimensions, and also highly depends on the loop area created by connection to power planes. It is extremely important to reduce the ESL of the decoupling as much as possible. This is achieved through thoughtful placement and layout techniques:

1. Place vias in pads of 0603 or 0402 capacitors.
2. Place vias between pads of larger size capacitors (0805 or larger).
3. Place vias beside pads if via-in-pad is not acceptable by manufacturer.
4. Minimize via length when possible.

   If power planes are close to top-side, placing capacitors on top-side surrounding the chip will result in significantly lower mounting inductance versus placing the capacitors on the bottom-side.

The resistance (ESR) of the capacitor is due to metal resistance and depends on the material properties of the component. Since it is a function of material properties, the ESR value differs dramatically across different vendor offerings of equivalent components. The ESR must be supplied by the capacitor vendor (or measured) and should be kept as low as possible.

In systems with tight real-estate constraints, it is attractive to place 0402 decoupling capacitors in the power and ground via array under the chip. This area is essentially free real estate since it cannot be used by any other components. It is recommended to start decoupling by adding one 0402 capacitor per VDD/GND pair.

The decoupling scheme starts with high-frequency decoupling capacitors placed in the power and ground via array under the chip. Figure 11 illustrates such a placement. Progressively higher valued capacitors ring the device, which lowers the impedance at lower frequencies. The bottom side of the board may also be used to ring the device with capacitors. X2Y capacitors should also be considered, as they can achieve a lower ESL. The complete decoupling scheme should be simulated to achieve the recommended impedance over the wide frequency range.

Figure 12: Recommended Decoupling Capacitor Placement Under the Device

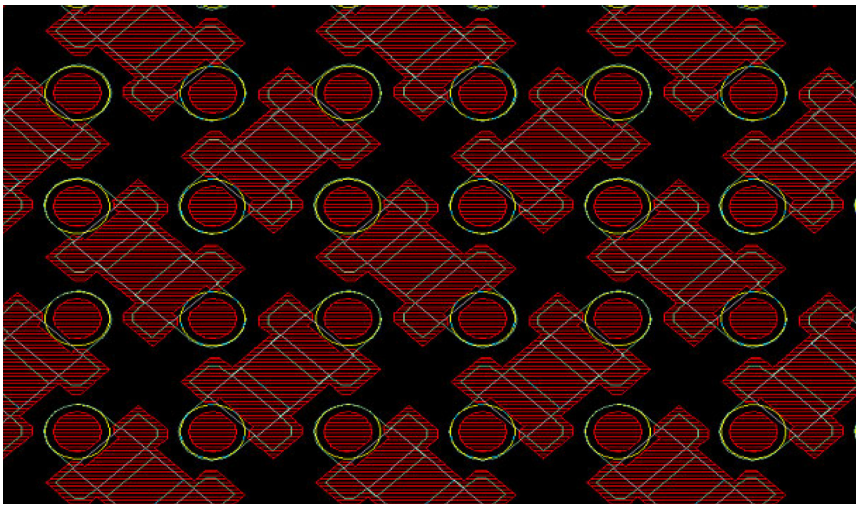


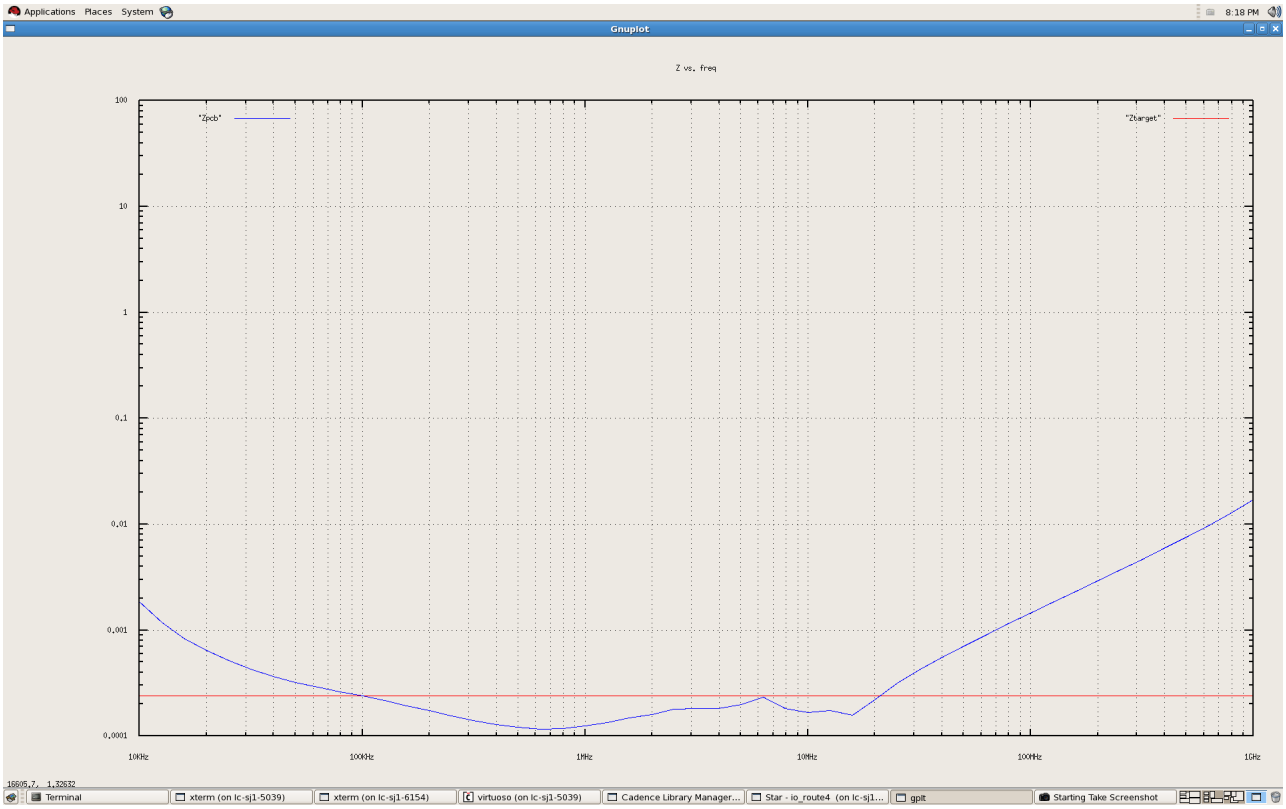
Table 5 gives the recommended decoupling scheme for the 16 nm KBP device.

Table 5: Core Supply PDN Example Decoupling Component Summary

Capacitor Size	Value	ESR	ESL	Count	Placement Notes
7.3 x 4.3 mm	470 µF	4.5 mΩ	1.00 nH	24	Place near regulator.
1206	100 µF	5.0 mΩ	0.70 nH	26	Place top/bottom-side in ring around chip.
1206	47 µF	5.0 mΩ	0.70 nH	20	Place top/bottom-side in ring around chip.
1206	22 µF	5.0 mΩ	0.70 nH	10	Place top/bottom-side in ring around chip.
1206	10 µF	5.0 mΩ	0.70 nH	10	Place top/bottom-side in ring around chip.
0402	4.7 µF	9.0 mΩ	0.55 nH	30	Place top/bottom-side in ring around chip.
0402	2.2 µF	9.0 mΩ	0.55 nH	30	Place top/bottom-side in ring around chip.
0402	1.0 µF	10.0 mΩ	0.40 nH	30	Place top/bottom-side in ring around chip.
0402	0.47 µF	10.0 mΩ	0.40 nH	60	Place bottom-side in BGA via array.
0402	0.22 µF	10.0 mΩ	0.40 nH	118	Place bottom-side in BGA via array.

Figure 13 graphs the impedance over frequency of the solution.

Figure 13: Impedance vs. Frequency for VDD Decoupling



2.3.1 SRAM Supply PDN Recommendation

Table 6 describes the recommended decoupling scheme for the VDDM supply. One capacitor under the BGA via array (23 total) in addition to a sufficiently designed LC output filter for the switching regulator is recommended. The impedance profile is shown in Figure 14.

Table 6: SRAM Supply PDN Example Decoupling Component Summary

Capacitor Size	Value	ESR	ESL	Count	Placement Notes
7.3 mm x 4.3 mm	470 µF	4.5 mΩ	1.00 nH	1	Place near regulator.
0402	1 µF	10.0 mΩ	0.40 nH	23	Place bottom-side in BGA via array.

Figure 14: Impedance vs. Frequency for VDDM Decoupling

2.3.2 LVA Supply PDN Recommendation

The LVA supplies require filters to remove high frequency noise. They are all SerDes supplies. See SerDes/Core PLL Supply Specifications for details on the filter requirements.

2.3.3 HVA Supply PDN Recommendation

One 1 µF 0402 capacitor per power pin placed under the BGA via array is recommended (11 total) for the 1.8V supply. One 1 µF 0402 capacitor per power pin placed under the BGA via array is recommended (18 total) for the 1.2V supply.

2.4 SerDes/Core PLL Supply Specifications

The KBP has two SerDes interfaces which consist of 36 high-speed 28 Gb/s lanes and one PCIe Generation-2 lane. The 28 Gb/s lanes have nine low-voltage PLL supplies (VDDSPLL1–9), nine low-voltage general lane supplies (VDDS1–9), one 1.2V termination supply (VDD12), and one 1.8V general supply that is shared amongst other miscellaneous non-SerDes circuits (VDD18). The PCIe lanes have one low-voltage PLL supply and one low-voltage general lane supply.

The KBP has one main core PLL that generates the core clock. It uses a 1.8V supply (VDDCPLL).

The supplies are summarized in Table 7.

Table 7: SerDes/Core PLL Supply Specifications

Supply Name	Supply/Conditions	Min.	Typical	Max.
Absolute Voltage	VDDSPLL1–9, VDDS1–9	0.775V	0.80V	0.825V
	VDDPC, VDDPCPLL	0.76V	0.80V	0.84V
	VDD12	1.165V	1.20V	1.235V
	VDD18	1.71V	1.8V	1.89V
	VDDCPLL	1.745V	1.8V	1.845V
Source current	VDDS1–9	–	770 mA	925 mA
	VDDSPLL1–9	–	100 mA	120 mA
	VDDPC	–	50 mA	65 mA
	VDDPCPLL	–	30 mA	65 mA
	VDD12	–	550 mA	800 mA
	VDD18	–	580 mA	700 mA
	VDDCPLL	–	40 mA	50 mA
AC ripple ratio	10 kHz to 100 MHz	–	–	1.5%
	VDDS1–9, VDD12, VDDPC, VDDPCPLL	–	–	1.25%
	VDDSPLL1–9	–	–	0.375%

The AC ripple specification is very stringent. To meet this specification and to isolate the supplies from random noise, it is required to filter all of the low-voltage SerDes supplies and the core PLL supply with a second-order low-pass LC filter. To avoid a filter, the regulator must meet the AC ripple specification and the supply must be isolated from other supplies (no sharing).

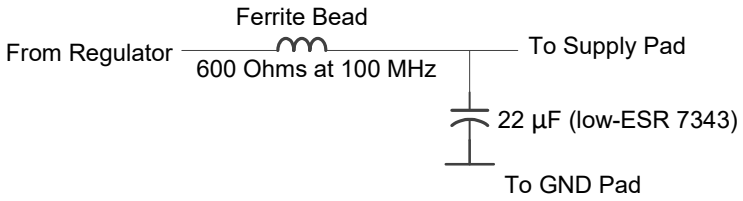
NOTE: Each supply requires its own filter (nine for VDDSPLL1–9), but three of the VDDS1–9 supplies may be merged and share a filter. Table 8 describes the recommended filter for each supply. Bandwidth is defined as the –3 db point at roll-off. The second order filter requires a 40 db attenuation/decade of frequency.

Table 8: Filter Recommendations for SerDes/Core PLL Supplies

Supply	Filter Requirement		Component Type	
	Filter	Bandwidth	Ferrite Bead	Capacitor
VDDS1–9, VDDSPLL1–9	LC filter or ferrite bead filter, second order	<50 kHz	1 µH L, 22 µF C or 600Ω at 100 MHz Ferrite bead	One 22 µF
VDDPC, VDDPCPLL	Ferrite bead filter, second order	<100 kHz	Ferrite bead 300Ω at 100 MHz	One 1 µF
VDDCPLL	Ferrite bead filter, second order	<100 kHz	Ferrite bead 120Ω @ 100 MHz DCR<1Ω Capacitors with DCR<15 mΩ	One 10 µF capacitor One 0.1 µF capacitor
VDD12, VDD18	No filter required. Must meet ripple specification.	–	–	–

The chosen inductor or ferrite bead should have a low ESR at low frequency so as to not degrade the DC voltage of the supply. The voltage specification listed in Table 7 must be met regardless of the IR drop. It may be difficult to find a low enough resistance for a ferrite bead for the VDDS1–9 supplies, especially if they are merged. In this case, an inductor with low ESR is recommended.

Figure 15: Example Filter for SerDes VDDS1–9 or VDDSPLL1–9 Supplies



2.5 Power Planes and Stack-up Placement

Due to the high level of digital switching current on the core supply, it is very important to minimize the via inductance between the power plane and BGA pins, as any increased inductance in the power path has a direct impact on the level of on-chip supply noise. Minimizing via inductance is accomplished by assigning the core power supply to a plane layer close to the component mounting side, effectively minimizing via length and inductive loop area. It is required to place the core supply plane within five layers of the component mounting side.

The board plane capacitance provides excellent decoupling and it is recommended to use multiple power and ground planes dedicated to the VDD and VSS rails. A power and ground plane pair separated by 4 mils of Megtron 6 has an approximate capacitance of 2 nF per 10 square inches. At a minimum, it is recommended to devote 10 square inches of the board power plane to VDD. VSS should be paired with VDD to ensure good decoupling.

The LVA and HVA supplies must be isolated from the noisy VDD supply to prevent noise coupling into the sensitive analog supplies. This can be achieved by physical separation and ground planes.

The LVA supply also exhibits switching current, though to a much lesser extent compared to the core supply. The LVA power plane can be placed as deep as 12 layers from the component mounting side.

Adjacent power/ground planes in the stack-up are very important in high-performance PCB designs. The added plane capacitance significantly lowers PDN impedance at high frequency. Wherever possible, it is recommended to utilize unused copper area to build additional plane capacitors with power/ground planes.

2.6 Sharing Supplies with Other Devices

Ideally, each device in the system is powered by its own, dedicated power supply. However, as real estate becomes constrained, component count may need to be reduced to fit the design within the allocated area. The easiest method of doing so is to consolidate power supplies for multiple devices. This section is meant to provide some guidance on this topic. Below is a general guideline for identifying devices that may be consolidated. In this section, the device's power supply input will be referred to as a load.

1. Group loads by nominal voltage.
2. Split groups into sub-groups by load type (analog/digital, high power/low power, SerDes/non-SerDes), noise sensitivity, voltage tolerance, etc.
3. Split sub-groups again by spatial location on the PCB.

After step 3, some judgment is needed to determine which sub-groups could be powered by a single supply, which require further division, and which could be merged to share a single supply. Elements to consider are IR voltage drop, transient load conditions, supply efficiency versus output current, and available real estate.

As mentioned earlier, the LVA supplies are candidates for sharing. In this case, it is required to filter each supply even if the ripple specification is met.

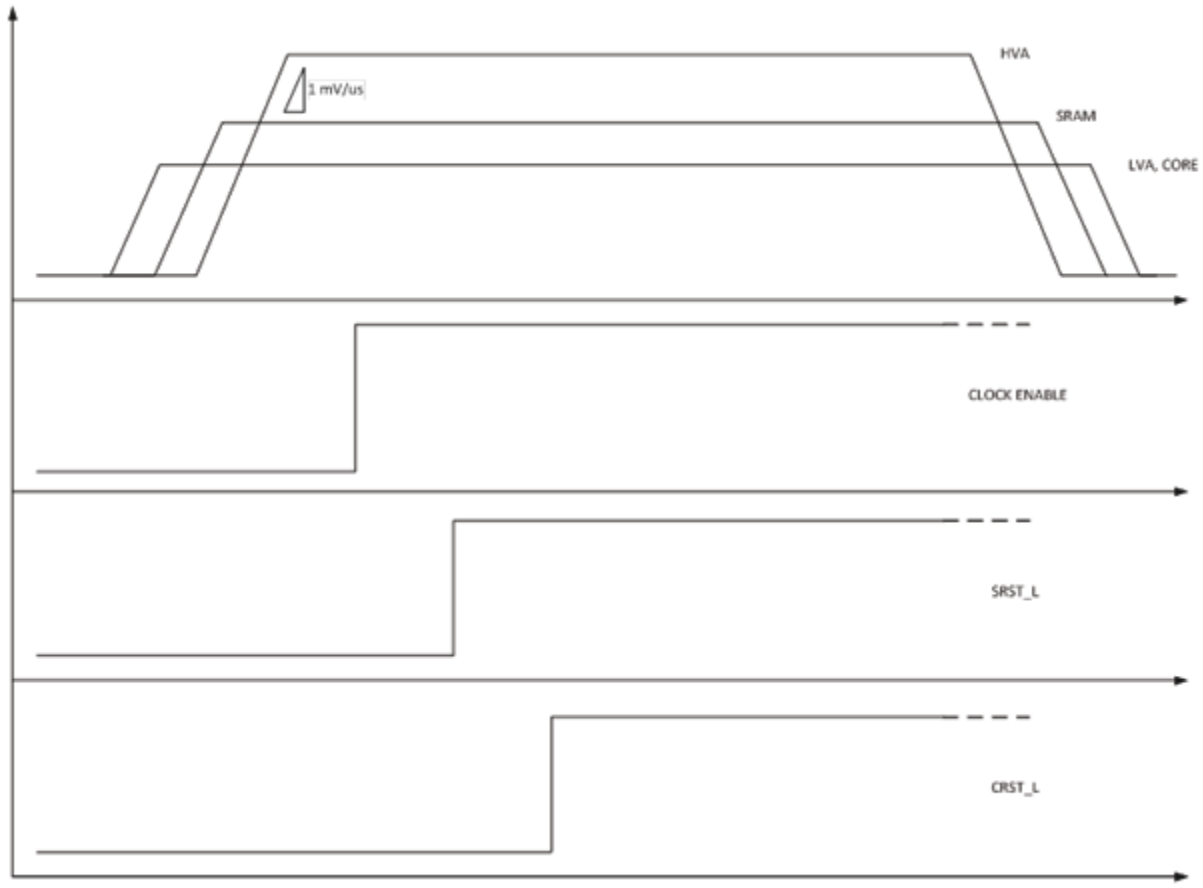
2.7 Power-On/Off Requirements

The main requirement to power on/off the device is to not allow the voltage difference between HVA, SRAM, and other supplies to exceed 1.0V. This should be accomplished using a sequenced supply power-up and power-down approach. The power supply ramp rates must be in the range of 5 mV/µs to 0.2 mV/µs (1 mV/µs recommended). The LVA and Core supplies turn on first, followed by the SRAM, and finally the HVA supplies. The SRAM voltage is allowed to turn on at the same time

as the LVA and Core supplies. Each supply should be at full rail voltage before the next supply starts to ramp. The power-down sequence is the reverse order starting with HVA supplies followed by SRAM and finally the LVA/Core supplies. The edge rates apply over the entire range of voltage. It is important that the device power-on from rails all at 0V and power-off to a final voltage of 0V.

Before power-up, it is required that all signal inputs are low so as to avoid turning on the ESD diodes and damaging the device. It is recommended to enable clocks and have their inputs toggling after power supplies are in regulation and before the reset signals are de-asserted. The internal core PLL takes about 10 us after enabling and stable reference clock to lock ensuring a stable core clock. SRST_L must wait 25 ms after power-on before being de-asserted. CRST_L must wait another 1.5 ms after SRST_L de-assertion before being de-asserted itself. PERST_L must wait at least 100 ms after power-on, 2 ms after SRST_L de-assertion, and 100 µs after stable and enabled reference clocks before de-assertion. Figure 16 illustrates the recommended approach to the power-on and power-off requirement.

Figure 16: Consecutive Approach Power Sequence and Reset Timing

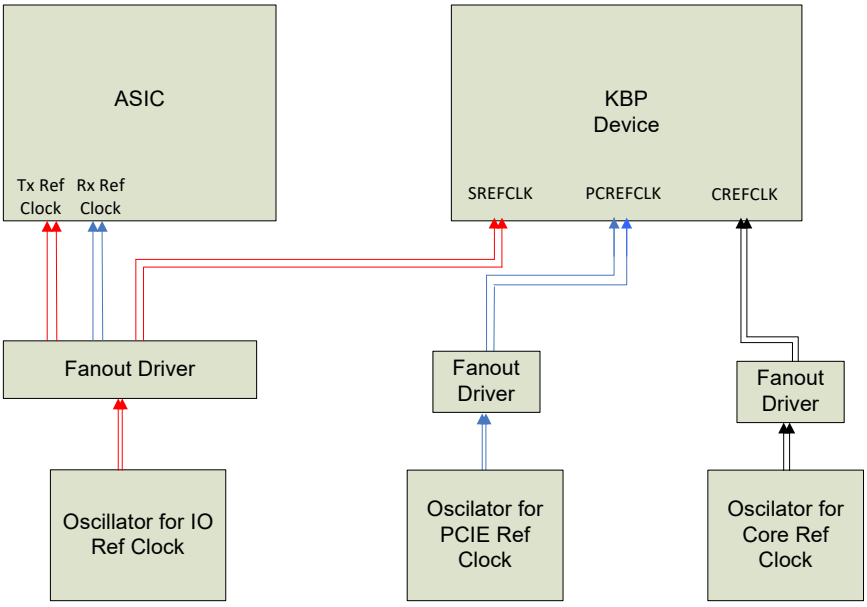


Chapter 3: Clocks

3.1 Overview

Figure 17 gives a general layout of the ideal clock topology.

Figure 17: Clock Topology Showing SREFCLK, PCREFCLK, and CREFCLK



This topology may not be possible to implement if the ASIC or host device's SerDes circuits require a reference clock frequency that does not match the KBP specification (125 MHz or 156.25 MHz). In this case, the total PPM difference between the ASIC or host device's reference clock source and the KBP's reference clock source must not exceed ±150 ppm.

All reference clocks are 100Ω differential clocks and each pair should be routed together with minimal skew between the positive and negative traces. They should also be shielded on all sides by their respective ground planes. VSS for the SerDes clocks and core clock). This means having VSS planes on top and bottom of the traces and lateral shielding traces or planes for the same layer of the traces. All lateral shielding must be stitched to the above and below planes.

All reference clocks are terminated internally with a nominal differential termination of 100Ω. External termination is not required.

NOTE: In configurations without the PCIe Generation-2 interface, PCREFCLK can be left unconnected.

3.2 SerDes Reference Clocks

SREFCLK is the clock reference for the high-speed SerDes circuits, while PCREFCLK is the clock reference for the Generation-2 PCIe circuits. Since the SerDes data rate is derived using the reference clock frequency, a precise reference is required to hit the desired data rate. Ideally, transmit and receive circuits on either side of the SerDes link operate at precisely the same data rate, which is the case when both reference clocks are derived from the same source. However, if this is not possible or is difficult to implement, the receiver circuits are able to handle small deviations in data rate. Table 9 shows the reference clock requirements for the high-speed SerDes clock SREFCLK.

Table 9: SREFCLK Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit.
Frequency	–	106.25	125/156.25	161.13	MHz
Frequency Offset	Between different REFCLKs	–50	–	+50	ppm
Signaling	CML	–	–	–	–
Amplitude	Differential Peak-Peak at Ball	0.8	1.0	1.4	V
Edge Rate	20%–80%	–	300	400	ps
Duty Cycle	–	40	50	60	%
Input Impedance	Differential	80	100	120	Ω
Common Mode Voltage	Internally biased	–	0.4	–	V
Integrated Phase Noise	12 kHz–20 MHz	–	–	0.3	ps RMS
Phase Noise	at 10 kHz	–	–	–110	dbc/Hz
	at 100 kHz	–	–	–130	dbc/Hz
	at 1 MHz	–	–	–130	dbc/Hz
	at 10 MHz	–	–	–150	dbc/Hz
	at 100 MHz	–	–	–150	dbc/Hz

The two SREFCLK signals must be externally AC coupled into the device with 10 nF or greater capacitors. Table 10 shows the reference clock requirements for the PCIe reference clock PCREFCLK.

Table 10: PCREFCLK Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit.
Frequency	–	–	100	–	MHz
Frequency Offset	Between different REFCLKs	–100	–	+100	ppm
Signaling	CML	–	–	–	–
Amplitude	Differential Peak-Peak at Ball	0.6	–	1.6	V
Amplitude	Single-Ended Absolute Voltage	–0.4		VDDPCPLL + 0.4	V
Edge Rate	30%–70%	–	–	470	ps
Duty Cycle	–	40	50	60	%
Input Impedance	Differential	80	120	120	Ω
Common Mode Voltage	At the BGA Ball	0.1	–	0.7	V
Integrated Phase Noise	12 kHz–20 MHz	–	–	1	ps RMS

For PCREFCLK, DC or AC coupling is allowed. DC coupling is the default in this device.

When DC coupling, the common-mode voltage range must be maintained as required by the BCM16K PCIe reference clock specifications. In this mode, the PCIe reference clock termination bias voltage is set by the common-mode voltage.

When AC coupling, the recommended capacitor value is 100 nF. In this mode, the PCIe reference clock termination bias voltage must be enabled within the BCM16K via software programming.

3.3 Core Clock

The CREFCLK input supplies the clock to the core logic circuits. The clock input feeds a PLL and multiplier block generates a clock in the range of 250 MHz–900 MHz, depending on CPSEL configuration settings. See the data sheet (16000-DS1xx) for details on the CPSEL configuration. Table 11 gives the reference clock requirements for the core clock CREFCLK.

Table 11: CREFCLK Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency	–	–	100/156.25	–	MHz
Frequency Offset	Error in desired frequency	–100	–	+100	ppm
Signaling	CML	–	–	–	–
Amplitude	Differential Peak-Peak at Ball	0.5	–	1.8	V
Edge Rate	20%–80% with 500 mV swing	–	–	375	ps
Duty Cycle	–	30	50	70	%
Input Impedance	Differential	80	100	120	Ω
Common Mode Voltage	Internally biased	–	0.9	–	V
Integrated Phase Noise	12 kHz–20 MHz	–	–	1	ps RMS

AC-coupling capacitors are not built into the device for CREFCLK. External 10 nF AC-coupling capacitors are required to be placed on the board.

Chapter 4: Thermal Considerations

4.1 Measuring Die Temperature

The 16 nm KBP device includes an on-die temperature sensor. The scheme and error is TBD.

4.1.1 Cooling Considerations

System designers must consider heat management in their designs. The 16 nm KBP is a high-thermal density device manufactured with state-of-the-art process technology. The amount of heat generated on these high-speed circuits creates a significant thermal management challenge. Special attention must be paid to power budgets and heat removal requirements.

Thermal dissipation performance must be understood prior to integrating the KBP on a printed circuit board to ensure the device operates within its defined temperature limits. A proper heat sink and appropriate air flow must be provided to ensure device functionality and reliability.

System designers must take into account the thermal effect on the downstream devices in the airflow from the heat generated by the upstream device, as the downstream device will end up with higher T_A.

The appropriate heat requirement and air flow can be calculated using the equations below. The junction temperature is equal to the ambient temperature plus an offset proportional to the internal power dissipation, P.

$T_J = T_A + \theta_{JA} \times P$

Where

- T_J = Junction Temperature
- T_A = Ambient Temperature
- θ_{JA} = Thermal Resistance
- P = Power of the Device

θ_{JA} includes the temperature rise from junction to case and case to the outside ambient environment.

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

The system designer must provide heat sink and air flow to provide an adequate value for θ_{CA}. Adequate cooling must be provided for the KBP to operate properly. The system designer must examine the environment, the enclosure, and the placement of the device.

4.2 Maximum Pressure Specifications

Table 12: Maximum Pressure Specifications

Parameter	Specification
Maximum Continuous Compressive Force	13.1 kg

Chapter 5: Interlaken Look-Aside Serial Interface (I-LA)

5.1 Overview

The 16 nm KBP device has 36 transmit and receive lanes that can be configured to operate at 10.3125 Gb/s, 12.5 Gb/s, 15 Gb/s, 25.78125 Gb/s, 27.34375 Gb/s, and 28.125 Gb/s data rates. The SerDes drivers and receivers have been implemented to work with channels that meet CEI-25G-SR, CEI-28G-SR, and HMC electrical specifications. The protocol used is Interlaken-LA.

The Interlaken-LA interface has a few important features to reduce routing difficulty:

- Per-lane TX/RX polarity inversion.
  Polarity can be swapped on any lane in the layout if it improves routing.
- Per-link lane reversal.
  This feature “flips” the interface lane ordering. For example, if lanes [17:0] are enabled and lane reversal is enabled, TX/RX[17:0] is remapped to TX/RX[0:17]. Lane reversal works on the port boundary of the physical lanes: TX/RX[35:0] for single port and TX/RX[17:0] and TX/RX[35:18] for dual port.

Refer to the appropriate data sheet for additional information.

5.2 High-Speed Routing and Board Layout Guidelines

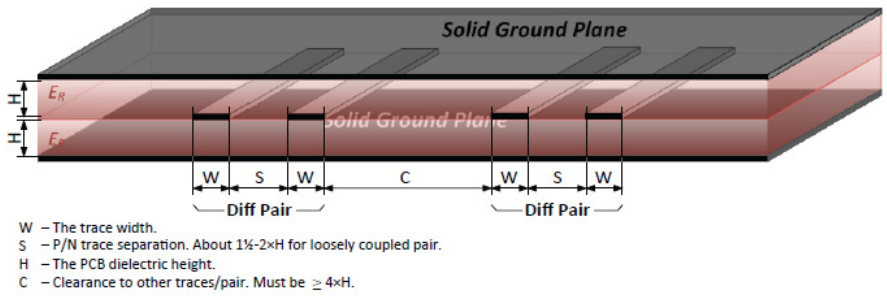
This section provides guidance on successfully implementing PCB channels with sufficient bandwidth to support 28.125 Gb/s Interlaken-LA serial links (ILA).

5.2.1 General Routing

Though the SerDes is terminated at 100Ω differential, the overall SerDes performance is improved if the user’s PCB interconnect is set to a slightly lower impedance. Use 95Ω differential impedance for the RX and TX signals. For the breakout region under the BGA, use 25Ω for common-mode signaling (or 50Ω single-ended routing). The recommended tolerance of the trace impedance is ±5%.

It is recommended to route the high-speed signals as a strip-line and not a micro-strip. Keep micro-strip routing short at less than 1 inch. Figure 18 shows a general differential pair geometry and stack-up.

Figure 18: General Differential Pair Geometry and Stack-up

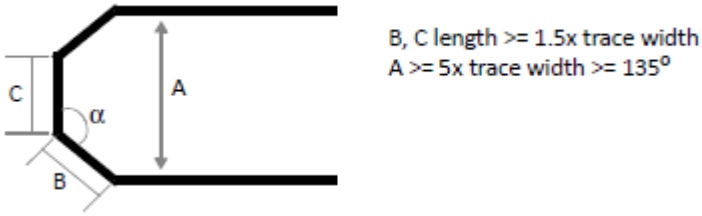


The trace width and intra-pair spacing is determined by the impedance target, board stack-up and other board properties. Wider traces are preferred to reduce copper loss, but should be kept to <10 mils. Use a tightly coupled differential pair.

Ideally, the trace routing should run in a straight line from source to destination. Avoid sharp bends in the trace routing. Use radius bend segments as illustrated in Figure 19. Curved routes are also acceptable.

NOTE: This type of routing adds skew to the P/N differential pair, which must be compensated. See "Skew " on page 36 for additional information.

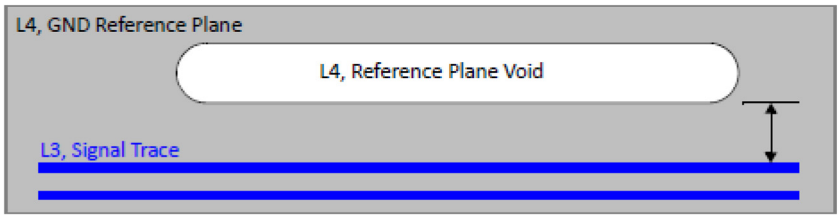
Figure 19: Use Radius Bend Segments



While a guard trace/ground patch is not required between signal pairs, if used, it must be stitched to VSS. The distance between stitching vias should be <40 mils.

All differential signals must be referenced to the VSS plane both above and below the signal layer. All VSS islands along the differential pairs must be stitched with a maximum spacing of 40 mils. Splits or voids in the VSS plane area under/above the signal traces are not allowed. The edge of a split/void in the reference plane must be at least 3x signal trace width from the signal trace. Figure 20 illustrates this requirement. Avoid overlapping power and ground islands/planes of different domains.

Figure 20: Routing Near Reference Plane Voids



Finally, if connectors are used, they must be certified for the line rate (for example, 28.125 Gb/s).

5.2.2 Crosstalk

To minimize crosstalk, it is recommended to route the TX and RX lanes on separate layers.

The sum of all crosstalk sources from BGA-to-BGA on a victim ILA receiver line should be kept at less than –46 dB at 14 GHz (28 Gb/s). RX NEXT has the most impact on the BER, so careful attention should be paid to this parameter. The insertion loss to crosstalk ratio is 25 dB for a 28.125 Gb/s link.

To reduce crosstalk, large inter-pair spacing is preferred. A minimum of 4x trace width spacing is recommended. In serpentine legs, to match routing length the spacing must be 5x the trace width to minimize coupling.

5.2.3 Skew

5.2.3.1 Differential Pair Skew

Skew between differential pairs lead to mode conversion (differential signal converted to common signal, and vice versa) and can shrink the eye opening. Skew between differential pairs is a result of any asymmetry in the channels as the signals pass through the channel, such as:

- Rounding a bend during routing (outside trace ends up slightly longer than inside trace)
- Remaining back-drill stub length differences (remaining stub is typically between 6 and 12 mil in length)
- Local dielectric constant variation due to fiberglass weave
- Driver, package, receiver induced asymmetries

Keep differential pair lengths as closely matched as possible to within 50 µm or 2 mils. When there is a mismatch, compensate for it near the location of the mismatch.

Skew compensation in bends can be done by bending in the opposite direction. However, this requires an even number of bends on the board which may not be possible. For small skews in the BGA breakout area, the trace can be lengthened right at the via, as shown in Figure 23.

NOTE: The impedance becomes single-ended in serpentine routing. Use 50Ω single-ended impedance in the serpentine areas and keep them as short as possible (<1 inch).

Figure 21: Removing Skew at the BGA Breakout Area

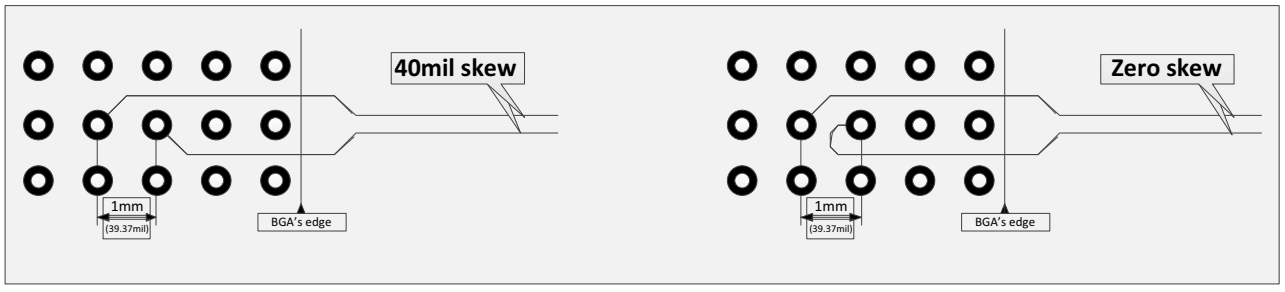


Figure 24 uses serpentine routing to remove large amounts of skew.

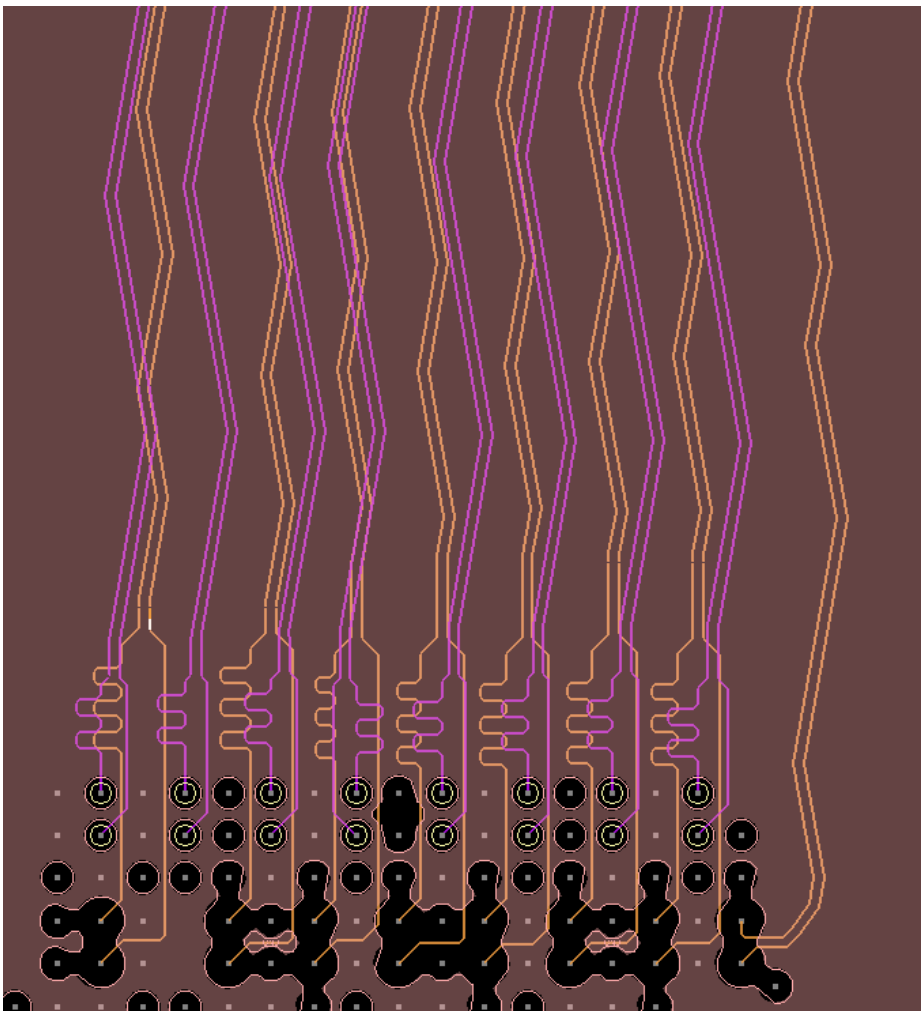
Figure 22: Using Serpentines to Remove Skew on Differential Pairs

Fiber-weave-induced skew is caused by asymmetry in local dielectric constant seen by one trace versus the other. The quoted dielectric constant of a laminate is the weighted average of the glass fiber content and resin content in the laminate. By nature of the fiberglass cloth, some areas will be resin-rich (lower dielectric constant) and others will be glass-rich (higher dielectric constant). Since dielectric constant affects propagation velocity, if one leg of a P/N pair ends up running primarily over resin-rich areas and the other over glass-rich areas, the result is skew in the received differential signal.

Fortunately, there are a few methods to combat fiber weave-induced-skew:

- Use a relatively flat cloth weave type, such as 2116, 3313, or better.
- Match differential-pair pitch to the glass-weave pitch, forcing P/N pairs to see equal variation.
- Rotate all layers by 10 to 15 degrees on a panel. Check with the FAB vendor as this depends on design size versus panel size.
- Route signals in a zig-zag fashion instead of straight along the X/Y axis. While this consumes more board space, it may be an appropriate trade-off to use a less-expensive material. This is illustrated in Figure 23.

Figure 23: BGA Component Breakout Example with Zig-Zag Routing Employed to Mitigate Fiber-Weave Skew



5.2.3.2 Lane-to-Lane Skew

Interlaken-LA lane-to-lane skew is highly robust. Per the Interlaken-LA specification, a receiver must be capable of handling lane-to-lane skew of 214 UI. The receiver and transmitter are budgeted 174 UI, which leaves PCB routing with 40 UI. Table 13 gives the mismatch of board traces in inches for each data rate supported by the KBP, given a PCB dielectric constant of 3.7 (similar to Megtron 6).

Table 13: Board Mismatch Budget vs. SerDes Data Rate

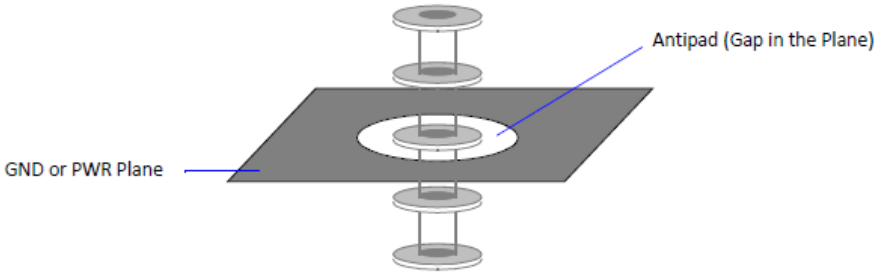
SerDes Data Rate (Gb/s)	Board Trace Mismatch Budget (inches)
10.3125	23.8
12.5	19.6
15.0	16.4
25.78125	9.5
28.125	8.7

5.2.4 Vias and PTH

Via design is extremely critical to the performance of the high-speed SerDes links. All signal via (pad and antipad) dimensions must be optimized for the appropriate RX and TX impedance through simulation. A 3D electromagnetic tool such as HFSS should be used for the simulation. The VSS stitching vias must be included in this simulation. Vias for different layer transitions require separate optimization (that is, vias for L1–L4 transition may be different than vias for L1–L18 transition).

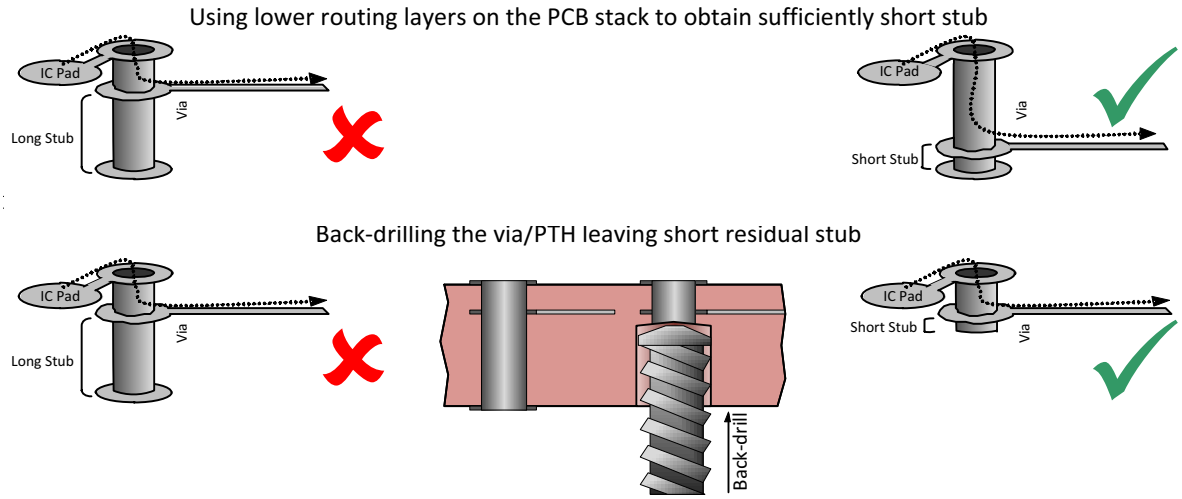
The package BGA pads, connector SMT pads, and AC-coupling capacitors (if applicable) must have a cutout in the VSS reference plane immediately under the component. Cutouts will also exist when transitioning PCB layers. The depth and dimension of the cutout should be determined by simulation to achieve optimal performance. Oblong oval or circular per via antipads are recommended. Table 24 illustrates an antipad during layer transitioning.

Figure 24: Antipad During Layer Transitioning



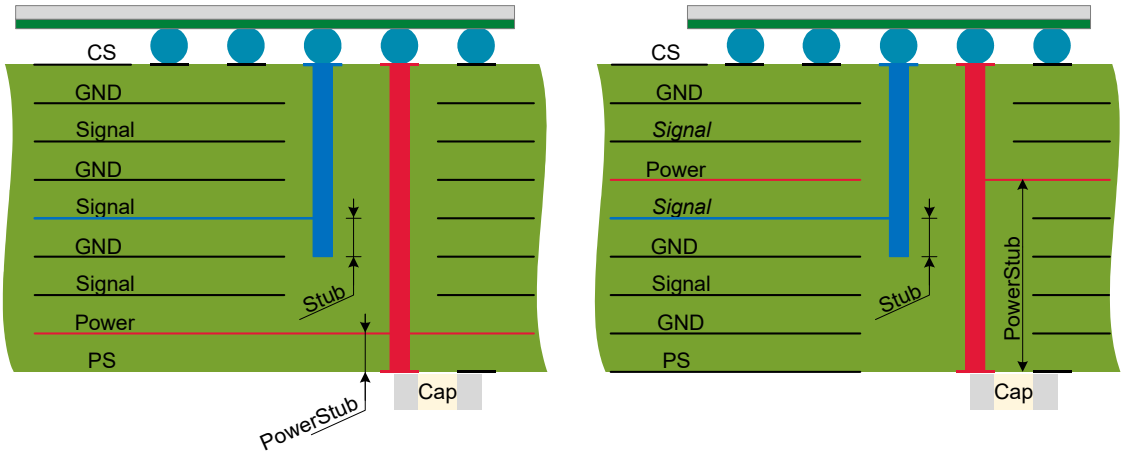
It is recommended to use via-in-pad. Blind or buried vias that have no via stubs are recommended. If via stubs do exist, they must be sufficiently short and must be removed by back-drilling. The remaining via stub must be < 6 mils in size. At such data rates, via stubs add extra impedance discontinuities and capacitance. Although sufficiently short via stubs may be obtained by routing on the lower board layers, this is not recommended for the high-speed SerDes signals that should be routed in the upper PCB layers and the resulting back-drilled stub. The bottom layers are to be avoided since the BGA via is hard to optimize due to the tight 1 mm pitch and the many surrounding vias that could degrade the signal. Figure 25 illustrates general techniques to reduce via stubs.

Figure 25: Via/PTH Stub Reduction Techniques



Ideally, when back drilling is used to remove stubs for signals, it would also be used on neighboring power and ground vias to eliminate reflections on the return path. This is not possible for vias that connect to a decoupling capacitor on the back side of the PCB. In this case, it is recommended that the SerDes power plane be located on a lower layer, closer to the capacitor. In this case, the stub will be minimized as shown in Figure 26.

Figure 26: Minimizing Power or Ground Stubs Connecting a Decoupling Capacitor



It is critical to minimize the number of vias (or layer transitions) in the signal path. The differential signal should be routed on one PCB layer. The number of vias within each leg of a differential pair must be the same. In addition, via placement across the differential pair must be symmetric. Stitching vias at layer transitions are recommended as shown in Figure 27. Pads should be removed on unused signal layers, as illustrated in Figure 28.

Figure 27: Ground Stitching Via Use

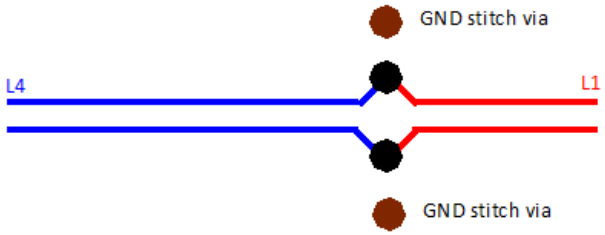


Figure 28: Removing Unused Pads to Improve Via/PTH Characteristics

5.2.5 BGA Breakout Pattern and Component Escape Routing

The TX differential pairs are located on the perimeter of the BGA, while the RX differential pairs are located inside the perimeter. Most designs require four signal layers to route the I-LA differential pairs in order to break out from the BGA via field. To reduce plane-gap discontinuities due to back-drill clearance requirements (and having to route traces over them), route signals further from the BGA via field edge on higher layers with the perimeter signals routed on the lower PCB layers. This assumes that the back-drill via opening is larger than the routing via opening and presents a larger obstacle to routing. Thus, RX signals are routed on higher PCB layers than the TX signals. With this methodology, via back-drill clearances will not affect the routing of any of the other signals.

With standard PCB manufacturing tolerances, maintaining differential routing through the BGA via field will probably not be possible. Using single-ended trace segments for component escape is acceptable and this section details the recommended escape strategy and routing techniques in the case where single-ended routing is used within the BGA via field.

There are four important things to check in component escape routing:

- Widen single-ended trace segments to meet 25Ω common-mode or 50Ω single-ended impedance.
- Length match single-ended segments between positive and negative legs of the differential pair as closely as reasonably possible to reduce mode conversion.
- Avoid routing over plane gaps whenever possible.
- Keep single-ended trace segments as short as possible to reduce impedance discontinuities.

The example in Figure 29 illustrates a poorly planned component escape routing strategy, which has inadvertently crossed gaps in the reference plane.

Figure 29: Inadvertent Routing of Traces Over a Plane Gap in the BGA Via Field

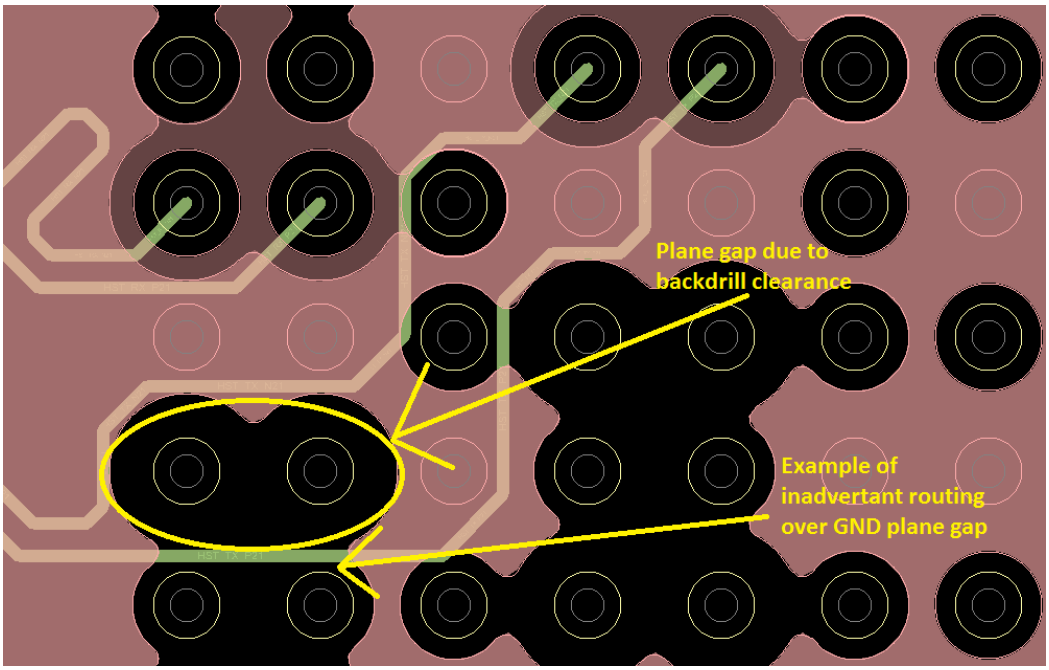


Figure 30 and Figure 31 show examples of recommended single-ended component escape routing. RX signals are routed on higher layers than TX signals to avoid back-drilled via gaps. Signal traces do not cross gaps in the reference planes, and single-ended segments are length matched before moving into differential routing.

Figure 30: Example RX Differential Pair BGA Breakout

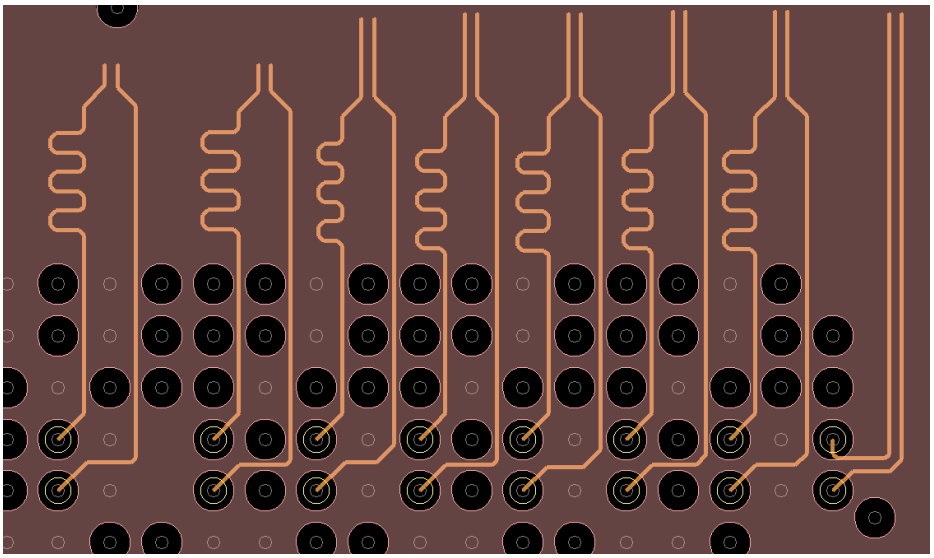
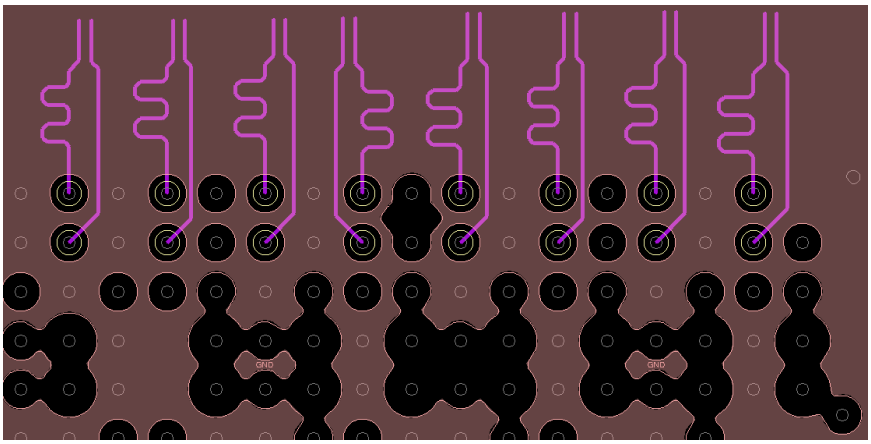


Figure 31: Example TX Differential Pair BGA Breakout



5.2.6 Channel Length and PCB Material Selection for High-Speed Signal Layers

The maximum possible channel length depends on the PCB material properties. In terms of electrical properties, the important factor is channel return loss. The high-speed links require a channel loss target of > –15 dB. The SerDes can handle higher return losses but will require different settings, which will increase the power of the link.

This section gives an example of board material selection based on a conductor width, roughness, and dielectric material to determine a general rule of thumb estimate of maximum channel length. The length is idealized and does not account for other sources of loss in the channel. It is expected that the customer will exercise due diligence for PCB material selection.

Given the channel lengths dictated by component placement, the next step can be to narrow down the list of potential PCB materials. The channel loss must be broken down into two components: dielectric and conductor attenuation. Dielectric loss is tabulated for several recommended PCB materials in Table 14.

Table 14: Dielectric Properties for Recommended High Speed PCB Materials

Dielectric Material	Dielectric Constant	Dissipation Factor	Atten. (dB/Inch/GHz)	Atten (dB/Inch) at 15 Gb/s	Atten (dB/Inch)at 25.78 Gb/s	Atten (dB/Inch) at 28.125 Gb/s
Nelco 4000 13SI	3.30	0.0080	0.03343	0.25069	0.43085	0.46996
Rogers 4003B	3.55	0.0027	0.01170	0.08775	0.15082	0.16451
Megtron 6 (R5775K Resin Based)	3.65	0.0020	0.00879	0.06591	0.11328	0.12356
Rogers 3003 (PTFE Based)	3.00	0.0013	0.00518	0.03884	0.06676	0.07281
Rogers 4350B	3.66	0.0037	0.01628	0.12210	0.20986	0.22891
Nelco 400013	3.70	0.0095	0.04203	0.31522	0.54176	0.59093
Taconic TSM-DS FastRise-27	2.70	0.0014	0.00529	0.03968	0.06820	0.07439

While often neglected, at high data rates, a significant component of total attenuation is copper loss. Due to skin effect, the surface roughness of the copper foil has a significant impact on overall signal attenuation. Surface roughness is averaged as an RMS value. Some common laminate surface roughness values are given in Table 15.

Table 15: Surface Roughness of Common Available Laminates

Profile	Surface Roughness
Standard	8 µm
Very Low Profile (VLP)	4 µm
Super/Hyper Very Low Profile (S/H-VLP)	2 µm

The factors affecting conductor loss are trace width, length, material conductivity, frequency (due to skin effect), and surface roughness. To reduce the skin effect, it is recommended to use a wider trace such as 7–8 mils. Other trace lengths are possible, but for the purpose of the example below, an 8 mil trace is assumed.

NOTE: The standard roughness imposes a large loss on the conductor. It is recommended to use a very low or super/hyper low profile laminate.

Copper loss and dielectric loss can be combined into an estimate of total attenuation per inch at the Nyquist frequency. Table 16 shows the attenuation per inch for various data rates, surface roughness, and recommended dielectric materials. Using better dielectrics, wider traces, and smooth copper can all reduce the attenuation of the signaling. It is advisable to compare each component's contribution to the attenuation and use resources appropriately to get the smallest attenuation for the cost. It is often much cheaper to use wider traces with smooth copper to reduce the total loss than it is to use very low loss dielectrics.

Table 16: Total Attenuation per Inch on an 8 mil Trace for Various Materials, Roughness and Data Rates

	Attenuation/Inch at 15 Gb/s		**Attenuation/Inch at 25.78 Gb/s**		**Attenuation/Inch at 28.125 Gb/s**	
Copper Roughness	2 µm	4 µm	2 µm	4 µm	2 µm	4 µm
Dielectric						
Nelco 4000 13SI	0.59302	0.81302	0.87964	1.20464	0.93867	1.28067
Rogers 4003B	0.43008	0.65008	0.59960	0.92460	0.63322	0.97522
Megtron 6 (R5775K Resin-Based)	0.40824	0.62824	0.56206	0.88706	0.59227	0.93427
Rogers 3003 (PTFE-Based)	0.38117	0.60117	0.51554	0.84054	0.54152	0.88352
Rogers 4350B	0.46443	0.68443	0.65864	0.98364	0.69761	1.03961
Nelco 400013	0.65755	0.87755	0.99054	1.31554	1.05964	1.40164
Taconic TSM-DS FastRise-27	0.38201	0.60201	0.51698	0.84198	0.54310	0.88510

Given total attenuation per inch, a maximum channel length can be found for each dielectric/copper combination to achieve a limit of –15 dB of total loss. Table 17 illustrates this for various data rates, surface roughness, and dielectric materials. Again this is a general rule of thumb. The customer is expected to do a detailed analysis to determine precise channel loss.

Table 17: Maximum Ideal Channel Length Limits for 8 mil Traces for Various Materials, Roughness and Data Rates

	Max. Channel Length with 15 dB Limit at 15 Gb/s		**Max. Channel Length with 15 dB Limit at 25.78 Gb/s**		**Max. Channel Length with 15 dB Limit @ 28.125 Gb/s**	
Copper Roughness	2 µm	4 µm	2 µm	4 µm	2 µm	4 µm
Dielectric						
Nelco 4000 13SI	25.3	18.4	17.1	12.5	16.0	11.7
Rogers 4003B	34.9	23.1	25.0	16.2	23.7	15.4
Megtron 6 (R5775K Resin-Based)	36.7	23.9	26.7	16.9	25.3	16.1
Rogers 3003 (PTFE-Based)	39.4	25.0	29.1	17.8	27.7	17.0
Rogers 4350B	32.3	21.9	22.8	15.2	21.5	14.4
Nelco 400013	22.8	17.1	15.1	11.4	14.2	10.7
Taconic TSM-DS FastRise-27	39.3	24.9	29.0	17.8	27.6	16.9

Even though micro-strip routing will be minimal to non-existent, care should be taken to the preferred PCB trace finish and plating process. Avoid using any finish or plating process that involves ferromagnetic materials such as nickel, which is standard for a gold plating process. Skin-effect-related losses are proportional to the square root of relative permeability of the material. For nickel, the relative permeability is 100 versus 1 for copper, so a nickel-gold plating process could exhibit 10 times the loss as a plain copper trace.

5.3 AC-Coupling Capacitors

For PCIe Rx pins, external AC-coupling capacitors are required. The recommended value is 100 nF. For the chip receiving the BCM16K PCIe Tx signals, it is required to have AC coupling (either built-in or on the board).

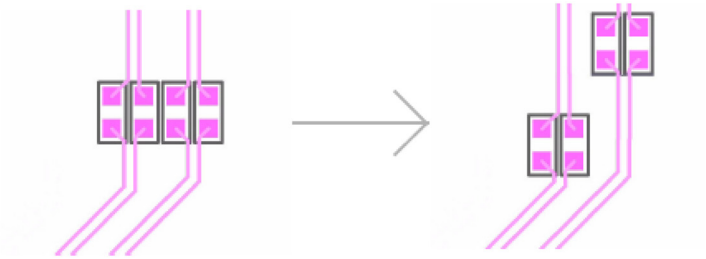
For PCIe reference clocks, DC or AC coupling is allowed. DC coupling is the default in this device.

When DC coupling, the common mode voltage range must be maintained as required by the BCM16K PCIe reference clock specifications. In this mode, the PCIe reference clock termination bias voltage is set by the common mode voltage.

When AC coupling, the recommended capacitor value is 100 nF. In this mode, the PCIe reference clock termination bias voltage must be enabled within the BCM52311 via software programming.

When placing series AC-coupling capacitors on the PCB, sufficient lane-to-lane spacing should be maintained. Their placement in relation to those for an adjacent lane should not be so close as to enable coupling between lanes. The exact spacing can be determined through simulation. It is recommended to stagger the AC-coupling capacitor placement as shown in Figure 32.

Figure 32: Series AC-Coupling Capacitor Staggered Placement



Due to the increased conductor width to connect to the AC-coupling capacitor, the impedance of this part of the trace will be significantly lower.

There are two methods to increase the impedance:

- Minimize the pad size of the component.
- Remove ground layers below pads until channel impedance is matched.
  Ensure the reference plane remains the same (ground-referenced).

5.4 Unused Lanes

Unused SerDes lanes should be left open and unconnected. Unused quads should be connected to an active supply and be powered down via software. The filtering and decoupling requirements for the unused quad supplies are relaxed so as to not require extra board components.

5.5 Simulation

IBIS/AMI models are provided for simulation and validation of the system performance. The full channel should be simulated, especially for data rates above 10 Gb/s or for long channels with a great deal of loss. The simulation will validate the eye at the receiver and whether the BER is acceptable.

In addition to the IBIS/AMI model, an S4P model of the package receiver and transmitter are provided as well as an S4P model of an example channel.

The recommended simulation tools are Agilent ADS and SiSoft QCD. CSP LinkEye is not available for this SerDes core.

Additional details can be found in the IBIS/AMI model package.

5.6 Receiver Eye Mask

The receiver eye mask shown in Figure 33 can be used to verify that the receiver is able to adequately recover the signal.

Figure 33: Receiver Eye Mask Diagram

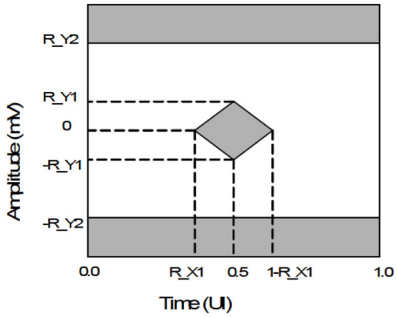


Table 18: Receiver Eye Mask Diagram Parameters

Parameter	Value
R_X1	0.35 UI
R_Y1	42.5 mV
R_Y2	800 mV

The SerDes also meets the eye mask compliance of the OIF CEI28G-SR specification. Refer to the appropriate data sheet for electrical requirements of the SerDes. It is not recommended to exceed 15 db of loss for the channel.

Chapter 6: Generation-2 PCIe Interface

6.1 Overview

The 16 nm KBP device has one Generation-2 PCIe lane consisting of one transmit and receive lane that runs at a 5 Gb/s data rate. Since the data rate is much lower than the Interlaken-LA interface, many stringent guidelines for the PCB may be relaxed. Also, the board material and processing will be optimized for higher speed, giving the relatively slow PCIe lane more margin.

6.2 High-Speed Routing Guidelines

This section provides guidance on successfully implementing a PCB channel with sufficient bandwidth to support a 5 Gb/s PCIe Generation-2 lane.

6.2.1 General Routing

- Use a 100Ω differential trace impedance for the RX and TX signals. The tolerance on this impedance is ±5%. For the breakout region under the BGA, use 25Ω for common-mode signaling.
- The PCIe lane can be routed either as a strip-line or as a micro-strip.
- Wider traces are preferred to reduce copper loss, but should be kept to <10 mils. Use a loosely coupled differential pair and avoid sharp bends in the trace routing.
- While a guard trace/ground patch is not required between the signal pair, if used it must be stitched to VSS. The distance between stitching vias should be <40 mils.
- All differential signals must be referenced to the VSS plane. All VSS islands along the differential pairs must be stitched with a maximum spacing of 40 mils. Splits or voids in the VSS plane area under/above the signal traces are not allowed. The edge of a split/void in the reference plane must be at least 3x signal trace width from the signal trace. Avoid overlapping power and ground islands/planes of different domains.

6.2.2 Crosstalk

- To minimize crosstalk, it is recommended to route the TX and RX lanes on separate layers.
- To reduce crosstalk, large inter-pair spacing is preferred. A minimum of 4x trace width spacing is recommended. In serpentine legs to match routing length the spacing must be 5x the trace width to minimize coupling.

6.2.3 Differential Pair Skew

Keep differential pair lengths as closely matched as possible to within 500 µm or 20 mils. When there is a mismatch, compensate for it near the location of the mismatch.

6.2.4 Vias and PTH

- All signal via (pad and antipad) dimensions must be optimized for the appropriate RX and TX impedance through simulation. Vias for different layer transitions require separate optimization (that is, vias for L1–L4 transition may be different than vias for L1–L18 transition).
- The package BGA pads, connector SMT pads, and AC-coupling capacitors must have a cutout in the VSS reference plane immediately under the component. Cutouts will also exist when transitioning PCB layers. The depth and dimension of the cutout should be determined by simulation to achieve optimal performance.

- It is recommended to use via-in-pad. Blind or buried vias, which have no via stubs are recommended. If via stubs do exist, they must be sufficiently short by using lower routing layers on the PCB stack or they must be removed by back-drilling. The remaining via stub must be <10 mils in size.
- It is critical to minimize the number of vias (or layer transitions) in the signal path. The differential signal should be routed on one PCB layer. The number of vias within each leg of a differential pair must be the same. In addition, via placement across the differential pair must be symmetric. Stitching vias at layer transitions are recommended. Pads should be removed on unused layers.

6.2.5 BGA Breakout Pattern and Component Escape Routing

Using single-ended trace segments for component escape is acceptable. There are four important things to check in component escape routing:

- Widen single-ended trace segments to meet 50Ω impedance.
- Length match single-ended segments between positive and negative legs of the differential pair as closely as reasonably possible.
- Avoid routing over plane gaps whenever possible.
- Keep single-ended trace segments as short as possible to reduce impedance discontinuities.

6.3 AC-Coupling Capacitors

For the PCIe RX pins, external AC-coupling capacitors are required. The recommended value is 100 nF. For the chip receiving the BCM16K PCIe TX signals, it is required to have AC coupling (either built-in or on the board).

For PCIe reference clocks, DC or AC coupling is allowed. DC-coupling is default in this device.

When DC coupling, the common mode voltage range must be maintained as required by the BCM16K PCIe reference clock specifications. In this mode, PCIe reference clock termination bias voltage is set by the common mode voltage.

When AC coupling, the recommended capacitor value is 100 nF. In this mode, the PCIe reference clock termination bias voltage must be enabled within the BCM16K via software programming.

6.4 Unused Lanes

If the PCIe is not to be used, the lanes should be left open and unconnected. The PCIe powers should be connected to an active supply and the link be powered down via software. The filtering and decoupling requirements for unused PCIe supplies are relaxed so as to not require extra components on the PCB. The PERST_L signal should also be grounded.

Chapter 7: Misc Layout Guidance

7.1 RESCAL Resistor Placement

The RESCAL[1:0] pins each need a 4.53 kΩ resistor with ≤1% accuracy connected to VSS. Analog circuits connected to the RESCAL[1:0] pins are sensitive to trace routing parasitics. It is recommended to use 0402 resistors and place them in the via array on the bottom side of the device. Adjacent to each RESCAL BGA is a corresponding VSS BGA making for easy placement of each resistor.

7.2 Open Drain Signals

The following signals are open drain and require an external pull-up resistor to drive to a logic 1 value:

- MDIO
- MDC
- SCL
- SDA
- GIO_L[1:0].

Each of these signals requires a 1 kΩ resistor connected to the VDD18 supply. The maximum voltage allowed on any 16 nm KBP low speed I/O is 1.98V. Voltages above this such as 2.5V or 3.3V will damage the device.

The drive strength of the I/O driving these signals is nominally 50Ω and varies from 45Ω to 55Ω.

7.3 DNC Signals

Some pins in the BGA pin list are designated DNC, which means “Do Not Connect”. These pins should remain floating.

7.4 Weak Drive Signals

Several pins have a weak internal drive on the pin. As an input, it is meant to provide a default logic level when not driven.

The following pins are weakly driven to a logic 1 (1.8V) value:

- TDI
- TMS
- TRST_L

MSEL[1:0] pins are weakly driven to a logic 0 value. The drive strength is rather weak at > 20 kΩ (over all conditions) so it is recommended to always drive these pins.

7.5 Static Configuration Signals

Several pins may only be used as a static configuration. In this case, it is recommended not to drive the signal directly with the power supply, but to connect through a 1 kΩ resistor to VDD18 or VSS. These signals include MPID[4:0], MSEL[1:0], CPSEL[4:0].

The drive strength of the I/O driving these signals is nominally 50Ω and varies from 45Ω to 55Ω.

7.6 Unused I^2C Interface

Since the I^2C interface is not currently used, it is recommended to connect both SCL and SDA to VDD18 through 1 kΩ resistors.

7.7 TDO

TDO is an output only driver pin. It is not recommended to attach any pull-up or pull-down resistors on this signal.

Revision History

52311-DG105; August 31, 2017

Updated:

- System Design

52311_KBP_16NM_DG-TI04; July 21, 2017

Updated:

- SerDes Reference Clocks
- AC-Coupling Capacitors

52311_KBP_16NM_DG-TI03-R; January 26, 2017

Updated:

- Table 1: “KBP Power Supply Inputs,” on page 8
- Table 7: “SerDes/Core PLL Supply Specifications,” on page 29
- “Power Planes and Stack-up Placement” on page 31
- Figure 16: “Consecutive Approach Power Sequence and Reset Timing,” on page 33
- Table 10: “PCREFCLK Requirements,” on page 35

52311_KBP_16NM_DG-TI02-R; December 14, 2016

Updated:

- Table 1: “KBP Power Supply Inputs,” on page 8
- “System Design” on page 11
- “Alternate Regulator Configuration” on page 17
- Table 7: “SerDes/Core PLL Supply Specifications,” on page 29
- “Power-On and Off Requirements” on page 32
- Table 9: “SREFCLK Requirements,” on page 34
- Table 10: “PCREFCLK Requirements,” on page 34
- Table 11: “CREFCLK Requirements,” on page 35
- “AC Coupling Capacitors” on page 54
- “Unused Lanes” on page 54
- “Static Configuration Signals” on page 56

Added:

- “Maximum Pressure Specifications” on page 37
- “TDO” on page 56

52311_KBP_16NM_DG-TI01-R; March 30, 2016

Updated:

- Table 1: “KBP Power Supply Inputs,” on page 13
- Figure 5: “AVS System Configuration,” on page 18
- Figure 6: “Alternate AVS Configuration,” on page 23
- Figure 8: “Configuration to Test Switching Regulator,” on page 24
- “System Design” on page 16
- Step 3 on page 25
- Step 5 on page 25
- Step 6 on page 25
- Step 10 on page 25
- “Open Drain Signals” on page 59
- “Weak Drive Signals” on page 59
- “Static Configuration Signals” on page 60

52311_KBP_16NM_DG-TI00-R; October 20, 2015

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