1,048,576 WORD ×4 BIT DYNAMIC RAM

**PRELIMINARY**

## DESCRIPTION

The TC514400APL/AJL/ASJL/AZL is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400APL/AJL/ASJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400APL/AJL/ASJL/AZL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ (300/350mil) and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

| | | TC514400APL/AJL/ASJL/AZL -70/-80/-10 | | |
|---|---|---|---|---|
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 70ns | 80ns | 100ns |
| $t_{AA}$ | Column Address Access Time | 35ns | 40ns | 50ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 20ns | 20ns | 25ns |
| $t_{RC}$ | Cycle Time | 130ns | 150ns | 180ns |
| $t_{PC}$ | Fast Page Mode Cycle Time | 45ns | 50ns | 60ns |

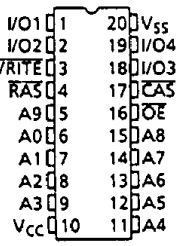
- Single power supply of 5V±10% with a built-in $V_{BB}$ generator
- Low Power
  - 550mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-70)
  - 468mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-80)
  - 413mW MAX. Operating (TC514400APL/AJL/ASJL/AZL-10)
  - 1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514400APL : DIP20-P-300C
  TC514400AJL : SOJ26-P-350
  TC514400ASJL: SOJ26-P-300A
  TC514400AZL : ZIP20-P-400A

## PIN NAMES

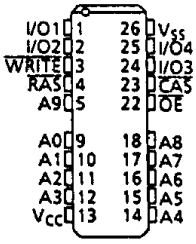
| | | | |
|---|---|---|---|
| A0~A9 | Address Inputs | $\overline{OE}$ | Output Enable |
| $\overline{RAS}$ | Row Address Strobe | I/O1~I/O4 | Data Input/Output |
| $\overline{CAS}$ | Column Address Strobe | $V_{CC}$ | Power (+5V) |
| $\overline{WRITE}$ | Read/Write Input | $V_{SS}$ | Ground |

## PIN CONNECTION (TOP VIEW)

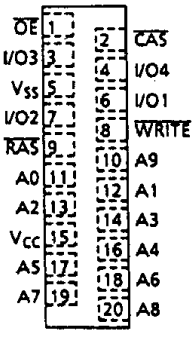
Plastic DIP



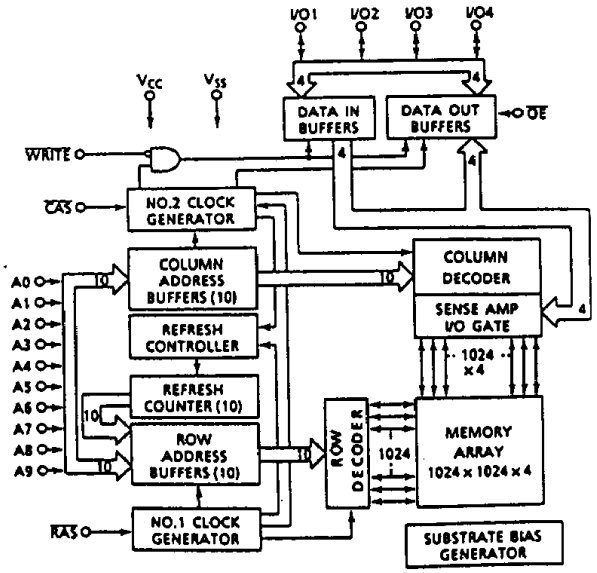

Plastic SOJ




Plastic ZIP




## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | -1~7 | V | 1 |
| Output Voltage | $V_{OUT}$ | -1~7 | V | 1 |
| Power Supply Voltage | $V_{CC}$ | -1~7 | V | 1 |
| Operating Temperature | $T_{OPR}$ | 0~70 | °C | 1 |
| Storage Temperature | $T_{STG}$ | -55~150 | °C | 1 |
| Soldering Temperature·Time | $T_{SOLDER}$ | 260·10 | °C·sec | 1 |
| Power Dissipation | $P_D$ | 700 | mW | 1 |
| Short Circuit Output Current | $I_{OUT}$ | 50 | mA | 1 |

## RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| $V_{IH}$ | Input High Voltage | 2.4 | - | 6.5 | V | 2 |
| $V_{IL}$ | Input Low Voltage | -1.0 | - | 0.8 | V | 2 |

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V ± 10%, Ta = 0~70°c)

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | OPERATING CURRENT<br>Average Power Supply Operating Current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}$ = $t_{RC}$ MIN.) | TC514400APL/AJL/ASJL/AZL-70 | – | 100 | mA | 3, 4 |
| | | TC514400APL/AJL/ASJL/AZL-80 | – | 85 | | 5 |
| | | TC514400APL/AJL/ASJL/AZL-10 | – | 75 | | |
| $I_{CC2}$ | STANDBY CURRENT<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | | – | 2 | mA | |
| $I_{CC3}$ | $\overline{RAS}$ ONLY REFRESH CURRENT<br>Average Power Supply Current, $\overline{RAS}$ Only Mode<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$: $t_{RC}$ = $t_{RC}$ MIN.) | TC514400APL/AJL/ASJL/AZL-70 | – | 100 | mA | 3, 5 |
| | | TC514400APL/AJL/ASJL/AZL-80 | – | 85 | | |
| | | TC514400APL/AJL/ASJL/AZL-10 | – | 75 | | |
| $I_{CC4}$ | FAST PAGE MODE CURRENT<br>Average Power Supply Current, Fast Page Mode<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC}$ = $t_{PC}$ MIN.) | TC514400APL/AJL/ASJL/AZL-70 | – | 70 | mA | 3, 4 |
| | | TC514400APL/AJL/ASJL/AZL-80 | – | 60 | | 5 |
| | | TC514400APL/AJL/ASJL/AZL-10 | – | 55 | | |
| $I_{CC5}$ | STANDBY CURRENT<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ – 0.2V) | | – | 200 | µA | |
| $I_{CC6}$ | $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT<br>Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$<br>Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}$ = $t_{RC}$ MIN.) | TC514400APL/AJL/ASJL/AZL-70 | – | 100 | mA | 3, 5 |
| | | TC514400APL/AJL/ASJL/AZL-80 | – | 85 | | |
| | | TC514400APL/AJL/ASJL/AZL-10 | – | 75 | | |
| $I_{CC7}$ | Battery Back Up Current<br>Average Power Supply Current, Battery Back Up Mode<br>($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = $V_{CC}$ – 0.2V, $\overline{WRITE}$ = $V_{CC}$ – 0.2V, A0~9 = $V_{CC}$ – 0.2V or 0.2V, I/O1~4 = $V_{CC}$ – 0.2V, 0.2V or OPEN : $t_{RC}$ = 125µs, $t_{RAS}$ = 300ns ~1µs) | | – | 400 | µA | 3, 6 |
| $I_{CC7}$ | Battery Back Up Current<br>Average Power Supply Current, Battery Back Up Mode<br>($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = $V_{CC}$ – 0.2V, $\overline{WRITE}$ = $V_{CC}$ – 0.2V, A0~9 = $V_{CC}$ – 0.2V or 0.2V, I/O1~4 = $V_{CC}$ – 0.2V, 0.2V or OPEN : $t_{RC}$ = 125µs, $t_{RAS}$ = $t_{RAS}$ MIN. ~300ns) | | – | 300 | µA | 3, 6 |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any input<br>(0V ≤ $V_{IN}$ ≤ 6.5V, All Other Pins Not Under Test = 0V) | | – 10 | 10 | µA | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT<br>($D_{OUT}$ is disabled, 0V ≤ $V_{OUT}$ ≤ 5.5V) | | – 10 | 10 | µA | |
| $V_{OH}$ | OUTPUT LEVEL<br>Output "H" Level Voltage ($I_{OUT}$ = – 5mA) | | 2.4 | – | V | |
| $V_{OL}$ | OUTPUT LEVEL<br>Output "L" Level Voltage ($I_{OUT}$ = 4.2mA) | | – | 0.4 | V | |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC}$ = 5V ± 10%, Ta = 0~70°c) (Notes 7, 8, 9)

| SYMBOL | PARAMETER | TC514400APL/AJL/ASJL/AZL-70 | | TC514400APL/AJL/ASJL/AZL-80 | | TC514400APL/AJL/ASJL/AZL-10 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| $t_{RC}$ | Random Read or Write Cycle Time | 130 | – | 150 | – | 180 | – | ns | |
| $t_{RMW}$ | Read-Modify-Write Cycle Time | 185 | – | 205 | – | 245 | – | ns | |
| $t_{PC}$ | Fast Page Mode Cycle Time | 45 | – | 50 | – | 60 | – | ns | |
| $t_{PRMW}$ | Fast Page Mode Read-Modify-Write Cycle Time | 100 | – | 105 | – | 125 | – | ns | |
| $t_{RAC}$ | Access Time from $\overline{RAS}$ | – | 70 | – | 80 | – | 100 | ns | 10,15 16 |
| $t_{CAC}$ | Access Time from $\overline{CAS}$ | – | 20 | – | 20 | – | 25 | ns | 10,15 |
| $t_{AA}$ | Access Time from Column Address | – | 35 | – | 40 | – | 50 | ns | 10,16 |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge | – | 40 | – | 45 | – | 55 | ns | 10 |
| $t_{CLZ}$ | $\overline{CAS}$ to output in Low-Z | 0 | – | 0 | – | 0 | – | ns | 10 |
| $t_{OFF}$ | Output Buffer Turn-off Delay | 0 | 20 | 0 | 20 | 0 | 20 | ns | 11 |
| $t_T$ | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns | 9 |
| $t_{RP}$ | $\overline{RAS}$ Precharge Time | 50 | – | 60 | – | 70 | – | ns | |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 70 | 10,000 | 80 | 10,000 | 100 | 10,000 | ns | |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode) | 70 | 200,000 | 80 | 200,000 | 100 | 200,000 | ns | |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 20 | – | 20 | – | 25 | – | ns | |
| $t_{RHCP}$ | $\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode) | 40 | – | 45 | – | 55 | – | ns | |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time | 70 | – | 80 | – | 100 | – | ns | |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 20 | 10,000 | 20 | 10,000 | 25 | 10,000 | ns | |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | 20 | 50 | 20 | 60 | 25 | 75 | ns | 15 |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 15 | 35 | 15 | 40 | 20 | 50 | ns | 16 |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | – | 5 | – | 5 | – | ns | |
| $t_{CP}$ | $\overline{CAS}$ Precharge Time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{ASR}$ | Row Address Set-Up Time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{RAH}$ | Row Address Hold Time | 10 | – | 10 | – | 15 | – | ns | |
| $t_{ASC}$ | Column Address Set-Up Time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{CAH}$ | Column Address Hold Time | 15 | – | 15 | – | 20 | – | ns | |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time | 35 | – | 40 | – | 50 | – | ns | |
| $t_{RCS}$ | Read Command Set-Up Time | 0 | – | 0 | – | 0 | – | ns | |
| $t_{RCH}$ | Read Command Hold Time | 0 | – | 0 | – | 0 | – | ns | 12 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

| SYMBOL | PARAMETER | TC514400APL/AJL/ASJL/AZL-70 | | TC514400APL/AJL/ASJL/AZL-80 | | TC514400APL/AJL/ASJL/AZL-10 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| $t_{RRH}$ | Read Command Hold Time referenced to $\overline{RAS}$ | 0 | - | 0 | - | 0 | - | ns | 12 |
| $t_{WCH}$ | Write Command Hold Time | 15 | - | 15 | - | 20 | - | ns | |
| $t_{WP}$ | Write Command Pulse Width | 15 | - | 15 | - | 20 | - | ns | |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 20 | - | 20 | - | 25 | - | ns | |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 20 | - | 20 | - | 25 | - | ns | |
| $t_{DS}$ | Data Set-Up Time | 0 | - | 0 | - | 0 | - | ns | 13 |
| $t_{DH}$ | Data Hold Time | 15 | - | 15 | - | 20 | - | ns | 13 |
| $t_{REF}$ | Refresh Period | - | 128 | - | 128 | - | 128 | ms | |
| $t_{WCS}$ | Write Command Set-UP Time | 0 | - | 0 | - | 0 | - | ns | 14 |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WRITE}$ Delay Time | 50 | - | 50 | - | 60 | - | ns | 14 |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WRITE}$ Delay Time | 100 | - | 110 | - | 135 | - | ns | 14 |
| $t_{AWD}$ | Column Address to $\overline{WRITE}$ Delay Time | 65 | - | 70 | - | 85 | - | ns | 14 |
| $t_{CPWD}$ | $\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time | 70 | - | 75 | - | 90 | - | ns | 14 |
| $t_{CSR}$ | $\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 5 | - | 5 | - | 5 | - | ns | |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 15 | - | 15 | - | 20 | - | ns | |
| $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 0 | - | 0 | - | 0 | - | ns | |
| $t_{CPT}$ | $\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle) | 40 | - | 40 | - | 50 | - | ns | |
| $t_{ROH}$ | $\overline{RAS}$ Hold Time referenced to $\overline{OE}$ | 10 | - | 10 | - | 20 | - | ns | |
| $t_{OEA}$ | $\overline{OE}$ Access Time | - | 20 | - | 20 | - | 25 | ns | |
| $t_{OED}$ | $\overline{OE}$ to Data Delay | 20 | - | 20 | - | 25 | - | ns | |
| $t_{OEZ}$ | Output buffer turn off Delay Time from $\overline{OE}$ | 0 | 20 | 0 | 20 | 0 | 20 | ns | 10 |
| $t_{OEH}$ | $\overline{OE}$ Command Hold Time | 20 | - | 20 | - | 25 | - | ns | |
| $t_{WTS}$ | Write Commamd Set-Up Time (Test Mode In) | 10 | - | 10 | - | 10 | - | ns | |
| $t_{WTH}$ | Write Commamd Hold Time (Test Mode In) | 10 | - | 10 | - | 10 | - | ns | |
| $t_{WRP}$ | $\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| $t_{WRH}$ | $\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 10 | - | 10 | - | 10 | - | ns | |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

| SYMBOL | PARAMETER | TC514400APL/AJL/ASJL/AZL-70 | | TC514400APL/AJL/ASJL/AZL-80 | | TC514400APL/AJL/ASJL/AZL-10 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| $t_{RC}$ | Random Read or Write Cycle Time | 135 | – | 155 | – | 185 | – | ns | |
| $t_{RMW}$ | Read-Modify-Write Cycle Time | 190 | – | 210 | – | 250 | – | ns | |
| $t_{PC}$ | Fast Page Mode Cycle Time | 50 | – | 55 | – | 65 | – | ns | |
| $t_{RMR}$ | Fast Page Mode Read-Modify-Write Cycle Time | 190 | – | 210 | – | 250 | – | ns | |
| $t_{RAC}$ | Access Time from $\overline{RAS}$ | – | 75 | – | 85 | – | 105 | ns | 10,15 16 |
| $t_{CAC}$ | Access Time from $\overline{CAS}$ | – | 25 | – | 25 | – | 30 | ns | 9,15 |
| $t_{AA}$ | Access Time from Column Address | – | 40 | – | 45 | – | 55 | ns | 9,16 |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge | – | 40 | – | 50 | – | 60 | ns | 10 |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 75 | 10,000 | 85 | 10,000 | 105 | 10,000 | ns | |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode) | 75 | 100,000 | 85 | 200,000 | 105 | 200,000 | ns | |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 25 | – | 25 | – | 30 | – | ns | |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time | 75 | – | 85 | – | 105 | – | ns | |
| $t_{RHCP}$ | $\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time | 45 | – | 55 | – | 65 | – | ns | |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 25 | 10,000 | 25 | 10,000 | 30 | 10,000 | ns | |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time | 40 | – | 45 | – | 55 | – | ns | |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WRITE}$ Delay Time | 55 | – | 55 | – | 65 | – | ns | 14 |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WRITE}$ Delay Time | 105 | – | 115 | – | 140 | – | ns | 14 |
| $t_{AWD}$ | Column Address to $\overline{WRITE}$ Delay Time | 70 | – | 75 | – | 90 | – | ns | 14 |
| $t_{CPWD}$ | $\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time | 75 | – | 80 | – | 95 | – | ns | 14 |
| $t_{OEA}$ | $\overline{OE}$ Access Time from | – | 25 | – | 25 | – | 30 | ns | |
| $t_{OEH}$ | $\overline{OE}$ Command Hold Time | 25 | – | 25 | – | 30 | – | ns | |

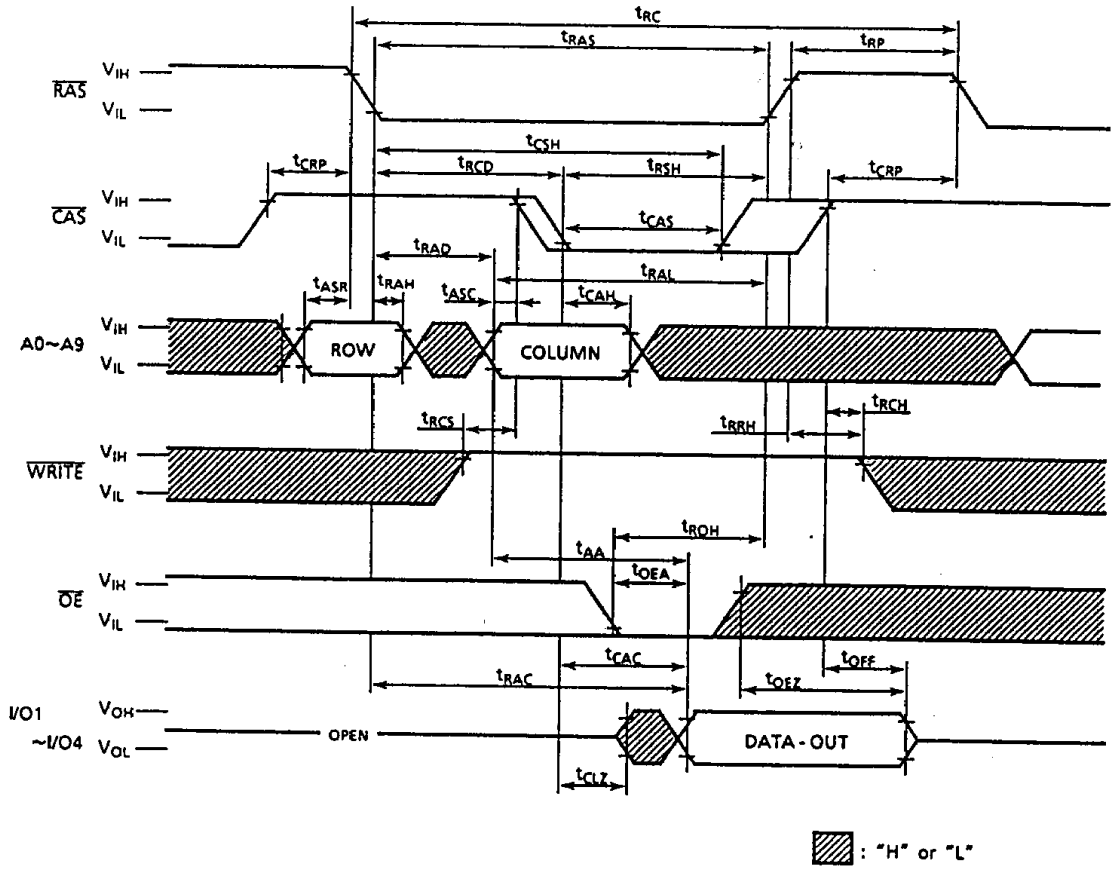
## CAPACITANCE ($V_{CC}$ = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $C_{I1}$ | Input Capacitance (A0~A9) | – | 5 | pF |
| $C_{I2}$ | Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$) | – | 7 | pF |
| $C_O$ | Input/Output Capacitance (I/O1~I/O4) | – | 7 | pF |

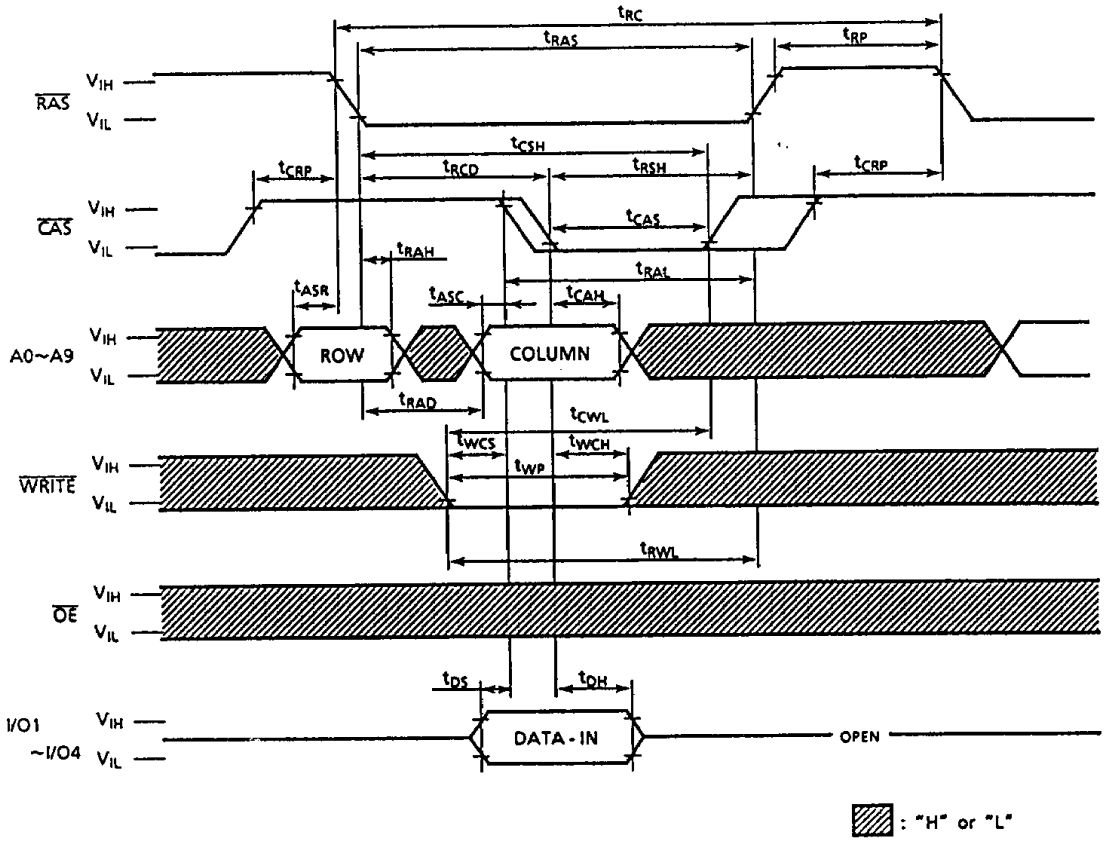
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to $V_{SS}$.
3. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC6}$, $I_{CC7}$ depend on cycle rate.
4. $I_{CC1}$, $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. $t_{RAS}$(max.)=1μs is only applied to refresh of battery-back up. $t_{RAS}$(max.)=10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume $t_T$=5ns.
9. $V_{IH}$ (min.) and $V_{IL}$ (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. $t_{OFF}$ (max.) and $t_{OEZ}$ (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the $t_{RCD}$ (max.) limit insures that $t_{RAC}$ (max.) can be met. $t_{RCD}$ (max.) is specified as a reference point only: If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max.) limit, then access time is controlled by $t_{CAC}$.
16. Operation within the $t_{RAD}$ (max.) limit insures that $t_{RAC}$ (max.) can be met. $t_{RAD}$ (max.) is specified as a reference point only: If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max.) limit, then access time is controlled by $t_{AA}$.

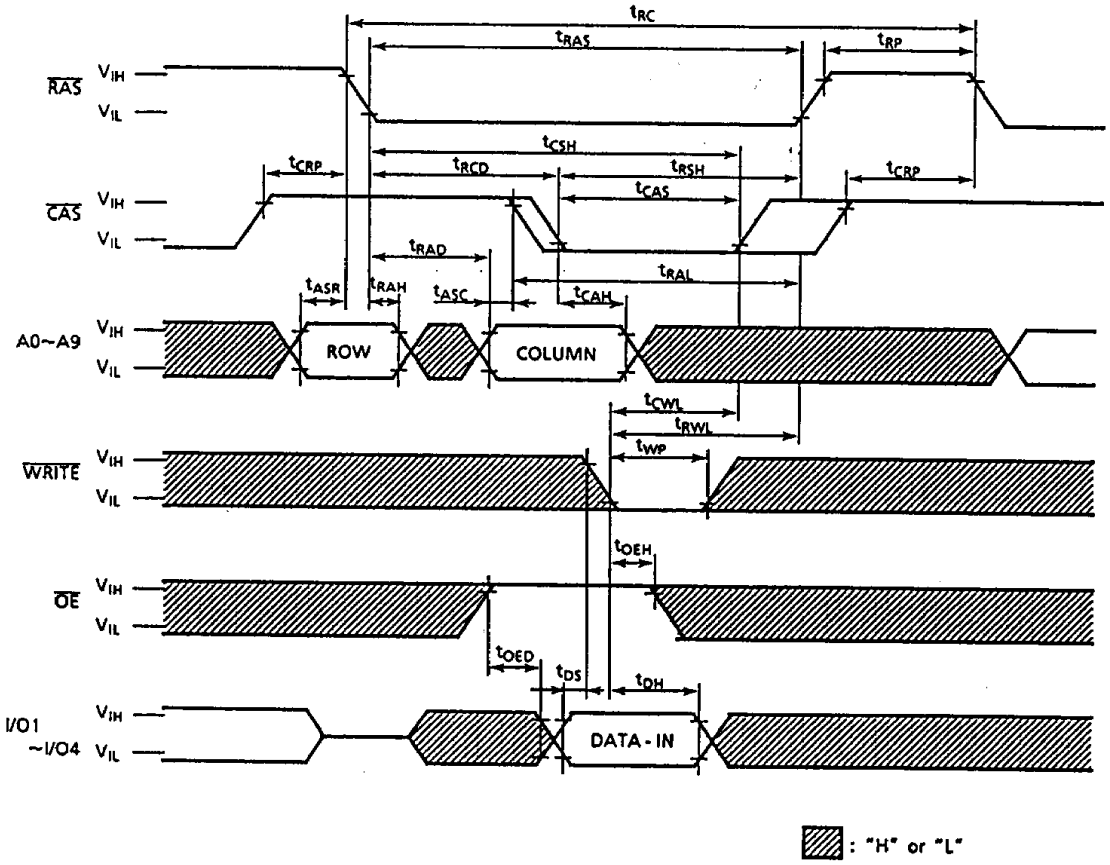
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1
~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

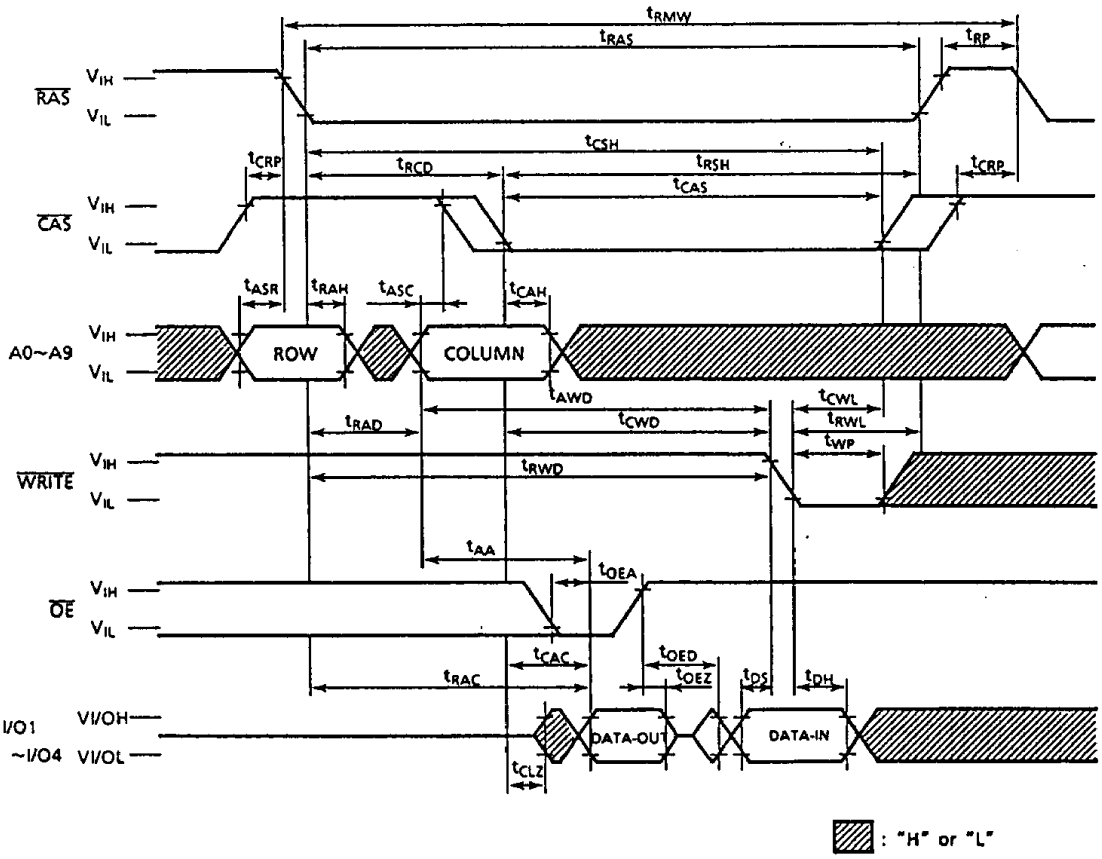
WRITE CYCLE (EARLY WRITE)



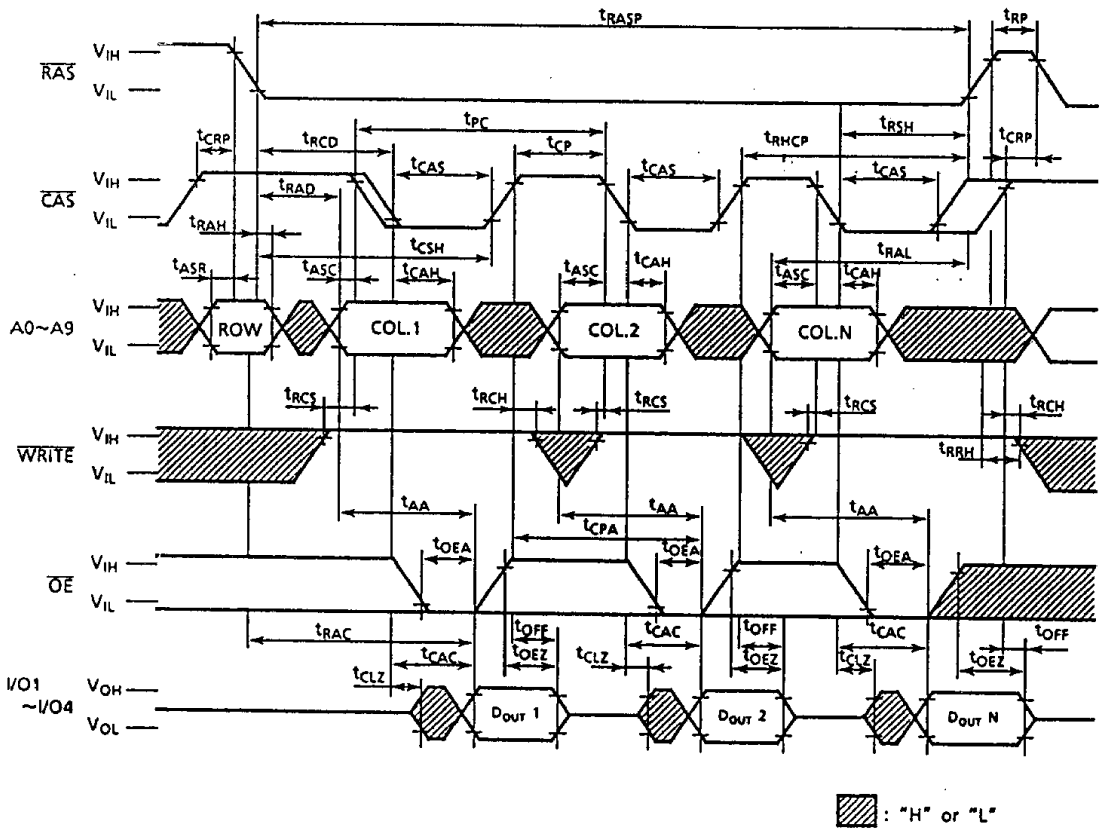
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



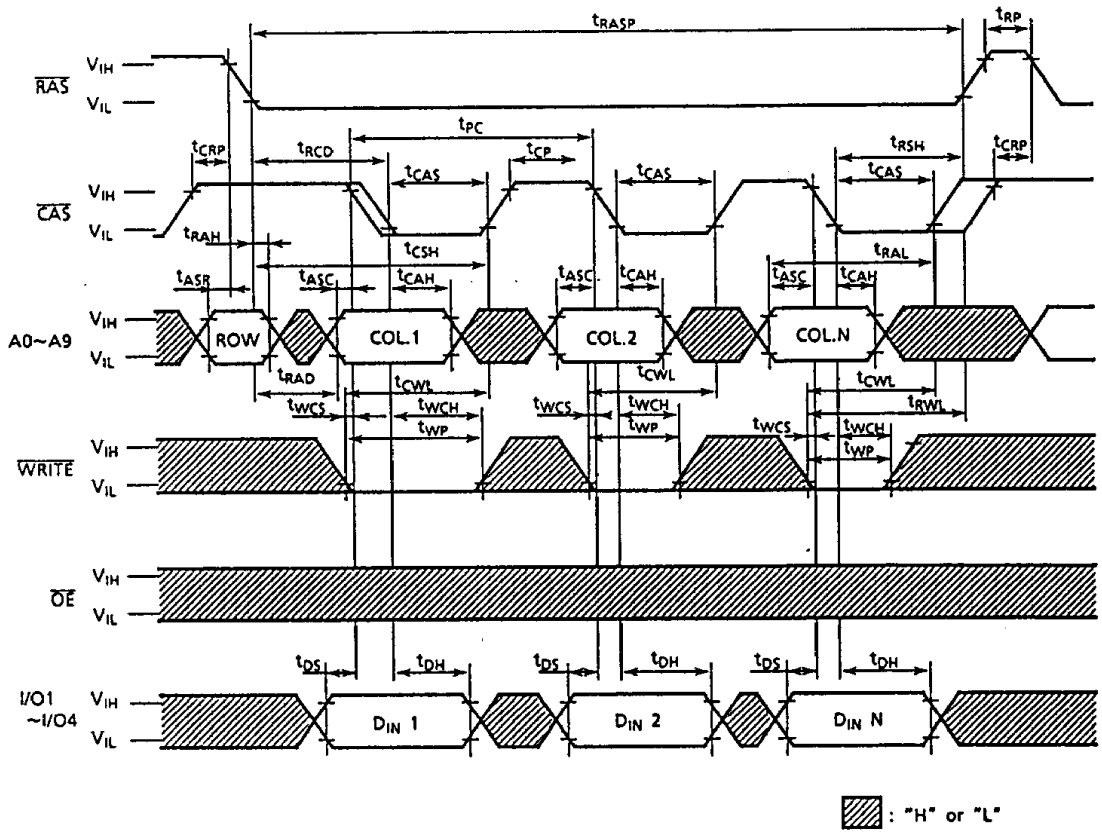
READ-MODIFY-WRITE CYCLE



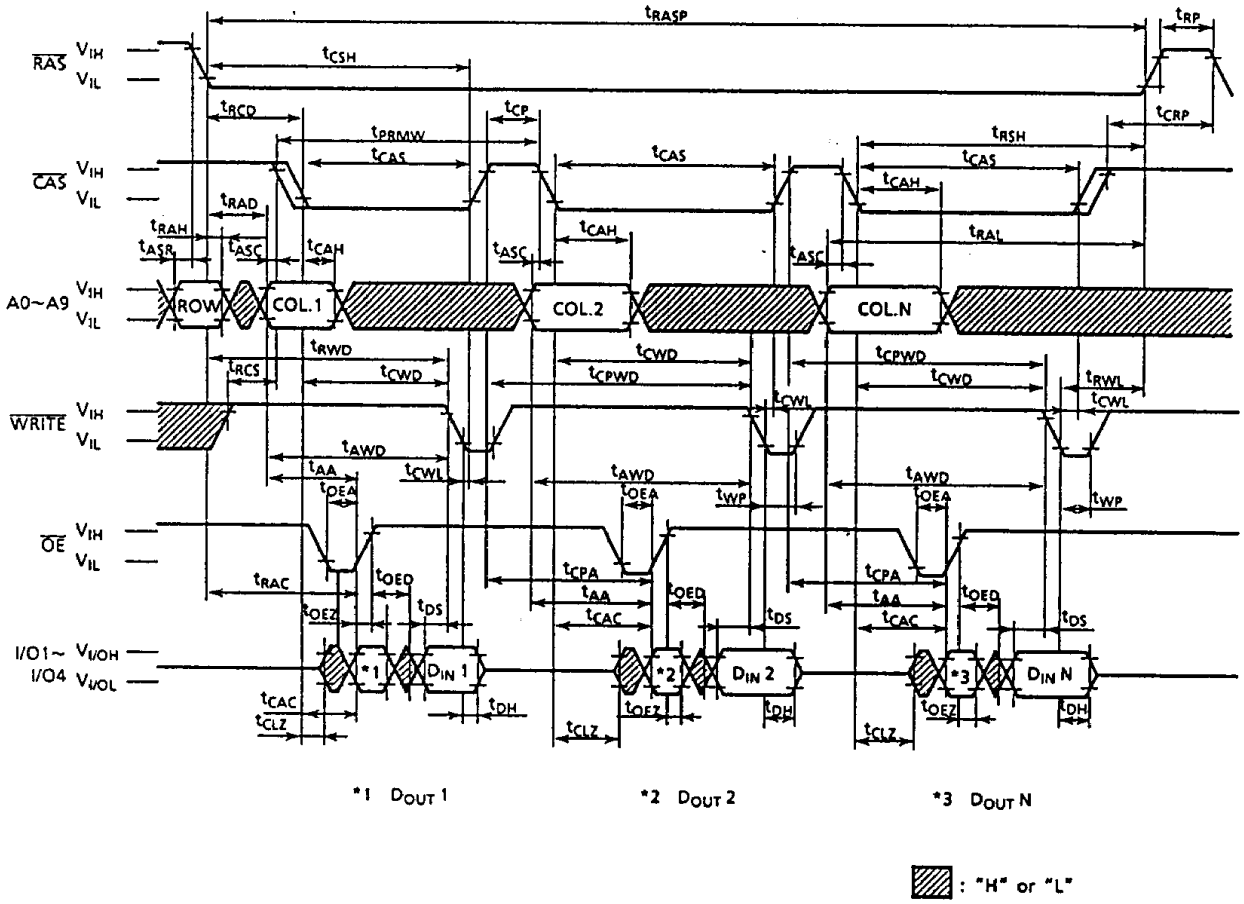
FAST PAGE MODE READ CYCLE



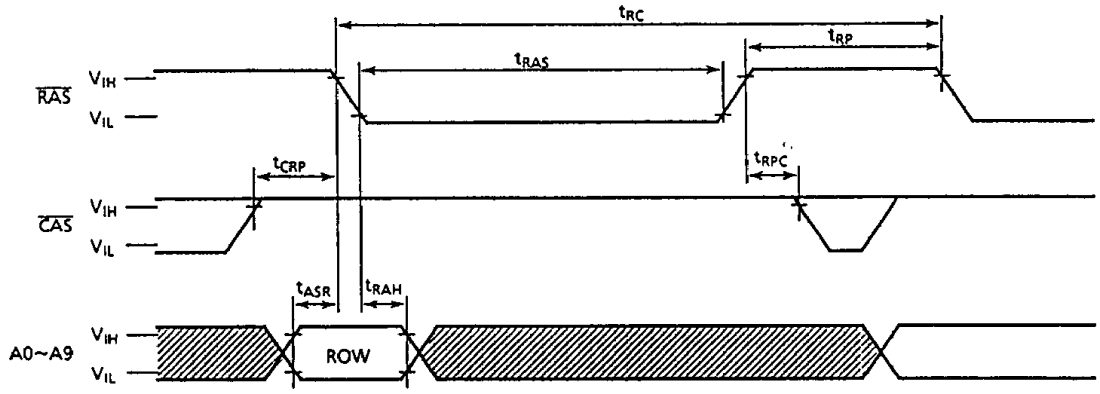
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



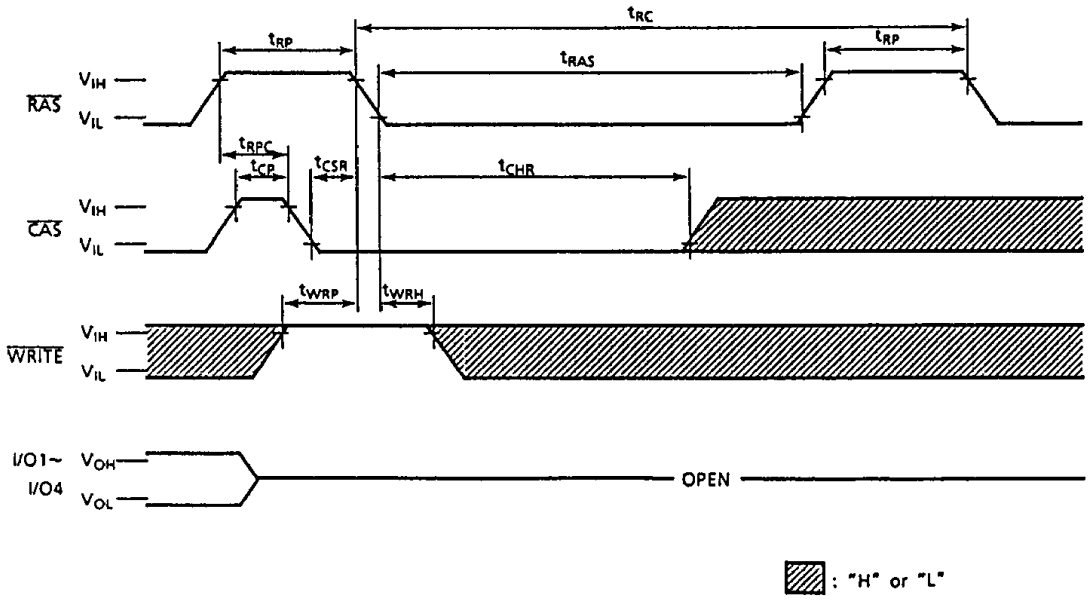
## $\overline{RAS}$ ONLY REFRESH CYCLE




Noto: $\overline{WRITE}$, $\overline{OE}$="H" or "L"

: "H" or "L"

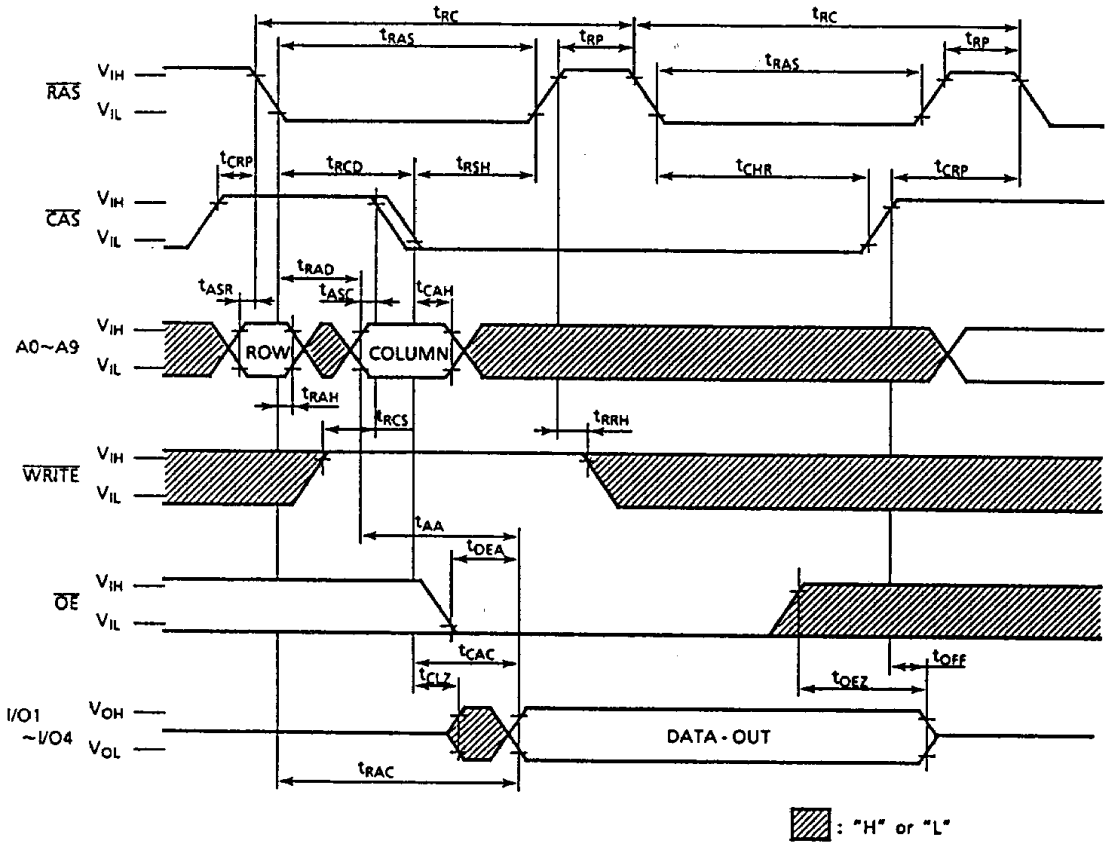
## $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



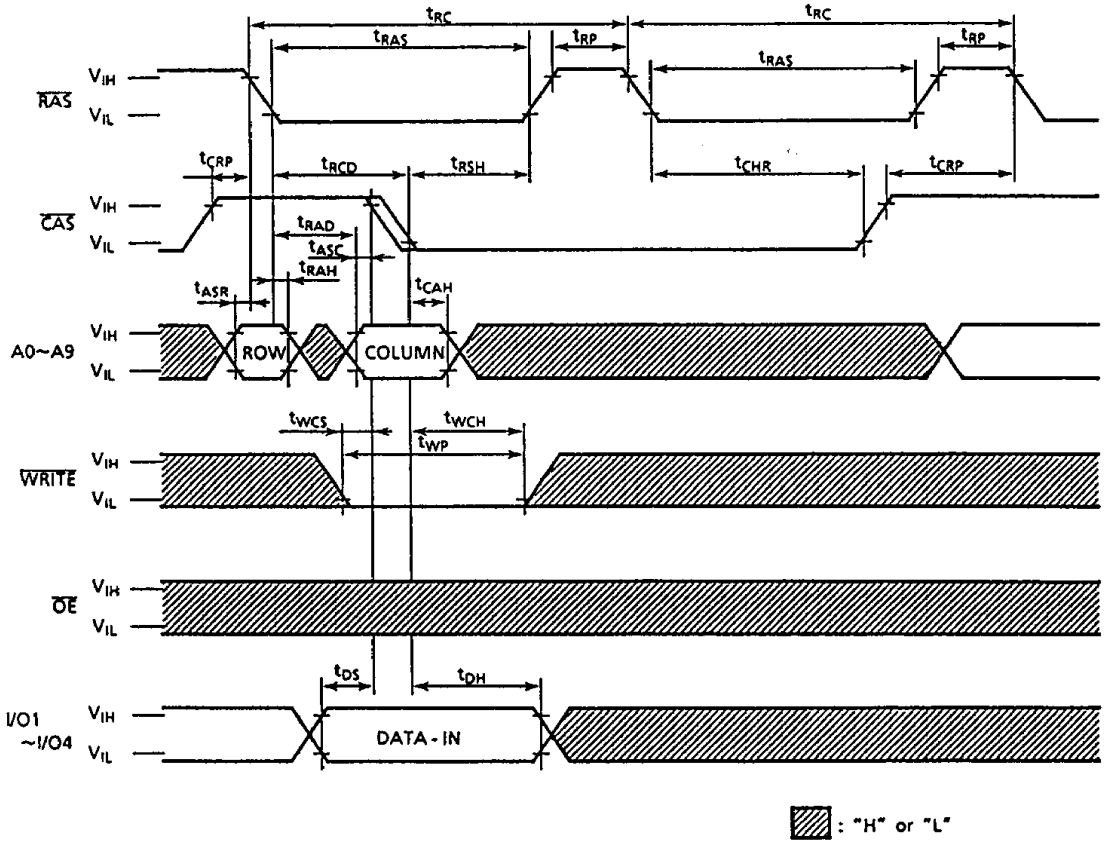

: "H" or "L"

Note: $\overline{OE}$, A0~A9="H" or "L"

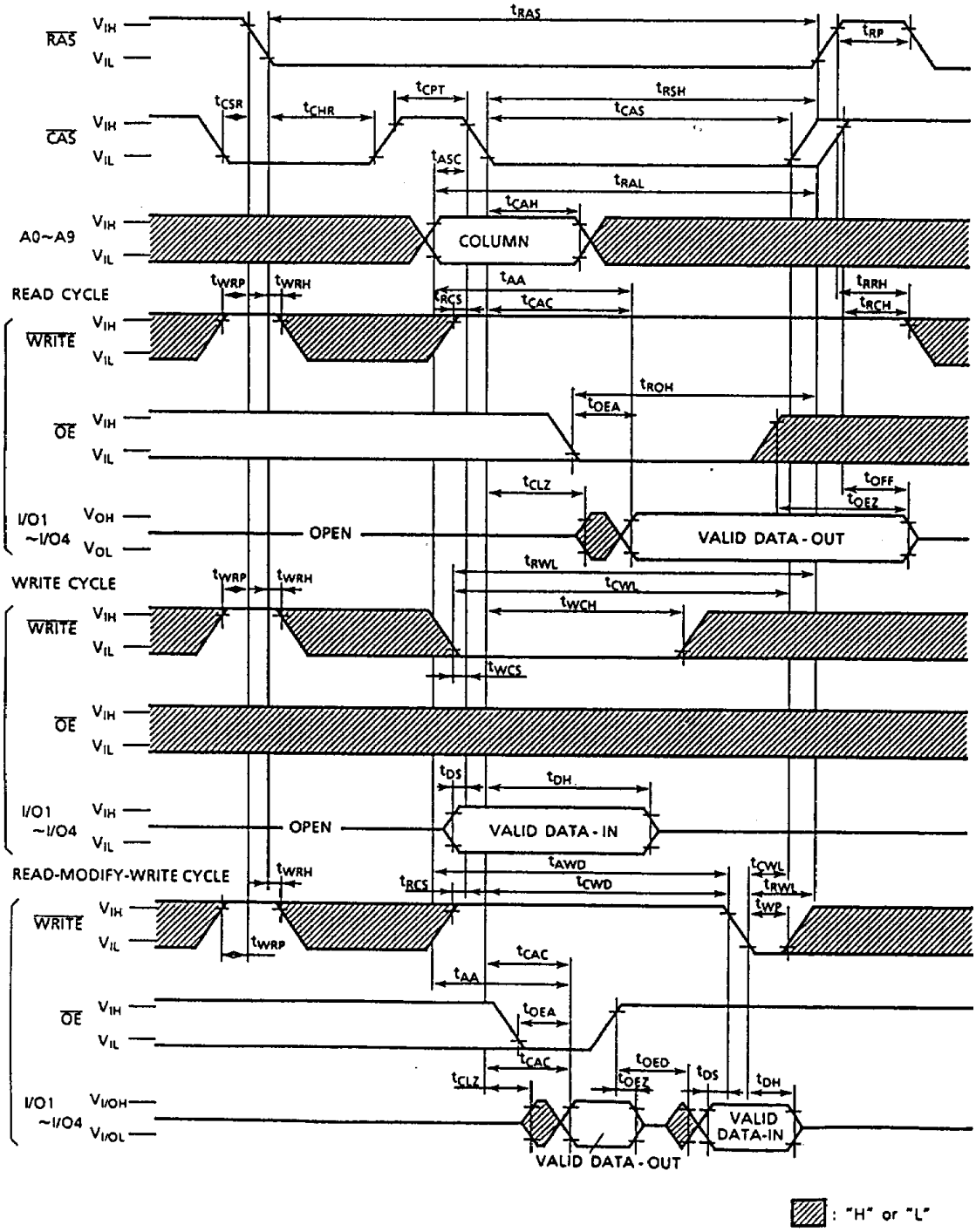
HIDDEN REFRESH CYCLE (READ)



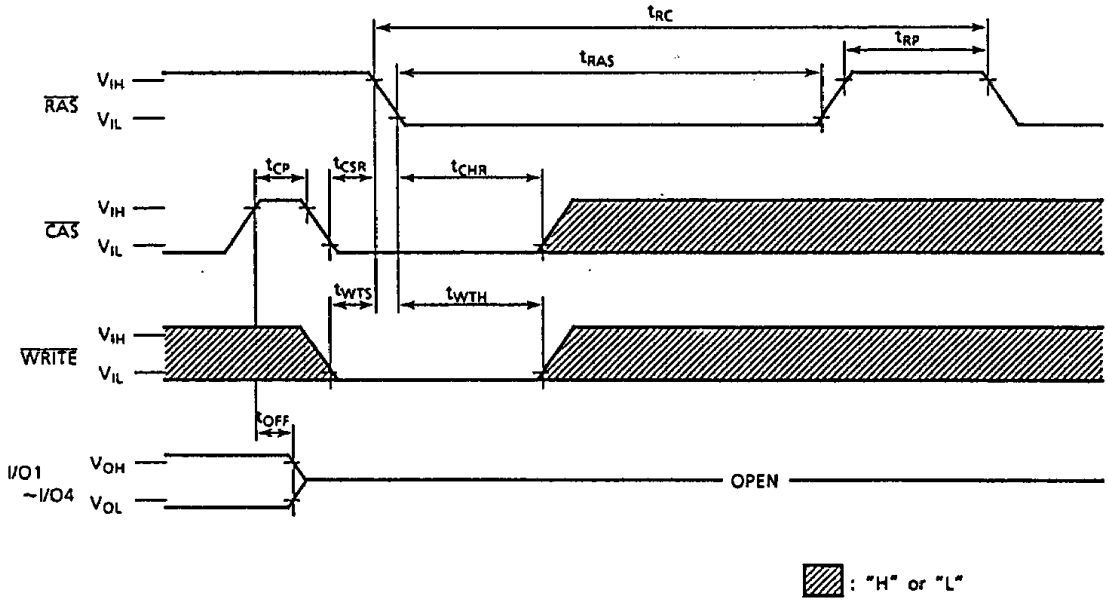
HIDDEN REEFRESH CYCLE (WRITE)



## $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



WRITE, CAS BEFORE RAS REFRESH CYCLE




Note: $\overline{OE}$, A0~A9: "H" or "L"

## TEST MODE

The TC514400APL/AJL/ASJL/AZL is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Aoc is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig.1 shows the block diagram of TC514400APL/AJL/ASJL/AZL. In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

## BLOCK DIAGRAM IN THE TEST MODE

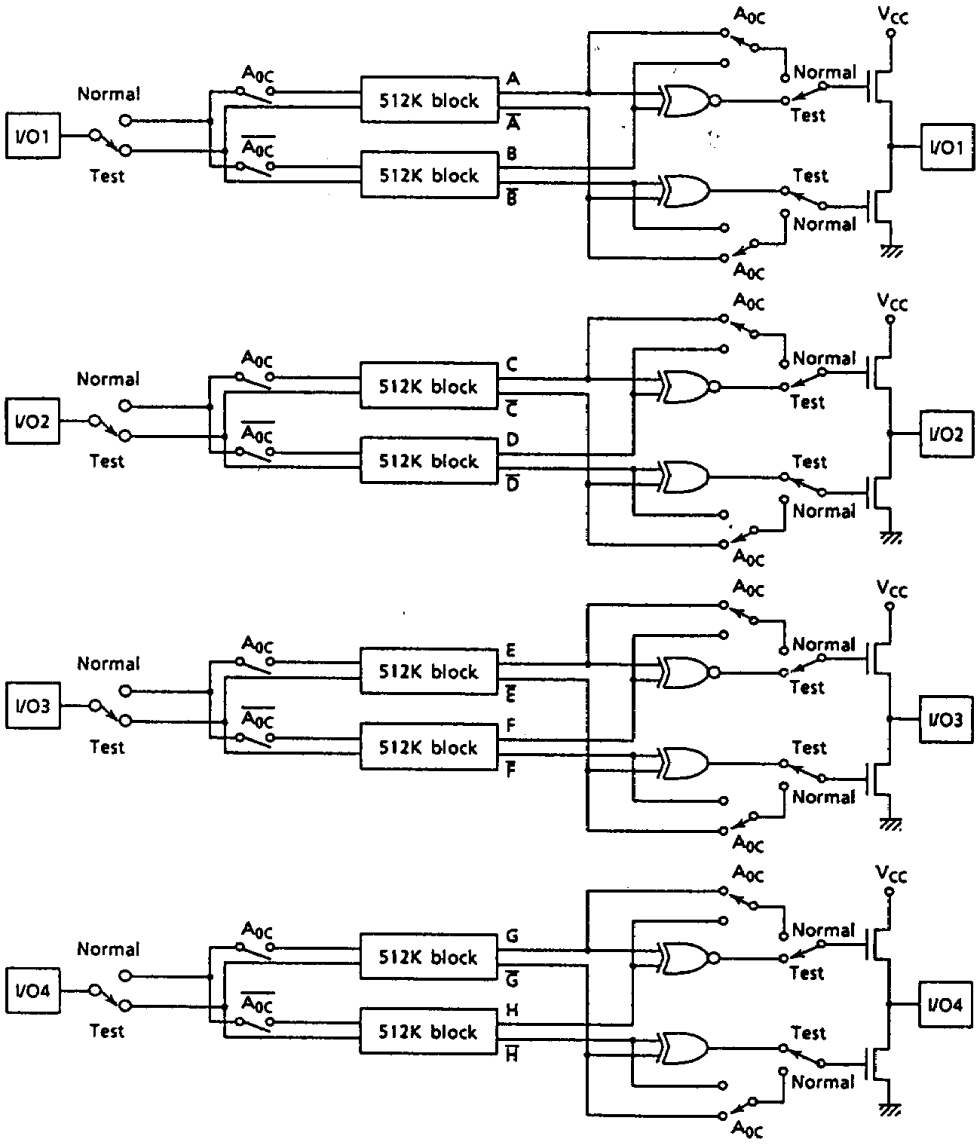



Fig. 1