NC State University

Department of Electrical and Computer Engineering

ECE 563: Fall 2021 (Rotenberg)

Project #3: Dynamic Instruction Scheduling

by

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NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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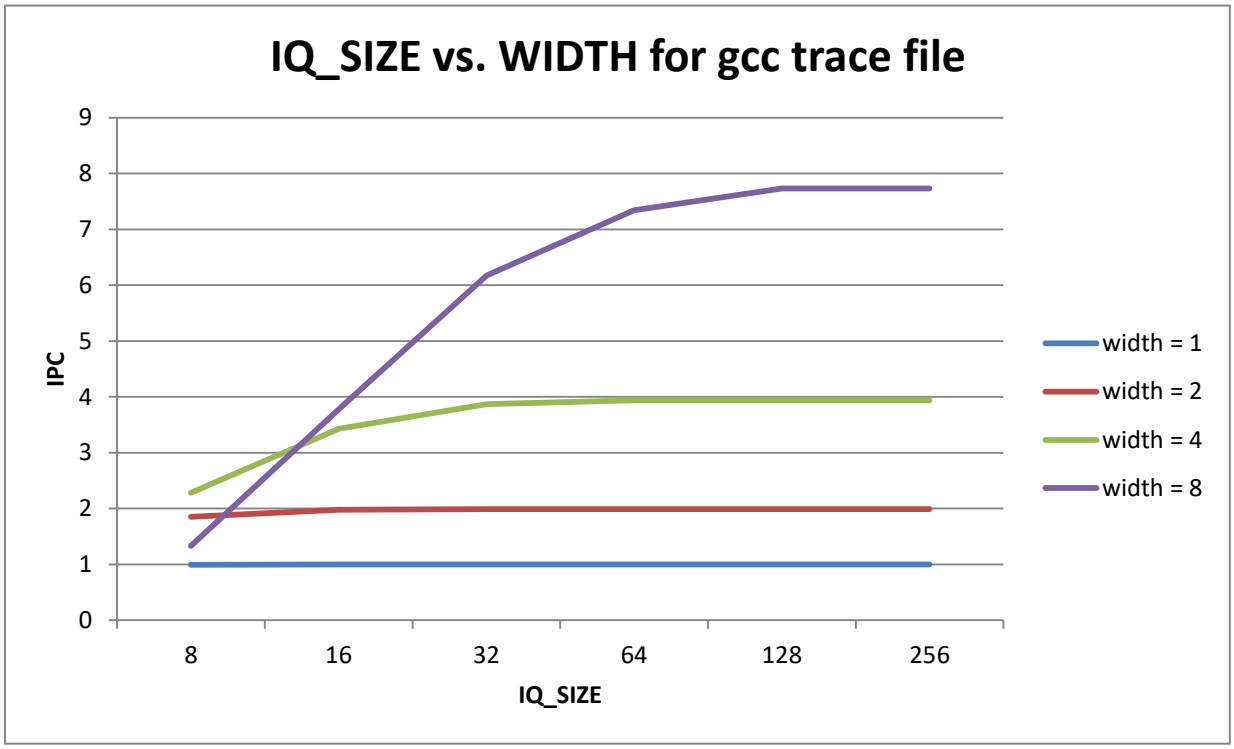
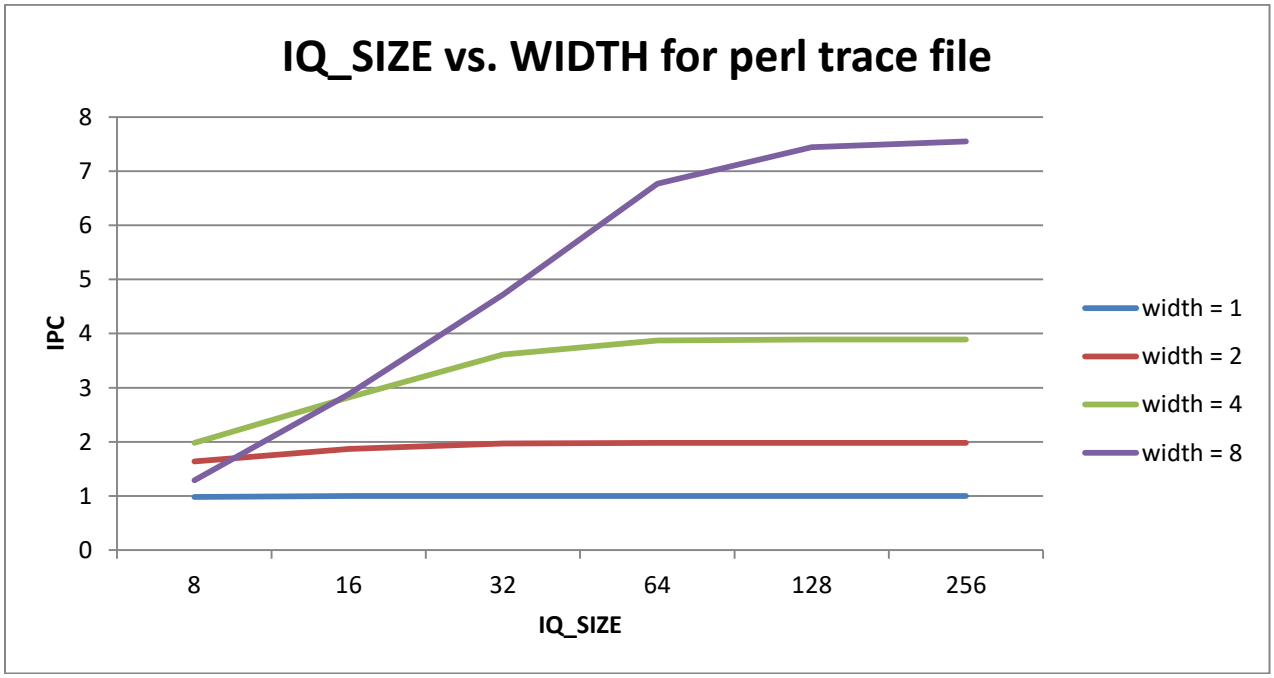
Course number: ECE 563

Varying IQ Size for different widths

1) Graphs:
   - gcc trace file



   - perl trace file



2) Graph Analysis:

Optimized IQ_Size per WIDTH		
	Benchmark = gcc	Benchmark = perl
WIDTH =1	8	8
WIDTH = 2	16	32
WIDTH = 4	32	64
WIDTH = 8	128	128

3) Discussion:

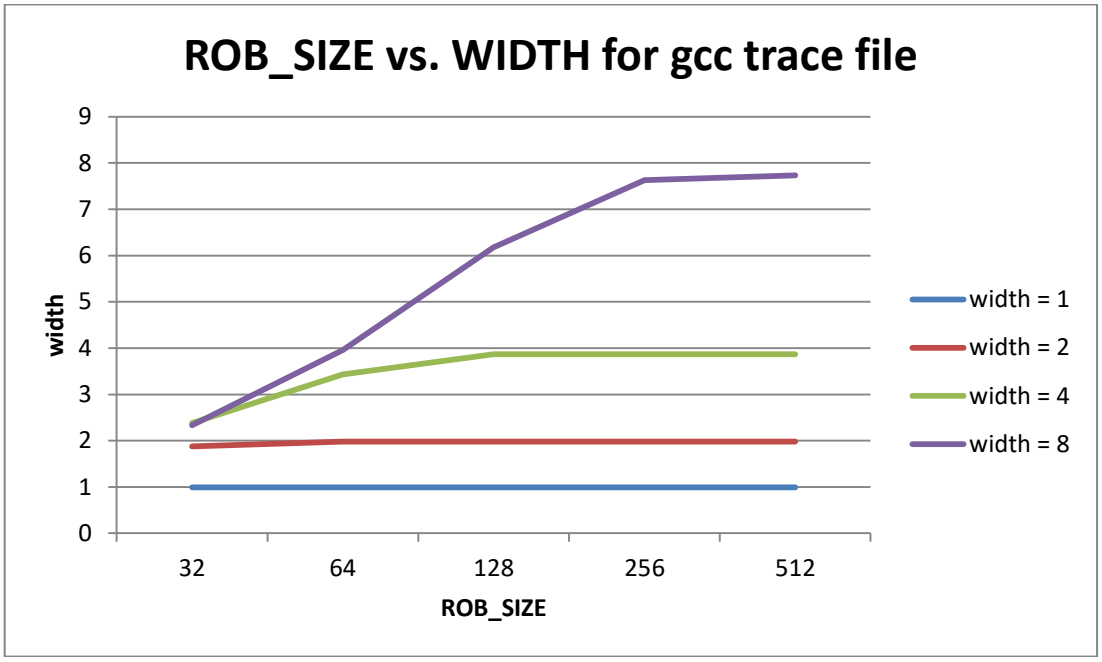
- The common trend that can be observed with all the graphs is that as the width increases with the increase in IQ size, the IPC value increases and it increasingly reaches a better value. The goal of a superscalar processor is to achieve an IPC that is close to WIDTH and as the width increases, the number of instructions going in increases which causes a stall. But as IQ size increases the queue takes longer to get packed and hence the stall decreases and this result in an increase in the instructions that are coming out and hence higher IPC values.

- The gcc benchmark shows a better value for IPC and this could be due to the reasons that there could be occurrences of hazards in perl benchmark more than gcc and hence IPC will not be as high or it could be because perl trace file has generally higher latency in the instructions that are consecutive to each other which also results in a lower IPC value for perl.

Varying ROB Size for different widths

Graphs

- gcc trace file



- perl trace file