Panasonic

MICROCOMPUTER   MN101E

MN101E29G/F29G
LSI User's Manual Vol.2

About This Manual

■Objective

The primary objective of this LSI manual is to describe the features of this product including an overview, CPU basic functions, interrupt, port, timer, serial interface, and other peripheral hardware functions.

Each section consists of brief functional information, block diagrams and the details of control registers including operation methods and setting examples.

■Structure of This Manual

Each section of this manual consists of a title, summary, main text, hint, precautions and warnings, and references.

The layout and definition of each section are shown below.

Header
Chapter number and
Chapter title

Section title

Sub section title

chapter 2
Basic CPU

2.8   Reset

2.8.1   Reset operation

Main text

the CPU contents are reset and registers are intialized when the NRST pin (P 27) is pulled to low.

■ Initiating a Reset
There are two methods to initiate a reset.
(1)   Drive the NRST pin low for at least four clock cycles.
NTST pin should be holded "low" for more than 4 clock cycles (200 ns a t a 20 NHz)

NRST pin

4 clock cycles
(200 ns at a 20 MHz)

Figure:2.8.1 MInimum Reset PUlse Width

(2)   Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P 27 (NRST) pin. And transfering to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT 7 flag becomes "1" and reset is released.

Hint

Important information
from the text.

On this LSI, the starting mode is NORMAL mode that high oscillation i s the base clock.

When the power voltage low circuit is connected to NTST pin, circuit t hat gives pulse for enough low level time at sudeen unconnected. And r set can be generated even if its pulse is low level as the oscillation clock is under 4 clocks,take notice of noise.

Precautions and
warnings

Please be sure to read
the precautions to prevent
any loss of functionality or
damage to the chip.

footer

Page # and
section title.

II-48   Reset

This page serves as an example to the explanations above. It may be different on an actual page.

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■Finding Desired Information

This manual provides three methods for finding the desired information quickly and easily.

1. Refer to the index at the front of the manual to locate the beginning of each section.

2. Refer to the table of contents at the front of the manual to locate the desired titles.

3. The chapter number and chapter title are located at the top corner of each page, and the section titles are located at the bottom corner of each page.

■Related Manuals

Note that the following related documents are available.

- "MN101E Series Instruction Manual"
  <Describes the instruction set.>

- "MN101C/MN101E Series Cross-assembler User's Manual"
  <Describes the assembler syntax and notation.>

- "MN101C/MN101E Series C Compiler User's Manual Usage Guide"
  <Describes the installation, commands and options of the C Compiler.>

- "MN101C/MN101E Series C Compiler User's Manual Language Description"
  <Describes the syntax of the C Compiler.>

- "MN101C/MN101E Series C Compiler User's Manual Library Reference"
  <Describes the standard library of the C Compiler.>

- "MN101C/MN101E Series Installation Manual"
  <Describes the steps to install the Integrated Development Environment (DebugFactory Builder), C compiler and the real-time OS. It also describes the procedure to setup the in-circuit emulator (PX-ICE101C/E).>

- "MN101C/MN101E/MN103L Series Software Development Environment Installation Manual"
  <Describes the steps to install the Integrated Development Environment (DebugFactory Builder), C compiler and the real-time OS. It also describes the procedure to setup the in-circuit emulator (PX-ICE101C/E-Advance, PX-ICE101C/E-Lite).>

■Contact Information

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Chapter 10 Watchdog Timer

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10.1 Overview

This LSI has a watchdog timer. This timer is used to detect software processing errors. It is controlled by the watchdog timer control register (WDCTR). And, once an overflow of watchdog timer is generated, a watchdog interrupt (WDIRQ) is generated. As a result of the generation twice, consecutively, of the watchdog interrupt, the software cannot execute in the intended sequence, thus the forceful reset is executed by the hardware.

10.1.1   Functions

Table:10.1.1 shows watchdog timer functions.

Table:10.1.1 Watchdog Timer Functions

Watchdog time-out period setup selection	2^{16} of system clock cycle 2^{18} of system clock cycle 2^{20} of system clock cycle
Watchdog timer enable	Stop Enable

10.1.2 Block Diagram

■ Watchdog Timer Block Diagram
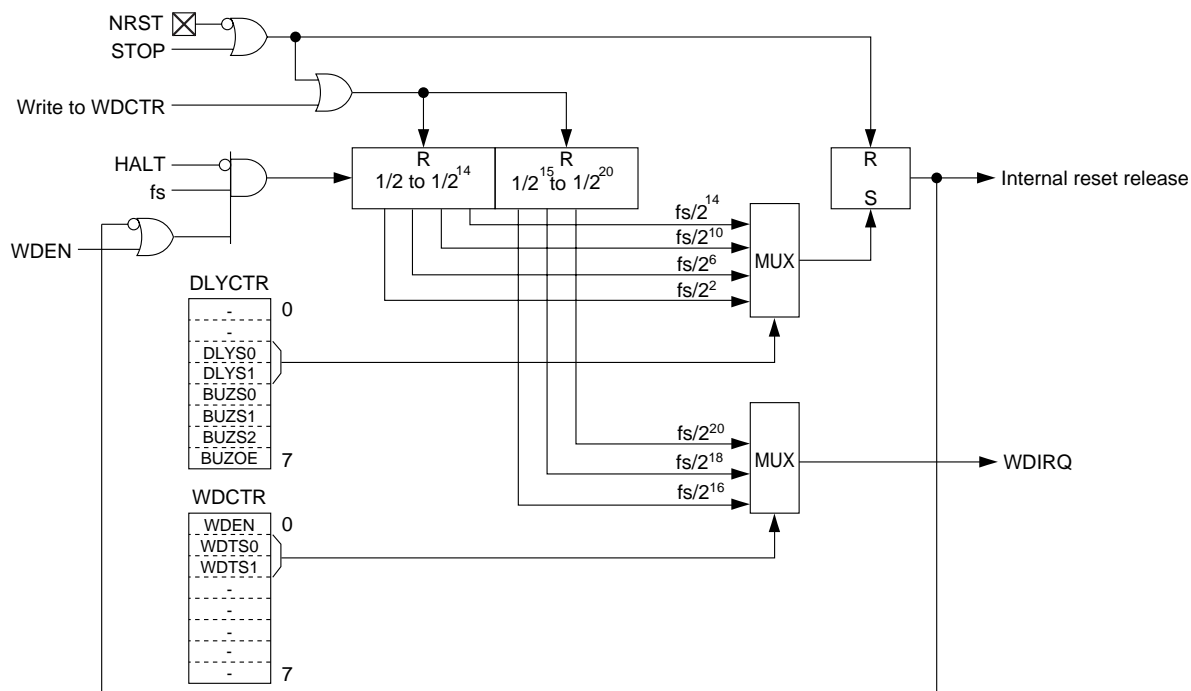
Figure:10.1.1 Block Diagram (Watchdog Timer)

The watchdog timer is also used as a timer to count the oscillation stabilization wait time. This is used as a watchdog timer except at recovering from STOP mode and at reset releasing.

The watchdog timer is initialized at reset or at STOP mode, and counts system clock (fs) as a clock source from the initial value (0x0000). The oscillation stabilization wait time is set by the oscillation stabilization wait time control register (DLYCTR).

10.2 Control Register

The watchdog timer is formed by the control register (WDCTR), (DLYCTR).

10.2.1 Control Registers

Table:10.2.1 shows the registers that control the watchdog timer.

Table:10.2.1 Watchdog Timer Control Register Functions

Register	Address	R/W	Function	Page
WDCTR	0x03F02	R/W	Watchdog timer control register	X-5
DLYCTR	0x03F03	R/W	Oscillation Stabilization Wait Time Control Register	X-6

10.2.2   Watchdog Timer Control Register

The watchdog timer is controlled by the watchdog timer control register (WDCTR).

■   Watchdog Timer Control Register (WDCTR:0x03F02)

bp	7	6	5	4	3	2	1	0
Flag	-	-	Reserved	Reserved	Reserved	WDTS1	WDTS0	WDEN
At reset	-	-	0	0	0	1	1	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5-3	Reserved	Always set to "0" *
2-1	WDTS1-0	Watchdog runaway detect cycles selection 00:2^{16} of system clock cycle 01:2^{18} of system clock cycle 1X:2^{20} of system clock cycle
0	WDEN	Watchdog timer enable 0:Watchdog timer is disabled 1:Watchdog timer is enabled

Once WDEN flag is set to "1", WDEN flag can't be cleared to "0". But when microcomputer reset is generated, WDEN flag is cleared to "0".

Always set "0" to the bp denoted by *.

■ Oscillation Stabilization Wait Time Control Register (DLYCTR:0x03F03)

bp	7	6	5	4	3	2	1	0
Flag	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-
At reset	0	0	0	0	0	0	-	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	-

bp	Flag	Description
7	BUZOE	Buzzer output selection(Buzzer Functions) 0:Buzzer output disable 1:Buzzer output enable
6-4	BUZS2-0	Buzzer output frequency(Buzzer Functions) 000:$fpll/2^{14}$ 001:$fpll/2^{13}$ 010:$fpll/2^{12}$ 011:$fpll/2^{11}$ 100:$fpll/2^{10}$ 101:$fpll/2^{9}$ 110:$fx/2^{4}$ 111:$fx/2^{3}$
3-2	DLYS1-0	Oscillation stabilization wait period selection 00:2^{14} of system clock cycle 01:2^{10} of system clock cycle 10:2^{6} of system clock cycle 11:2^{2} of system clock cycle
1-0	-	-

We recommend selecting the oscillation stabilization time of high-speed and slow-speed oscillation by set of DLYS1-0 flag after consulting with oscillator manufacturers.

About buzzer function refer to [Chapter 11 Buzzer].

10.3 Operation

10.3.1 Operation

The watchdog timer counts system clock (fs) as a clock source. If the watchdog timer is overflowed, the watchdog interrupt (WDIRQ) is generated as non maskable interrupt (NMI). At reset, the watchdog timer is stopped, but once the operation is enabled, it cannot be stopped except at reset. The watchdog timer control register (WDCTR) sets when the watchdog timer is released or how long the time-out period should be.

As a result of the generation twice, consecutively, of the watchdog interrupt (WDIRQ), the software cannot execute in the intended sequence, thus the forceful reset is executed by the hardware.

The watchdog timer cannot stop, once it starts operation.
However, the watchdog timer stops during the Stop mode and the HALT mode.

■   Usage of Watchdog Timer

When the watchdog timer is used, constant clear in program is needed to prevent an overflow of the watchdog timer. As a result of the software failure, the software cannot execute in the intended sequence, thus the watchdog timer overflows to detect errors.

Programming of the watchdog is generally done in the last step of its programming.

■   How to Detect Incorrect Code Execution

The watchdog timer is executed to be cleared in the certain cycle on the correct code execution. In this LSI, the watchdog timer detects errors when,

The watchdog timer overflows.

When the watchdog timer detects any error, the watchdog interrupt (WDIRQ) is generated as a non maskable interrupt (NMI).

■ How to clear Watchdog Timer

The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR) regardless of the writing data to the register. It is recommended that the bit set (BSET) instructions and etc., which do not change the WDCTR - register's values.

■ Watchdog Time-out Period

The watchdog time-out period is decided by the bp2, 1 (WDTS1-0) of the watchdog timer control register (WDCTR) and the system clock (fs). When the watchdog timer is not cleared till this setting value, it is regarded as an error and the watchdog interrupt (WDIRQ) of the non maskable interrupt (NMI) is generated.

The system clock is decided by setting of the CPU mode control register (CPUM).

[Chapter 2. 2.6 Clock Switching]

The watchdog time-out period is generally set from the execution time for main routine of program. That should be set the longer cycle than the value of the execution time or main routine divided by natural number (1, 2, · · · ·). And set the command of the watchdog timer clear to the main routine as that value makes the same cycle.

■ Watchdog Timer and CPU Mode

The relation between this watchdog timer and CPU mode features are as follows;

Table:10.3.1 Watchdog Timer Condition in Each CPU Operation Mode

CPU operation mode	Watchdog timer condition
NORMAL	Counting up with the system clock. * The counting is continued regardless of switching in NORMAL, IDLE, SLOW mode.
IDLE	
SLOW	
HALT	Counting is stopped (the couting value is retained.)
STOP	Counting is stopped (the couting value is retained.) * Watchdog interrupts cannot be generated in STOP mode.
After recovering from STOP	Counting is continued after the oscillation stabilization wait time if the detection of the incorrect code execution is enabled. Counting is stopped in the condition that the counting of the oscillation stabilization wait time is proceeded if the detection of the incorrect code execution is disabled.
After reset release	Counting is stopped.

In the system use STOP mode, it branches whether STOP mode is used or not in the execution of program. However, in this case, the counting value of the watchdog timer is different.

10.3.2　Setup Example

The watchdog timer detects errors. On the following example, the time-out period is set to $2^{18} \times$ system clock cycle.

An example setup procedure, with a description of each step is shown below.

■　Initial Setup Program (Watchdog Timer Initial Setup Example)

Setup Procedure	Description
(1) Set the time-out period WDCTR(0x03F02) bp2-1:WDTS1-0 =01	(1) Set the WDTS1-0 flag of the watchdog timer control register (WDCTR) to "01" to select the time-out period to $2^{18} \times$ system clock cycle.
(2) Start the watchdog timer operation WDCTR(0x03F02) bp0:WDEN =1	(2) Set the WDEN flag of the WDCTR register to start the watchdog timer operation.

■　Main Routine Program (Watchdog Timer Constant Clear Setup Example)

Setup Procedure	Description
(1) Set the watchdog timer for the constant clear Writing to WDCTR(0x03F02) (c.f.)BSET (WDCTR) WDEN (bp0:WDEN=1)	(1) Clear the watchdog timer by the cycle from $2^{18} \times$ system clock cycle. The watchdog timer clear should be inserted in the main routine, with the same cycle, and to be the set cycle. It is recommended that the bit set (BSET) instructions and etc., which do not change the WDCTR - register's value.

■　Interrupt Service Routine Setup

Setup Procedure	Description
(1) Set the watchdog interrupt service routine NMICR(0x03FE1) TBNZ　　　(NMICR),WDIR,WDPR0	(1) If the watchdog timer overflows, the non maskable interrupt is generated. Confirm that the WDIR flag of the non maskable interrupt control register (NMICR) is "1" in the interrupt processing rootine and execute the appropriate processing for system.

> The operation, just before the watchdog interrupt may be executed wrongly. In that case, proper operation is not guaranteed.

Chapter 11 Buzzer

11.1 Overview

This LSI has a buzzer. It can output the square wave that multiply by $1/2^9$ to $1/2^{14}$ of the high frequency oscillation clock, or by $1/2^3$ to $1/2^4$ of the low frequency oscillation clock.

11.1.1   Functions

Table:11.1.1 shows the buzzer functions.

Table:11.1.1 Buzzer Functions

output selection	Buzzer output disable Buzzer output enable
buzzer reverse output	inversion output
output pin selection	A port: P53, P54 output(P54 is buzzer reverse output of P53) B port: P15, P16 output(P16 is buzzer reverse output of P15)
Buzzer output frequency selection	$fpll/2^{14}$ $fpll/2^{13}$ $fpll/2^{12}$ $fpll/2^{11}$ $fpll/2^{10}$ $fpll/2^{9}$ $fx/2^{4}$ $fx/2^{3}$
Oscillation stabilization wait cycle selection	$fs/2^{14}$ $fs/2^{10}$ $fs/2^{6}$ *1 $fs/2^{2}$ *1

*1: Do not use at high-speed operation (NORMAL mode).

　　 Use at slow-speed operation (SLOW mode).

Pins can be switched to RMOUTA/RMOUTB/RMOUTC.

　　　　　　　　BUZZERA (P53)
　　　　　　　　NBUZZERA (P54)
　　　　　　　　BUZZERB (P15)
　　　　　　　　NBUZZERB (P16)

On the text, if there is not much functional difference in pins A and B, "A" and "B" of the pin names are omitted.

At the instant that the BUZOE flag is set to "0", the output of the buzzer becomes "Low".

11.1.2 Block Diagram

■ Buzzer Block Diagram
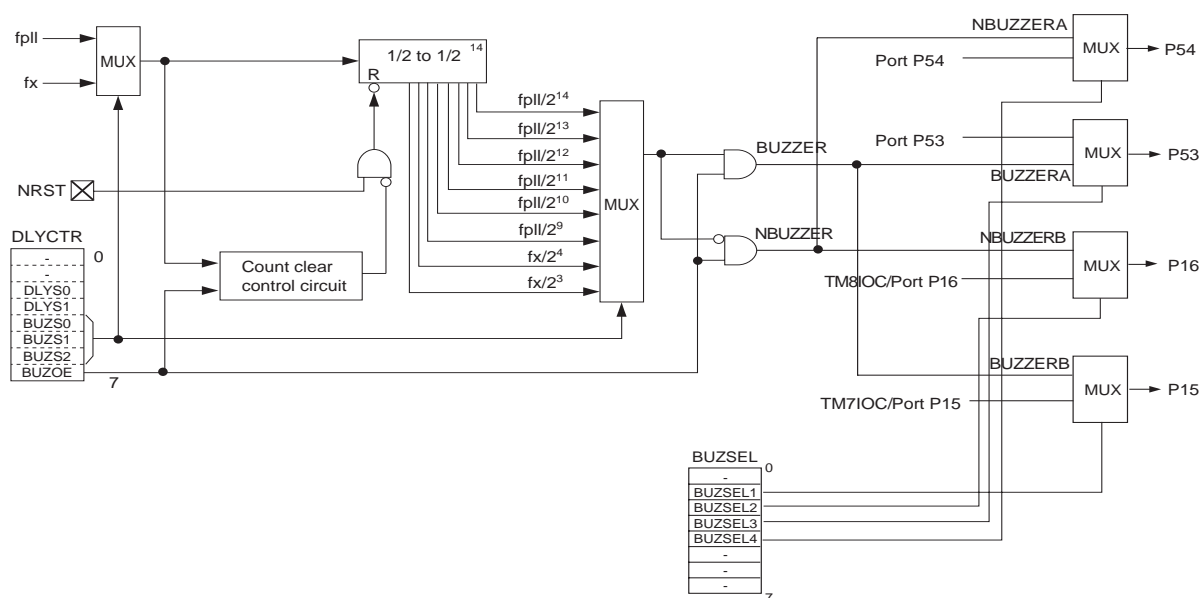
Figure:11.1.1 Buzzer Block Diagram

11.2 Control Register

Buzzer is controlled of the oscillation stabilization wait time control register (DLYCTR) of upper 4 bits.

11.2.1 Registers

Table:11.2.1 shows the Oscillation Stabilization Wait Time Control Register.

Table:11.2.1 Buzzer Control Register

Register	Address	R/W	Functions	Page
DLYCTR	0x03F03	R/W	Oscillation Stabilization Wait Time Control Register	XI-6
P5DIR	0x03F35	R/W	Port 5 direction control register	IV-80
P1OMD	0x03EE1	R/W	Port 1 output mode register	IV-27
P1DIR	0x03F31	R/W	Port 1 direction control register	IV-26
BUZSEL	0x03EE2	R/W	Buzzer output selection register	XI-5

11.2.2   Buzzer Output Selection Register (BUZSEL)

■ Buzzer Output Selection Register (BUZSEL:0x03EE2)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	BUZSEL4	BUZSEL3	BUZSEL2	BUZSEL1	-
At reset	-	-	-	0	0	0	0	-
Access	-	-	-	R/W	R/W	R/W	R/W	-

bp	Flag	Description
7-5	-	-
4	BUZSEL4	Buzzer A reverse output selection 0:Port P54 1:NBUZZERA
3	BUZSEL3	Buzzer A output selection 0:Port P53 1:BUZZERA
2	BUZSEL2	Buzzer B reverse output selection 0:TM8IOC/P16 1:NBUZZERB
1	BUZSEL1	Buzzer B output selection 0:TM7IOC/P15 1:BUZZERB
0	-	-

11.2.3 Oscillation Stabilization Wait Time Control Register (DLYCTR)

■ Oscillation Stabilization Wait Time Control Register (DLYCTR:0x03F03)

bp	7	6	5	4	3	2	1	0
Flag	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-
At reset	0	0	0	0	0	0	-	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	-

bp	Flag	Description
7	BUZOE	Buzzer output selection 0:Buzzer output disable 1:Buzzer output enable
6-4	BUZS2-0	Buzzer output frequency selection 000:$f_{pll}/2^{14}$ 001:$f_{pll}/2^{13}$ 010:$f_{pll}/2^{12}$ 011:$f_{pll}/2^{11}$ 100:$f_{pll}/2^{10}$ 101:$f_{pll}/2^{9}$ 110:$f_x/2^{4}$ 111:$f_x/2^{3}$
3-2	DLYS1-0	Oscillation stabilization wait period selection (*Watchdog Timer Functions) 00:$f_s/2^{14}$ 01:$f_s/2^{10}$ 10:$f_s/2^{6}$ *1 11:$f_s/2^{2}$ *1
1-0	-	-

*1:Do not use at high-speed operation (NORMAL mode).

Use at slow-speed operation (SLOW mode).

The BUZ0E flag and BUZS2 to 0 flags should not be set at the same time.

DLYS1 to 0 flag is setting flag of watchdog timer function. Refer to [Chapter 10 Watchdog Timer] for watchdog timer function.

11.3 Operation

11.3.1 Operation

■ Buzzer

Buzzer outputs the square wave, having frequency $1/2^9$ to $1/2^{14}$ of the high oscillation clock (fpll), or $1/2^3$ to $1/2^4$ of the low oscillation clock (fx). The BUZS 2, 1, 0 flag of the oscillation stabilization wait time control register (DLYCTR) set the frequency of the buzzer output. The BUZOE flag of the oscillation stabilization wait time control register (DLYCTR) sets buzzer output ON / OFF.

■ Buzzer Output Frequency

The frequency of buzzer output is decided by the frequency of the high oscillation clock (fpll) or the low oscillation clock (fx) and the bit 6, 5, 4 (BUZS2, BUZS1, BUZS0) of the oscillation stabilization wait time control register (DLYCTR).

Table:11.3.1 Buzzer Output Frequency

fpll	fx	BUZS2	BUZS1	BUZSO	Buzzer output frequency
10 MHz	-	0	1	0	2.44 kHz
10 MHz	-	0	1	1	4.88 kHz
4 MHz	-	0	1	1	1.95 kHz
4 MHz	-	1	0	0	3.91 kHz
-	32 kHz	1	1	0	2 kHz
-	32 kHz	1	1	1	4 kHz

At the instant that the BUZOE flag is set to "0", the output of the buzzer (BUZZER and NBUZZER) becomes "Low".

11.3.2 Setup Example

■ Setup Example

Buzzer outputs the square wave of 2.44 kHz from P53 pin. It is used 10 MHz as the high oscillation clock (fpll).

An example of setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the buzzer frequency DLYCTR (0x03F03) bp6-4 :BUZS2-0 =010	(1) Set BUZS2 to BUZS0 flag of the oscillation stabilization wait time control register (DLYCTR) to "010" to select $fpll/2^{12}$ to the buzzer frequency. When the high oscillation clock fpll is 10 MHz, the buzzer output frequency is 2.44 kHz.
(2) Set P53 pin BUZSEL (0x03EE2) bp3 :BUZSEL3 =1 P5DIR (0x03F35) bp3 :P5DIR3 =1	(2) Set BUZSEL3 flag of the buzzer output selection register (BUZSEL) to "1" to set the P53 pin to a special function pin. Set P5DIR3 flag of port 5 direction control register (P5DIR) to "1" to set output mode; then, the low level is output from the P53 pin.
(3) Buzzer output ON DLYCTR (0x03F03) bp7 :BUZOE =1	(3) Set the BUZSE flag of the oscillation stabilization wait time control register (DLYCTR) to "1" to output the square wave of the buzzer output frequency set by the P53 pin.
(4) Buzzer output OFF DLYCTR (0x03F03) bp7 :BUZOE =0	(4) Set the BUZOE flag of the oscillation stabilization wait time control register (DLYCTR) to "0" to clear, and P53 pin outputs low level.

Setup of the buzzer output enable should be done after setup of the buzzer frequency. When the low oscillation clock (fx) dividing is selected as the buzzer output frequency and the buzzer output is switched disable from enable, the buzzer dividing counter is not cleared unless more than 1 clock of the low oscillation clock is secured. When enable buzzer output again, enable buzzer output after waiting one clock of low-speed oscillation clock.

Chapter 12 Serial Interface

12

12.1 Overview

This LSI has 6 serial interfaces (serial 0, serial 1, serial 2, serial 3, serial 4 and serial 5).

Serial interfaces 0, 1, 2 and 3 can be used for clock synchronous and UART (duplex) communication. Serial interfaces 4 can be used for clock synchronous and IIC (multi-master) communication. Serial interface 5 can be used for IIC (slave) communication.

Table:12.1.1 Serial Interface Communication Types

	Serial 0	Serial 1	Serial 2	Serial 3	Serial 4	Serial 5
Clock synchronous	O	O	O	O	O	-
UART(duplex)	O	O	O	O	-	-
Single master IIC	-	-	-	-	-	-
Multi master IIC	-	-	-	-	O	-
Slave IIC	-	-	-	-	-	O

Table:12.1.2 shows the pins used for serial interface. Serial interfaces can switch pins to A type or B type. For A pin, "A" is added to the end of its name. For B pin, "B" is added to the end of its name.

Table:12.1.2 Serial Interface Pins

		Serial 0		Serial 1		Serial 2	
Pin switching function		O		O		O	
Clock synchronous	Data I/O pin	SBO0A (P50)	SBO0B (P43)	SBO1A (P01)	SBO1B (P75)	SBO2A (P70)	SBO2B (P30)
	Data input pin	SBI0A (P51)	SBI0B (P44)	SBI1A (P00)	SBI1B (P76)	SBI2A (P71)	SBI2B (P31)
	Clock I/O pin	SBT0A (P52)	SBT0B (P45)	SBT1A (P02)	SBT1B (P77)	SBT2A (P72)	SBT2B (P32)
UART(duplex)	Data I/O pin	TXD0A (P50)	TXD0B (P43)	TXD1A (P01)	TXD1B (P75)	TXD2A (P70)	TXD2B (P30)
	Data input pin	RXD0A (P51)	RXD0B (P44)	RXD1A (P00)	RXD1B (P76)	RXD2A (P71)	RXD2B (P31)
Multi master IIC	Data I/O pin	-		-		-	
	Clock I/O pin	-		-		-	
Slave IIC	Data I/O pin	-		-		-	
	Clock I/O pin	-		-		-	

		Serial 3		Serial 4		Serial 5	
Pin switching function		O		O		O	
Clock synchronous	Data I/O pin	SBO3A (P04)	SBO3B (P40)	SBO4A (P66)	SBO4B (P33)	-	
	Data input pin	SBI3A (P05)	SBI3B (P41)	SBI4A (P65)	SBI4B (P35)	-	
	Clock I/O pin	SBT3A (P06)	SBT3B (P42)	SBT4A (P67)	SBT4B (P34)	-	
UART(duplex)	Data I/O pin	TXD3A (P04)	TXD3B (P40)	-		-	
	Data input pin	RXD3A (P05)	RXD3B (P41)	-		-	
Multi master IIC	Data I/O pin	-		SDA4A (P66)	SDA4B (P33)	-	
	Clock I/O pin	-		SCL4A (P67)	SCL4B (P34)	-	
Slave IIC	Data I/O pin	-		-		SDA5A (P73)	SDA5B (P46)
	Clock I/O pin	-		-		SCL5A (P74)	SCL5B (P47)

In the text, if there is not much functional difference in pins A or B, "A" and "B" of the pin names are omitted.

12.1.1   Functions

Table:12.1.3 shows clock synchronous serial interface functions. Table:12.1.4 show UART (duplex) serial interface functions. Table:12.1.5 shows single master IIC interface functions. Table:12.1.6 shows slave IIC interface functions.

Table:12.1.3 Clock Synchronous Serial Interface Functions

	Serial 0	Serial 1	Serial 2	Serial 3	Serial 4
Interrupt	SC0TIRQ	SC1TIRQ	SC2IRQ	SC3IRQ	SC4TIRQ
Pins	SBO0 SBI0 SBT0	SBO1 SBI1 SBT1	SBO2 SBI2 SBT2	SBO3 SBI3 SBT3	SBO4 SBI4 SBT4
3-channel type	O	O	O	O	O
2-channel type	O (SBO0,SBT0)	O (SBO1,SBT1)	O (SBO2,SBT2)	O (SBO3,SBT3)	O (SBO4,SBT4)
Specification of transfer bit count (1 to 8 bits)	O	O	O	O	O
Selection of start condition	O	O	O	O	O
Specification of the first transfer bit	O	O	O	O	O
Input edge/output edge	O	O	O	O	O
SBOn output control after final data moved out (H/L/final data hold)	O	O	O	O	O
Communication function at standby mode (only slave reception is available)	O	O	O	O	O
Continuous operation (ATC1 concomitant use)	O	O	O	O	O
Selection of transfer clock dividing	O	O	O	O	-
Selection of transfer clock dividing ratio	Divided by 8/ divided by16	Divided by 8/ divided by16	Divided by 8/ divided by16	Divided by 8/ divided by16	-
Clock source	fpll/2 fpll/4 fpll/16 fpll/64 fs/2 fs/4 External clock Timer 0 to 4, A output	fpll/2 fpll/4 fpll/16 fpll/64 fs/2 fs/4 External clock Timer 0 to 4, A output	fpll/2 fpll/4 fpll/16 fpll/64 fs/2 fs/4 External clock Timer 0 to 4, A output	fpll/2 fpll/4 fpll/16 fpll/64 fs/2 fs/4 External clock Timer 0 to 4, A output	fpll/2 fpll/4 fpll/16 fpll/32 fs/2 fs/4 External clock Timer 0 to 4, A output
Maximum transfer rate	5.0 MHz	5.0 MHz	5.0 MHz	5.0 MHz	5.0 MHz
fpll: machine clock (high-speed oscillation) fs: system clock					

Set the transfer rate which is slower than the system clock (fs).

Table:12.1.4 UART (duplex) Serial Interface Functions

		Serial0	Serial1	Serial2	Serial3
Interrupt	(at transmission completion) (at reception completion)	SC0TIRQ SC0RIRQ	SC1TIRQ SC1RIRQ	SC2TIRQ SC2RIRQ	SC3TIRQ SC3RIRQ
Pins		TXD0 RXD0	TXD1 RXD1	TXD2 RXD2	TXD3 RXD3
2-channel type		O			
1-channel type		O (TXD0)	O (TXD1)	O (TXD2)	O (TXD3)
Specification of transfer bit count/frame selection		7 bits + 1STOP 7 bits + 2STOP 8 bits + 1STOP 8 bits + 2STOP			
Selection of parity bit		O			
Parity bit control		0 parity 1 parity Odd parity Even parity			
Specification of the first transfer bit		O			
Selection of transfer clock dividing ratio		Divided by 8/divided by16			
Clock source		fpll/2 fpll/4 fpll/16 fpll/64 fs/2 fs/4 Timer 0 to 4, A output			
Maximum transfer rate		300 Kbps			
fpll: machine clock (high speed oscillation) fs: system clock In UART communication, a transfer clock is obtained by dividing a clock source internally.					

! Set the transfer rate which is slower than the system clock (fs).

Table:12.1.5 Multi Master IIC Serial Interface Functions

		Serial 4
Interrupt		SC4TIRQ(communication complete interrupt)
		SC4SIRQ(stop condition detection interrupt)
Pins		SDA4A/SDA4B,SCL4A/SCL4B
Communication mode	Master transmission	O
	Master reception	O
	Slave transmission	O
	Slave reception	O
Transfer format	Addressing format	O
	Free data format	At master communication only
Address format	7-bit address	O
	General call	O
Communication format	Standard mode (100 bit/s)	O
	High-speed mode (400 bit/s)	O
Specification of first transfer bit		1 to 8 bits(at master communication)
		8 bits (at slave communication)
Specification of transfer first bit		O
ACK bit selection		At master communication only
ACK bit level selection		O
Clock sources		fpll/2
		fpll/4
		fpll/16
		fpll/32
		fs/2
		fs/4
		Timer 0 to 4, A output
Transfer rate = clock source divided by 8.		

Table:12.1.6 Multi Master IIC Serial Interface Functions

		Serial 5
Interrupt		SC5TIRQ
Pins		SDA5A/SDA5B/SCL5A/
		SCL5B
Address format	7-bit address	O
	10-bit address	O
	General call	O
Maximum transfer rate		High-speed mode 400 KHz

Set the transfer rate which is slower than the system clock (fs).

12.1.2   Block Diagram

■ Serial Interface 0 Block Diagram
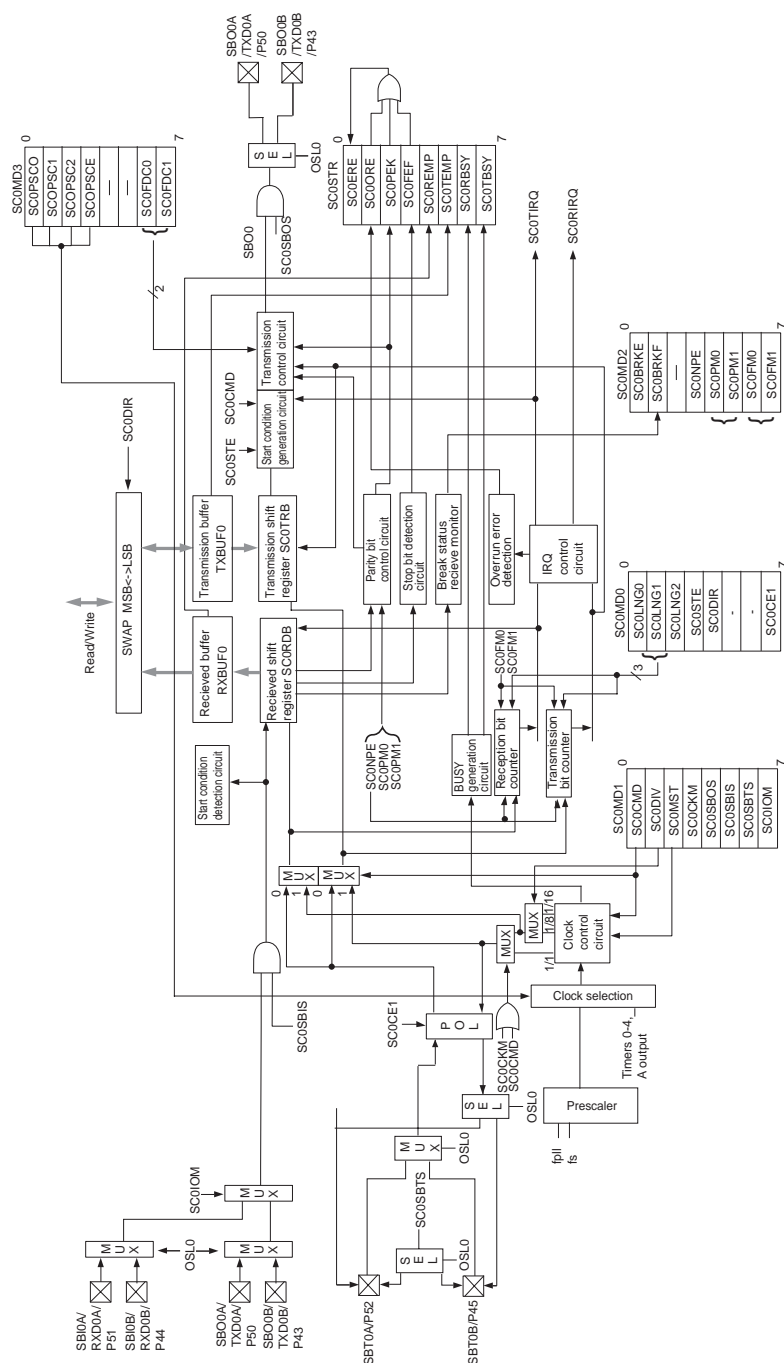
Figure:12.1.1 Serial Interface 0 Block Diagram

■ Serial Interface 1 Block Diagram
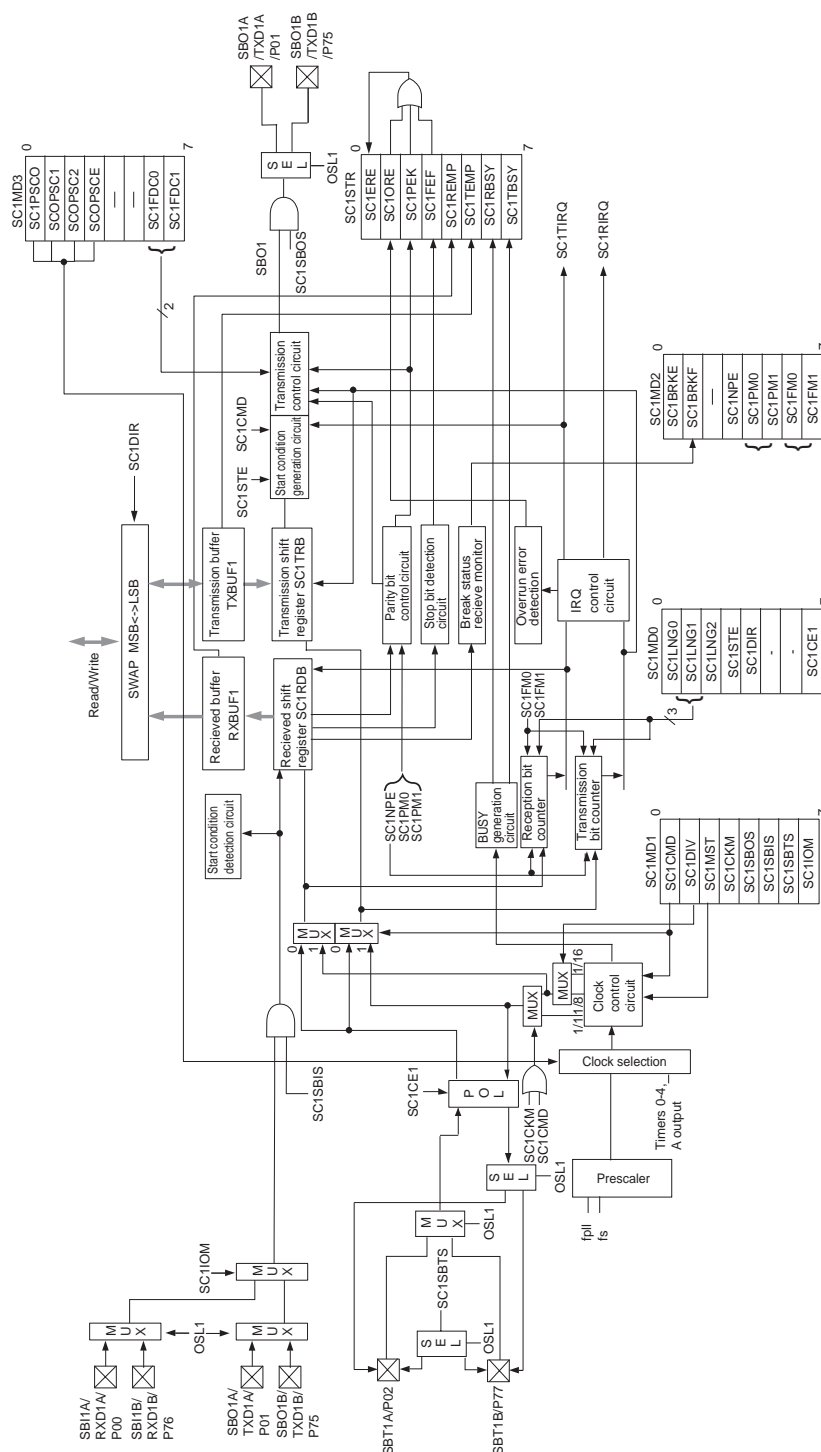
Figure:12.1.2 Serial Interface 1 Block Diagram

■ Serial Interface 2 Block Diagram
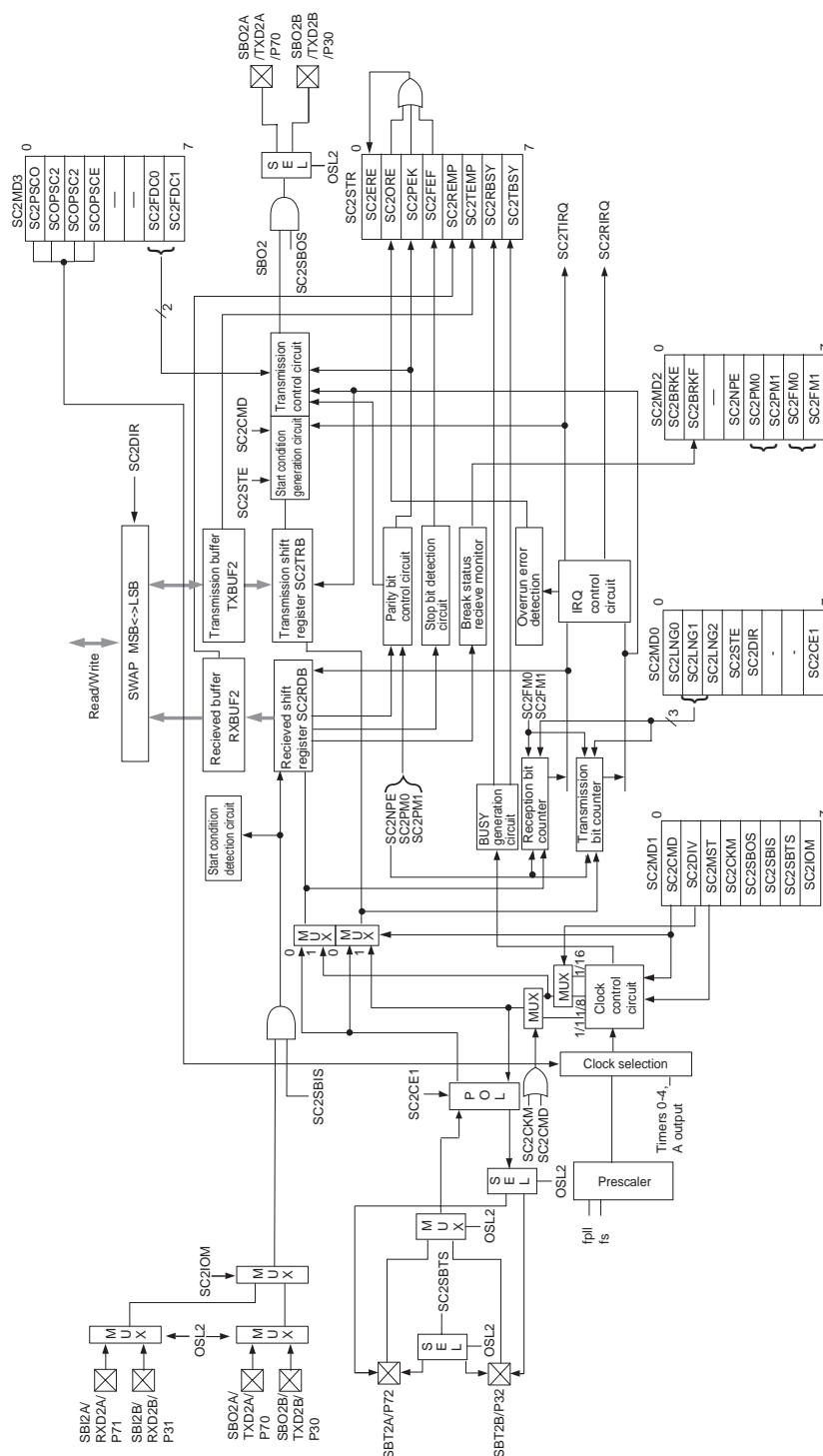
Figure:12.1.3 Serial Interface 2 Block Diagram

■ Serial Interface 3 Block Diagram
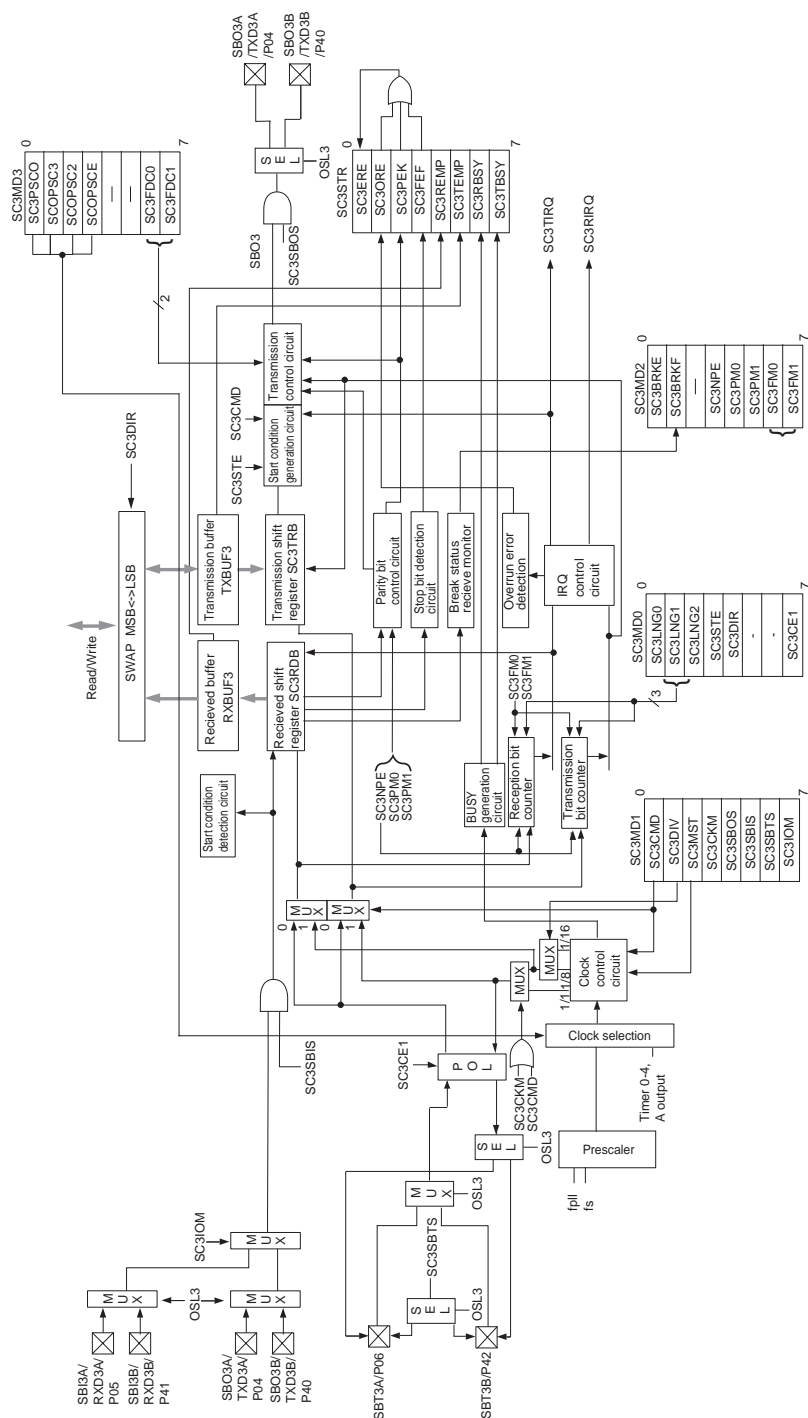
Figure:12.1.4 Serial Interface 3 Block Diagram

■ Serial Interface 4 Block Diagram
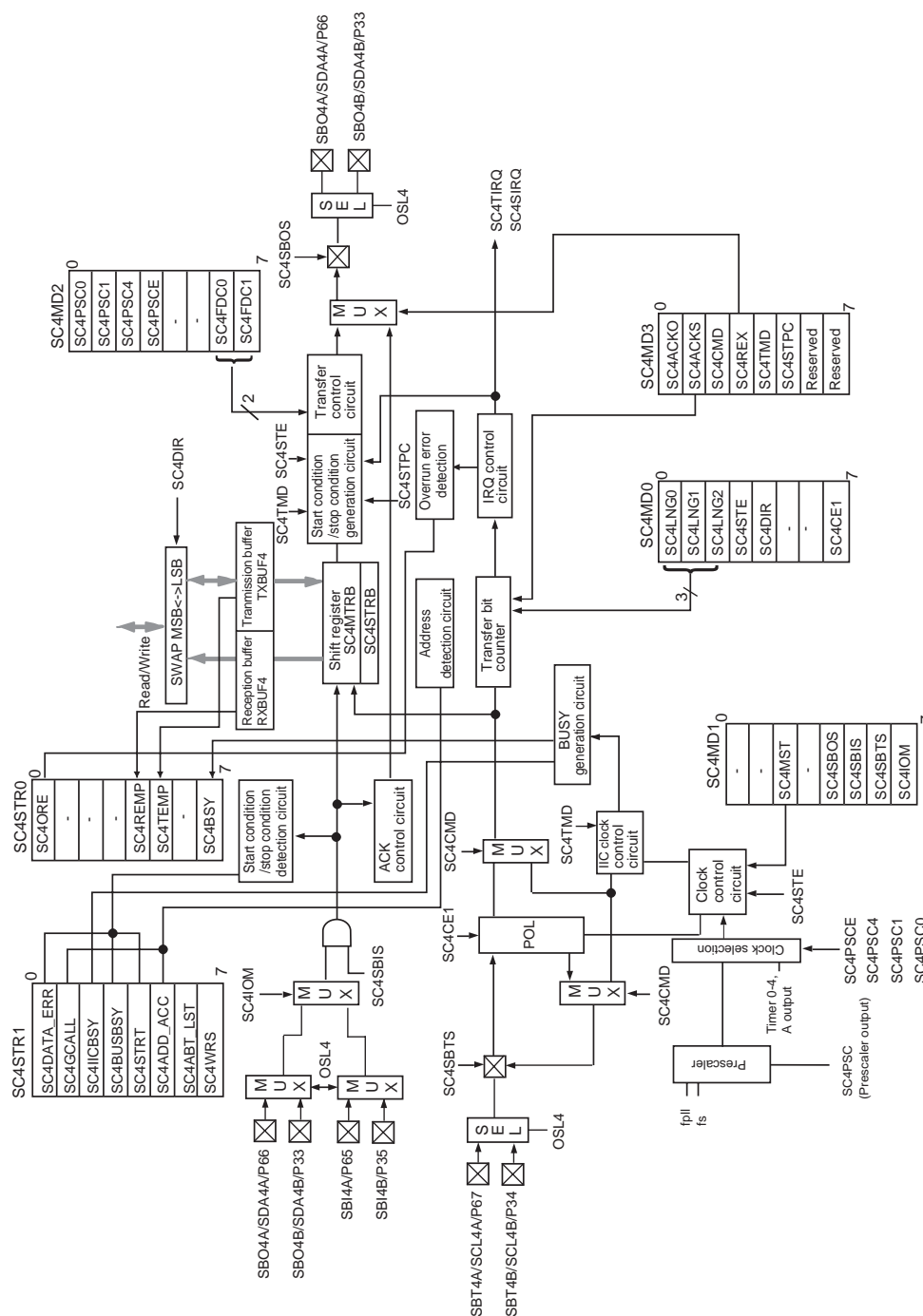
Figure:12.1.5 Serial Interface 4 Block Diagram

■ Serial Interface 5 Block Diagram
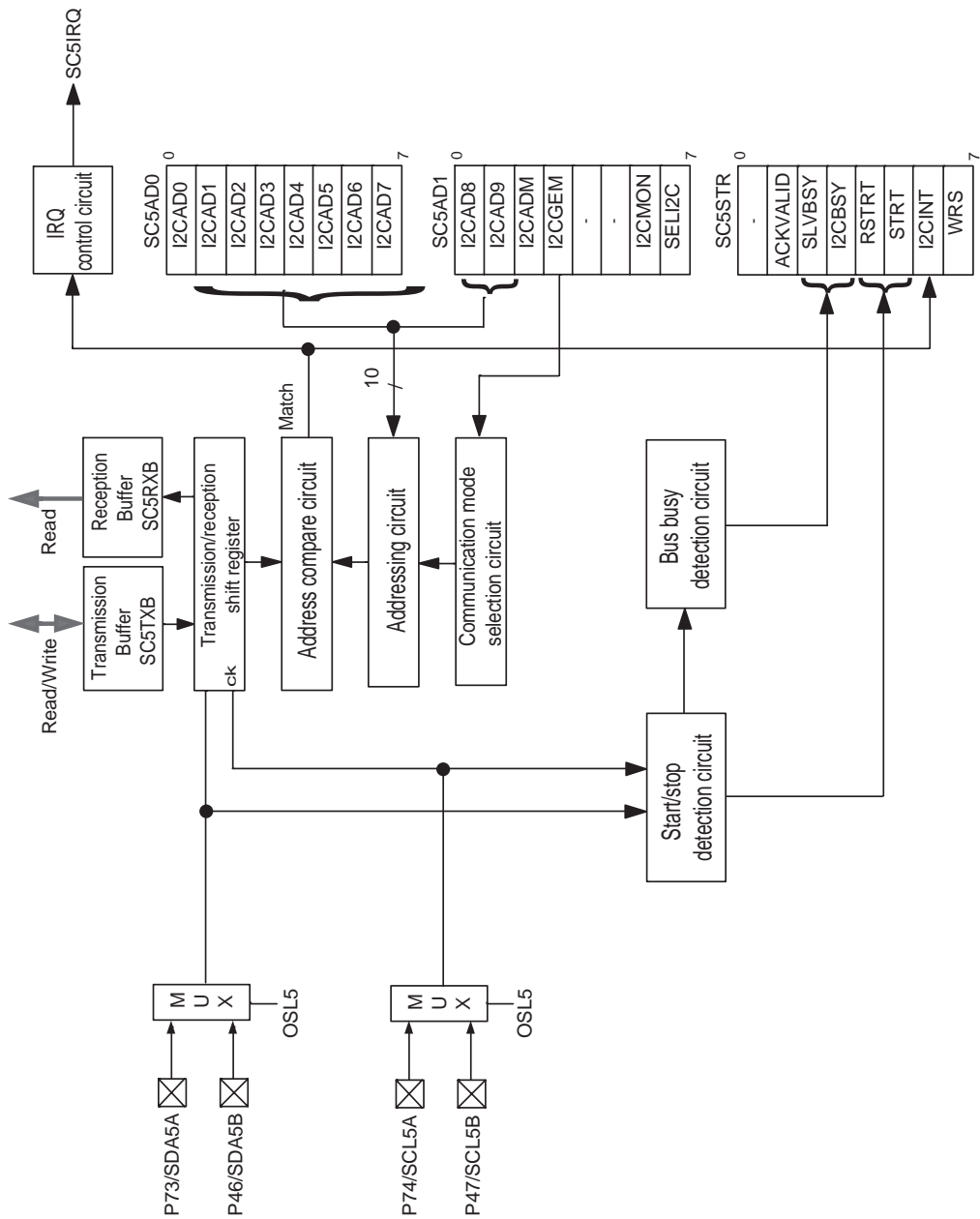
Figure:12.1.6 Serial Interface 5 Block Diagram

12.2 Control Registers

12.2.1 Registers

Table:12.2.1 shows registers to control serial interface.

Table:12.2.1 Serial Interface Control Registers

	Register	Address	R/W	Function	Page
Serial 0	SC0MD0	0x03F91	R/W	Serial interface 0 mode register 0	XII-24
	SC0MD1	0x03F92	R/W	Serial interface 0 mode register 1	XII-25
	SC0MD2	0x03F93	R/W	Serial interface 0 mode register 2	XII-27
	SC0MD3	0x03F94	R/W	Serial interface 0 mode register 3	XII-28
	SC0STR	0x03F95	R	Serial interface 0 status register	XII-29
	RXBUF0	0x03F96	R	Serial interface 0 reception data buffer	XII-23
	TXBUF0	0x03F97	R/W	Serial interface 0 transmission data buffer	XII-23
	SC0SEL	0x03F90	R/W	Serial 0 I/O pin switching control register 3	XII-17
	P5ODC	0x03EF3	R/W	Port 5 Nch open-drain control register	IV-81
	P5DIR	0x03F35	R/W	Port 5 direction control register	IV-80
	P5PLUD	0x03F45	R/W	Port 5 pull-up/pull-down resistor control register	IV-80
	P40DC	0x03EF2	R/W	Port 4 Nch open-drain control register	IV-67
	P4DIR	0x03F34	R/W	Port 4 direction control register	IV-66
	P4PLUD	0x03F44	R/W	Port 4 pull-up/pull-down resistor control register	IV-66
	PERIICR	0x03FFE	R/W	Peripheral function group interrupt control register	III-41
	SC0TICR	0x03FF7	R/W	Serial 0 UART transmission interrupt control register	III-35

	Register	Address	R/W	Function	Page
Serial 1	SC1MD0	0x03F99	R/W	Serial interface1 mode register 0	XII-24
	SC1MD1	0x03F9A	R/W	Serial interface 1 mode register 1	XII-25
	SC1MD2	0x03F9B	R/W	Serial interface 1 mode register 2	XII-27
	SC1MD3	0x03F9C	R/W	Serial interface 1 mode register 3	XII-28
	SC1STR	0x03F9D	R	Serial interface 1 status register	XII-29
	RXBUF1	0x03F9E	R	Serial interface 1 reception data buffer	XII-23
	TXBUF1	0x03F9F	R/W	Serial interface 1 transmission data buffer	XII-23
	SC1SEL	0x03FA0	R/W	Serial 1 I/O pin switching control register 3	XII-18
	P0ODC	0x03EF0	R/W	Port 0 Nch open-drain control register	IV-12
	P0DIR	0x03F30	R/W	Port 0 direction control register	IV-10
	P0PLUD	0x03F40	R/W	Port 0 pull-up/pull-down resistor control register	IV-10
	P7ODC	0x03EF5	R/W	Port 7 Nch open-drain control register	IV-109
	P7DIR	0x03F37	R/W	Port 7 direction control register	IV-108
	P7PLUD	0x03F47	R/W	Port 7 pull-up/pull-down resistor control register	IV-108
	PERIICR	0x03FFE	R/W	Peripheral function group interrupt control register	III-41
	SC1TICR	0x03FF8	R/W	Serial 1 UART transmission interrupt control register	III-35
Serial 2	SC2MD0	0x03FA1	R/W	Serial interface 2 mode register 0	XII-24
	SC2MD1	0x03FA2	R/W	Serial interface 2 mode register 1	XII-25
	SC2MD2	0x03FA3	R/W	Serial interface 2 mode register 2	XII-27
	SC2MD3	0x03FA4	R/W	Serial interface 2 mode register 3	XII-28
	SC2STR	0x03FA5	R	Serial interface 2 status register	XII-29
	RXBUF2	0x03FA6	R	Serial interface 2 reception data buffer	XII-23
	TXBUF2	0x03FA7	R/W	Serial interface 2 transmission data buffer	XII-23
	SC2SEL	0x03FBF	R/W	Serial 2 I/O pin switching control register	XII-19
	P7ODC	0x03EF5	R/W	Port 7 Nch open-drain control register	IV-109
	P7DIR	0x03F37	R/W	Port 7 direction control register	IV-108
	P7PLUD	0x03F47	R/W	Port 7 pull-up/pull-down resistor control register	IV-108
	P3ODC	0x03EF1	R/W	Port 3 Nch open-drain control register	IV-53
	P3DIR	0x03F33	R/W	Port 3 direction control register	IV-52
	P3PLUD	0x03F43	R/W	Port 3 pull-up/pull-down resistor control register	IV-52
	SC2RICR	0x03FF9	R/W	Serial 2 UART reception interrupt control register	III-36
	SC2TICR	0x03FFA	R/W	Serial 2 UART transmission interrupt control register	III-37

	Register	Address	R/W	Function	Page
Serial 3	SC3MD0	0x03FA9	R/W	Serial interface 3 mode register 0	XII-24
	SC3MD1	0x03FAA	R/W	Serial interface 3 mode register 1	XII-25
	SC3MD2	0x03FAB	R/W	Serial interface 3 mode register 2	XII-27
	SC3MD3	0x03FAC	R/W	Serial interface 3 mode register 3	XII-28
	SC3STR	0x03FAD	R	Serial interface 3 status register	XII-29
	RXBUF3	0x03FAE	R	Serial interface 3 reception data buffer	XII-23
	TXBUF3	0x03FAF	R/W	Serial interface 3 transmission data buffer	XII-23
	SC3SEL	0x03F98	R/W	Serial 3 I/O pin switching control register	XII-20
	P0ODC	0x03EF0	R/W	Port 0 Nch open-drain control register	IV-12
	P0DIR	0x03F30	R/W	Port 0 direction control register	IV-10
	P0PLUD	0x03F40	R/W	Port 0 pull-up/pull-down resistor control register	IV-10
	P40DC	0x03EF2	R/W	Port 4 Nch open-drain control register	IV-67
	P4DIR	0x03F34	R/W	Port 4 direction control register	IV-66
	P4PLUD	0x03F44	R/W	Port 4 pull-up/pull-down resistor control register	IV-66
	PERIICR	0x03FFE	R/W	Peripheral function group interrupt control register	III-41
	SC3TICR	0x03FFB	R/W	Serial 3 UART transmission interrupt control register	III-38
Serial 4	SC4MD0	0x03FB0	R/W	Serial interface 4 mode register 0	XII-31
	SC4MD1	0x03FB1	R/W	Serial interface 4 mode register 1	XII-32
	SC4MD2	0x03FB2	R/W	Serial interface 4 mode register 2	XII-33
	SC4MD3	0x03FB3	R/W	Serial interface 4 mode register 3	XII-34
	SC4AD0	0x03FB4	R/W	Serial interface 4 address set register 0	XII-35
	SC4STR0	0x03FB6	R/W	Serial interface 4 status register 0	XII-36
	SC4STR1	0x03FB7	R/W	Serial interface 4 status register 1	XII-37
	RXBUF4	0x03FB8	R	Serial interface 4 reception data buffer	XII-30
	TXBUF4	0x03FB9	R/W	Serial interface 4 transmission data buffer	XII-30
	SC4SEL	0x03FA8	R/W	Serial 4 I/O pin switching control register	XII-21
	P6DIR	0x03F36	R/W	Port 6 direction control register	IV-93
	P3DIR	0x03F33	R/W	Port 3 direction control register	IV-52
	SC4ICR	0x03FFC	R/W	Serial 4 interrupt control register	III-39

	Register	Address	R/W	Function	Page
Serial 5	SC5AD0	0x03FBA	R/W	Serial interface 5 address set register 0	XII-40
	SC5AD1	0x03FBB	R/W	Serial interface 5 address set register 1	XII-40
	SC5RXB	0x03FBC	R	Serial interface 5 reception data buffer	XII-39
	SC5TXB	0x03FBD	R/W	Serial interface 5 transmission data buffer	XII-39
	SC5STR	0x03FBE	R	Serial interface 5 status register	XII-41
	SC5SEL	0x03FC6	R/W	Serial 5 I/O pin switching control register	XII-22
	P7ODC	0x03EF5	R/W	Port 7 Nch open-drain control register	IV-109
	P7DIR	0x03F37	R/W	Port 7 direction control register	IV-108
	P7PLUD	0x03F47	R/W	Port 7 pull-up/pull-down resistor control register	IV-108
	P7OUT	0x03F17	R/W	Port 7 output register	IV-107
	P4ODC	0x03EF2	R/W	Port 4 Nch open-drain control register	IV-67
	P4DIR	0x03F34	R/W	Port 4 direction control register	IV-66
	P4PLUD	0x03F44	R/W	Port 4 pull-up/pull-down resistor control register	IV-66
	P4OUT	0x03F11	R/W	Port 4 output register	IV-65
	PERIICR	0x03FFE	R/W	Peripheral function group interrupt control register	III-41

> If changing the setting value of mode registers, execute rewriting after setting the serial forced reset (set both SCnSBIS flag and SCnSBOS flag of SCnMD1 to "0") (n = 0 to 3).

> If changing the setting value of mode register (except for SC4STE flag, SC4STPC flag, SC4REX flag and SC4ACK0 flag) and address setting registers, execute rewriting after setting the serial forced reset (set both SC4SBIS flag and SC4SBOS flag of the SC4MD1 to "0").

12.2.2 Serial I/O Pin Switching Control Registers 0-5

Pins are commonly used in serial interfaces 0 to 5.

The SCnSEL registers are used for switching pins.

■ Serial 0 I/O Pin Switching Control Register (SC0SEL:0x03F90)

bp	7	6	5	4	3	2	1	0
Flag	SBO0SEL	SC0BRP2	SC0BRP1	SC0BRP0	OSL0	SC0SEL2	SC0SEL1	SC0SEL0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SBO0SEL	UART reverse output selection 0: UART output 1: UART reverse output
6-4	SC0BRP2-0	Timer clock output selection XX0: Timer output 001: Timer output/2 011: Timer output/4 101: Timer output/8 111: Timer output/16
3	OSL0	Serial output port selection 0: System A 1: System B
2-0	SC0SEL2-0	Timer selection X00: Timer 0 X01: Timer 1 010: Timer 2 011: Timer 3 110: Timer 4 111: Timer A

■ Serial 1 I/O Pin Switching Control Register (SC1SEL:0x03FA0)

bp	7	6	5	4	3	2	1	0
Flag	SBO1SEL	SC1BRP2	SC1BRP1	SC1BRP0	OSL1	SC1SEL2	SC1SEL1	SC1SEL0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SBO1SEL	UART reverse output selection 0: UART output 1: UART reverse output
6-4	SC1BRP2-0	Timer clock output selection XX0: Timer output 001: Timer output/2 011: Timer output/4 101: Timer output/8 111: Timer output/16
3	OSL1	Serial output port selection 0: System A 1: System B
2-0	SC1SEL2-0	Timer selection X00: Timer 0 X01: Timer 1 010: Timer 2 011: Timer 3 110: Timer 4 111: Timer A

■ Serial 2 I/O Pin Switching Control Register (SC2SEL:0x03FBF)

bp	7	6	5	4	3	2	1	0
Flag	SBO2SEL	SC2BRP2	SC2BRP1	SC2BRP0	OSL2	SC2SEL2	SC2SEL1	SC2SEL0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SBO2SEL	UART reverse output selection 0: UART output 1: UART reverse output
6-4	SC2BRP2-0	Timer clock output selection XX0: Timer output 001: Timer output/2 011: Timer output/4 101: Timer output/8 111: Timer output/16
3	OSL2	Serial output port selection 0: System A 1: System B
2-0	SC2SEL2-0	Timer selection X00: Timer 0 X01: Timer 1 010: Timer 2 011: Timer 3 110: Timer 4 111: Timer A

■ Serial 3 I/O Pin Switching Control Register (SC3SEL:0x03F98)

bp	7	6	5	4	3	2	1	0
Flag	SBO3SEL	SC3BRP2	SC3BRP1	SC3BRP0	OSL3	SC3SEL2	SC3SEL1	SC3SEL0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SBO3SEL	UART reverse output selection 0: UART output 1: UART reverse output
6-4	SC3BRP2-0	Timer clock output selection XX0: Timer output 001: Timer output/2 011: Timer output/4 101: Timer output/8 111: Timer output/16
3	OSL3	Serial output port selection 0: System A 1: System B
2-0	SC3SEL2-0	Timer selection X00: Timer 0 X01: Timer 1 010: Timer 2 011: Timer 3 110: Timer 4 111: Timer A

■ Serial 4 I/O Pin Switching Control Register (SC4SEL:0x03FA8)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	SC4BRP2	SC4BRP1	SC4BRP0	OSL4	SC4SEL2	SC4SEL1	SC4SEL0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set "0". *
6-4	SC4BRP2-0	Timer clock output selection XX0: Timer output 001: Timer output/2 011: Timer output/4 101: Timer output/8 111: Timer output/16
3	OSL4	Serial output port selection 0: System A 1: System B
2-0	SC4SEL2-0	Timer selection X00: Timer 0 X01: Timer 1 010: Timer 2 011: Timer 3 110: Timer 4 111: Timer A

Always set "0" to the bp denoted by *.

■ Serial 5 I/O Pin Switching Control Register (SC5SEL:0x03FC6)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	OSL5	Reserved	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	Reserved	Always set "0". *
3	OSL5	Serial output port selection 0: System A 1: System B
2-0	Reserved	Always set "0". *

Always set "0" to the bp denoted by *.

12.2.3   Serial Interface 0, 1, 2 and 3 Control Registers

Serial interfaces 0 to 3 can be used for clock synchronous and UART (duplex) communication.

Each serial interface is composed of 2 buffers and 5 registers.

- Serial interface n reception data buffer (RXBUFn)

- Serial interface n transmission data buffer (TXBUFn)

- Serial interface n mode register 0 (SCnMD0)

- Serial interface n mode register 1 (SCnMD1)

- Serial interface n mode register 2 (SCnMD2)

- Serial interface n mode register 3 (SCnMD3)

- Serial interface n status register (SCnSTR)

"n" = 0, 1, 2 and 3 for serial interfaces 0, 1, 2 and 3 respectively in section 12.2.3 Serial Interface 0, 1, 2 and 3 Control Register.

■ Serial Interface n Reception Data Buffer (RXBUF0:0x03F96, RXBUF1:0x03F9E, RXBUF2:0x03FA6, RXBUF3:0x03FAE)

bp	7	6	5	4	3	2	1	0
Flag	RXBUFn7	RXBUFn6	RXBUFn5	RXBUFn4	RXBUFn3	RXBUFn2	RXBUFn1	RXBUFn0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Serial Interface n Transmission Data Buffer (TXBUF0:0x03F97, TXBUF1:0x03F9F, TXBUF2:0x03FA7, TXBUF3:0x03FAF)

bp	7	6	5	4	3	2	1	0
Flag	TXBUFn7	TXBUFn6	TXBUFn5	TXBUFn4	TXBUFn3	TXBUFn2	TXBUFn1	TXBUFn0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Serial Interface n Mode Register 0 (SC0MD0:0x03F91, SC1MD0:0x03F99, SC2MD0:0x03FA1, SC3MD0:0x03FA9)

bp	7	6	5	4	3	2	1	0
Flag	SCnCE1	-	-	SCnDIR	SCnSTE	SCnLNG2	SCnLNG1	SCnLNG0
At reset	0	-	-	0	0	1	1	1
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SCnCE1	Transmission data output edge 0: Falling 1: Rising Reception data input edge 0: Rising 1: Falling
6-5	-	-
4	SCnDIR	Transfer bit specification 0: MSB first 1: LSB first
3	SCnSTE	Start condition selection 0: Disable start condition 1: Enable start condition
2-0	SCnLNG2-0	Synchronous serial transfer bit count 000: 1bit 001: 2bit 010: 3bit 011: 4bit 100: 5bit 101: 6bit 110: 7bit 111: 8bit

■ Serial Interface n Mode Register 1 (SC0MD1:0x03F92, SC1MD1:0x03F9A, SC2MD1:0x03FA2, SC3MD1:0x03FAA)

bp	7	6	5	4	3	2	1	0
Flag	SCnIOM	SCnSBTS	SCnSBIS	SCnSBOS	SCnCKM	SCnMST	SCnDIV	SCnCMD
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SCnIOM	Serial data input pin selection 0: Data input from SBIn (RXDn) 1: Data input from SBOn (TXDn)
6	SCnSBTS	SBTn pin function selection 0: Port 1: Serial clock I/O
5	SCnSBIS	Serial data input control selection 0: "1" input 1: Serial data input
4	SCnSBOS	SBOn (TXDn) pin function selection 0: Port 1: Serial data output
3	SCnCKM	Transfer clock divide selection 0: Not divided 1: Divided
2	SCnMST	Clock master/salve selection 0: Clock slave 1: Clock master
1	SCnDIV	Transfer clock divide selection 0: Divided by 8 1: Divided by 16
0	SCnCMD	Synchronous serial/duplex UART selection 0: Synchronous serial 1: Duplex UART

If selecting the external clock (clock slave), set the internal clock that has the same or lower clock cycle to the external clock.

When set both bp5 of SCnSBIS flag and bp4 of SCnSBOS flag to "0", the serial forced reset is set and serial function is stopped.

If setting the communication state of this serial interface to "UART", set the mode register (SCnMD1) to the serial interface mode with "H" level of the serial data input pin.

If changing the setting value of mode registers, execute rewriting after setting the serial forced reset (set both SCnSBIS flag and SCnSBOS flag of SCnMD1 to "0") (n = 0 to 3).

■ Serial Interface n Mode Register 2 (SC0MD2:0x03F93, SC1MD2:0x03F9B, SC2MD2:0x03FA3, SC3MD2:0x03FAB)

bp	7	6	5	4	3	2	1	0
Flag	SCnFM1	SCnFM0	SCnPM1	SCnPM0	SCnNPE	-	SCnBRKF	SCnBRKE
At reset	0	0	0	0	0	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	-	R	R/W

bp	Flag	Description
7-6	SCnFM1-0	Frame mode specification 00: Data 7 bits + stop 1 bit 01: Data 7 bits + stop 2 bits 10: Data 8 bits + stop 1 bit 11: Data 8 bits + stop 2 bits
5-4	SCnPM1-0	Additional bit specification At transmission At reception 00: Add "0" Check for "0" 01: Add "1" Check for "1" 10: Add odd parity Check for odd parity 11: Add even parity Check for even parity
3	SCnNPE	Parity enable 0: Enable parity bit 1: Disable parity bit
2	-	-
1	SCnBRKF	Break status receive monitor 0: Data reception 1: Break reception
0	SCnBRKE	Break status transmit control 0: Data transmission 1: Break transmission

■ Serial Interface n Mode Register 3 (SC0MD3:0x03F94, SC1MD3:0x03F9C, SC2MD3:0x03FA4, SC3MD3:0x03FAC)

bp	7	6	5	4	3	2	1	0
Flag	SCnFDC1	SCnFDC0	-	-	SCnPSCE	SCnPSC2	SCnPSC1	SCnPSC0
At reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SCnFDC1-0	Output selection after SBO final data transmit 00: Fix at "1" (High) output 10: Fix at "0" (Low) output 01: Final data hold 11: Prohibited
5-4	-	-
3	SCnPSCE	Prescaler count control 0: Disable count 1: Enable count
2-0	SCnPSC2-0	Selection clock 000:fpll/2 001:fpll/4 010:fpll/16 011:fpll/64 100:fs/2 101:fs/4 11X:Timer output * Timers 0 to 4 and A can be selected by the SCnSEL2-0 flag of SCnSEL register

If selecting the external clock (clock slave), set the internal clock that has the same or lower clock cycle to the external clock.

■ Serial Interface n Status Register (SC0STR:0x03F95, SC1STR:0x03F9D, SC2STR:0x03FA5, SC3STR:0x03FAD)

bp	7	6	5	4	3	2	1	0
Flag	SCnTBSY	SCnRBSY	SCnTEMP	SCnREMP	SCnFEF	SCnPEK	SCnORE	SCnERE
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7	SCnTBSY	Serial bus status 0:Other use 1:Serial transmission in progress
6	SCnRBSY	Serial bus status 0:Other use 1:Serial reception in progress
5	SCnTEMP	Transmission buffer empty flag 0:Empty 1:Full
4	SCnREMP	Reception buffer empty flag 0:Empty 1:Full
3	SCnFEF	Frame error detection 0:No error 1:Error
2	SCnPEK	Parity error detection 0:No error 1:Error
1	SCnORE	Overrun error detection 0:No error 1:Error
0	SCnERE	Error monitor flag 0:No error 1:Error

12.2.4   Serial Interface 4 Control Registers

Serial interfaces 4 can be used for clock synchronous and multi master IIC communication.

This serial interface is composed of 2 buffers and 8 registers.

- Serial interface 4 reception data buffer (RXBUF4)

- Serial interface 4 transmission data buffer (TXBUF4)

- Serial interface 4 mode register 0 (SC4MD0)

- Serial interface 4 mode register 1 (SC4MD1)

- Serial interface 4 mode register 2 (SC4MD2)

- Serial interface 4 mode register 3 (SC4MD3)

- Serial interface 4 address set register 0 (SC4AD0)

- Serial interface 4 address set register 1 (SC4AD1)

- Serial interface 4 status register 0 (SC4STR0)

- Serial interface 4 status register 1 (SC4STR1)

■   Serial Interface 4 Reception Data Buffer (RXBUF4:0x03FB8)

bp	7	6	5	4	3	2	1	0
Flag	RXBUF47	RXBUF46	RXBUF45	RXBUF44	RXBUF43	RXBUF42	RXBUF41	RXBUF40
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■   Serial Interface 4 Transmission Data Buffer (TXBUF4:0x03FB9)

bp	7	6	5	4	3	2	1	0
Flag	TXBUF47	TXBUF46	TXBUF45	TXBUF44	TXBUF43	TXBUF42	TXBUF41	TXBUF40
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2.5   Serial Interface 4 Mode Register

■ Serial Interface 4 Mode Register 0 (SC4MD0:0x03FB0)

bp	7	6	5	4	3	2	1	0
Flag	SC4CE1	-	-	SC4DIR	SC4STE	SC4LNG2	SC4LNG1	SC4LNG0
At reset	0	-	-	0	0	1	1	1
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SC4CE1	Transmission data output edge 0: Falling 1: Rising Reception data input edge 0: Rising 1: Falling
6-5	-	-
4	SC4DIR	Transfer bit specification 0: MSB first 1: LSB first
3	SC4STE	Start condition selection 0: Disable start condition 1: Enable start condition
2-0	SC4LNG2-0	Transfer bit count 000: 1bit 001: 2bit 010: 3bit 011: 4bit 100: 5bit 101: 6bit 110: 7bit 111: 8bit

■ Serial Interface 4 Mode Register 1 (SC4MD1:0x03FB1)

bp	7	6	5	4	3	2	1	0
Flag	SC4IOM	SC4SBTS	SC4SBIS	SC4SBOS	-	SC4MST	-	-
At reset	0	0	0	0	-	0	-	-
Access	R/W	R/W	R/W	R/W	-	R/W	-	-

bp	Flag	Description
7	SC4IOM	Serial data input pin selection 0: Data input form SBI4 1: Data input from SBO4 (SDA4)
6	SC4SBTS	SBT4 pin function selection 0: Port 1: Transfer clock I/O
5	SC4SBIS	Serial input control selection 0: "1" input 1: Serial input
4	SC4SBOS	SBO4 (SDA4) pin function selection 0: Port 1: Serial data output
3	-	-
2	SC4MST	Clock master/salve selection 0: Clock slave 1: Clock master
1-0	-	-

> If changing the setting value of mode register (except for SC4STE flag, SC4STPC flag, SC4REX flag and SC4ACK0 flag) and address setting registers, execute rewriting after setting the serial forced reset (set both SC4SBIS flag and SC4SBOS flag of the SC4MD1 to "0").

■ Serial Interface 4 Mode Register 2 (SC4MD2:0x03FB2)

bp	7	6	5	4	3	2	1	0
Flag	SC4FDC1	SC4FDC0	-	-	SC4PSCE	SC4PSC2	SC4PSC1	SC4PSC0
At reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SC4FDC1-0	Output selection after SBO4 final data transmit 00: Fix at "1" (High) output 01: Final data hold 10: Fix at "0" (Low) output 11: Prohibited
5-4	-	-
3	SC4PSCE	Prescaler count control 0: Disable count 1: Enable count
2-0	SC4PSC2-0	Selection clock 000: fpll/2 001: fpll/4 010: fpll/16 011: fpll/32 100: fs/2 101: fs/4 11X:Timer output *Timers 0 to 4 and A can be selected by the SC4SEL2-0 flag of SC4SEL register

■ Serial Interface 4 Mode Register 3 (SC4MD3:0x03FB3)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	SC4STPC	SC4TMD	SC4REX	SC4CMD	SC4ACKS	SC4ACKO
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description	
7-6	Reserved	Always set to "0". *	
5	SC4STPC	Stop condition generation request flag in IIC communication *1 0: Not generated 1: Generated	
4	SC4TMD	Communication mode selection in IIC communication 0: Standard mode 1: High-speed mode	
3	SC4REX	Transmission/reception mode selection in IIC master communication 0: Transmission 1: Reception	
2	SC4CMD	Synchronous serial/IIC selection 0: Synchronous serial 1: IIC	
1	SC4ACKS	ACK bit enable 0: Disable 1: Enable	
0	SC4ACKO	At transmission mode (SC4REX=0) ACK bit detection flag 0: ACK detection 1: NACK detection	At reception mode (SC4REX=1) ACK bit level specification *2 0: ACK transmission 1: NACK transmission

---

(!) *1: Cannot Write "0"; can write "1" only.
Cannot write at serial forced reset (when the SC4SBOS flag and SC4CSBIS flag of the
SC4MD1 register are "0").
*2: Cannot read the SC4ACKO value at reception mode (SC4REX=1).

(!) Set the setting data to the serial interface 4 mode register 3 by Mov instruction once, not by
BSET/BCLR control. After read the data from the serial interface 4 mode register 3,change
the specific bit and write the data to the register. These operations is prohibiting. SC4ACKO
data will be destroyed.

(!) Always set "0" to the bp denoted by asterisk.

12.2.6   Serial Interface 4 Address Set Register

Serial interface 4 has 7 bits of the address set registers.

■   Serial Interface 4 Address Set Register 0 (SC4AD0:0x03FB4)

bp	7	6	5	4	3	2	1	0
Flag	SC4AD7	SC4AD6	SC4AD5	SC4AD4	SC4AD3	SC4AD2	SC4AD1	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Do not word access to SC4AD0 register.

12.2.7   Serial Interface 4 Status Register

■ Serial Interface 4 Status Register 0 (SC4STR0:0x03FB6)

bp	7	6	5	4	3	2	1	0
Flag	SC4BSY	-	SC4TEMP	SC4REMP	-	-	-	SC4ORE
At reset	0	-	0	0	-	-	-	0
Access	R	-	R	R	-	-	-	R/W

bp	Flag	Description
7	SC4BSY	Clock synchronous communication serial bus status 0:Other use 1:Serial transmission in progress
6	-	-
5	SC4TEMP	Transmission buffer empty flag 0: Empty 1: Full
4	SC4REMP	Reception buffer empty flag 0: Empty 1: Full
3-1	-	-
0	SC4ORE	Overrun error detection 0:No error 1:Error

■ Serial Interface 4 Status Register 1 (SC4STR1:0x03FB7)

bp	7	6	5	4	3	2	1	0
Flag	SC4WRS	SC4ABT_ LST	SC4ADD_ ACC	SC4STRT	SC4BUS BSY	SC4IICBSY	SC4GCALL	SC4DATA_ ERR
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R	R	R	R	R	R/W

bp	Flag	Description
7	SC4WRS	Data transfer direction determine flag in slave communication 0: Master→slave 1: Slave→master
6	SC4ABT_LST	Arbitration lost detection flag 0: Not detected 1: Detected
5	SC4ADD_ACC	Slave address compare flag 0: Address unmatched 1: Address matched
4	SC4STRT	Start condition detection flag 0: Not detected 1: Detected
3	SC4BUSBSY	Bus busy flag 0: Bus free status 1: Bus busy status
2	SC4IICBSY	Serial bus status in IIC communication 0: Other use 1: Serial transmission is in progress
1	SC4GCALL	General call detection flag 0: Not detected 1: Detected
0	SC4DATA_ER R	Communication abnormal detection flag 0: Not detected 1: Detected

SC4ABT_LST flag can not write "1", can write "0" only.

12.2.8　Serial Interface 5 Control Register

Serial interfaces 5 can be used for IIC (slave).

This serial interface is composed of 2 buffers and 3 registers.

- Serial interface 5 address set register 0 (SC5AD0)

- Serial interface 5 address set register 1 (SC5AD1)

- Serial interface 5 transmission data buffer (SC5TXB)

- Serial interface 5 reception data buffer (SC5RXB)

- Serial interface 5 status register (SC5STR)

12.2.9   Serial Interface 5 Data Buffer Register

Serial interface 5 has each of 8-bit data buffer register for transmission/reception

■ Serial Interface 5 Reception Data Buffer (SC5RXB:0x03FBC)

bp	7	6	5	4	3	2	1	0
Flag	I2CRXB7	I2CRXB6	I2CRXB5	I2CRXB4	I2CRXB3	I2CRXB2	I2CRXB1	I2CRXB0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	I2CRXB7-0	Serial interface 5 reception data buffer

■ Serial Interface 5 Transmission Data Buffer (SC5TXB:0x03FBD)

bp	7	6	5	4	3	2	1	0
Flag	I2CTXB7	I2CTXB6	I2CTXB5	I2CTXB4	I2CTXB3	I2CTXB2	I2CTXB1	I2CTXB0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-0	I2CTXB7-0	Serial interface 5 transmission data buffer

12.2.10 Serial Interface 5 Mode Register

■ Serial Interface 5 Address Set Register 0 (SC5AD0:0x03FBA)

bp	7	6	5	4	3	2	1	0
Flag	I2CAD7	I2CAD6	I2CAD5	I2CAD4	I2CAD3	I2CAD2	I2CAD1	I2CAD0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-0	I2CAD7-0	Serial interface 5 address set register

■ Serial Interface 5 Address Set Register 1(SC5AD1:0x03FBB)

bp	7	6	5	4	3	2	1	0
Flag	SELI2C	I2CMON	-	-	I2CGEM	I2CADM	I2CAD9	I2CAD8
At reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SELI2C	Reset control 0: Reset status 1: Operation status
6	I2CMON	Monitor mode selection 0: Communication mode 1: Monitor mode
5-4	-	-
3	I2CGEM	Communication mode selection 0: Standard communication mode 1: General call communication mode
2	I2CADM	Address mode selection 0: 7-bit address mode 1: 10-bit address mode
1-0	I2CAD9-8	Address setting

■ Serial interface 5 Status Register (SC5STR:0x03FBE)

bp	7	6	5	4	3	2	1	0
Flag	WRS	I2CINT	STRT	RSTRT	I2CBSY	SLVBSY	ACKVALID	-
At reset	1	0	0	0	0	0	0	-
Access	R	R	R	R	R	R	R	-

bp	Flag	Description
7	WRS	Data transfer direction determination flag 0: Slave→Master 1: Master→Slave
6	I2CINT	Interrupt detection flag 0: Undetected 1: Detected
5	STRT	Start condition detection flag 0: Undetected 1: Detected
4	RSTRT	Retart condition detection flag 0: Undetected 1: detected
3	I2CBSY	Bus busy flag 0: Bus free status 1: Bus busy status
2	SLVBSY	Slave busy flag 0: Other use 1: Data transnission is in progress
1	ACKVALID	ACK detection flag 0: Undetected 1: Detected
0	-	-

12.3 Clock Synchronous Serial Interface

12.3.1 Operation

This section describes the clock synchronous communication method of serial interfaces 0 to 4.

"n"= 0 to 4 for serial interfaces 0 to 4 respectively in section 12.3.1 Operation.

■ Communication Type

The communication mode can be selected from 3-channel type (clock pin (SBTn pin), data output pin (SBOn pin), data input pin (SBIn pin)) or 2-channel type (clock pin (SBTn pin), data I/O (SBOn pin)). Set the communication mode by the SCnIOM flag of the SCnMD1 register. In 2-channel reception, select "serial data input " by setting the SCnSBIS flag of the SCnMD1 register to "1". The SBIn pin can be used as a general port.

■ Activation Factor for Communication

Table:12.3.1 shows activation factors for communication. In master communication, the transfer clock is generated by communication activation factors. In slave communication, except during communication, the signal input from SBTn pin is masked in serial interface to prevent errors by noise or so; thus, input an external clock after releasing the mask by communication activation factors.

In addition, if "set transmission data" or "set dummy data" for communication activation factors, input the external clock after more than 3.5 transfer clock interval after the data set to TXBUFn. This wait time is needed to load the data from TXBUFn to the internal shift register.

Table:12.3.1 Synchronous Serial Interface Activation Factors

	Activation factors	
	Transmission	Reception
Master communication	Set transmission data	Set dummy data
		Input start condition
Slave communication	Input clock after transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

Except during communication, SBTn pin is masked in serial interface to prevent errors by noise. In slave communication, set data to TXBUFn or input a clock to the SBTn pin after a start condition is input.

To communicate properly, more than 3.5 transfer clock after the data set to TXBUFn is needed to input the external clock.

■   Transfer Bit Setup

The transfer bit count is selected from 1 to 8 bits. Set it by the SCnLNG2 to 0 flags of the SCnMD0 register (at reset: 111). The SCnLNG2 to 0 flags hold the former set values until they are set again.

■   Start Condition Setup

The SCnSTE flag of the SCnMD0 register sets whether a start condition is enabled or disabled. When the data (SBIn (3 channels) or SBOn (2 channels)) pin changes from "H" to "L" during the clock (SBTn) pin = "H", setting the SCnCE1 flag of SCnMD0 register to "0" allows a start condition to be recognized. When the data (SBIn (3 channels) or SBOn pin (2 channels)) pin changes from "H" to "L" during the clock (SBTn) pin = "L", setting the SCnCE1 flag to "1" allows a start condition to be recognized. Set the SCnSBOS flag and the SCnSBIS flag of the SCnMD1 register to "0" respectively to change the start condition enable/disable setting. When operating transmission and reception at the same time, select "start condition disable"; otherwise, it may cause improper operations.

■   First Transfer Bit Setup

Either MSB first or LSB first at transfer can be selected. Set the first bit by the SCnDIR flag of the SCnMD0 register.

■   Transmission Data Buffer

The transmission data buffer TXBUFn is a reserved buffer that stores data to be loaded into the internal shift register. Set data to be transmitted in the transmission data buffer TXBUFn. The data is loaded into the internal shift register automatically. The data loading period of 3 transfer clocks is needed for loading data. In data loading period, setting another data in TXBUFn may cause an error. Whether during data loading period or not is determined by monitoring the transmission buffer empty flag SCnTEMP of SCnSTR. When data is set in TXBUFn, the SCnTEMP flag is set to "1" and loading is finished; when communication is restarted, the SCnTEMP flag is cleared to "0" automatically.
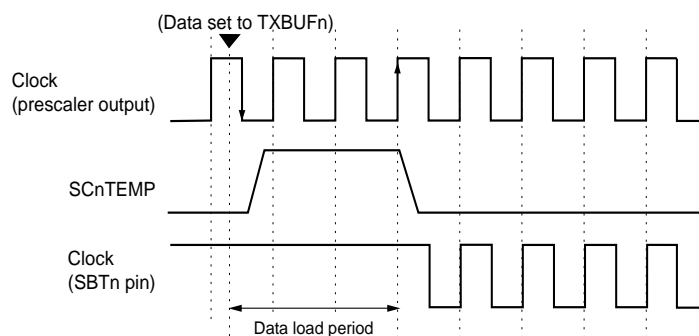
Figure:12.3.1 Transmission Data Buffer

■ Reception Data Buffer

The reception data buffer RXBUFn of serial interfaces 0, 1, 3 and 4 are reserved buffers that push the data received by the internal shift register. After the communication complete interrupts SCnTIRQ is generated, data in the internal shift register are automatically stored in the reception data buffers RXBUFn. RXBUFn can store data up to 1 byte. Read data of RXBUFn before the next reception is completed since RXBUFn is rewritten every time when communication is completed. The reception data buffer empty flags SCnREMP is set to "1" after SCn-TIRQ is generated. SCnREMP is cleared to "0" when reading RXBUFn.

If a start condition is input to restart during communication, the transmission data is invalid. Set the transmission data in TXBUFn again to restart communication.

RXBUFn is rewritten every time when communication is completed. In continuous communication, read data of RXBUFn before the next reception is completed.

■ Transmit Bit Count and First Transfer Bit

In transmission, when the transfer bit is 1 bit to 7 bits, the data storing method to the transmission data buffer differs depending on the first transfer bit specification. At MSB first, store data in the upper bits of TXBUFn. When there are 6 bits to be transferred, if data "A" to "F" are stored in bp2 to bp7 of TXBUFn, they are transferred from "F" to "A", as shown on Figure:12.3.2. At LSB first, store data in the lower bits of TXBUFn. When there are 6 bits to be transferred if data "A" to "F" are stored to bp0 to bp5 of TXBUFn, they are transferred from "A" to "F", as shown on Figure:12.3.3.

	7	6	5	4	3	2	1	0
TXBUFn	F	E	D	C	B	A		
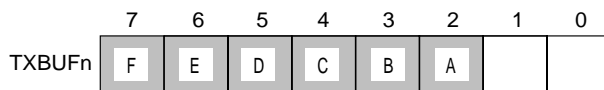
Figure:12.3.2 Transfer Bit Count and First Transfer Bit (At MSB First) 1

	7	6	5	4	3	2	1	0
TXBUFn			F	E	D	C	B	A
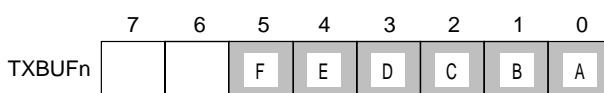
Figure:12.3.3 Transfer Bit Count and First Transfer Bit (At LSB First) 1

■ Receive Bit Count and First Transfer Bit

In reception, when the transfer bit is 1 to 7 bits, the data storing method to the reception data buffer RXBUFn dif-
fers depending on the first transfer bit specification. At MSB first, data are stored in the lower bits of RXBUFn.
When there are 6 bits to be transferred, if data "A" to "F" are stored in bp5 to bp0 of RXBUFn from "A" to "F", as
shown on Figure:12.3.4. At LSB first, data are stored in the upper bits of RXBUFn. When there are 6 bits to be
transferred, as shown on Figure:12.3.5, data "A" to "F" are stored in bp2 to bp7 of RXBUFn from "A" to "F".

Figure:12.3.4 Receive Bit Count and Transfer First Bit (At MSB First)
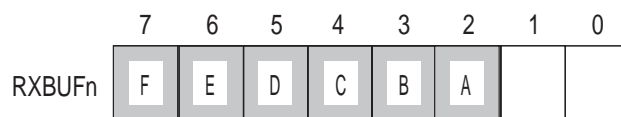
Figure:12.3.5 Receive Bit Count and Transfer First Bit (At LSB First)

When the reception transfer bit is 1 to 7 bits, data except reception data of the specified
transfer bit is indefinite. Mask reception data by and instructions to use.

■ Continuous Mode

This serial interface has a continuous communication function. If data is set in the transmission data buffer
TXBUFn during transmission, the transmission buffer empty flag SCnTEMP is set, and continuous transmission
is operated automatically. Set data in TXBUFn before the communication complete interrupt SCn(T)IRQ is gen-
erated since data is loaded into the internal shift register. Communication blanks, from SCn(T)IRQ generation to
the next transfer clock output, are 4 transfer clocks.

■ Automatic Continuous Transfer by ATC

This serial interface can start up by ATCn, the automatic data transfer function built-in this LSI. When starting by ATCn, data up to 255 byte can be transferred continuously. For the start-up method by ATCn, refer to transfer modes 8 to 9 in Chapter 16 16.1 Automatic Transfer Controller.

> When the slave reception is executed with the start condition "enable" at the continuous communication, the system configuration is needed to notify the master of the read completion. Without the notification, the data before read may be overwritten.

■ Input Edge/Output Edge Setup

An output edge of transmission data and an input edge of reception data can be set by the SCnCE1 flag of the SCnMD0 register. When the SCnCE1 flag = "0", transmission data is output synchronously at the falling edge of the clock; when the SCnCE1 flag = "1", the data is output synchronously at the rising edge. When the SCnCE1 flag = "0", reception data is loaded synchronously at the rising edge of the clock; when the SCnCE1 flag = "1", the data is loaded synchronously at the falling edge.

Table:12.3.2 Transmission Data Output Edge and Reception Data Input Edge

SCnCE1	Transmission data output edge	Reception data input edge
0		
1		

■ Clock Setup

The clock source can set the dedicated prescaler or timer (2 lines) output. Set it by the SCnPSC2 to 0 of the SCnMD3 register. The dedicated prescaler starts to operate when "prescaler operation" is selected by the SCnP-SCE flag of the SCnMD3 register. Either the internal clock (clock master) or the external clock (clock slave) can be selected by the SCnMST flag of the SCnMD1 register. If selecting the external clock, set the internal clock that has the same clock cycle or lower to the external clock by the SCnMD3 register. Table:12.3.3 shows the internal clock source that can be set by the SCnMD3 register.

Table:12.3.3 Synchronous Serial Interface Clock Source

		Serial 0	Serial 1	Serial 2	Serial 3	Serial 4
Clock source (internal clock)	fpll/2	O	O	O	O	O
	fpll/4	O	O	O	O	O
	fpll/8	-	-	-	-	-
	fpll/16	O	O	O	O	O
	fpll/32	-	-	-	-	O
	fpll/64	O	O	O	O	-
	fs/2	O	O	O	O	O
	fs/4	O	O	O	O	O
	Timer 0 output	O	O	O	O	O
	Timer 1 output	O	O	O	O	O
	Timer 2 output	O	O	O	O	O
	Timer 3 output	O	O	O	O	O
	Timer 4 output	O	O	O	O	O
	Timer A output	O	O	O	O	O

The transfer speed should be up to 5.0 MHz. If the transfer clock is over 5.0 MHz, the transfer data may not be sent correctly.

Set the SCnSBIS flag and SC0SBOS flag of the SCnMD1 register to "0" to switch clock setting.

■ Data Input Pin Setup

3-channel type (clock pin (SBTn pin), data output pin (SBOn pin) and data input pin (SBIn pin)) or 2-channel type (clock pin (SBTn pin) and data I/O pin (SBOn pin)) can be selected as communication mode. Set it by the SCnIOM flag of the SCnMDI register. The SBIn pin can be used only for serial data input. The SBOn pin can select whether serial data input or output. Selecting "data input from SBOn pin" sets 2-channel communication; thus, I/O mode selection of the port direction control register controls direction of the SBOn pin to switch transmission/reception because. At this time, the SBIn pin can be used as a general port since it is not used.

> In reception, if SCnIOM of the SCnMD1 register is set to "1" and "serial data input from the SBOn pin" is selected, the SBIn pin can be used as a general port.

■ Reception Buffer Empty Flag

After reception completion (the communication complete interrupt SCnTIRQ, data is automatically stored to RXBUFn from the internal shift register. If data is stored to the shift register RXBUFn when the SCnSBIS flag of the SC0MDn register is set to "serial input", the reception buffer empty flag SCnREMP of the SCnSTR register is set to "1". This indicates that the received data is waiting to be read. SCnREMP is cleared to "0" by reading data of RXBUFn.

■ Transmission Buffer Empty Flag

During communication (till the communication complete interrupt SCnTIRQ is generated since data is loaded into the internal shift register) if data is set in TXBUFn, the transmission buffer empty flag SCnTEMP of the SCnSTR register is set to "1". This indicates that the next transmission is waiting to be loaded. When data is loaded to the internal shift register from TXBUFn after SCnTIRQ is generated and SC0TEMP is cleared to "0", the next transfer starts automatically.

■ Overrun Error and Error Monitor Flag (Serial 0, Serial 1, Serial 2 and Serial 3)

When the next data reception is completed before reading data of the reception data buffer RXBUFn received at previous communication, an overrun error is generated and the SCnORE flag of the SCnSTR is set to "1". At the same time, the error monitor flag SCnERE is set indicating that the reception has an error. The SCnORE flag is cleared after the next communication complete interrupt SCnTIRQ is generated since reading data of the RXBUFn. SCnERE is cleared as the SCnORE flag is cleared. These error flags have no effects on communication operation.

■ Reception BUSY Flag (Serial 0, Serial 1, Serial 2 and Serial 3)

If data is set in RXBUFn or a start condition is recognized when the SCnSBIS flag of the SCnMD1 register is set to "serial data input", the BUSY flag SCnRBSY of the SCnSTR register is set to "1". the SCnRBSY flag is cleared to "0" after the communication complete interrupts SCnTIRQ is generated. During continuous communication, the SCnRBSY flag is held in set. If the transmission buffer empty flags SCnTEMP is cleared to "0" when the communication complete interrupts SCnTIRQ is generated, SCnRBSY is cleared to "0". If the SCnSBIS flag is set to "0" during communication, the SCnRBSY flag is cleared to "0".

■ Transmission BUSY Flag (Serial 0, Serial 1, Serial 2 and Serial 3)

If data is set in TXBUFn or a start condition is recognized when the SCnSBOS flag of the SCnMD1 register is set to "serial data output", the SCnTBSY flag of the SCnSTR register is set. After the communication complete interrupt SCnTIRQ is generated, the flag is cleared to "0". During continuous communication, the SCnTBSY flag is held in set. If the transmission buffer empty flag SCnTEMP is cleared to "0" when the communication complete interrupts SCnTIRQ is generated, SCnTBSY flag is cleared to "0". If the SCnSBOS flag is set to "0" during communication, the SCnTBSY flag is reset to "0".

■ BUSY Flag (Serial 4)

If data is set in TXBUF4, or a start condition is recognized, the SC4BSY flag of the SC4STR0 is set. It is cleared to "0" after the communication complete interrupt SC4IRQ is generated. During continuous communication, the SC4BSY flag is held in set. If the transmission buffer empty flag SC4TEMP is "0" when the communication complete interrupt SC4IRQ is generated, SC4BSY is cleated to "0".

■ Emergency Reset

This serial interface has an emergency reset function for malfunction. The SCnSBOS flag and the SCnSBIS flag of the SCnMD1 register should be set to "0" (SBOn pin function: port, input data: "1" input) to operate an emergency reset.

At emergency reset, the status register (the SCnBRKF flag of the SCnMD2 register, all flags of the SC0STR, SC1STR and SC2STR registers, the bp6 to 0 flags of the SC4STR1 register and bp5 (SC4STPC flag) of the SC4MD3 register) is initialized to the reset value, but the set value of the any other control registers are held.

■ Last Bit of Transmission Data

The following table shows the data output hold period of the last bit at transmission and the required minimum data input period of the last bit at reception. The internal clock should be set at slave to keep the data hold time at transmission.

Table:12.3.4 Last Bit Data Length of Transfer Data

	The last bit data hold period at transmission	The last bit data input period at reception
At master	1 bit data length	1 bit data length (minimum)
At slave	[1 bit data length of external clock $\times$ 1/2] + [internal clock cycle $\times$ (1/2 to 3/2)]	

When the start condition is disabled (SCnSTE flag = 0), SBOn output after the data output hold period of the last bit can be set as indicated in Table:12.3.5 by the set values of the SCnFDC1 to 0 flags of the SCnMD3 register.

After a reset is released, the output before a serial transfer is "H" despite the set value of the SCnFDC1 to 0 flags. When the start condition is enabled (SCnSTE flag = 1), "H" is output despite the set values of the SCnFDC1 to 0 flags.

Table:12.3.5 SBOn Output after the Data Output Hold Period of the Last Bit (Without Start Condition)

SCnFDC1 flag	SCnFDC0 flag	SBO0 output after the last bit data output holding
0	0	"1"(High) output fix
1	0	"0"(Low) output fix
0	1	Last data holding
1	1	Prohibited

■ Other Control Flag Setup (Serial 0, Serial 1, Serial 2 and Serial 3)

The flags shown below are not needed to be set or monitored since they are not used at clock synchronous communication.

Table:12.3.6 Other Control Flags

Serial 0		Serial 1		Serial 2		Serial 3		Detail
Register	Flag	Register	Flag	Register	Flag	Register	Flag	
SC0MD2	SC0BRKE	SC1MD2	SC1BRKE	SC2MD2	SC2BRKE	SC3MD2	SC3BRKE	Break status transmission control
	SC0BRKF		SC1BRKF		SC2BRKF		SC3BRKF	Break status reception monitor
	SC0NPE		SC1NPE		SC2NPE		SC3NPE	Parity enable
	SC0PM 1-0		SC1PM 1-0		SC2PM 1-0		SC3PM 1-0	Additonal bit specification
	SC0FM 1-0		SC1FM 1-0		SC2FM 1-0		SC3FM 1-0	Frame mode specification
SC0STR	SC0PEK	SC1STR	SC1PEK	SC2STR	SC2PEK	SC3STR	SC3PEK	Parity error detection
	SC0FEF		SC1FEF		SC2FEF		SC3FEF	Frame error detection

12.3.2　Timing

■　Transmission Timing
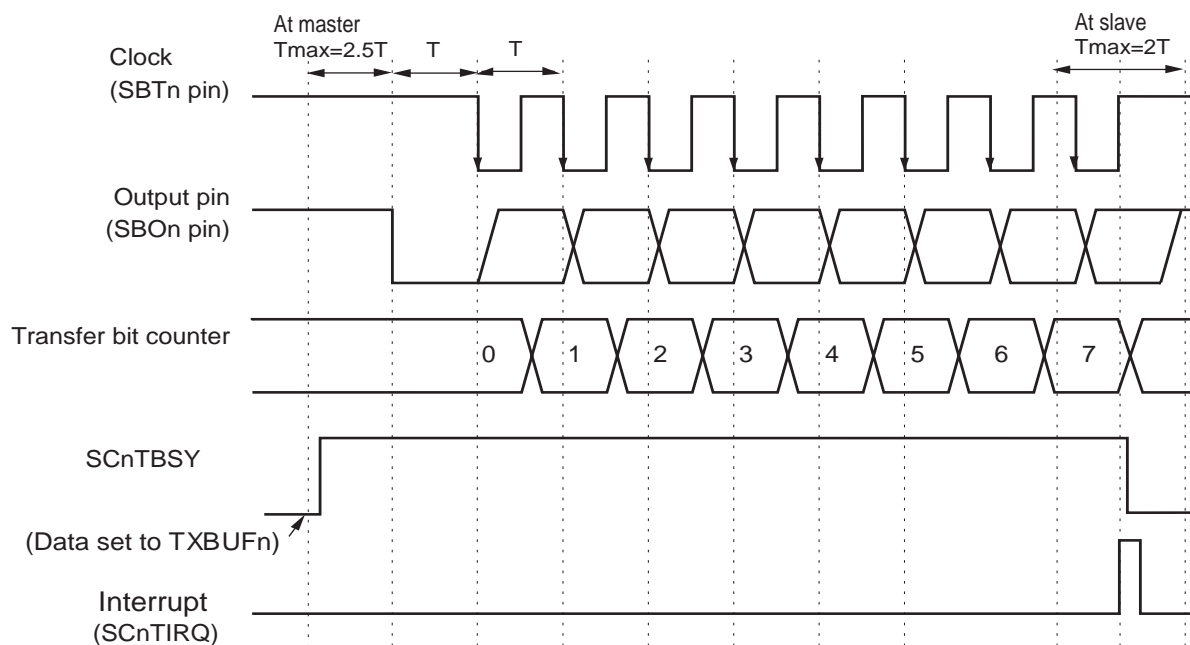
Figure:12.3.6　Transmission Timing (At Falling Edge, Start Condition is Enabled)
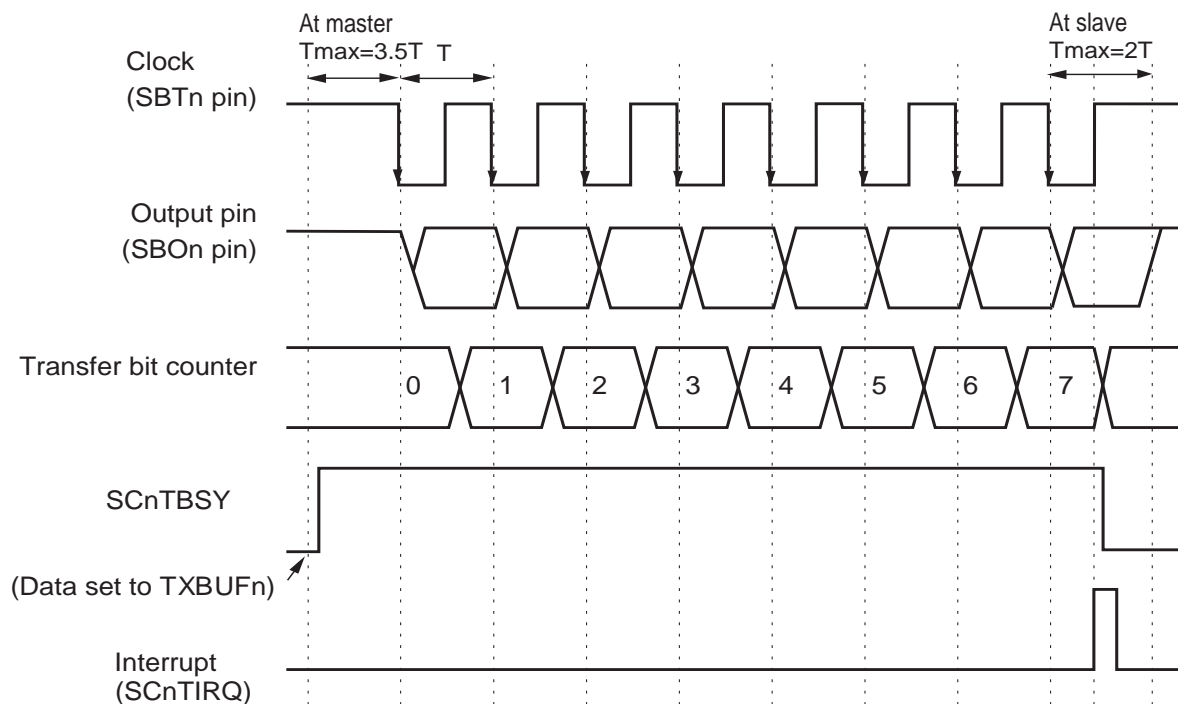
Figure:12.3.7 Transmission Timing (At Falling Edge, Start Condition is Disabled)
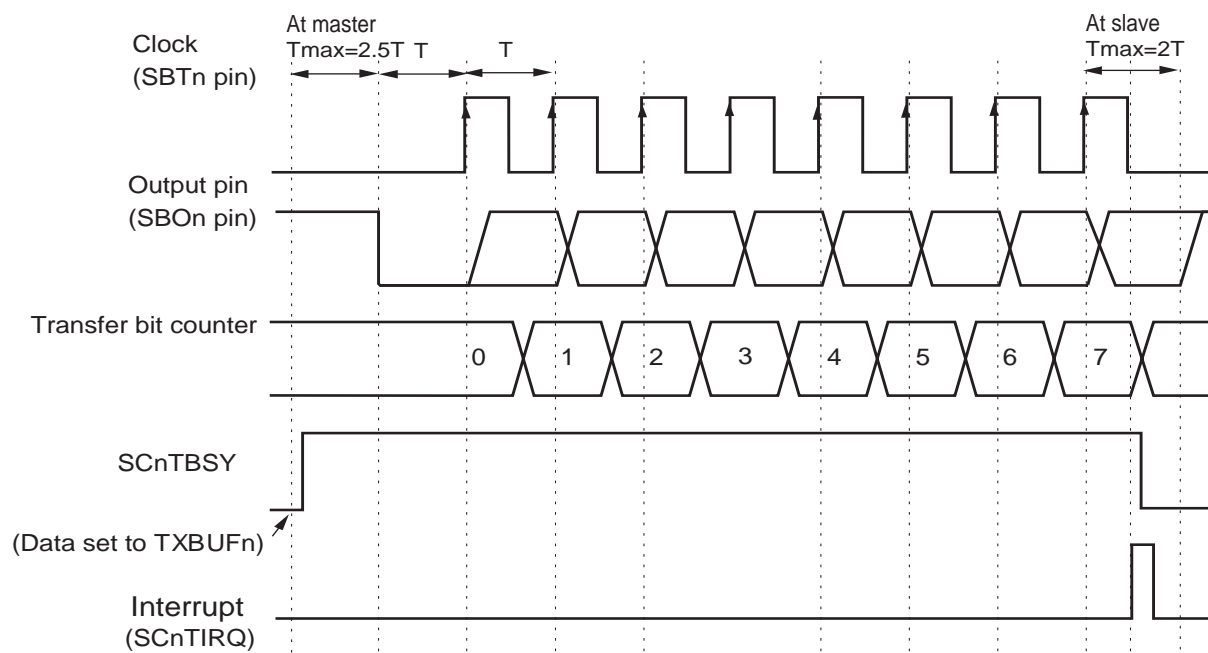
Figure:12.3.8 Transmission Timing (At Rising Edge, Start Condition is Enabled)
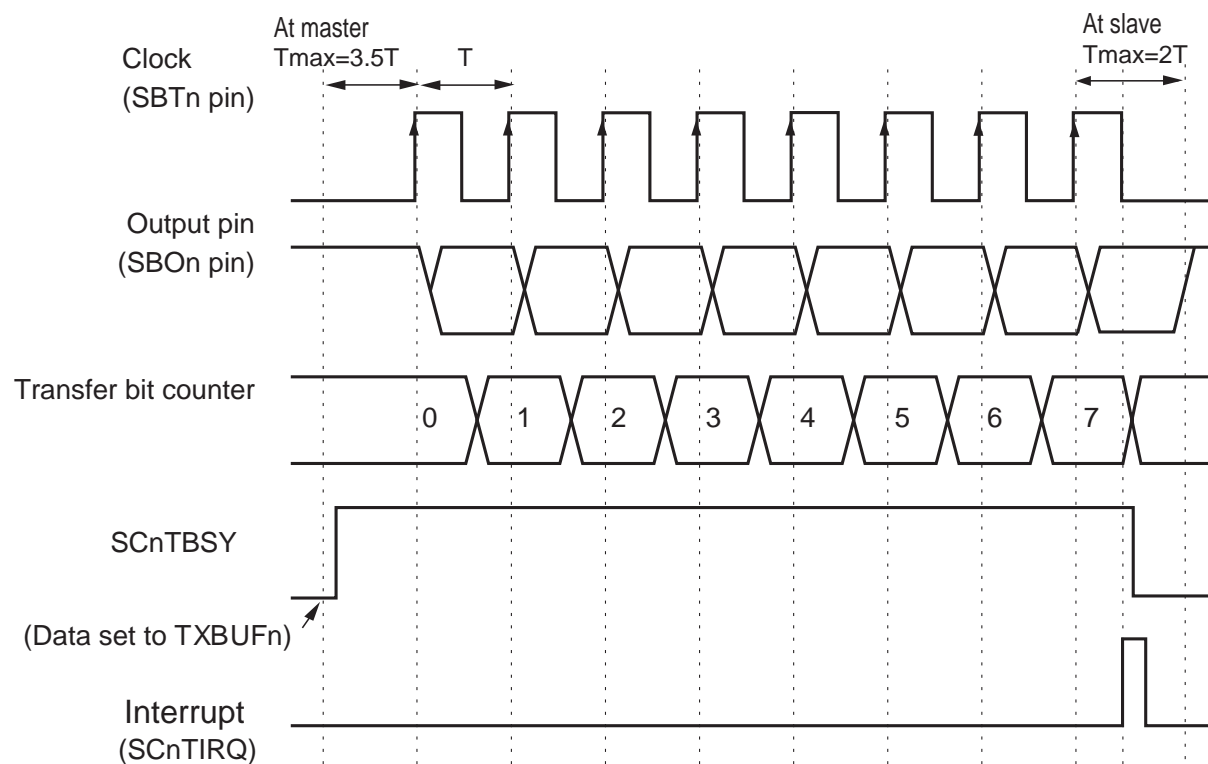
Figure:12.3.9 Transmission Timing (At Rising Edge, Start Condition is Disabled)

■ Reception Timing
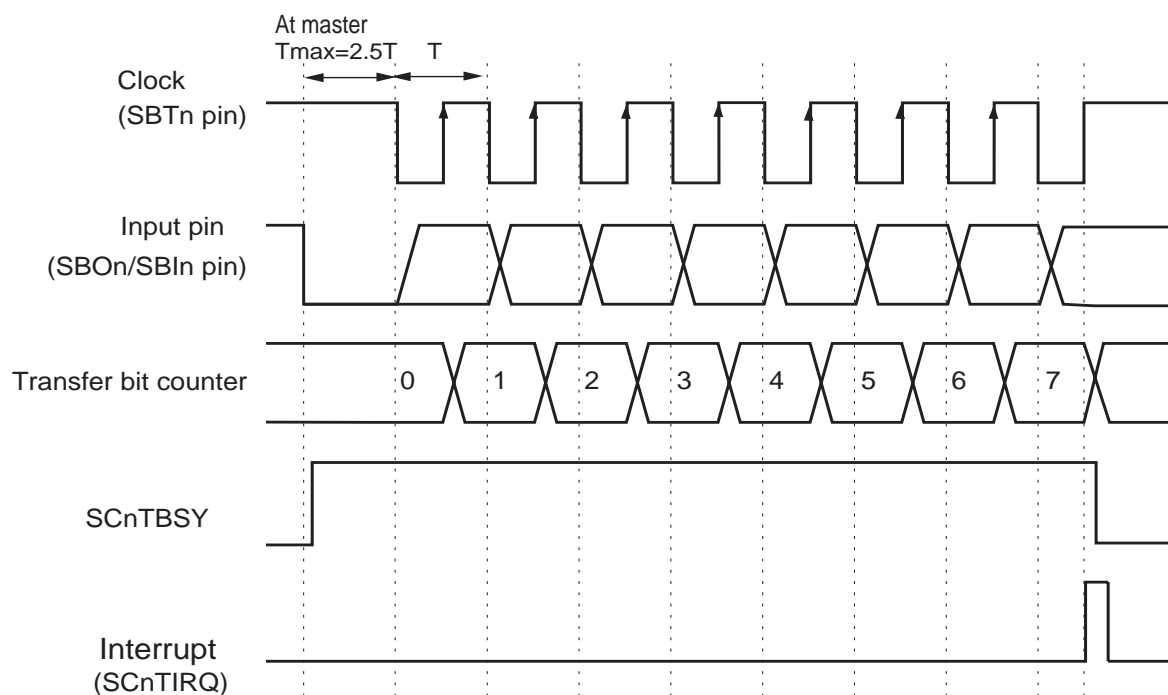
Figure:12.3.10 Reception Timing (At Rising Edge, Start Condition is Enabled)
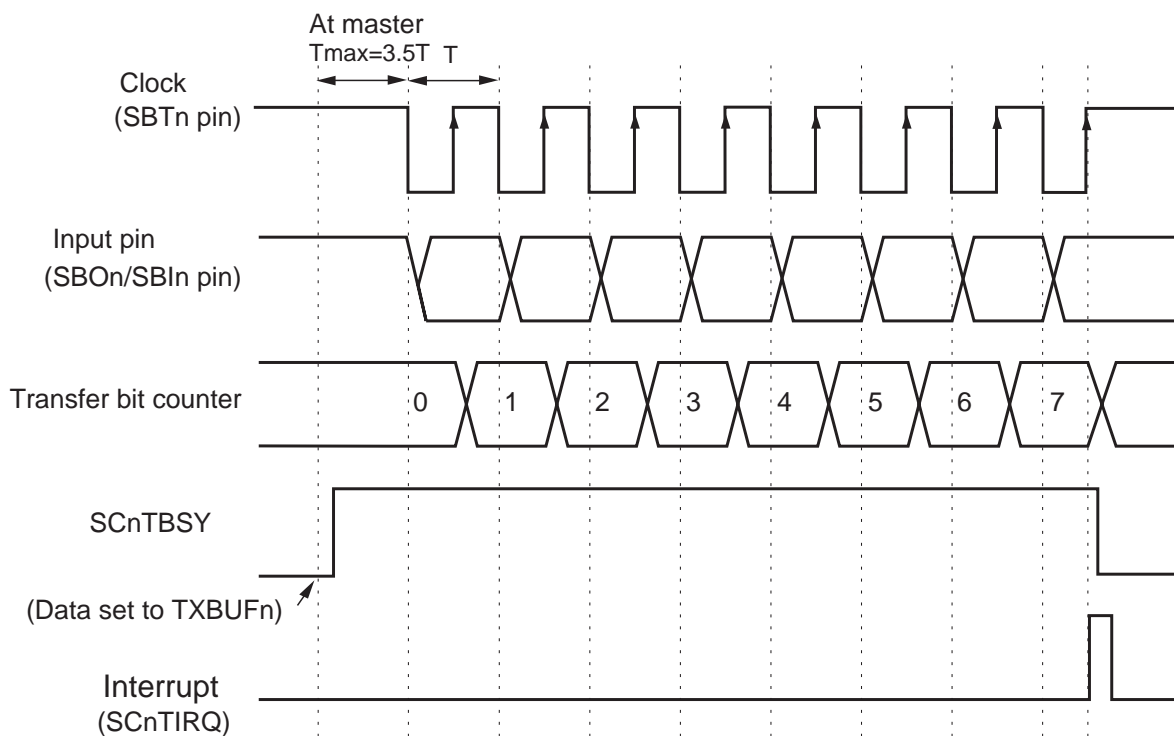
Figure:12.3.11 Reception Timing (At Rising Edge, Start Condition is Disabled)
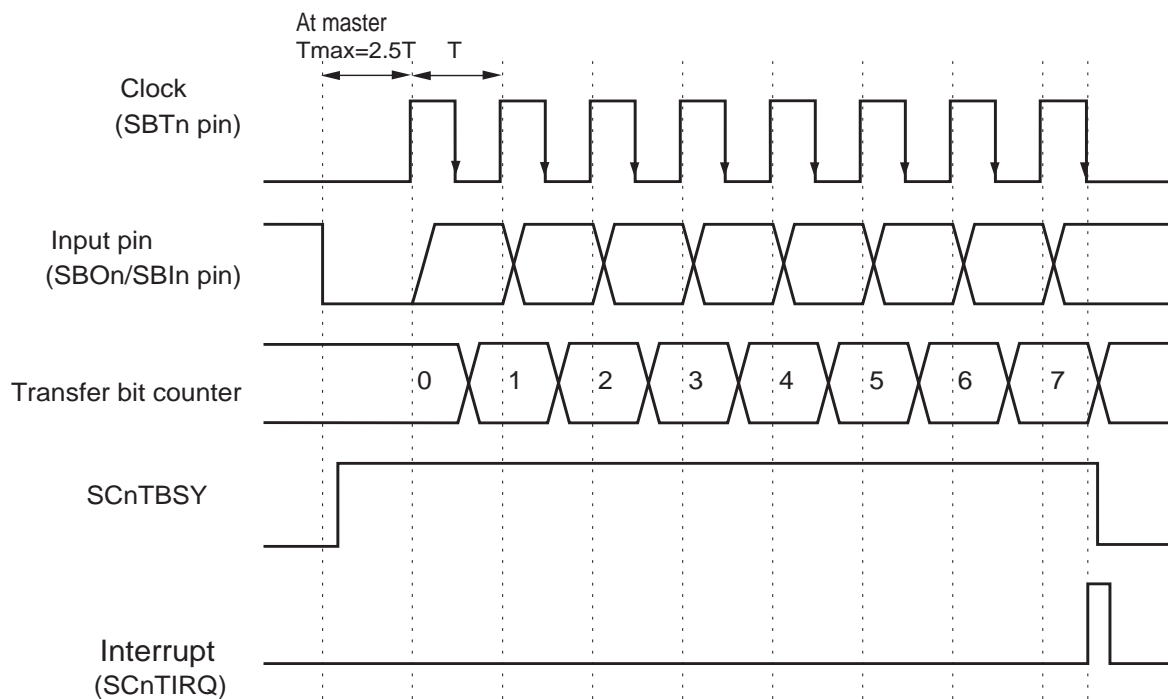
Figure:12.3.12 Reception Timing (At Falling Edge, Start Condition is Enabled)
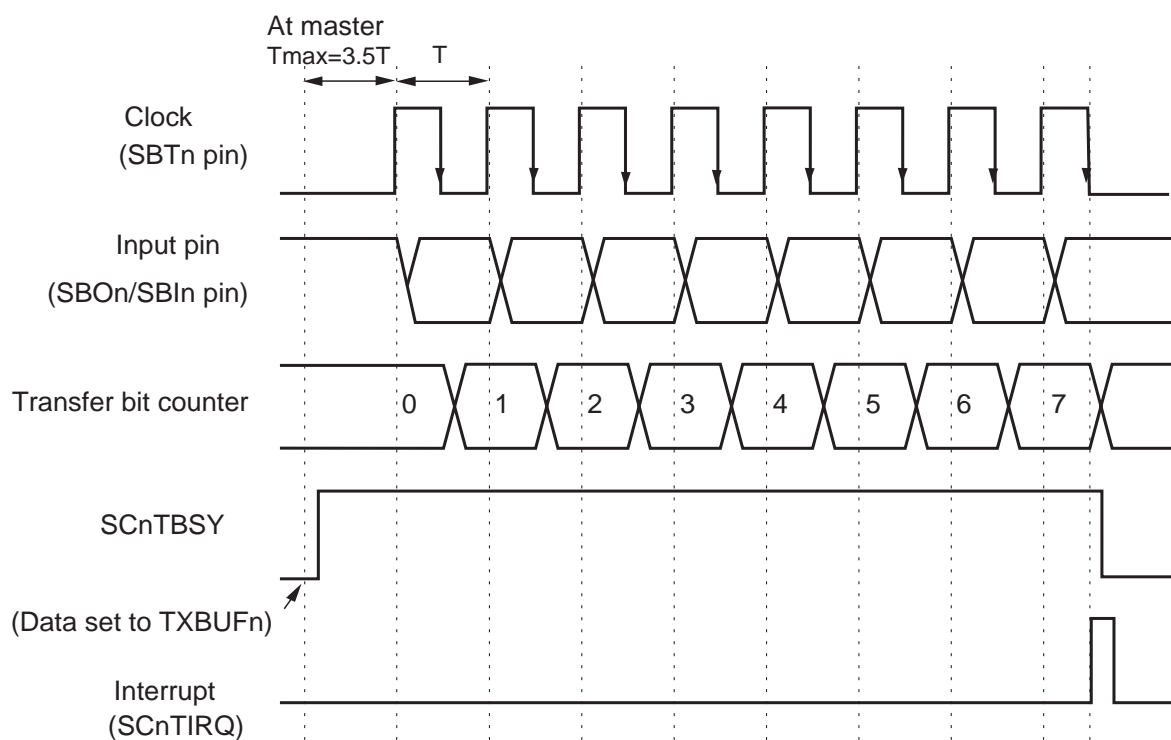
Figure:12.3.13 Reception Timing (At Falling Edge, Start Condition is Disabled)

■ Transmission/Reception Timing 1

When transmission and reception are executed at the same time, the SCnCE1 flag of the SCnMD0 register should be set to "0" or "1". As data is received at the opposite edge timing of the output edge of transmission data, set the polarity of the reception data input edge to opposite polarity of the output edge of transmission data.

When transmission and reception are executed with the start condition "enable", "the start condition enable" should be selected with the other party of communication with which the microcontroller is exchanging data. Select "the start condition disable" by setting of SCnSTE flag of SCnMD0 register when transmission and reception are executed simultaneously. Otherwise, improper communication may occur.
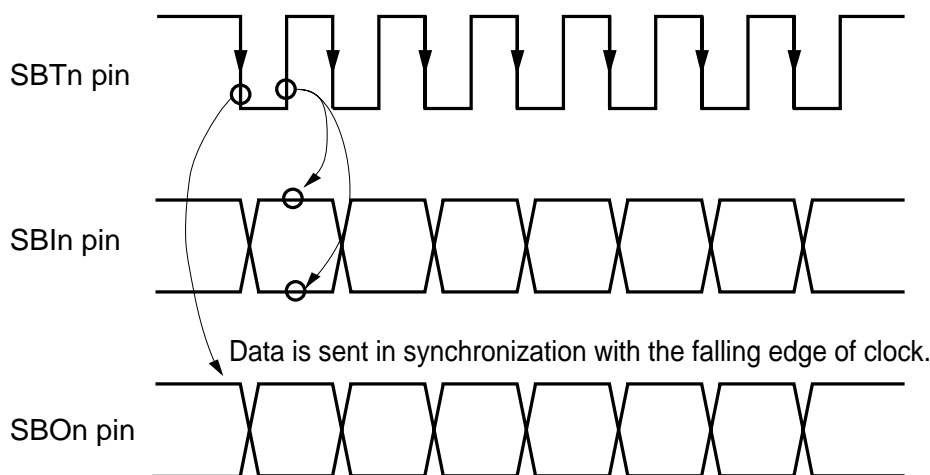
Figure:12.3.14 Transmission/ Reception Timing (Reception: at Rising Edge, Transmission: at Falling Edge)
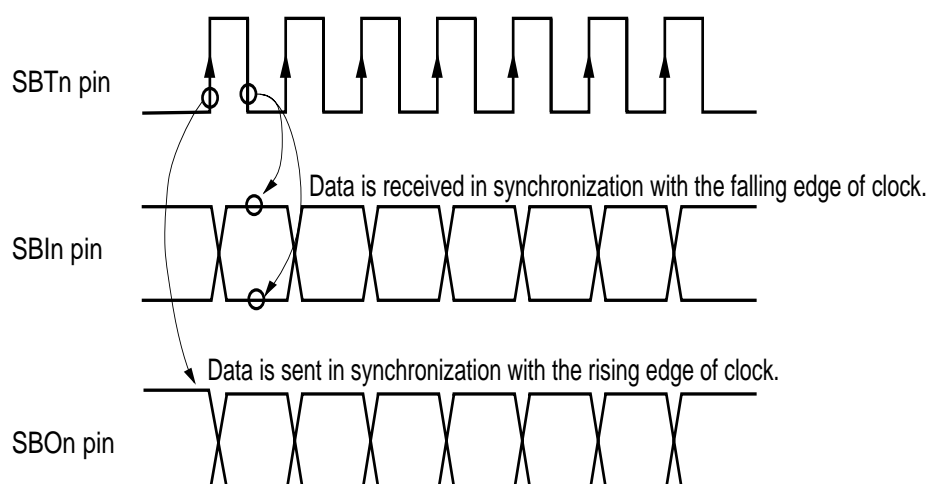
Figure:12.3.15 Transmission/Reception Timing (Reception: at Falling Edge, Transmission: at Rising Edge)

When operating transmission and reception at the same time, select "start condition disable"; otherwise, it may cause improper operations.

■ Communication in STANDBY mode

This serial interface has the following method for recovering from STANDBY mode.

This serial interface can execute slave reception at STANDBY mode. CPU operation status can be recovered from STANDBY mode to CPU operation mode by the communication complete interrupt SCnTIRQ that occurs after slave reception.

(At STANDBY mode, continuous reception is not available since the next data can not be accepted after the data of the transfer bit count, set by the SCnLNG2 to 0 flags of the SCnMD0 register, is received once.) Read the received data from the reception data buffer RXBUFn after recovering to CPU operation mode.

In reception at STANDBY mode, communication with the start condition enabled is not available. Disable the start condition. The dummy data should be set in the transmission data buffer TXBUFn before transition to STANDBY mode.
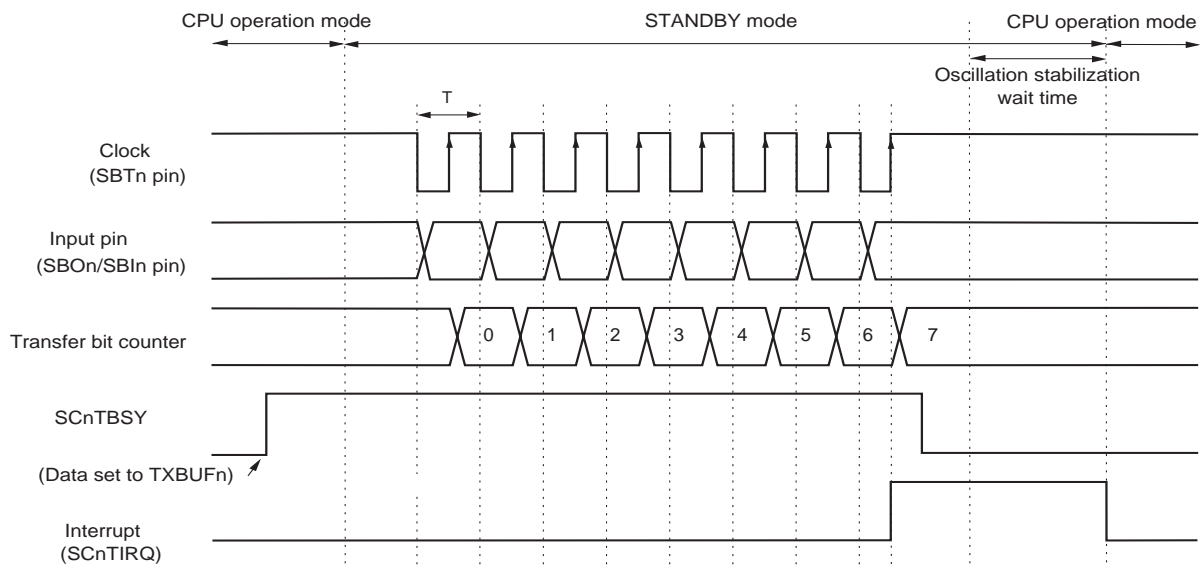
Figure:12.3.16 Reception Timing at Standby Mode (Reception: at Rising Edge, Start Condition is Disabled)

12.3.3   Pin Setup

■ Synchronous Serial Interface 0 Pin Setup

Port	Channel	Type	Pin	M/S	SC0SEL register — Serial 0 I/O pin switching (0:P50-P52, 1:P43-P45) — OSL0	PnDIR register — I/O mode selection (0: input mode, 1: output mode) — PnDIRm	PnODC register — Nch open-drain output selection / Arbitrary setting (0: push/pull, 1:Nch open-drain) — PnODCm	PnPLUD register — Pull-up/pull-down resistor selection / Arbitrary setting (0: not added, 1: added) — PnPLUDm	SC0MD1: Serial data input selection (0: data input from SBI0, 1: data input from SBO0) — SC0IOM	SC0MD1: SBT0 pin function selection (0: port, 1: transfer clock I/O) — SC0SBTS	SC0MD1: Serial input control selection (0:"1" input, 1: serial input) — SC0SBIS	SC0MD1: SBO0 (RXD0) pin function selection (0: port, 1: serial data output) — SC0SBOS
P5	3 channels	Transmission only	P50/SBO0A		0	P5DIR0:1	P5ODC0	P5PLUD0	0	1	0	1
			-			-	-	-				
			P52/ SBT0A	Master		P5DIR2:1	P5ODC2	P5PLUD2				
			SBT0A	Slave		P5DIR2:0	-					
		Reception only	-		0	-	-	-	0	1	1	0
			P51/SBI0A			P5DIR1:0	-	-				
			P52/ SBT0A	Master		P5DIR2:1	P5ODC2	P5PLUD2				
			SBT0A	Slave		P5DIR2:0	-					
		Transmission/ reception	P50/SBO0A		0	P5DIR0:1	P5ODC0	P5PLUD0	0	1	1	1
			P51/SBI0A			P5DIR1:0	-	-				
			P52/ SBT0A	Master		P5DIR2:1	P5ODC2	P5PLUD2				
			SBT0A	Slave		P5DIR2:0	-					
	2 channels	Transmission	P50/SBO0A		0	P5DIR0:1	P5ODC0	P5PLUD0	1	1	0	1
			-			-	-	-				
			P52/ SBT0A	Master		P5DIR2:1	P5ODC2	P5PLUD2				
			SBT0A	Slave		P5DIR2:0	-					
		Reception	P50/SBO0A		0	P5DIR0:0	-	-	1	1	1	0
			-			-	-	-				
			P52/ SBT0A	Master		P5DIR2:1	P5ODC2	P5PLUD2				
			SBT0A	Slave		P5DIR2:0	-					
P4	3 channels	Transmission only	P43/SBO0B		1	P4DIR3:1	P4ODC3	P4PLUD3	0	1	0	1
			-			-	-	-				
			P45/ SBT0B	Master		P4DIR5:1	P4ODC5	P4PLUD5				
			SBT0B	Slave		P4DIR5:0	-					
		Reception only	-		1	-	-	-	0	1	1	0
			P44/SBI0B			P4DIR4:0	-	-				
			P45/ SBT0B	Master		P4DIR5:1	P4ODC5	P4PLUD5				
			SBT0B	Slave		P4DIR5:0	-					
		Transmission/ reception	P43/SBO0B		1	P4DIR3:1	P4ODC3	P4PLUD3	0	1	1	1
			P44/SBI0B			P4DIR4:0	-	-				
			P45/ SBT0B	Master		P4DIR5:1	P4ODC5	P4PLUD5				
			SBT0B	Slave		P4DIR5:0	-					
	2 channels	Transmission	P43/SBO0B		1	P4DIR3:1	P4ODC3	P4PLUD3	1	1	0	1
			-			-	-	-				
			P45/ SBT0B	Master		P4DIR5:1	P4ODC5	P4PLUD5				
			SBT0B	Slave		P4DIR5:0	-					
		Reception	P43/SBO0B		1	P4DIR3:0	-	-	1	1	1	0
			-			-	-	-				
			P45/ SBT0B	Master		P4DIR5:1	P4ODC5	P4PLUD5				
			SBT0B	Slave		P4DIR5:0	-					

■ Synchronous Serial Interface 1 Pin Setup

Port	Channel	Type	Pin		SC1SEL register — Serial 1 I/O pin switching — OSL1 (0:P00-P02, 1:P75-P77)	PnDIR register — I/O mode selection — PnDIRm (0: input mode, 1: output mode)	PnODC register — Nch open-drain output selection — Arbitrary setting — PnODCm (0: push/pull, 1:Nch open-drain)	PnPLUD register — Pull-up/pull-down resistor selection — Arbitrary setting — PnPLUDm (0: not added, 1: added)	SC1MD1 — Serial data input selection — SC1IOM (0: data input from SBI1, 1: data input from SBO1)	SC1MD1 — SBT1 pin function selection — SC1SBTS (0: port, 1: transfer clock I/O)	SC1MD1 — Serial input control selection — SC1SBIS (0:"1" input, 1: serial input)	SC1MD1 — SBO1 (RXD1) pin function selection — SC1SBOS (0: port, 1: serial data output)
P0	3 channels	Transmission only	P01/SBO1A		0	P0DIR1:1	P0ODC1	P0PLUD1	0	1	0	1
			-			-	-	-				
			P02/ SBT1A	Master		P0DIR2:1	P0ODC2	P0PLUD2				
				Slave		P0DIR2:0	-					
		Reception only	-		0	-	-	-	0	1	1	0
			P00/SBI1A			P0DIR0:0	-	-				
			P02/ SBT1A	Master		P0DIR2:1	P0ODC2	P0PLUD2				
				Slave		P0DIR2:0	-					
		Transmission/ reception	P01/SBO1A		0	P0DIR1:1	P0ODC1	P0PLUD1	0	1	1	1
			P00/SBI1A			P0DIR0:0	-	-				
			P02/ SBT1A	Master		P0DIR2:1	P0ODC2	P0PLUD2				
				Slave		P0DIR2:0	-					
	2 channels	Transmission	P01/SBO1A		0	P0DIR1:1	P0ODC1	P0PLUD1	1	1	0	1
			-			-	-	-				
			P02/ SBT1A	Master		P0DIR2:1	P0ODC2	P0PLUD2				
				Slave		P0DIR2:0	-					
		Reception	P01/SBO1A		0	P0DIR1:0	-	-	1	1	1	0
			-			-	-	-				
			P02/ SBT1A	Master		P0DIR2:1	P0ODC2	P0PLUD2				
				Slave		P0DIR2:0	-					
P7	3 channels	Transmission only	P75/SBO1B		1	P7DIR5:1	P7ODC5	P7PLUD5	0	1	0	1
			-			-	-	-				
			P77/ SBT1B	Master		P7DIR7:1	P7ODC7	P7PLUD7				
				Slave		P7DIR7:0	-					
		Reception only	-		1	-	-	-	0	1	1	0
			P76/SBI1B			P7DIR6:0	-	-				
			P77/ SBT1B	Master		P7DIR7:1	P7ODC7	P7PLUD7				
				Slave		P7DIR7:0	-					
		Transmission/ reception	P75/SBO1B		1	P7DIR5:1	P7ODC5	P7PLUD5	0	1	1	1
			P76/SBI1B			P7DIR6:0	-	-				
			P77/ SBT1B	Master		P7DIR7:1	P7ODC7	P7PLUD7				
				Slave		P7DIR7:0	-					
	2 channels	Transmission	P75/SBO1B		1	P7DIR5:1	P7ODC5	P7PLUD5	1	1	0	1
			-			-	-	-				
			P77/ SBT1B	Master		P7DIR7:1	P7ODC7	P7PLUD7				
				Slave		P7DIR7:0	-					
		Reception	P75/SBO1B		1	P7DIR5:0	-	-	1	1	1	0
			-			-	-	-				
			P77/ SBT1B	Master		P7DIR7:1	P7ODC7	P7PLUD7				
				Slave		P7DIR7:0	-					

■ Synchronous Serial Interface 2 Pin Setup

Port	Channel	Type	Pin		Pin setup (flag setup)							
					SC2SEL register	PnDIR register	PnODC register	PnPLUD register	SC2MD1register			
					Serial 2 I/O pin switching	I/O mode selection	Nch open-drain output selection / Aribitary setting	Pull-up/pull-down resistor selection / Aribitary setting	Serial data input selection	SBT2 pin function selection	Serial input control selection	SBO2 (RXD2) pin function selection
					0:P70-P72 / 1:P30-P32	0: input mode / 1: output mode	0: push/pull / 1:Nch open-drain	0: not added / 1: added	0: data input from SBI2 / 1: data input from SBO2	0: port / 1: transfer clock I/O	0:"1" input / 1: serial input	0: port / 1: serial data output
					OSL2	PnDIRm	PnODCm	PnPLUDm	SC2IOM	SC2SBTS	SC2SBIS	SC2SBOS
P7	3 channels	Transmission only	P70/SBO2A		0	P7DIR0:1	P7ODC0	P7PLUD0	0	1	0	1
			-			-	-	-				
			P72/ SBT2A	Master		P7DIR2:1	P7ODC2	P7PLUD2				
				Slave		P7DIR2:0	-					
		Reception only	-		0	-	-	-	0	1	1	0
			P71/SBI2A			P7DIR1:0	-	-				
			P72/ SBT2A	Master		P7DIR2:1	P7ODC2	P7PLUD2				
				Slave		P7DIR2:0	-					
		Transmission /reception	P70/SBO2A		0	P7DIR0:1	P7ODC0	P7PLUD0	0	1	1	1
			P71/SBI2A			P7DIR1:0	-	-				
			P72/ SBT2A	Master		P7DIR2:1	P7ODC2	P7PLUD2				
				Slave		P7DIR2:0	-					
	2 channels	Transmission	P70/SBO2A		0	P7DIR0:1	P7ODC0	P7PLUD0	1	1	0	1
			-			-	-	-				
			P72/ SBT2A	Master		P7DIR2:1	P7ODC2	P7PLUD2				
				Slave		P7DIR2:0	-					
		Reception	P70/SBO2A		0	P7DIR0:0	-	-	1	1	1	0
			-			-	-	-				
			P72/ SBT2A	Master		P7DIR2:1	P7ODC2	P7PLUD2				
				Slave		P7DIR2:0	-					
P3	3 channels	Transmission only	P30/SBO2B		1	P3DIR0:1	P3ODC0	P3PLUD0	0	1	0	1
			-			-	-	-				
			P32/ SBT2B	Master		P3DIR2:1	P3ODC2	P3PLUD2				
				Slave		P3DIR2:0	-					
		Reception only	-		1	-	-	-	0	1	1	0
			P31/SBI2B			P3DIR1:0	-	-				
			P32/ SBT2B	Master		P3DIR2:1	P3ODC2	P3PLUD2				
				Slave		P3DIR2:0	-					
		Transmission /reception	P30/SBO2B		1	P3DIR0:1	P3ODC0	P3PLUD0	0	1	1	1
			P31/SBI2B			P3DIR1:0	-	-				
			P32/ SBT2B	Master		P3DIR2:1	P3ODC2	P3PLUD2				
				Slave		P3DIR2:0	-					
	2 channels	Transmission	P30/SBO2B		1	P3DIR0:1	P3ODC0	P3PLUD0	1	1	0	1
			-			-	-	-				
			P32/ SBT2B	Master		P3DIR2:1	P3ODC2	P3PLUD2				
				Slave		P3DIR2:0	-					
		Reception	P30/SBO2B		1	P3DIR0:0	-	-	1	1	1	0
			-			-	-	-				
			P32/ SBT2B	Master		P3DIR2:1	P3ODC2	P3PLUD2				
				Slave		P3DIR2:0	-					

■ Synchronous Serial Interface 3 Pin Setup

Port	Channel	Type	Pin	Pin (M/S)	SC3SEL register — Serial 3 I/O pin switching (0:P04-P06 / 1:P40-P42) — OSL3	PnDIR register — I/O mode selection (0: input mode / 1: output mode) — PnDIRm	PnODC register — Nch open-drain output selection — Arbitrary setting (0: push/pull / 1:Nch open-drain) — PnODCm	PnPLUD register — Pull-up/pull-down resistor selection — Arbitrary setting (0: not added / 1: added) — PnPLUDm	SC3MD1 register — Serial data input selection (0: data input from SBI3 / 1: data input from SBO3) — SC3IOM	SC3MD1 — SBT3 pin function selection (0: port / 1: transfer clock I/O) — SC3SBTS	SC3MD1 — Serial input control selection (0:"1" input / 1: serial input) — SC3SBIS	SC3MD1 — SBO3 (RXD3) pin function selection (0: port / 1: serial data output) — SC3SBOS
P0	3 channels	Transmission only	P04/SBO3A		0	P0DIR4:1	P0ODC4	P0PLUD4	0	1	0	1
			-			-	-	-				
			P06/SBT3A	Master		P0DIR6:1	P0ODC6	P0PLUD6				
				Slave		P0DIR6:0	-					
		Reception only	-		0	-	-	-	0	1	1	0
			P05/SBI3A			P0DIR5:0	-	-				
			P06/SBT3A	Master		P0DIR6:1	P0ODC6	P0PLUD6				
				Slave		P0DIR6:0	-					
		Transmission /reception	P04/SBO3A		0	P0DIR4:1	P0ODC4	P0PLUD4	0	1	1	1
			P05/SBI3A			P0DIR5:0	-	-				
			P06/SBT3A	Master		P0DIR6:1	P0ODC6	P0PLUD6				
				Slave		P0DIR6:0	-					
	2 channels	Transmission	P04/SBO3A		0	P0DIR4:1	P0ODC4	P0PLUD4	1	1	0	1
			-			-	-	-				
			P06/SBT3A	Master		P0DIR6:1	P0ODC6	P0PLUD6				
				Slave		P0DIR6:0	-					
		Reception	P04/SBO3A		0	P0DIR4:0	-	-	1	1	1	0
			-			-	-	-				
			P06/SBT3A	Master		P0DIR6:1	P0ODC6	P0PLUD6				
				Slave		P0DIR6:0	-					
P4	3 channels	Transmission only	P40/SBO3B		1	P4DIR0:1	P4ODC0	P4PLUD0	0	1	0	1
			-			-	-	-				
			P42/SBT3B	Master		P4DIR2:1	P4ODC2	P4PLUD2				
				Slave		P4DIR2:0	-					
		Reception only	-		1	-	-	-	0	1	1	0
			P41/SBI3B			P4DIR1:0	-	-				
			P42/SBT3B	Master		P4DIR2:1	P4ODC2	P4PLUD2				
				Slave		P4DIR2:0	-					
		Transmission /reception	P40/SBO3B		1	P4DIR0:1	P4ODC0	P4PLUD0	0	1	1	1
			P41/SBI3B			P4DIR1:0	-	-				
			P42/SBT3B	Master		P4DIR2:1	P4ODC2	P4PLUD2				
				Slave		P4DIR2:0	-					
	2 channels	Transmission	P40/SBO3B		1	P4DIR0:1	P4ODC0	P4PLUD0	1	1	0	1
			-			-	-	-				
			P42/SBT3B	Master		P4DIR2:1	P4ODC2	P4PLUD2				
				Slave		P4DIR2:0	-					
		Reception	P40/SBO3B		1	P4DIR0:0	-	-	1	1	1	0
			-			-	-	-				
			P42/SBT3B	Master		P4DIR2:1	P4ODC2	P4PLUD2				
				Slave		P4DIR2:0	-					

■ Synchronous Serial Interface 4 Pin Setup

Port	Channel	Type	Pin		SC4SEL register — Serial 4 I/O pin switching — 0:P65-P67 / 1:P33-P35 (OSL4)	PnDIR register — I/O mode selection — 0: input mode / 1: output mode (PnDIRm)	PnODC register — Nch open-drain output selection — Aribitary setting — 0: push/pull / 1:Nch open-drain (PnODCm)	PnPLUD register — Pull-up/pull-down resistor selection — Aribitary setting — 0: not added / 1: added (PnPLUDm)	SC4MD1 register — Serial data input selection — 0: data input from SBI4 / 1: data input from SBO4 (SC4IOM)	SBT4 pin function selection — 0: port / 1: transfer clock I/O (SC4SBTS)	Serial input control selection — 0:"1" input / 1: serial input (SC4SBIS)	SBO4 (RXD4) pin function selection — 0: port / 1: serial data output (SC4SBOS)
P6	3 channels	Transmission only	P66/SBO4A		0	P6DIR6:1	P6ODC6	P6PLUD6	0	1	0	1
			-			-	-	-				
			P67/ SBT4A	Master		P6DIR7:1	P6ODC7	P6PLUD7				
				Slave		P6DIR7:0	-					
		Reception only	-		0	-	-	-	0	1	1	0
			P65/SBI4A			P6DIR5:0	-	-				
			P67/ SBT4A	Master		P6DIR7:1	P6ODC7	P6PLUD7				
				Slave		P6DIR7:0	-					
		Transmission /reception	P66/SBO4A		0	P6DIR6:1	P6ODC6	P6PLUD6	0	1	1	1
			P65/SBI4A			P6DIR5:0	-	-				
			P67/ SBT4A	Master		P6DIR7:1	P6ODC7	P6PLUD7				
				Slave		P6DIR7:0	-					
	2 channels	Transmission	P66/SBO4A		0	P6DIR6:1	P6ODC6	P6PLUD6	1	1	0	1
			-			-	-	-				
			P67/ SBT4A	Master		P6DIR7:1	P6ODC7	P6PLUD7				
				Slave		P6DIR7:0	-					
		Reception	P66/SBO4A		0	P6DIR6:0	-	-	1	1	1	0
			-			-	-	-				
			P67/ SBT4A	Master		P6DIR7:1	P6ODC7	P6PLUD7				
				Slave		P6DIR7:0	-					
P3	3 channels	Transmission only	P33/SBO4B		1	P3DIR3:1	P3ODC3	P3PLUD3	0	1	0	1
			-			-	-	-				
			P34/ SBT4B	Master		P3DIR4:1	P3ODC4	P3PLUD4				
				Slave		P3DIR4:0	-					
		Reception only	-		1	-	-	-	0	1	1	0
			P35/SBI4B			P3DIR5:0	-	-				
			P34/ SBT4B	Master		P3DIR4:1	P3ODC4	P3PLUD4				
				Slave		P3DIR4:0	-					
		Transmission /reception	P33/SBO4B		1	P3DIR3:1	P3ODC3	P3PLUD3	0	1	1	1
			P35/SBI4B			P3DIR5:0	-	-				
			P34/ SBT4B	Master		P3DIR4:1	P3ODC4	P3PLUD4				
				Slave		P3DIR4:0	-					
	2 channels	Transmission	P33/SBO4B		1	P3DIR3:1	P3ODC3	P3PLUD3	1	1	0	1
			-			-	-	-				
			P34/ SBT4B	Master		P3DIR4:1	P3ODC4	P3PLUD4				
				Slave		P3DIR4:0	-					
		Reception	P33/SBO4B		1	P3DIR3:0	-	-	1	1	1	0
			-			-	-	-				
			P34/ SBT4B	Master		P3DIR4:1	P3ODC4	P3PLUD4				
				Slave		P3DIR4:0	-					

12.3.4   Setup Example

■ Transmission/Reception Setup Example

The setup example for clock synchronous serial communication using serial 1 is shown. Table:12.3.7 shows the conditions at transmission/reception. The basic setup procedures are the same in serials 0 and 2 to 4. However, pin settings (4) and (5) differ in each serial.

Table:12.3.7 Setup Examples for Synchronous Serial Interface Transmission/Reception

Setup item	Set to
Serial data input selection	SB1A
Transfer bit count	8 bits
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Output edge	Rising edge
Clock	Clock master
Clock source	fs/2
Clock source divide-by-8 (serial 0, serial 1 , serial 2 and serial 3)	Not divided by 8
SBT1/SBO1 pin style	Nch open-drain
SBT1 pin pull-up resistor	Added
SBO1 pin pull-up resistor	Added
Serial 1 communication complete interrupt	Enabled
SBO1 output after last data output	"1"(H) fix

An example setup procedure, with a description of each step is shown below

Setup Procedure	Description

(1) Select the prescaler operation
   SC1MD3 (0x03F9C)
   bp3 :SC1PSCE =1
	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler count enable".

(2) Select the clock source
   SC1MD3 (0x03F9C)
   bp2-0 :SC1PSC2-0 =100
	(2) Set the SC1PSC2 to 0 flags of the SC1MD3 register to "100" to select fs/2 to the clock source.

(3) Control the SBO1 output after the last data output
   SC1MD3 (0x03F9C)
   bp7,6 :SC1FDC1-0 =00
	(3) Set the SC1FDC1 to 0 flags of the SC1MD3 register to "0, 0" to select "1" (High) output fix after the SBO1 last data output.

(4) Control the pin style [set the pin corresponding to each serial]
   P0ODC(0x03EF0)
   bp2-1 :P0ODC2-1 =11
   P0PLUD(0x03F40)
   bp2-1 :P0PLUD2-1 =11
	(4) Set the P0ODC2-1 flags of the P0ODC register to "11" to select Nch open-drain to the SBO1/SBT1 pin style. Set the P0PLUD2-1 flags of the P0PLUD register to "11" to enable the pull-up resistor.
	(set the pin corresponding to each serial)

(5) Control the pin direction [set the pin corresponding to each serial]
   P0DIR (0x03F30)
   bp2-1 :P0DIR2-1 =11
	(5) Set the P0DIR2 -1 flags of the port 0 direction control register (P0DIR) to "11" to set P01 and P02 to output mode and P00 to input mode.
	(set the pin corresponding to each serial)

Setup Procedure	Description

(6) Set the SC1MD0 register
  Select the transfer bit count
  SC1MD0 (0x03F99)
  bp2-0 :SC1LNG2-0 =111
 	
  Select the start condition
  SC1MD0 (0x03F99)
  bp3 :SC1STE =0
 	
  Select the transfer first bit
  SC1MD0 (0x03F99)
  bp4 :SC1DIR =0
 	
  Select the transfer edge
  SC1MD0 (0x03F99)
  bp7 :SC1CE1 =1
	(6) Set the SC1LNG2 to 0 flags of the serial 1 mode register (SC1MD0) to "111" to set the transfer bit count to 8 bits.
	
	Set the SC1STE flag of the SC1MD0 register to "0" to disable the start condition.
	
	Set the SC1DIR flag of the SC1MD0 register to "0" to set MSB as the transfer first bit.
	
	Set the SC1CE1 flag of the SC1MD0 register to "1" to set the transmission data input edge to "rising" and the reception data output edge to "falling".

(7) Set the SC1MD1 register
  Select the communication type
  SC1MD1 (0x03F9A)
  bp0 :SC1CMD =0
 	
  Select the transfer clock
  SC1MD1 0x03F9A)
  bp2 :SC1MST =1
  bp3 :SC1CKM =0 (serial 0, 1, 2 and 3)
 	
  Control the pin function
  SC1MD1 (0x03F9A)
  bp4 :SC1SBOS =1
  bp5 :SC1SBIS =1
  bp6 :SC1SBTS =1
  bp7 :SC1IOM =0
	(7) Set the SC1CMD flag of the SC1MD1 register to "0" to select the synchronous serial.
	
	Set the SC1MST flag of the SC1MD1 register to "1" to select the clock master (internal clock); and, set the SC1CKM flag to "0" to select "the source clock not divided by 8" for serial 0, 1, 2 and 3.
	
	Set the SC1SBOS, SC1SBIS and SC1SBTS flags of the SC1MD1 register to "1" to set the SBO1 pin to the serial data output, the SBI1 pin to the serial data input and the SBT1 pin to the serial clock input/output. Set the SC1IOM flag to "0" to set the serial data input from the SBI1 pin.

(8) Set the interrupt level
  PSW
  bp6 :MIE =0
  SC1TICR (0x03FF8)
  bp7-6 :SC1LV1-0 =10
	(8) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt level by the SC1LV1 to 0 flags of the serial 1 interrupt control register (SC1TICR).

(9) Enable the interrupt
  SC1TICR (0x03FF8)
  bp1 :SC1TIE =1
  PSW
  bp6 :MIE =1
	(9) Set the SC1TIE flag of the SC1TICR register to "1" to enable the interrupt. If any interrupt request flag (SC1TIR of the SC1TICR register) is already set, clear SC1TIR prior to enabling the interrupt. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.

(10) Start the serial transmission
  Transmission data→TXBUF1 (0x03F9F)
  Reception data→input the SBI1A pin
	(10) Set the transmission data to the serial transmission data buffer TXBUF1. The transfer clock is generated; and, transmission or reception is started. When transmission is finished, the serial 1 communication end interrupt SC1TIRQ is generated.
	 [Chapter 3 3.1.4. Maskable Interrupt Control Register Setup]

*Each setup in (1) to (3) and (6) to (7) can be set at the same time.

Set the SCnSBIS of the SCnMD1 register to "0" and select a port in order to operate only transmission with 3 channels; and, set the SCnSBOS of the SCnMD1 register to "0" and select a port in order to operate only reception.

Serial data is input and output from the SBOn pin in communication with 2 channels by connecting the SBOn pin. The port direction control register switches I/O. SCnSBIS of the SCnMD1 register must be set to "1" to select "serial data input". The SBIn pin can be used as a general port.

This serial interface has an emergency reset function. If the communication is needed to be stopped by force, set SCnSBOS and SCnSBIS of the SCnMD1 register to "0".

To set each flag, follow the setup procedure in order as described. All control registers (refer to Table:12.2.1 except TXBUFn, RXBUFn and SCnTRB) must be set prior to activating communication.

The transfer rate must be under 5.0 MHz for setting a transfer clock by the SCnMD3 register.

■ Reception Setup Example (STANDBY Mode Reception)

The following shows the setup example for STANDBY mode reception of clock synchronous serial communication using serial 1. Table:12.3.8 shows the condition at reception. The basic procedures are the same in serial 0 and 2 to 4. Pin settings (4) and (5) differ in each serial.

Table:12.3.8 Setup Examples for Synchronous Serial Interface Reception

Setup item	Set to
Serial data input selection	SBI1A
Transfer bit count	8 bits
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Output edge	Rising edge
Clock	Clock slave
Clock source	fs/2
Clock source divide-by-8 (serial 0, 1, 2 and 3)	Not divided by 8
SBT1/SBO1 pin style	Nch open-drain
SBT1 pin pull-up resistor	Added
SBO1 pin pull-up resistor	Added
Serial 1 communication complete interrupt	Enabled
SBO1 output after last data output	"1"(H) fix

An example setup procedure, with a description of each step is shown below

Setup Procedure	Description
(1) Select the prescaler operation SC1MD3 (0x03F9C) bp3 :SC1PSCE =1	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler count enable"
(2) Select the clock source SC1MD3 (0x03F9C) bp2-0 :SC1PSC2-0 =100	(2) Set the SC1PSC2 to 0 flags of the SC1MD3 register to "100" to select fs/2 to the clock source.
(3) Control the SBO0 output after the last data output SC1MD3 (0x03F9C) bp7,6 :SC1FDC1-0 =00	(3) Set the SC1FDC1 to 0 flags of the SC1MD3 register to "0, 0" to select "1" (High) output fix after the SBO1 last data output.
(4) Control the pin style [set the pin corresponding to each serial] P0ODC(0x03EF0) bp2-1 :P0ODC2-1 =11 P0PLUD(0x03F40) bp2-1 :P0PLUD2-1 =11	(4) Set the P0ODC2-1 flags of the P3ODC register to "11" to select Nch open-drain to the SBO1/SBT1 pin style. Set the P0PLUD2-1 flags of the P0PLUD register to "11" to enable the pull-up resistor. (set the pin corresponding to each serial)
(5) Control the pin direction [set the pin corresponding to each serial] P0DIR (0x03F30) bp2 :P0DIR2 =0 bp0 :P0DIR0 =0	(5) Set the P0DIR2 flag of the port 0 pin direction control register (P0DIR) to "0" and set the P0DIR0 flag to "0" to set P00 and P02 to input mode (set the pin corresponding to each serial)

Setup Procedure	Description
(6) Set the SC1MD0 register 　　Select the transfer bit count 　　SC1MD0 (0x03F99) 　　bp2-0 :SC1LNG2-0 =111 　　Select the start condition 　　SC1MD0 (0x03F99) 　　bp3 :SC1STE =0 　　Select the transfer first bit 　　SC1MD0 (0x03F99) 　　bp4 :SC1DIR =0 　　Select the transfer edge 　　SC1MD0 (0x03F99) 　　bp7 :SC1CE1 =1	(6) Set the SC1LNG2 to 0 flags of the serial 1 mode register (SC1MD0) to "111" to set the transfer bit count to 8 bits. Set the SC1STE flag of the SC1MD0 register to "0" to disable the start condition. Set the SC1DIR flag of the SC1MD0 register to "0" to select MSB as the transfer first bit. Set the SC1CE1 flag of the SC1MD0 register to "1" to set the transmission data input edge to "rising" and the reception data output edge to "falling".
(7) Set the SC1MD1 register 　　Select the communication type 　　SC1MD1 (0x03F9A) 　　bp0 :SC1CMD =0 　　Select the transfer clock 　　SC1MD1 (0x03F9A) 　　bp2 :SC1MST =0 　　bp3 :SC1CKM =0 (serial 0,1 and 2) 　　Control the pin function 　　SC1MD1 (0x03F9A) 　　bp4 :SC1SBOS =0 　　bp5 :SC1SBIS =1 　　bp6 :SC1SBTS =1 　　bp7 :SC1IOM =0	(7) Set the SC1CMD flag of the SC1MD1 register to "0" to select the synchronous serial. Set the SC1MST flag of the SC1MD1 register to "0" to select the clock slave (external clock); and, set the SC1CKM flag to "0" to select "the source clock not divided by 8" for serial 0, 1 and 2. Set the SC1SBIS and SC1SBTS flags of the SC1MD1 register to "1" to set the SBI1 pin to the serial input and the SBT1 pin to the transfer clock input/output. Set the SC1IOM flag "0" to set the serial data input from the SBI1 pin. Set the SC1SBOS flag to "0" to select the port as the SBO1 pin function.
(8) Set the interrupt level 　　PSW 　　bp6 :MIE =0 　　SC1TICR (0x03FF8) 　　bp7-6 :SC1LV1-0 =10	(8) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt level by the SC1LV1 to 0 flags of the serial 1 interrupt control register (SC1TICR).
(9) Enable the interrupt 　　SC1TICR (0x03FF8) 　　bp1 :SC1TIE =1 　　PSW 　　bp6 :MIE =1	(9) Set the SC1TIE flag of the SC1TICR register to "1" to enable the interrupt. If any interrupt request flag (SC1TIR of the SC1TICR register) is already set, clear SC1TIR prior to enabling the interrupt. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.
(10) Start the serial transmission 　　Dummy data → TXBUF1 (0x03F9F)	(10) Set dummy data to the serial transmission data buffer TXBUF1.
(11) Transfer to STOP mode 　　CPUM(0x03F00) 　　bp3:STOP =1	(11) Set the STOP flag of the CPUM register to "1" to transfer to the stop mode.

Setup Procedure	Description
(12) Start the serial communication Transmission clock → input SBT1A pin Received data → input SBI1A pin	(12) Input the transfer clock to the SBT1 pin and transfer data to the SBI1 pin.
(13) Recover from the standby mode	(13) The serial1 communication complete interrupt SC1TIRQ is generated at the same time of the 8th bits data reception, then, CPU is recovered from the stop mode to the normal mode after the oscillation stabilization wait.

*Each setup (1) to (3) and (6) to (7) can be set at the same time.

The slave reception at STANDBY mode should be used without the start condition to receive data properly.

Serial data is input and output from the SBOn pin in communication with 2 channels by connecting the SBOn pin. The port direction control register PnDIR switches I/O. SCnSBIS of the SCnMD1 register must be set to "1" to select "serial data input". The SBIn pin can be used as a general port.

This serial interface has a emergency reset function. If the communication is needed to be stopped by force, set SCnSBOS and SCnSBIS of the SCnMD1 register to "0".

To set each flag, follow the setup procedure in order as described. All control registers (refer to Table:12.2.1, except TXBUFn, RXBUFn and SCnTRB) must be set prior to activating communication.

The transfer rate must be under 5.0 MHz for setting a transfer clock by the SCnMD3 register.

Insert three NOP instructions right after the instruction of the transition to HALT, STOP mode.

12.4 Duplex UART Serial Interface

12.4.1 Operation

Serial interfaces 0, 1, 2 and 3 can be used for duplex UART communication.

> If setting the communication state of this serial interface to "UART", set the mode register (SCnMD1) to the serial interface mode with "H" level of the serial data input pin.

> "n" = 0, 1, 2 and 3 for serial interfaces 0, 1, 2 and 3 respectively in section 12.4.1 Operation.

■ Activation Factor for Communication

Setting data in the transmission data buffer TXBUFn generates a start condition, and transmission will start. Receiving a start condition starts reception. In reception, when the data length of "L" for the start bit is longer than 0.5 bit, a start condition is recognized.

■ Transmission

When data is set in the transmission data buffer TXBUFn, transmission is automatically started. When the transmission is completed, the serial n transmission complete interrupt SCnTIRQ is generated.

■ Reception

When a start condition is recognized, reception is started after the transfer bit counter that counts transfer bits is cleared. When reception is completed, the serial n reception complete interrupt SCnRIRQ is generated.

■ Duplex communication

On duplex communication, transmission and reception can be executed independently at the same time. The frame mode and parity bit of the data used on transmission/reception should have the same polarity.

■ Transfer Bit Count Setup

The transfer bit count is automatically set when the frame mode is specified by the SCnFM1 to 0 flags of the SCnMD2 register. If the SCnCMD flag of the SCnMD1 register is set to "1" and UART communication is selected, the setting of the synchronous serial transfer bit count selection flags SCnLNG2 to 0 of the SCnMD0 register is no more valid.

■ Pin switching

Serial interface n switches pins to A (TXDnA, RXDnA) or B (TXDnB, RXDnB) by the OSLn flag of the SCnSEL register.

■ Data Input Pin Setup

A communication mode can be selected from 2-channel (data output pin (TXDn pin), data input pin (RXDn pin)) mode and 1-channel (data I/O pin TXDn pin) mode. Set the communication mode by the SCnIOM flag of the SC0MD1 register. The RXDn pin can be used only for serial data input. The TXDn pin can be used for serial data input or output. If "data input from the TXDn pin" is selected, the communication mode is 1-channel; so, transmission and reception can be switched by the direction control of the TXDn pin with I/O selection of the port direction control register. At this time, the RXDn pin can be used as a general port since it is not used.

■ Reception Buffer Empty Flag

When the reception complete interrupt SCnRIRQ is generated, data is automatically stored from the internal shift register to RXBUFn . If data is stored in the shift register RXBUFn, the reception buffer empty flag SCnREMP of the SCnSTR register is set to "1". That indicates that the reception data is waiting to be read.

SCnREMP is cleared to "0" by reading the RXBUFn data.

■ Reception BUSY Flag

When a start condition is recognized, the SCnRBSY flag of the SCnSTR register is set to "1". It is cleared to "0" after the reception complete interrupt SCnRIRQ is generated. If the SCnSBIS flag is set to "0" during reception, the SCnRBSY flag is cleared to "0".

■ Transmission BUSY Flag

When data is set in TXBUFn, the SCnTBSY flag of the SCnSTR register is set to "1". It is cleared to "0" after the transmission complete interrupt SCnTIRQ is generated. During continuous communication, the SCnTBSY flag is held in set. If the transmission buffer empty flag SCnTEMP is "0" when the transmission complete interrupt SCnTIRQ is generated, the SCnTBSY is cleared to "0". If the SCnSBOS flag is set to "0" during transmission, the SCnTBSY flag is cleared to "0".

■ Frame Mode and Parity Check Setup

The data format at UART communication is shown below.

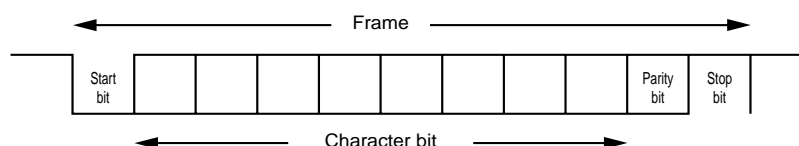Figure:12.4.1 Transmission/Reception Data Format of UART Serial Interface

The transmission/reception data consists of start bit, character bit, parity bit and stop bit. Table:12.4.1 shows the types of data that can be set.

Table:12.4.1 UART Serial Interface Transmission/Reception Data

Start bit	1 bit
Character bit	7,8 bits
Parity bit	fixed at 0, fixed at 1, odd, even, none
Stop bit	1,2 bits

The frame mode is set by the SCnFM1 to 0 flags of the SCnMD2 register. Table:12.4.2 shows the types of frame mode that can be set. If the SCnCMD flag of the SCnMD1 register is set to "1" and UART communication is selected, the transfer bit counts of the SCnLNG2 to 0 flags of the SCnMD0 register are no more valid.

Table:12.4.2 UART Serial Interface Frame Mode

SCnMD2 register		Frame mode
SCnFM1	SCnFM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bits
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

The parity bit is for detecting wrong bits of transmission/reception data. Table:12.4.3 shows the types of the parity bit. The parity bit is set by the SCnNPE and SCnPM1 to 0 flags of the SCnMD2 register.

Table:12.4.3 Parity Bit of UART Serial Interface

SCnMD2			Parity bit	Setup
SCnNPE	SCnPM1	SCnPM0		
0	0	0	Fixed at 0	Set parity bit to "0"
0	0	1	Fixed at 1	Set parity bit to "1"
0	1	0	Odd parity	Control the total of "1" of parity bit and character bit to be odd
0	1	1	Even parity	Control the total of "1" of parity bit and character bit to be even
1	-	-	None	Do not add parity bit

■ Break Status Transmission Control Setup

The SCnBRKE flag of the SCnMD2 register generates the break status. If SCnBRKE is set to "1" to select the break transmission, all bits from start bits to stop bits transfer "0".

■ Reception Error

At reception, there are 3 types of errors; an overrun error, a parity error and a framing error. The reception error can be determined by checking the SCnORE, SCnPEK and SCnFEF flags of the SCnSTR register. If one of these flags has an error, the SCnERE flag of the SCnSTR register is set to "1". The SCnPEK and SCnFEF flags of the reception error flags are renewed at generation of the reception complete interrupt SCnRIRQ. The SCnORE flag is cleared simultaneously when the next communication complete interrupt SCnRIRQ is generated after the RXBUFn data is read. The the reception error determination should be operated before the next communication is completed. Those error flags have no effects on communication operation. Table:12.4.4 shows reception error factors of reception errors.

Table:12.4.4 Reception Error Factors of UART Serial Interface

Flag	Reception error		
SCnORE	Overrun error	Next data is received before reading the reception buffer	
SCnPEK	Parity error	At fixed to 0	when parity bit is "1"
		At fixed to 1	When parity bit is "0"
		Odd parity	When the total of "1" of parity bit and character bit is even
		Even parity	When the total of "1" of parity bit and character bit is odd
SCnFEF	Framing error	Stop bit is not detected	

■ Determination of Break Status Reception

Reception at break status can be determined by the SCnBRKF flag. If all received data from the start bit and the stop bit are "0", the SCnBRKF flag of the SCnMD2 register is set and determines that the break status is generated. The SCnBRKF flag is set at the reception complete interrupt SCnRIRQ generation.

■ Continuous Transmission

This serial interface has a continuous transfer function. If data is set in the transmission data buffer TXBUFn during transmission, the transmission buffer empty flag SCnTEMP is set and continue transmission is operated automatically. Any communication blanks are generated. Set the next data to TXBUFn before the transmission complete interrupt SCnTIRQ is generated since data is setup to tranmission shift register.

■ Clock Setup

A transfer clock is not necessary at UART communication, but the clock setup is necessary for determining the data transmission/reception timing within the serial interface. Select the timer used as a baud rate timer by the SCnMD3 register.

The SCnSBIS and SCnSBOS flags of the SCnMD1 should be set to "0" before switching the clock setting.

■ Receive Bit Count and First Transfer Bit

In reception, when transfer bit counts = 7 bits, the data storing method for the reception data buffer RXBUFn differs depending on the first transfer bit specification. At MSB first, data are stored in the upper bits of RXBUFn. When transfer bit counts = 7 bits, as shown on Figure:12.4.2, data "A" to "G" are stored in bp7 to bp1 of RXBUFn. At LSB first, data are stored in the lower bits of RXBUFn. When transfer bit counts = 7 bits, as shown on Figure:12.4.3, data "A" to "G" are stored in bp0 to bp6 of RXBUFn.
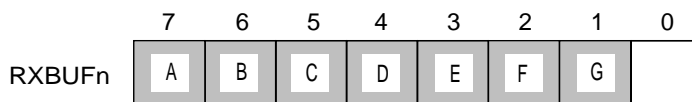

Figure:12.4.2 Receive Bit Count and First Transfer Bit (At MSB First)
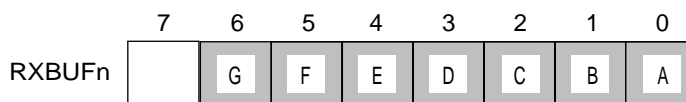

Figure:12.4.3 Receive Bit Count and First Transfer Bit (At LSB First)

■ Transfer Speed Setup

The transfer speed can be set using a baud rate timer. The setup example for the transfer speed is shown below.

Table:12.4.5 UART Serial Interface Transfer Speed

	Setup	Register	Page
Serials 0-3	Serial 0 to 3 clock source (timers 0-4 and A outputs)	SC0MD3	XII-28
		SC1MD3	XII-28
		SC2MD3	XII-28
		SC3MD3	XII-28
	Timer 0 clock sourcer	TM0MD	V-16
	Timer 1 clock sourcer	TM1MD	V-17
	Timer 2 clock source	TM2MD	V-18
	Timer 3 clock source	TM3MD	V-19
	Timer 4 clock source	TM4MD	V-20
	Timer A clock source	TMAMD	VI-6
	Timer 0 compare register	TM0OC	V-13
	Timer 1 compare register	TM1OC	V-13
	Timer 2 compare register	TM2OC	V-13
	Timer 3 compare register	TM3OC	V-13
	Timer 4 compare register	TM4OC	V-14
	Timer A compare register	TMAOC	VI-5

Timer compare register is set as follows;

overflow cycle = (set value of compare register + 1) × timer clock cycle

baud rate = 1 / (overflow cycle × 2 ×8)("8" is divide-by-8 clock source)

therefore,

set value of compare register = timer clock frequency/(baud rate × 2 × 8) - 1

For example, when setting the baud rate to 300 bps at clock source fs/4 (fpll = 8 MHz, fs = fpll/2), the set value should be as follows:

set value of compare register = $(8 \times 10^6/2/4)/(300 \times 2 \times 8)$ - 1

$$= 207$$

$$= 0xCF$$

The following pages show the timer clock source at the standard transfer rate and the set value of the compare register when fs=fpll/2.

Transfer rate should be selected under 300 kbps.

fpll (MHz)	Clock source (timer)	Transfer speed (bit/s)									
		300		960		1200		2400		4800	
		Set value	Calculated value	Set value	Calculated value	Set value	Calculated value	Set value	Calculated value	Set value	Calculated value
4.00	fpll	-	-	-	-	207	1202	103	2404	51	4808
	fpll/4	207	300	64	962	51	1202	25	2404	12	4808
	fpll/16	51	300	-	-	12	1202	-	-	-	-
	fpll/32	25	300	-	-	-	-	-	-	-	-
	fpll/64	12	300	-	-	-	-	-	-	-	-
	fs/2	207	300	64	962	51	1202	25	2404	12	4808
	fs/4	104	297	-	-	25	1202	12	2404	-	-
4.19	fpll	-	-	-	-	217	1201	108	2403	54	4761
	fpll/4	217	300	67	963	-	-	-	-	-	-
	fpll/16	-	-	16	963	-	-	6	2338	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	217	300	67	963	-	-	-	-	-	-
	fs/4	108	300	33	963	-	-	13	2338	-	-
8.00	fpll	-	-	-	-	-	-	207	2404	103	4808
	fpll/4	-	-	129	962	103	1202	51	2404	25	4808
	fpll/16	103	300	-	-	25	1202	12	2404	-	-
	fpll/32	51	300	-	-	12	1202	-	-	-	-
	fpll/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	129	962	103	1202	51	2404	25	4808
	fs/4	207	300	64	962	51	1202	25	2404	12	4808
8.38	fpll	-	-	-	-	-	-	217	2403	108	4805
	fpll/4	-	-	135	963	108	1201	-	-	-	-
	fpll/16	108	300	33	963	-	-	13	2338	-	-
	fpll/32	-	-	16	963	-	-	6	2338	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	135	963	108	1201	-	-	-	-
	fs/4	217	300	67	963	-	-	-	-	-	-
12.00	fpll	-	-	-	-	-	-	-	-	155	4808
	fpll/4	-	-	194	962	155	1202	77	2404	38	4808
	fpll/16	155	300	-	-	38	1202	-	-	-	-
	fpll/32	77	300	-	-	-	-	-	-	-	-
	fpll/64	38	300	-	-	-	-	-	-	-	-
	fs/2	-	-	194	962	155	1202	77	2404	38	4808
	fs/4	-	-	-	-	77	1202	38	2404	-	-
16.00	fpll	-	-	-	-	-	-	-	-	207	4808
	fpll/4	-	-	-	-	207	1202	103	2404	51	4808
	fpll/16	207	300	64	962	51	1202	25	2404	12	4808
	fpll/32	103	300	-	-	25	1202	12	2404	-	-
	fpll/64	51	300	-	-	12	1202	-	-	-	-
	fs/2	-	-	-	-	207	1202	103	2404	51	4808
	fs/4	-	-	129	962	103	1202	51	2404	25	4808
20.00	fpll	-	-	-	-	-	-	-	-	-	-
	fpll/4	-	-	-	-	-	-	129	2404	64	4808
	fpll/16	-	-	-	-	64	1202	-	-	-	-
	fpll/32	129	300	-	-	-	-	-	-	-	-
	fpll/64	64	300	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	129	2404	64	4808
	fs/4	-	-	162	959	129	1202	64	2404	-	-

Figure:12.4.4 Setup Value of UART Serial Interface Transfer Speed (decimal)
when setting devide-by-8 clock source

fpll (MHz)	Clock source (timer)	Transfer speed (bit/s)									
		9600		19200		28800		31250		38400	
		Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value
4.00	fpll	25	9615	12	19231	-	-	7	31250	-	-
	fpll/4	-	-	-	-	-	-	1	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
4.19	fpll	26	9699	-	-	-	-	-	-	-	-
	fpll/4	-	-	-	-	-	-	-	-	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
8.00	fpll	51	9615	25	19231	-	-	15	31250	12	38462
	fpll/4	12	9615	-	-	-	-	3	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
8.38	fpll	54	9523	26	19398	-	-	-	-	-	-
	fpll/4	-	-	-	-	-	-	-	-	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
12.00	fpll	77	9615	38	19231	25	28846	23	31250	-	-
	fpll/4	-	-	-	-	-	-	5	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	5	31250	-	-
	fs/4	-	-	-	-	-	-	2	31250	-	-
16.00	fpll	103	9615	51	19231	-	-	31	31250	25	38462
	fpll/4	25	9615	12	19231	-	-	7	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	25	9615	-	-	-	-	7	31250	-	-
	fs/4	12	9615	-	-	-	-	2	31250	-	-
20.00	fpll	129	9615	64	19231	-	-	39	31250	-	-
	fpll/4	-	-	-	-	-	-	9	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	9	31250	-	-
	fs/4	-	-	-	-	-	-	4	31250	-	-

Figure:12.4.5 Setup Value of UART Serial Interface Transfer Speed (decimal)
when setting devide-by-8 clock source

fpll (MHz)	Clock source (timer)	Transfer speed (bit/s)									
		300		960		1200		2400		4800	
		Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value
4.00	fpll	-	-	129	962	103	1202	51	2404	25	4808
	fpll/4	104	297	-	-	25	1202	12	2404	-	-
	fpll/16	25	300	-	-	-	-	-	-	-	-
	fpll/32	12	300	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	103	300	-	-	25	1202	12	2404	-	-
	fs/4	51	297	-	-	12	1202	-	-	-	-
	fs/8	25	300	-	-	-	-	-	-	-	-
4.19	fpll	-	-	135	963	108	1201	-	-	-	-
	fpll/4	109	297	33	963	-	-	-	-	-	-
	fpll/16	26	303	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	109	297	33	963	-	-	-	-	-	-
	fs/4	54	297	16	963	-	-	6	2338	-	-
	fs/8	26	303	-	-	-	-			-	-
8.00	fpll	-	-	-	-	-	-	103	2404	51	4808
	fpll/4	208	300	64	962	51	1202	25	2404	12	4808
	fpll/16	51	300	-	-	12	1202	-	-	-	-
	fpll/32	25	300	-	-	-	a	-	-	-	-
	fpll/64	12	300	-	-	-	-	-	-	-	-
	fs/2	208	300	64	962	51	1202	25	2404	12	4808
	fs/4	103	300	-	-	25	1202	12	2404	-	-
	fs/8	51	300	-	-	12	1202	-	-	-	-
8.38	fpll	-	-	-	-	217	1202	108	2403	-	-
	fpll/4	218	300	67	963	-	-	27	2338	-	-
	fpll/16	55	297	16	963	-	-	6	2338	-	-
	fpll/32	27	303	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	67	963	-	-	27	2338	-	-
	fs/4	109	300	33	963	-	-	13	2338	-	-
	fs/8	55	297	16	963	-	-	6	2338	-	-
12.00	fpll	-	-	-	-	-	-	155	2404	77	4808
	fpll/4	-	-	-	-	77	1202	38	2404	-	-
	fpll/16	77	300	-	-	-	-	-	-	-	-
	fpll/32	38	300	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	77	1202	38	2404	-	-
	fs/4	154	302	-	-	38	1202	-	-	-	-
	fs/8	77	300	-	-	-	-	-	-	-	-
16.00	fpll	-	-	-	-	-	-	207	2404	103	4808
	fpll/4	-	-	-	-	103	1202	51	2404	25	4808
	fpll/16	103	300	-	-	25	1202	12	2404	-	-
	fpll/32	51	300	-	-	12	1202	-	-	-	-
	fpll/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	103	1202	51	2404	25	4808
	fs/4	208	300	64	962	51	1202	25	2404	12	4808
	fs/8	103	300	-	-	25	1202	12	2404	-	-
20.00	fpll	-	-	-	-	-	-	-	-	-	-
	fpll/4	-	--	162	959	129	1201	64	2403	-	-
	fpll/16	129	300	-	-	-	-	-	-	-	-
	fpll/32	64	300	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	--	-	-
	fs/2	-	-	162	959	129	1201	64	2403	-	-
	fs/4	129	300	80	965	64	1201	-	-	-	-
	fs/8	129	300	-	-	-	-	-	-	-	-

Figure:12.4.6 Setup Value of UART Serial Interface Transfer Speed (decimal)
when setting devide-by-16 clock source

fpll (MHz)	Clock source (timer)	Transfer speed (bit/s)									
		9600		19200		28800		31250		38400	
		Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value	Set value	Caluculated value
4.00	fpll	12	9615	-	-	-	-	3	31250	-	-
	fpll/4	-	-	-	-	-	-	-	-	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-
4.19	fpll	-	-	-	-	-	-	-	-	-	-
	fpll/4	-	-	-	-	-	-	-	-	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-
8.00	fpll	25	9615	12	19231	-	-	7	31250	-	-
	fpll/4	-	-	-	-	-	-	1	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-
8.38	fpll	26	9699	-	-	-	-	-	-	-	-
	fpll/4	-	-	-	-	-	-	-	-	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-
12.00	fpll	38	9615	-	-	12	28847	11	31251	-	-
	fpll/4	-	-	-	-	-	-	2	31251	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	2	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-
16.00	fpll	51	9615	25	19231	-	-	11	31250	12	38462
	fpll/4	12	9615	-	-	-	-	3	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-
20.00	fpll	64	9615	-	-	-	-	19	31250	-	-
	fpll/4	-	-	-	-	-	-	4	31250	-	-
	fpll/16	-	-	-	-	-	-	-	-	-	-
	fpll/32	-	-	-	-	-	-	-	-	-	-
	fpll/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	4	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
	fs/8	-	-	-	-	-	-	-	-	-	-

Figure:12.4.7 Setup Value of UART Serial Interface Transfer Speed (decimal)
when setting devide-by-16 clock source

The items shown below are the same as clock synchronous serial. Refer to the following pages.

■ First Transfer Bit Setup

Refer to: XII-43

■ Transmission Data Buffer

Refer to: XII-43

■ Reception Data Buffer

Refer to: XII-44

■ Transmit Bit Count and First Transfer Bit

Refer to: XII-44

■ Transmission Buffer Empty Flag

Refer to: XII-48

■ Emergency Reset

Refer to: XII-49

12.4.2   Timing

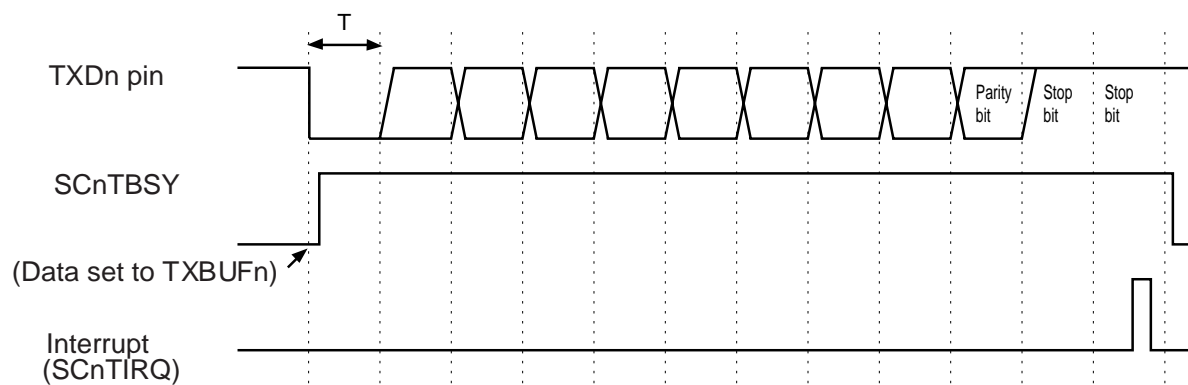■ Transmission Timing

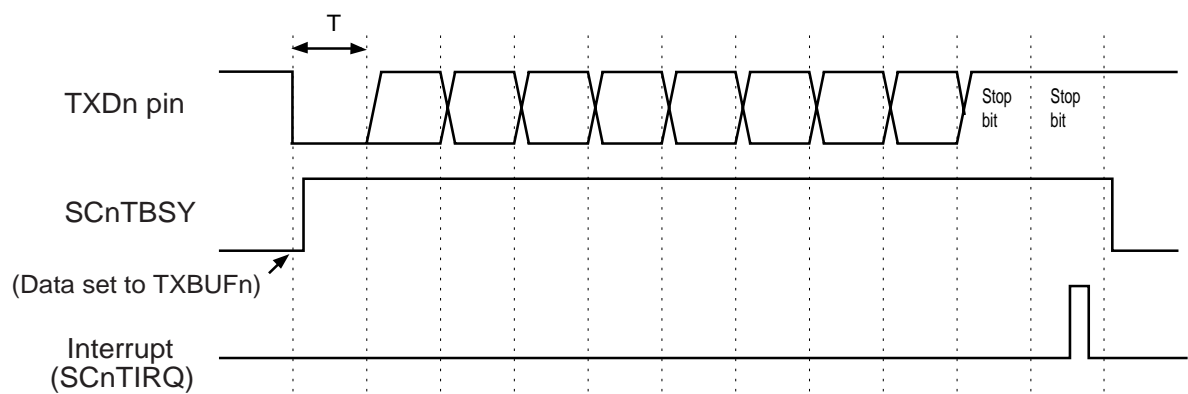Figure:12.4.8 Transmission Timing (Parity Bit is Enabled)

Figure:12.4.9 Transmission Timing (Parity Bit is Disabled)
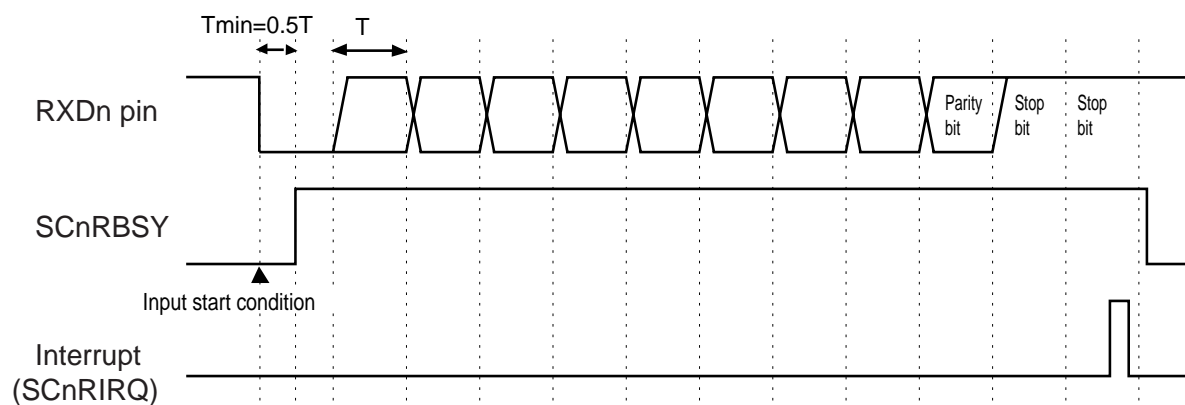
■ Reception Timing

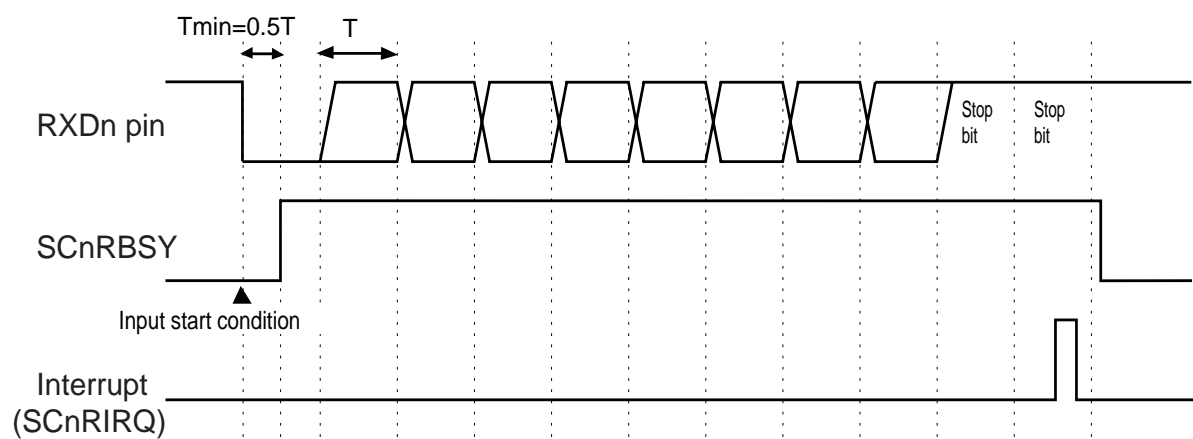Figure:12.4.10 Reception Timing (Parity Bit is Enabled)

Figure:12.4.11 Reception Timing (Parity Bit is Disabled)

12.4.3   Pin Setup

■ UART Serial Interface 0 Pin Setup

Port	Channel	Type	Pin	Pin setup (flag setup)						
				SC0SEL register	PnDIR register	PnODC register	PnPLUD register	SC0MD1 register		
				Serial 0 I/O pin switching	I/O mode selection	Nch open-drain output selection	Pull-up/pull-down resistor selection	Serial data input selection	Serial input control selection	SBO0 (TXD0) pin function selection
						Aribitary setting	Aribitary setting			
				0:P50-P51	0: input mode	0: push/pull	0: not added	0: data input from RXD0	0:"1" input	0: port
				1:P43-P44	1: output mode	1:Nch open-drain	1: added	1: data input from TXD0	1: serial input	1: serial data output
				OSL0	PnDIRm	PnODCm	PnPLUDm	SC0IOM	SC0SBIS	SC0SBOS
P5	2 channels	Transmission only	P50/TXD0A	0	P5DIR0:1	P5ODC0	P5PLUD0	0	0	1
			-		-	-	-			
		Reception only	-	0	-	-	-	0	1	0
			P51/RXD0A		P5DIR1:0	-	-			
		Transmission /reception	P50/TXD0A	0	P5DIR0:1	P5ODC0	P5PLUD0	0	1	1
			P51/RXD0A		P5DIR1:0	-	-			
	1 channel	Transmission	P50/TXD0A	0	P5DIR0:1	P5ODC0	P5PLUD0	0	0	1
			-		-	-	-			
		Reception	P50/TXD0A	0	P5DIR0:1	P5ODC0	P5PLUD0	1	1	0
			-		-	-	-			
P4	2 channels	Transmission only	P43/TXD0B	1	P4DIR3:1	P4ODC3	P4PLUD3	0	0	1
			-		-	-	-			
		Reception only	-	1	-	-	-	0	1	0
			P44/RXD0B		P4DIR4:0	-	-			
		Transmission /reception	P43/TXD0B	1	P4DIR3:1	P4ODC3	P4PLUD3	0	1	1
			P44/RXD0B		P4DIR4:0	-	-			
	1 channel	Transmission	P43/TXD0B	1	P4DIR3:1	P4ODC3	P4PLUD3	1	0	1
			-		-	-	-			
		Reception	P43/TXD0B	1	P4DIR3:1	P4ODC3	P4PLUD3	1	1	0
			-		-	-	-			

■ UART Serial Interface 1 Pin Setup

Port	Channel	Type	Pin	SC1SEL register — Serial 1 I/O pin switching — 0:P00-P01 / 1:P75-P76 — OSL1	PnDIR register — I/O mode selection — 0: input mode / 1: output mode — PnDIRm	PnODC register — Nch open-drain output selection — Aribitary setting — 0: push/pull / 1:Nch open-drain — PnODCm	PnPLUD register — Pull-up/pull-down resistor selection — Aribitary setting — 0: not added / 1: added — PnPLUDm	SC1MD1 register — Serial data input selection — 0: data input from RXD1 / 1: data input from TXD1 — SC1IOM	SC1MD1 register — Serial input control selection — 0:"1" input / 1: serial input — SC1SBIS	SC1MD1 register — SBO1 (TXD1) pin function selection — 0: port / 1: serial data output — SC1SBOS
P0	2 channels	Transmission only	P01/TXD1A	0	P0DIR1:1	P0ODC1	P0PLUD1	0	0	1
			-		-	-	-			
		Reception only	-	0	-	-	-	0	1	0
			P00/RXD1A		P0DIR0:0	-	-			
		Transmission /reception	P01/TXD1A	0	P0DIR1:1	P0ODC1	P0PLUD1	0	1	1
			P00/RXD1A		P0DIR0:0	-	-			
	1 channel	Transmission	P01/TXD1A	0	P0DIR1:1	P0ODC1	P0PLUD1	0	0	1
			-		-	-	-			
		Reception	P01/TXD1A	0	P0DIR1:1	P0ODC1	P0PLUD1	1	1	0
			-		-	-	-			
P7	2 channels	Transmission only	P75/TXD1B	1	P7DIR5:1	P7ODC5	P7PLUD5	0	0	1
			-		-	-	-			
		Reception only	-	1	-	-	-	0	1	0
			P76/RXD1B		P7DIR6:0	-	-			
		Transmission /reception	P75/TXD1B	1	P7DIR5:1	P7ODC5	P7PLUD5	0	1	1
			P76/RXD1B		P7DIR6:0	-	-			
	1 channel	Transmission	P75/TXD1B	1	P7DIR5:1	P7ODC5	P7PLUD5	1	0	1
			-		-	-	-			
		Reception	P75/TXD1B	1	P7DIR5:1	P7ODC5	P7PLUD5	1	1	0
			-		-	-	-			

■ UART Serial Interface 2 Pin Setup

Port	Channel	Type	Pin	Pin setup (flag setup)						
				SC2SEL register	PnDIR register	PnODC register	PnPLUD register	SC2MD1 register		
				Serial 2 I/O pin switching	I/O mode selection	Nch open-drain output selection	Pull-up/pull-down resistor selection	Serial data input selection	Serial input control selection	SBO2 (TXD2) pin function selection
						Aribitary setting	Aribitary setting			
				0:P70-P71	0: input mode	0: push/pull	0: not added	0: data input from RXD2	0:"1" input	0: port
				1:P30-P31	1: output mode	1:Nch open-drain	1: added	1: data input from TXD2	1: serial input	1: serial data output
				OSL2	PnDIRm	PnODCm	PnPLUDm	SC2IOM	SC2SBIS	SC2SBOS
P7	2 channels	Transmission only	P70/TXD2A	0	P7DIR0:1	P7ODC0	P7PLUD0	0	0	1
			-		-	-	-			
		Reception only	-	0	-	-	-	0	1	0
			P71/RXD2A		P7DIR1:0	-	-			
		Transmission /reception	P70/TXD2A	0	P7DIR0:1	P7ODC0	P7PLUD0	0	1	1
			P71/RXD2A		P7DIR1:0	-	-			
	1 channel	Transmission	P70/TXD2A	0	P7DIR0:1	P7ODC0	P7PLUD0	0	0	1
			-		-	-	-			
		Reception	P70/TXD2A	0	P7DIR0:1	P7ODC0	P7PLUD0	1	1	0
			-		-	-	-			
P3	2 channels	Transmission only	P30/TXD2B	1	P3DIR0:1	P3ODC0	P3PLUD0	0	0	1
			-		-	-	-			
		Reception only	-	1	-	-	-	0	1	0
			P31/RXD2B		P3DIR1:0	-	-			
		Transmission /reception	P30/TXD2B	1	P3DIR0:1	P3ODC0	P3PLUD0	0	1	1
			P31/RXD2B		P3DIR1:0	-	-			
	1 channel	Transmission	P30/TXD2B	1	P3DIR0:1	P3ODC0	P3PLUD0	1	0	1
			-		-	-	-			
		Reception	P30/TXD2B	1	P3DIR0:1	P3ODC0	P3PLUD0	1	1	0
			-		-	-	-			

■ UART Serial Interface 3 Pin Setup

Port	Channel	Type	Pin	Pin setup (flag setup)						
				SC3SEL register	PnDIR register	PnODC register	PnPLUD register	SC3MD1 register		
				Serial 3 I/O pin switching	I/O mode selection	Nch open-drain output selection	Pull-up/pull-down resistor selection	Serial data input selection	Serial input control selection	SBO3 (TXD3) pin function selection
						Aribitary setting	Aribitary setting			
				0:P04-P05	0: input mode	0: push/pull	0: not added	0: data input from RXD3	0:"1" input	0: port
				1:P40-P41	1: output mode	1:Nch open-drain	1: added	1: data input from TXD3	1: serial input	1: serial data output
				OSL3	PnDIRm	PnODCm	PnPLUDm	SC3IOM	SC3SBIS	SC3SBOS
P0	2 channels	Transmission only	P04/TXD3A -	0	P0DIR4:1 -	P0ODC4 -	P0PLUD4 -	0	0	1
		Reception only	- P05/RXD3A	0	- P0DIR5:0	- -	- -	0	1	0
		Transmission /reception	P04/TXD3A P05/RXD3A	0	P0DIR4:1 P0DIR5:0	P0ODC4 -	P0PLUD4 -	0	1	1
	1 channel	Transmission	P04/TXD3A -	0	P0DIR4:1 -	P0ODC4 -	P0PLUD4 -	0	0	1
		Reception	P04/TXD3A -	0	P0DIR4:1 -	P0ODC4 -	P0PLUD4 -	1	1	0
P4	2 channels	Transmission only	P40/TXD3B -	1	P4DIR0:1 -	P4ODC0 -	P4PLUD0 -	0	0	1
		Reception only	- P41/RXD3B	1	- P4DIR1:0	- -	- -	0	1	0
		Transmission /reception	P40/TXD3B P41/RXD3B	1	P4DIR0:1 P4DIR1:0	P4ODC0 -	P4PLUD0 -	0	1	1
	1 channel	Transmission	P40/TXD3B -	1	P4DIR0:1 -	P4ODC0 -	P4PLUD0 -	1	0	1
		Reception	P40/TXD3B -	1	P4DIR0:1 -	P4ODC0 -	P4PLUD0 -	1	1	0

12.4.4   Setup Example

■ Transmission/Reception Setup

The setup example at UART transmission/reception using serial 1 is shown below. Table:12.4.6 shows the conditions at transmission/reception. The basic procedures are the same in serials 0, 2 and 3. Pin settings (3) and (4) differ in each serial.

Table:12.4.6 UART Interface Transmission Reception Setup Condition

Setup item	Set to
Serial data input selection	RXD1A
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer A
TXD1/RXD1 pin style	Nch open-drain
Pull-up resistor of TXD1 pin	Added
Parity bit add/check	"0" added/checked
Serial 1 transmission complete interrupt	Enabled
Serial 1 reception complete interrupt	Enabled

An example setup procedure, with a description of each step is shown below

Setup Procedure	Description

(1) Select the clock source
   SC1SEL (0x03FA0)
   bp2-0 :SC1SEL2-0 =111
   SC1MD3 (0x03FA0)
   bp2-0 :SC1PSC2-0 =111
	(1) Set the SC1SEL2-0 flags of the SC1SEL register and the SC1PSC2-0 flags of the SC1MD3 register to "111" to select timer A output as a clock source.

(2) Control the pin style [set the pin corresponding to each serial]
   P0ODC (0x03EF0)
   bp1-0 :P0ODC1-0 =11
   P0PLUD (0x03F40)
   bp0 :P0PLUD0 =1
	(2) Set the P0ODC1-0 flags of the P0ODC register to "11" to select Nch open-drain as styles of the TXD0 pin and the RXD0 pin. Set the P0PLUD0 flag of the P0PLUD register to "1" to enable the pull-up resistor. (set the pin corresponding to each serial.)

(3) Control the pin direction [set the pin corresponding to each serial]
   P0DIR(0x03F30)
   bp1-0 :P0DIR1-0 =01
	(3) Set the P0DIR1-0 flags of the port 0 direction control register (P0DIR) to "01" to set P00 to output mode and P01 to input mode
	(set the pin corresponding to each serial.).

(4) Set the SC1MD0 register
   Select the start condition
   SC1MD0 (0x03F99)
   bp3 :SC1STE =1
 	
   Select the transfer first bit
   SC1MD0 (0x03F99)
   bp4 :SC1DIR =0
	(4) Set the SC1STE flag of the SC1MD0 register to "1" to enable start condition.
	
	Set the SC1DIR flag of the SC1MD0 register to "0" to select MSB as the transfer first bit.

Setup Procedure	Description
(5) Set the SC1MD2 register 　Control the output data 　SC1MD2 (0x03F9B) 　bp0 :SC1BRKE =0 　Select the added parity bit 　SC1MD2 (0x03F9B) 　bp3 :SC1NPE =0 　bp5-4 :SC1PM1-0 =00 　Specify the frame mode 　SC1MD2 (0x03F9B) 　bp7-6 :SC1FM1-0 =11	(5) Set the SC1BRKE flag of the SC1MD2 register to "0" to select serial data transmission. 　Set the SC1PM1 to 0 flags of the SC1MD2 register to "00" to select 0 parity, and set the SC1NPE flag to "0" to enable add parity bit. 　Set the SC1FM1 to 0 flags of the SC1MD2 register to "11" to select 8 bits + 2 stop bits at the frame mode.
(6) Set the SC1MD1 register 　Select the communication type 　SC1MD1 (0x03F9A) 　bp0 :SC1CMD =1 　Select the clock dividing 　SC1MD1 (0x03F9A) 　bp3 :SC1CKM =1 　bp2 :SC1MST =1 　Control the pin function 　SC1MD1 (0x03F9A) 　bp4 :SC1SBOS =1 　bp5 :SC1SBIS =1 　bp7 :SC1IOM =0	(6) Set the SC1CMD flag of the SC1MD1 register to "1" to select the duplex UART. 　Set the SC1CKM flag of the SC1MD1 register to "1" to select "divided by 8" at source clock. 　The SC1MST flag should be always set to "1" to select a clock master. 　Set the SC1SBOS and SC1SBIS flags of the SC1MD1 register to "1" to set the TXD0 pin to serial data output and the RXD1 pin to serial data input.
(7) Set the baud rate timer	(7) Set the baud rate by the TMAMD register and the TMAOC register. Set the TMAEN flag to "1" to operate timer A. 　 [Chapter VI 6.4 Serial Transfer Clock Output]
(8) Enable the interrupt 　PSW 　bp6 :MIE =0 　IRQEPEN(0x03F4E) 　bp1 :IRQEPEN1 =1 　PERIICR(0x03FFE) 　bp1 :PERIIE =1 　SC1TICR (0x03FF8) 　bp1 :SC1TIE =1 　PSW 　bp6 :MIE =1	(8) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the IRQEPEN1 flag of IRQEPEN register to "1" to enable the serial 1 URAT reception interrupt. Set the PERIIE flag of the PERIICR register to "1", and the SC1TIE flag of the SC1TICR register to "1" to enable the interrupt request. If any the interrupt request is already set, clear the request flag. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.
(9) Start the serial transmission 　The transmission → TXBUF1 (0x03F9F) 　The reception data → input to the RXD1A pin	(9) Transmission is started by setting transmission data to the serial transmission data buffer (TXBUF1). When the transmission is finished, the serial 1 transmission complete interrupt (SC1TIRQ) is generated. If a start bit is detected, the received data is loaded into the RXBUF1; and, the serial 1 reception complete interrupt (SC1RIRQ) is generated..

* Each setup in (5), (6) and (7) can be set at the same time.

Serial data is input/output from the TXDn pin for 1-channel communication with connecting the TXDn/RXDn pin. The port direction control register switches I/O. In reception, set SCnS-BIS of the SCnMD1 register to "1" to select serial data input. The RXDn pin can be used as a general port.

This serial interface has an emergency reset function. If communication is needed to be stopped by force, set SCnSBOS and SCnSBIS of the SCnMD1 register to "0".

To set each flag, follow the setup procedure in order as described. All control registers (refer to Table:12.2.1, except TXBUFn and RXBUFn) must be set prior to activating communication.

When communication format of this serial interface set to "UART", set the Serial interface n mode register 1 (SCnMD1) by serial data input pin is set to "H" level.

12.5 Multi Master IIC Interface

12.5.1 Multi Master IIC Interface

Multi master IIC serial communication is available with serial interface 4. This IIC interface communicates by complying with the data transfer format of Philips IIC-BUS. Table:12.1.5 shows IIC serial interface functions.

■ Data I/O Pin Setup

Use the SDA4 pin (common use with SBO4 pin) for data input/output. Set the SC4IOM flag of the SC4MD1 register to "1" to input the serial data from the SDA4 (SBO4) pin. The SBI4 pin can be used as a general port; make sure to set the SC4SBIS flag of the SC4MD1 register to "1" to set "serial data input".

> Make sure to set the SC4SBIS flag of the SC4MD1 register to "serial data input" regardless of transmission/reception in order to detect the start condition and ACK bit reception.

> Nch open-drain should be used for pin format because the bus is switched between use and open by hardware during communication. Even in reception, select "output" for direction control of the SDA4 pin (SBO4 pin).

■ Input Edge/Output Edge Setup

In IIC communication, data is always received at the falling edge of the clock regardless of the SC4CE1 value.

■ Master/Slave Selection

Multi master IIC function (clock master/clock slave) or slave-dedicated IIC function (clock slave) can be selected with the SC4MST of the SC4MD1 register. To switch to clock slave operation from clock master operation, detect the start condition from another master or detect the arbitration lost at the clock master operation.

■ Slave Address Setup

This serial interface can set 7-bit slave address.

■ Transfer Format

Two formats are available for IIC bus transfer; addressing format and free data format. In addressing format, 1 to 2 byte address data which consists of the slave address (7/10 bits) and R/W bit (1 bit) is transmitted after the start condition, and transmission/reception is executed. In free data format, data is transmitted immediately after the start condition. Regarding the free data format, this LSI only supports IIC master communication. The following presents the communication sequences. The shaded regions of Figure:12.5.1,Figure:12.5.2,Figure:12.5.3 are the data transmitted from other IIC.
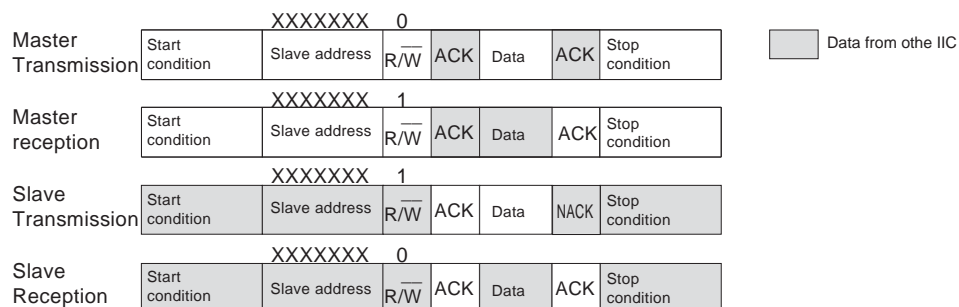
■ Addressing Format

• 7 bit address

Figure:12.5.1 Communication Sequence in 7 bit Address Mode
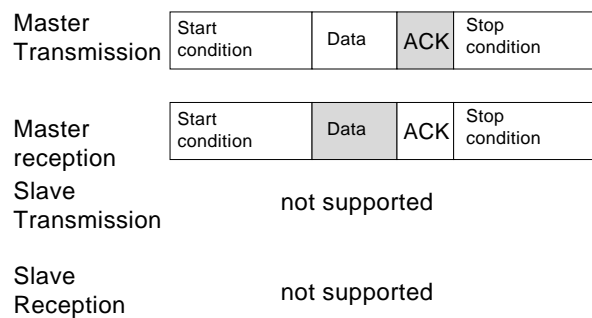
• Free data format

Figure:12.5.2 Communication Sequence in Free Data Format

■ Clock Setup

The clock source is selected from the dedicated prescaler and timer output (timers 0-4, A) with the SC4MD2 register. The dedicated prescaler starts to operate by selecting "prescaler count enable" with the SC4MD2.

The following table shows the clock source selection condition.

Table:12.5.1 Clock Source Selection Condition

Communication condition	Clock source selection condition
Master communication only (when only this IIC is set as the master)	Standard mode: 800 kHz or less High-speed mode: 3.2 MHz or less
Master/slave communication	Standard mode: 500 kHz or more, 800 kHz or less High-speed mode: 3.2 MHz
Slave communication only (when SC4MST=0)	Standard mode: 500 kHz or more High-speed mode: 3.4 MHz or more

In master communication, the transfer clock is obtained by dividing the clock source by 8. Duty is H:L=1:1 in standard mode and H:L=3:5 in high-speed mode. In master communication, set the clock source so that the transfer clock is not over 100 kHz in standard mode and 400 kHz in high-speed mode. Select the transfer rate so that its value is 0.8 times or over of other master.

In slave communication, Set the clock source to 500 kHz or over in standard mode and 3.4 MHz or over in high-speed mode. However, when the transfer rate and duty of the master are identified, any clock source which satisfies the following conditions can be selected.

Table:12.5.2 Transfer Rate Duty and Clock Source Selection Condition

Transfer rate duty	Slave clock source selection condition
1:1	Transfer rate $\times$ 4 or over
1:2/2:1	Transfer rate $\times$ 6 or over
1:3/3:1	Transfer rate $\times$ 8 or over

Table:12.5.3 IIC Interface Clock Source

	Multi master IIC
Clock source (Internal clock)	fpll/2
	fpll/4
	fpll/16
	fpll/32
	fs/2
	fs/4
	Timer output (0 to 4, A)

In IIC master communication, transfer clock is obtained by dividing the clock source by 8. In master communication, set the clock source with the SC4MD2 register so that the transfer clock is not over 100 kHz in the standard mode and 400 kHz in the high-speed mode. Select the transfer rate which is more than 0.8 times of the other master.

In slave communication, set the clock source to 500 kHz or over in the standard mode, 3.4 MHz or over in the high-speed mode, or set to the value which is 6 times or larger than the transfer rate.

When switching the clock setup, always set the SC4SBIS flag and SC4SBOS flag of the SC4MD1 register to "0" before switching the clock setting.

■ Activation Factor for Communication

(Master communication)

Set data (at transmission) or dummy data (at reception) in the transmission buffer (TXBUF4). The start condition and the transfer clock are generated, and communication starts regardless of transmission/reception.

(Slave communication)

Detecting the start condition starts reception. When the received address matches the address set by the address set registers 0 and 1, or a general call is detected, the slave address compare flag is set and slave communication starts.

■ Interrupt

Two interrupts, a communication complete interrupt and a stop condition detection interrupt, are available in this serial interface. Table:12.5.4 presents the interrupt generation factors.

Table:12.5.4 IIC Communication Generation Factor

Interrupt	Interrupt generation factor
Communication complete interrupt	Master communication completed (after 1 byte data + ACK) Slave address matched (after ACK) Slave communication completed (after 1 byte data + ACK) Slave communication completed (communication data instability detection)
Stop condition detection interrupt	Detection of other master-generated stop condition

■ Start Condition Setup

In master communication, a start condition is always generated at the first communication despite the SC4STE value of the SC4MD0 register. Select whether the start condition is enabled or disabled after the second byte communication by the SC4STE of the SC4MD0 register.

Enable/disable of the start condition can be determined in each communication by setting the enable/disable before each communication data setup.
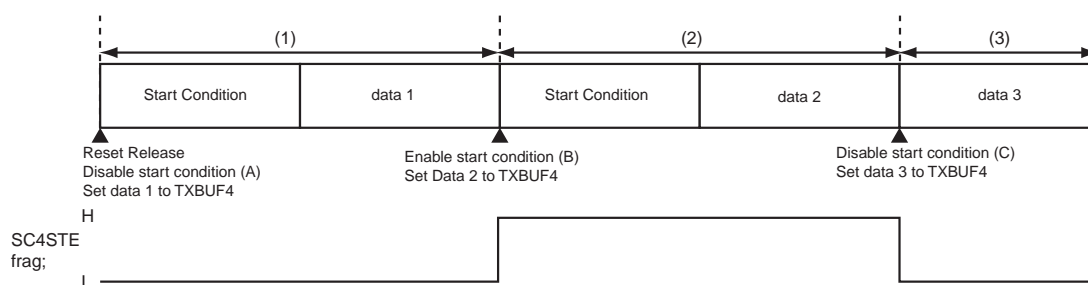
Start Condition Setup Example

Figure:12.5.3 Start Condition Setup Example

(1)   At the first communication, start condition is added regardless of SC4STE value.

(2)   Start condition is added by setting start condition to "enable" at (B).

(3)   Start condition is not added by setting start condition to "disable" at (C).

■ Stop Condition Generation

Stop condition is formed if the data (SDA) pin changes from "L" to "H" when the clock (SCL) pin is "H". Writing "1" in the SC4STPC flag of the SC4MD3 register by program starts the stop condition output. When the stop condition is generated, the SC4STPC flag is automatically cleared.

The stop condition should be requested only when this IIC occupies the bus as the master and communication is completed. In the stop condition generated by this IIC, the stop condition detection interrupt is not generated.
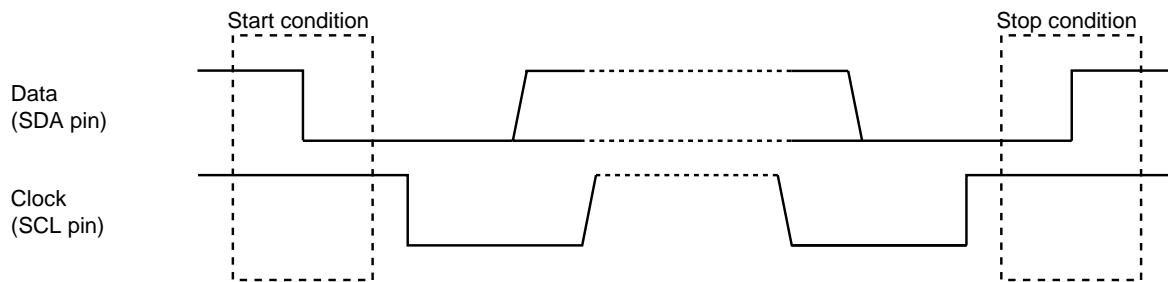
Figure:12.5.4 Start Condition and Stop Condition

Do not write to transmission buffer (TXBUF4) until bus busy flag BUSBSY (SCSTR1:bp3) is set to "0" after the stop condition is requested (SC4MD3: bp5 "1" writing) as master. The waveform of stop condition may not be properly generated.

■ Start/Restart Condition Detection

If the data (SDA) pin changes from "H" to "L" while the clock (SCL) pin is "H", a start condition is detected and the SC4STRT flag and SC4BUSBSY flag of the SC4STR1 register are set to "1". The SC4STRT flag is cleared to "0" by setting data in TXBUF4 at the interrupt process immediately after the slave address reception. The SC4STRT flag is also set if a restart condition is detected. If the address transmitted from the master does not match the slave address, the address is automatically cleared by the hardware as the address mismatch is detected.
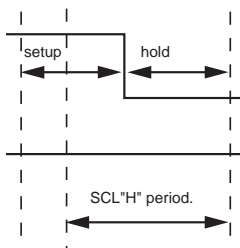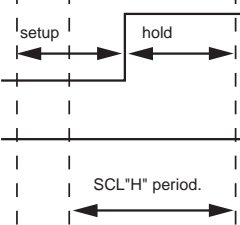
■ Stop Condition Detection

If the data (SDA) pin changes from "L" to "H" while the clock (SCL) pin is "H", a start condition is detected; then, the stop condition detection interrupt is generated and the SC4BUSBSY flag of the SC4STR1 register is cleared.

■ Start Condition/Stop Condition Detection Condition

This IIC detects the start condition and stop condition on bus lines by the sampling with the internal clock. The detection conditions are as follows.

Table:12.5.5 Start Condition/Stop Condition Detection Condition

Start Condition		SCL "H" period	3-lock source or over
		SDA setup	2-clock source or over
		SDA hold	2-clock source or over
Stop Condition		SCL "H" period	3-clock source or over
		SDA setup	2-clock source or over
		SDA hold	2-clock source or over

■ Communication Data Instability Detection

When it is detected that the data line (SDA4 pin) changes while the clock line (SCL4 pin) is "H" after start condition is detected, the communication data is recognized as unstable and the SC4DATA_ERR flag of the SC4STR1 is set to "1". In slave communication, immediately the communication complete interrupt SC4TIRQ is generated and the communication ends. In master communication, 1-byte communication continues. In this case, the communication is not properly performed; so, SC4DATA_ERR flag should be cleared with program. The re-execution of communication is required. If SC4DATA_ERR flag is not cleared , the subsequent start condition and communication data instability cannot be detected.

■ Transmission at Master Communication/Reception Mode Setup and Operation

In master communication, select the transmission or reception mode by the SC4REX flag of the SC4MD3 register. The first data always communicates with adding a start condition despite the set value of the SC4STE flag. The start condition is output from this master serial interface.

In master operation, transmission is executed by setting the slave address and R/W bit in the first data after the start condition generation at the addressing format. In the master reception, check the ACK signal from the slave in the interrupt process after the address data transmission is finished, and switch to the reception mode.

When communicating with the other devices without finishing the communication, regenerate the start condition and transmit the slave address and R/W bit again. In reception, the SDA4 line is automatically released and will be in reception wait status. When the data storage is completed, the reception acknowledge (ACK bit) is transmitted. [Refer to Figure:12.5.11 Master Transmission Timing, Figure:12.5.12 Master Reception Timing]

■ Slave Communication

This serial interface performs address determination by automatically obtaining the received data after detecting the start condition on IIC bus. The communication complete interrupt (SC4TIRQ) is generated only when the address transmitted from master matches the set slave address. Data transmission and reception are determined by the SC4WRS flag of the SC4STR1 register. When SC4WRS = "0", slave reception is selected; when SC4WRS = "1", slave transmission is selected. In slave transmission, the bus line is released by setting transmission data in the TXBUF4 register, and data transmission starts with the clock transmitted from the master. It is not necessary to set data to TXBUF4 register because bus line is automatically opened when NACK is received. In slave reception, the bus line is released by setting dummy data in the TXBUF4 register, and data reception starts with the clock transmitted from the master.

■ Address Compare Flag

When the address transmitted from the master matches the slave address, the address compare flag SC4ADD_ACC flag of SC4STR1 register is set to "1" and ACK is automatically transmitted.

■ General Call Communication

This serial interface supports general call communication. When a general call is detected, the SC4ADD_ACC flag and SC4GCALL flag of the SC4STR1 register are set.

■ Reception of Acknowledgement (ACK bit) after Data Transmission

Whether the ACK bit is enabled or disable is selected by the SC4ACKS flag of the SC4MD3 register. If the ACK bit is enabled, data (1 to 8 bits) is transmitted and the ACK bit is received from the data receiver. When receiving the ACK bit, the data line (SDA4) is automatically released. In master operation, the clock for ACK bit reception is output one time, and the ACK bit is stored in the SC4ACK0 flag of the SC4MD3 register. There is no shift operation of the reception register RXBUF4 by the ACK bit reception clock. When the received ACK bit level is "L", the reception of the receiver is properly operated. It indicates the reception wait status for the next data.

When the ACK bit level is "H", the receiver may finish the reception process. At master operation, finish the communication by writing "1" in the SC4STPC flag of the SC4MD3 register or issue the slave address again by generating a restart condition. At slave operation, it is not necessary to set data to TXBUF4 register because the transmission is finished by automatically releasing the data line (SDA4). In this case, the slave address compare flag is cleared. To continue the communication, an address match is required again.
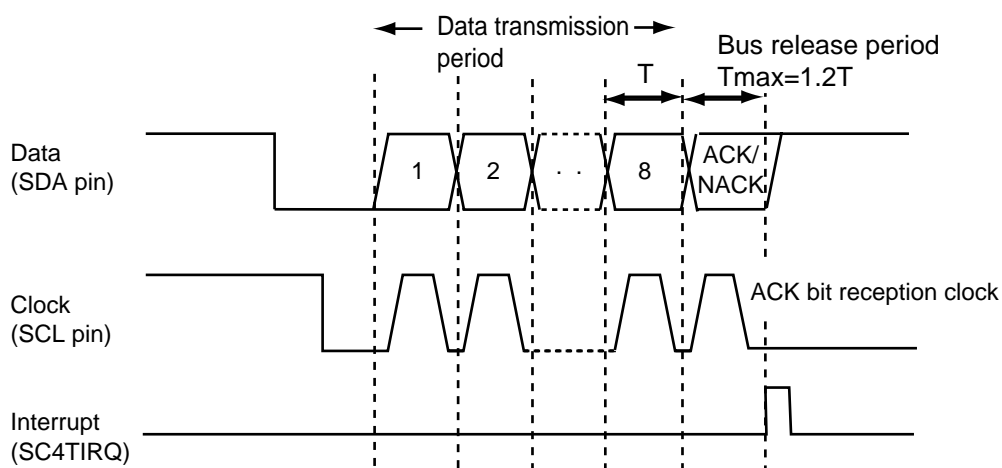
Figure:12.5.5 ACK Bit Reception Timing after 8-bit Data Transmission

■ Transmission of Acknowledgement (ACK bit) after Data Reception

Enable/disable of ACK bit can be selected in the same way as the ACK bit reception. When ACK bit is enabled, ACK bit and clock is output after receiving the data (1 to 8 bit). To continue the reception, output "L" leveled ACK bit. To finish the reception, output "H" leveled ACK bit. ACK bit level for output can be set with SC4ACK0 flag the SC4MD3 register.
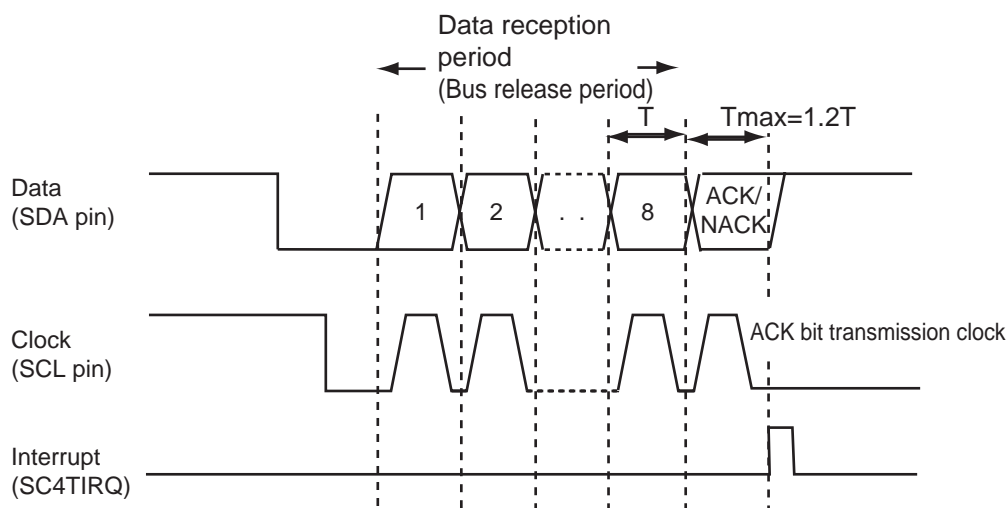

Figure:12.5.6 ACK Bit Transmission Timing after 8-bit Data Reception

■ Arbitration Lost

During master transmission, data bus(SDA) compares output data from this circuit with every 1-bit to detect the competition with other masters. When the output data does not match the data bus, it judges as the communication is not permitted(arbitration lost). The SC4ABT_LST flag of the SC4STR1 register is set instantly. It releases the data bus and the clock bus and continues slave reception. A communicate complete interrupt is not generated by the arbitration lost detection. However, a communicate complete interrupt is generated when matching the slave address after the detection of arbitration lost. Confirm the SC4ABT_LST flag at next interrupt generation timing(stop condition detection interrupt, communicate complete interrupt). When SC4ABT_LST flag is "1", execute communication again after the release of IIC bus because the master transmission is not formed.
In this case, clear the SC4ABT_LST flag by the program.

■ Busy Flag

This serial interface contains 2 busy flags (SC4BUSBSY, SC4IICBSY) in the SC4STR1 register.

The SC4BUSBSY flag is set to "1" in IIC bus communication. It is automatically set when a start condition is detected on IIC bus and cleared when a stop condition is detected.

The SC4IICBSY flag is "1" while this serial interface is communicating. In master communication, this flag is "1" at data loading, start condition generation, data communication, ACK communication, and stop condition generation. In slave communication, the flag is "1" at ACK output, data communication, and ACK communication when the address transmitted from the master matches the slave address. If a restart condition is detected, the SC4IICBSY flag is cleared, and it becomes "1" again at ACK output when the address transmitted from the master matches the slave address. See the timing charts from page 99 for the timing of flag set/clear.

The time is required between the data is set to TXBUF4 register and the SC4IICBSY flag is set (the communication is started) at most the internal transfer clock 1 cycle.

■ Handshake with Clock Synchronous Mechanism

In master operation, the bus clock is monitored by sampling with the clock source selecting the SCL pin. If the bus clock is detected that the signal level of the transfer clock differs from that of this LSI, it is judged that the handshake with clock synchronous mechanism is activated, and the clock is extended. With this operation, the master speed can be matched to the bus clock speed.
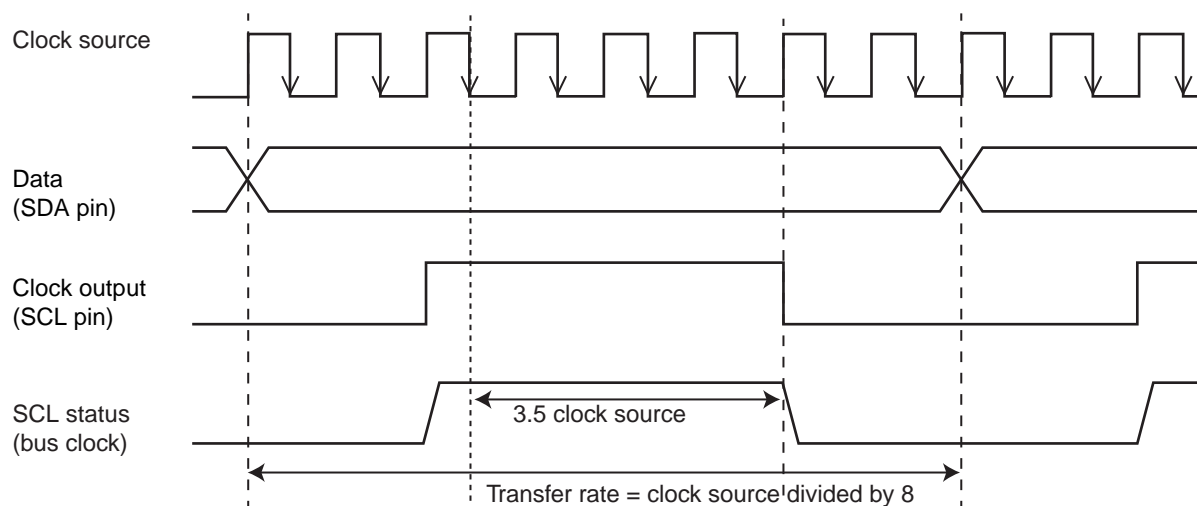
Figure:12.5.7 Without "L" Period Extension from the Other Clock (Standard Mode)
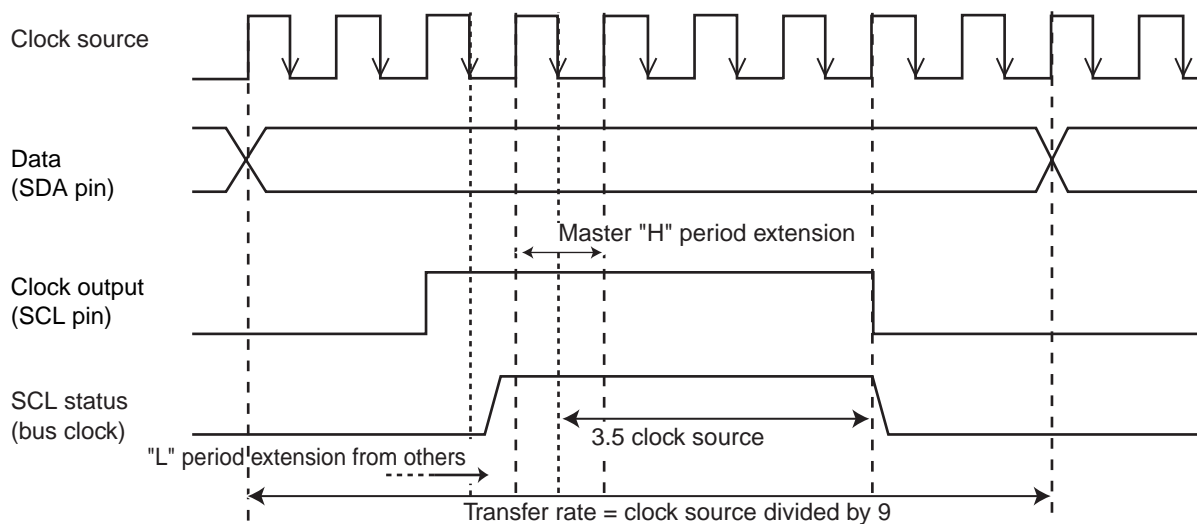
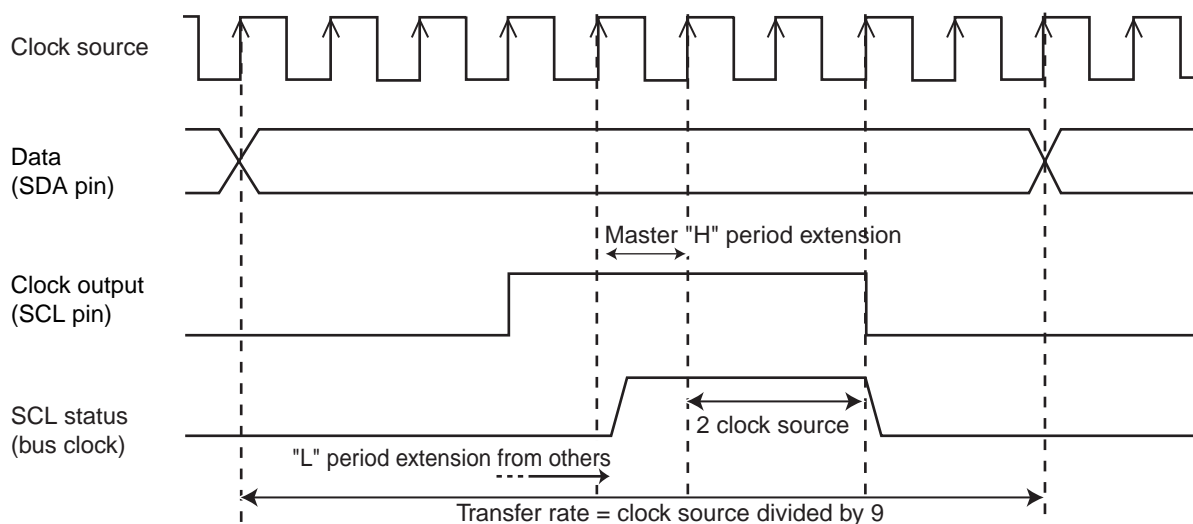Figure:12.5.8 With "L" Period Extension from the Other Clock (Standard Mode)

Clock source

Data
(SDA pin)

Clock output
(SCL pin)

SCL status
(bus clock)

2 clock source

Transfer rate = clock source divided by 8
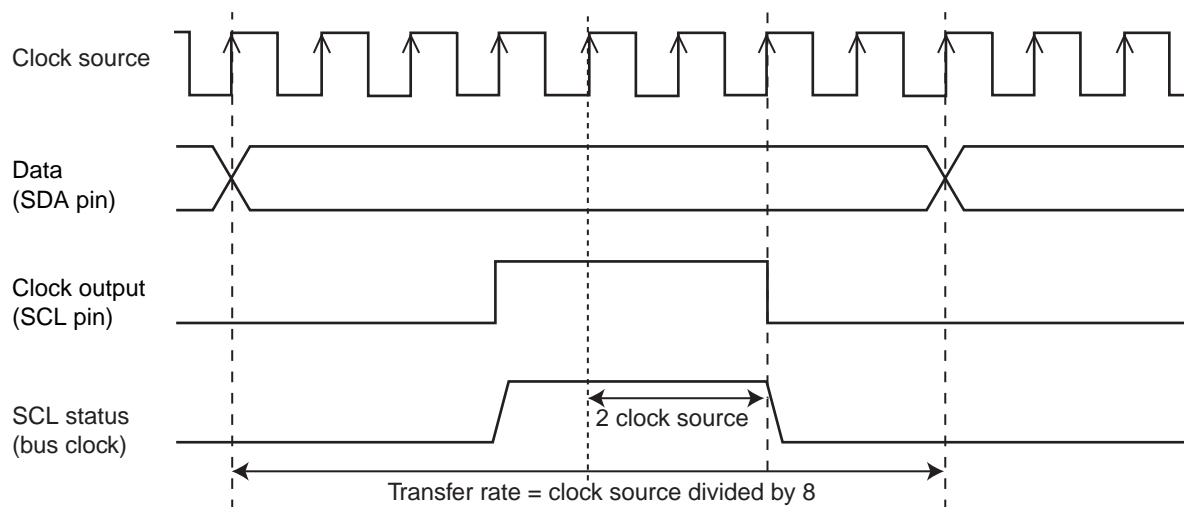
Figure:12.5.9 Without "L" Period Extension from the Other Clock (High-speed Mode)

Clock source

Data
(SDA pin)

Clock output
(SCL pin)

SCL status
(bus clock)

Master "H" period extension

2 clock source

"L" period extension from others

Transfer rate = clock source divided by 9

Figure:12.5.10 With "L" Period Extension from the Other Clock (High-speed Mode))

To obtain the intended transfer rate, design the bus clock so that the rising time of the SCL signal does not exceed 0.5 clock (standard mode) or 1 clock (high-speed mode) of the clock source.

The following items are the same as the clock synchronous serial interface. Refer to the following pages.

■ Automatic Continuous Transfer by ATC0/ATC1

Refer to: XII-46

■ First Transfer Bit Setup

Refer to: XII-43

■ Transmission Data Buffer

Refer to: XII-43

■ Reception Data Buffer

Refer to: XII-44

■ Transmission Bit Count and First Transfer Bit

Refer to: XII-44

■ Emergency Reset

Refer to: XII-49

In communication, bus usage/release is switched by hardware. Set the pin type to N-ch open-drain. At reception, set the direction control of the SDA4 pin (SBO4 pin) to "output".

■ Master Transmission Timing
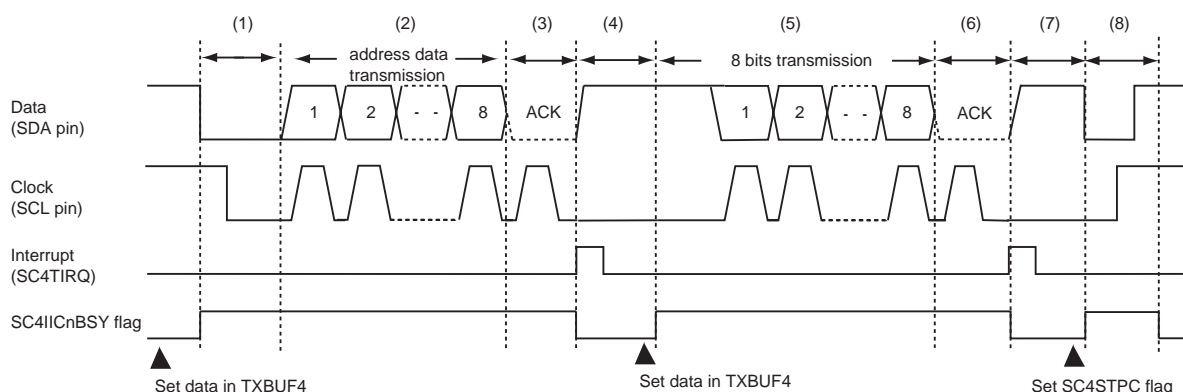
Figure:12.5.11 Master Transmission Timing

(1) Start condition output

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the data is set to TXBUF4.

(2) Address data output

(3) Bus released period, ACK bit reception

(4) Interrupt process

- Communication start: set data in TXBUF4.

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.

(5) Transmission data output

(6) Bus released period, ACK bit reception

(7) Interrupt process

- Communication end: set the SC4STPC flag.

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the SC4STPC flag is set.

(8) Stop condition generation
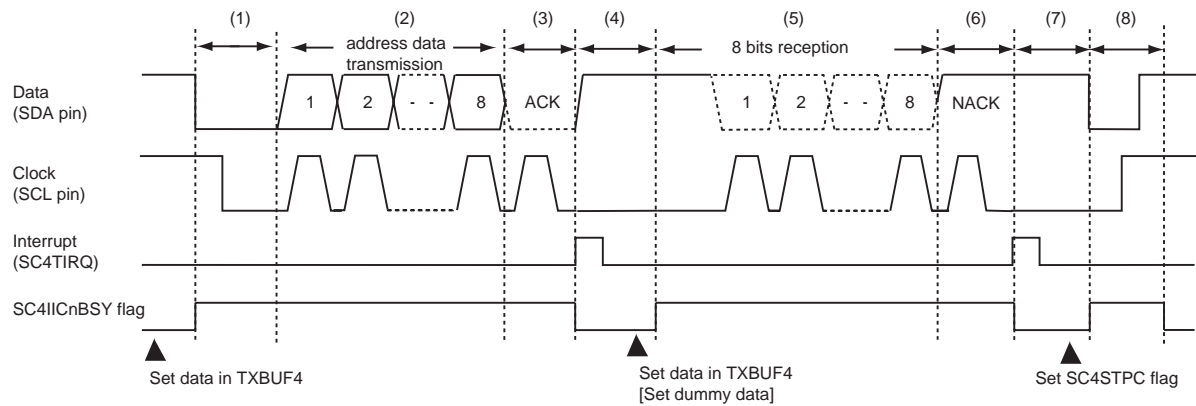
■ Master Reception Timing

Figure:12.5.12 Master Reception Timing

(1) Start condition output

(2) Address data output

(3) Bus released period, ACK bit reception

(4) Interrupt process

- Reception mode setup: SC4REX $=0\rightarrow1$

- Communication start: set dummy data in TXBUF4.

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.

(5) Bus released period, ACK bit reception

(6) NACK bit output

(7) Interrupt process

- Communication end: set the SC4STPC flag.

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the SC4STPC flag is set.

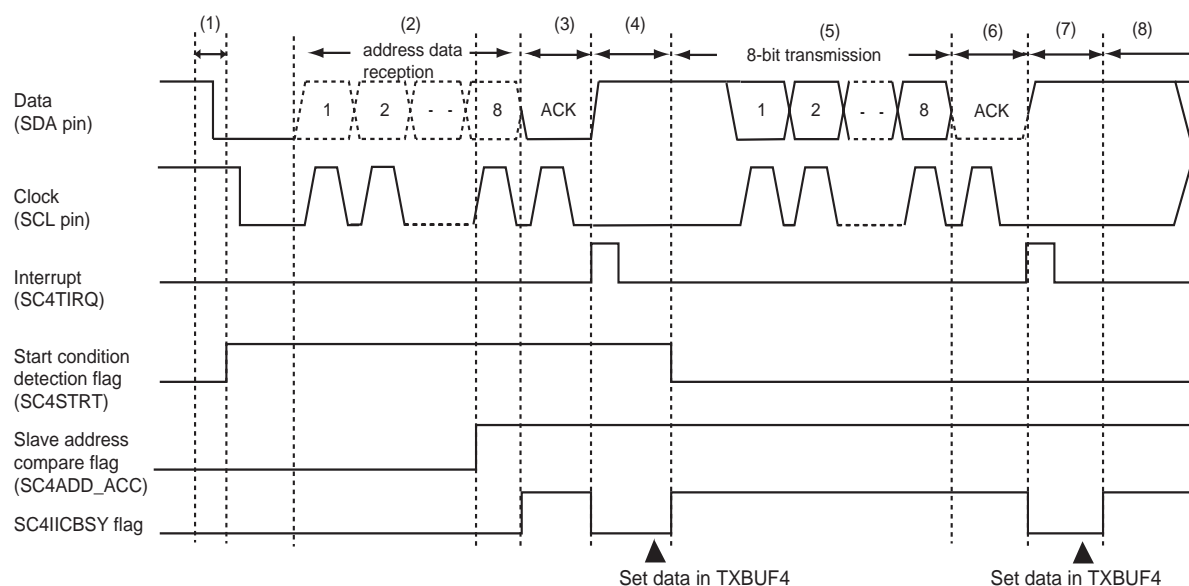(8) Stop condition generation

■ Slave Transmission Timing

Figure:12.5.13 Slave Transmission Timing

(1) Bus released period, start condition detection

(2) Bus released period, address data reception

(3) ACK bit output

(4) Interrupt process

    - Communication start: Set data in TXBUF4.

    - The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.

(5) Transmission data output

(6) Bus released period, ACK bit reception

(7) Interrupt process

    - Communication start: Set data in TXBUF4.

    - The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.

(8) Transmission data output
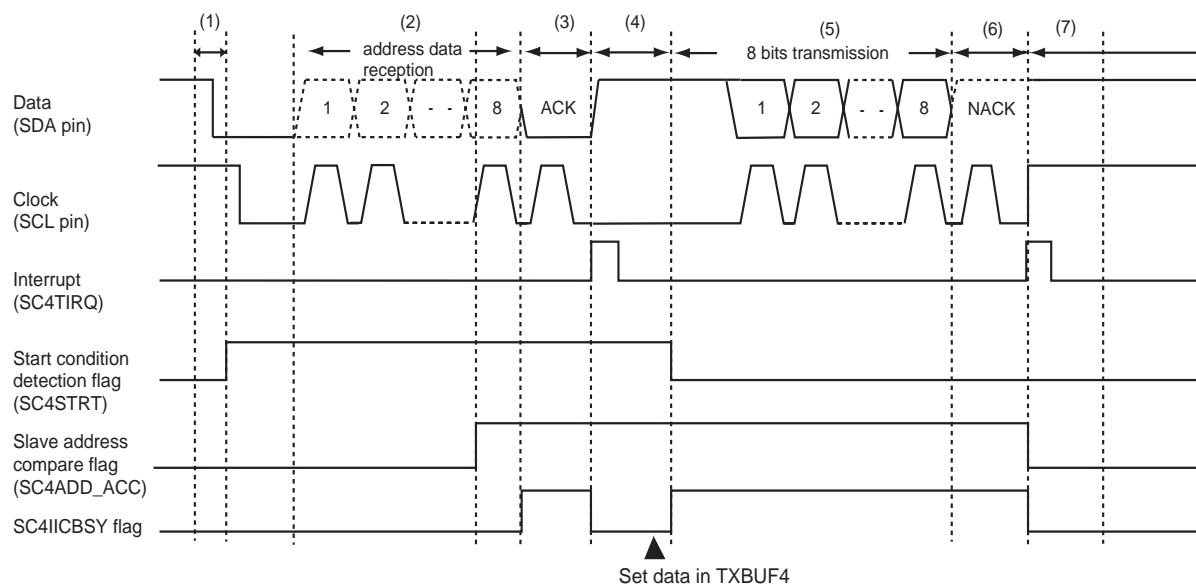
■ Slave Transmission Timing (NACK Reception)

Figure:12.5.14 Slave Transmission Timing (NACK Reception)

(1) Bus released period, start condition detection

(2) Bus released period., address data reception

(3) ACK bit output

(4) Interrupt process

    - Communication start: Set data in TXBUF4.

    - The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.

(5) Transmission data output

(6) Bus released period, NACK bit reception

(7) Bus released period

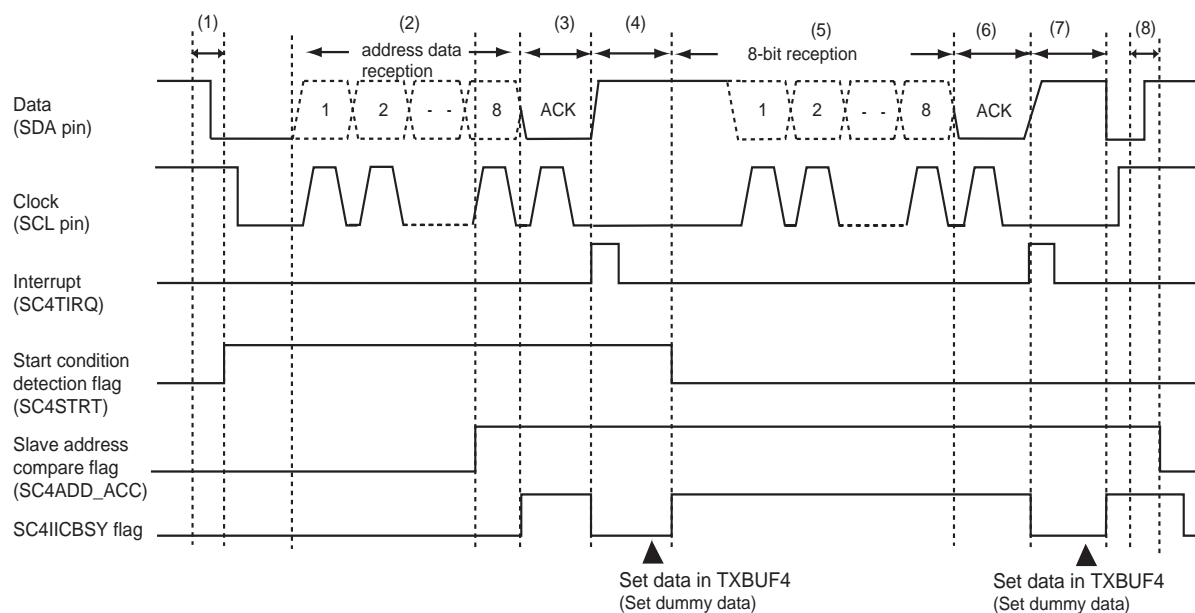■ Slave Reception Timing (Stop Condition Detection)

Figure:12.5.15 Slave Reception Timing (Stop Condition Detection)

(1) Bus released period, start condition detection

(2) Bus released period, address data reception

(3) ACK bit output

(4) Interrupt process

    - Communication start: Set dummy data in TXBUF4.

    - The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.

(5) Bus released period, data reception

(6) ACK bit output

(7) Interrupt process

    - Communication start: Set dummy data in TXBUF4.

    - The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.

(8) Stop condition detection

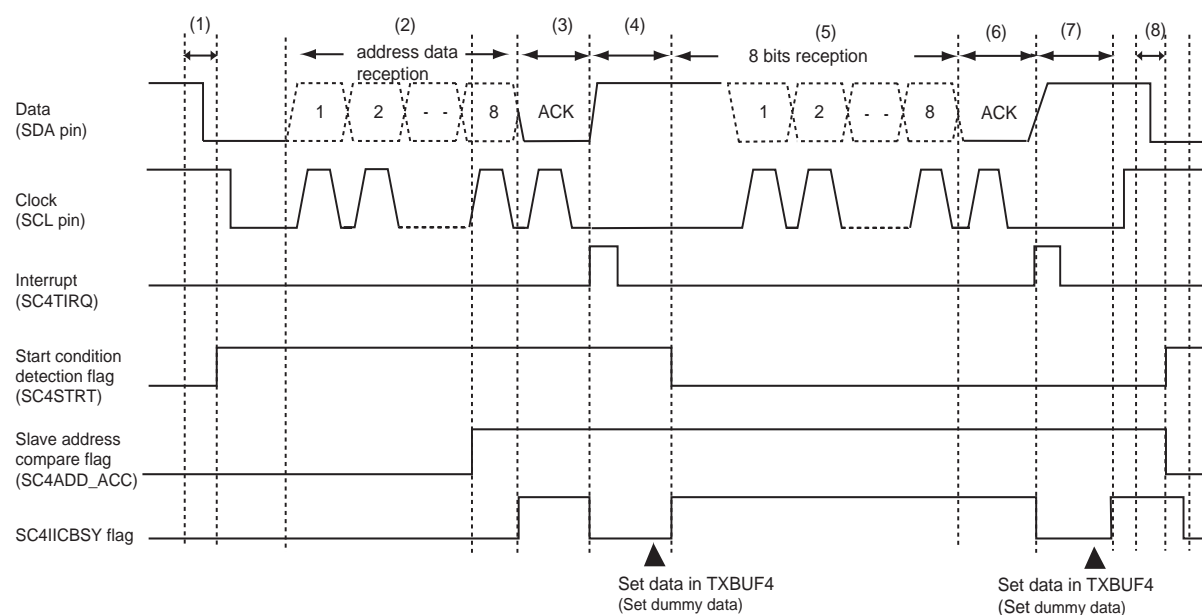■ Slave Reception Timing (Restart Condition Detection)

Figure:12.5.16 Slave Reception Timing (Restart Condition Detection)

(1) Bus released period, start condition detection

(2) Bus released period, address data reception

(3) ACK bit output

(4) Interrupt process

- Communication start: Set dummy data in TXBUF4.

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.

(5) Bus released period, data reception

(6) ACK bit output

(7) Interrupt process

- Communication start: Set dummy data in TXBUF4.

- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.

(8) Restart condition detection

* Serial data input selection

12.5.2   Pin Setup

■   IIC (Multi Master) Serial Interface 4 Pin Setup

Port	Type	Pin	Pin setup (flag setup)							
			SC4SEL register	PnDIR register	PnODC register	PnPLUD register	SC4MD1 register			
			Serial 4 I/O pin switching	I/O mode selection	Nch open-drain output selection	Pull-up/pull-down resistor selection	Serial data input selection	SBT3 pin function selection	Serial input control selection	SBO4 (SDA4) pin function selection
			0:P66-P67 1:P33-P34	0: input mode 1: output mode	0: push/pull 1:Nch open-drain	0: not added 1: added	0: data input from SBI4 1: data input from SBO4	0: port 1: transfer clock I/O	0:"1" input 1: serial input	0: port 1: serial data output
			OSL4	PnDIRm	PnODCm	PnPLUm	SC4IOM	SC4SBTS	SC4SBIS	SC4SBOS
P6	Transmission	P66/SDA4A	0	P6DIR6:1	P6ODC6:1	P6PLUD6:1	1	1	1	1
		P67/SCL4A		P6DIR7:1	P6ODC7:1	P6PLUD7:1				
	Reception	P66/SDA4A	0	P6DIR6:1	P6ODC6:1	P6PLUD6:1	1	1	1	1
		P67/SCL4A		P6DIR7:1	P6ODC7:1	P6PLUD7:1				
P3	Transmission	P33/SDA4B	1	P3DIR3:1	P3ODC3:1	P3PLUD3:1	1	1	1	1
		P34/SCL4B		P3DIR4:1	P3ODC4:1	P3PLUD4:1				
	Reception	P33/SDA4B	1	P3DIR3:1	P3ODC3:1	P3PLUD3:1	1	1	1	1
		P34/SCL4B		P3DIR4:1	P3ODC4:1	P3PLUD4:1				

12.5.3   Setup Example

■ Master Transmission Setup Example

The following describes the setup example for multiple data transmission to all the devices on IIC bus using the serial 4 IIC interface function. Table:12.5.6 shows communication conditions.

Table:12.5.6 Setup Conditions of Multi Master IIC Communication

Item	Set to
Serial data input selection	SDA4A
Transfer bit count	8 bits
Start condition	Enabled (after 2nd communication: disabled)
First transfer bit	MSB
ACK bit	Enabled
IIC communication mode	Standard mode
Clock source	fpll/32
Pin	A system (port 6)
SCL4/SDA pin type	Nch open-drain
SCL4 pin pull-up resistor	Added
SDA4 pin pull-up resistor	Added
Master/Slave setting	Master (Multimaster)

An example setup procedure is shown below.

Setup Procedure	Description

(1) Select the prescaler operation.
    SC4MD2(0x03FB2)
    bp3: SC4PSCE =1
	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select "prescaler count enable".

(2) Select the clock source.
    SC4MD2(0x03FB2)
    bp2-0: SC4PSC2-0 =011
	(2) Select the clock source by the SC4MD2 register. Set bp2-0 to "011" to select fpll/32.

(3) Select the pin
    SC4SEL0(0x03FAB)
    bp3 :OSL4 =0
	(3) Set the OSL4 flag of SC4SEL register to "0" to select A system (port 6) for the I/O pin.

Setup Procedure	Description
(4) Control the pin type. P6ODC(0x03EF4) bp6: P6ODC6 =1 bp7: P6ODC7 =1 P6PLUD(0x03F46) bp6: P6PLUD6 =1 bp7: P6PLUD7 =1	(4) Set the P6ODC6, P6ODC7 flags of the P6ODC register to "1,1" to select Nch open-drain for the SDA4/SCL4 pin type. Set the P6PLUD6, P6PLUD7 flags of the P6PLU Dregister to "1,1" to add pull-up resistor.
(5) Control the pin direction. P6DIR(0x03F36) bp6: P6DIR6 =1 bp7: P6DIR7 =1	(5) Set the P6DIR6, P6DIR7 flags of the port 6 pin direction control register (P6DIR) to "1,1" to set P66 and P67 to output mode.
(6) Set SC4MD3 register Set ACK bit. SC4MD3(0x03FB3) bp0 :SC4ACK0 =x bp1 :SC4ACKS =1 Set the communication mode. SC4MD3(0x03FB3) bp4 :SC4TMD =0 Select the communication type. SC4MD3(0x03FB3) bp2 :SC4CMD =1 Select Transmission/Reception Select transmission/reception mode. SC4MD3(0x03FB3) bp3 :SC4REX =0	(6) Set the SC4ACKS flag of the serial 4 mode register 3 (SC4MD3) to "1" to select "ACK bit enabled". ACK bit is received at transmission and the level setting of ACK bit with the SC4ACKO flag is not required.Set the SC4TMD flag of SC4MD3 register to "0" to set standard mode.Set the SC4CMD flag of SC4MD3 register to "1" to select IIC.Set the SC4REX flag of SC4MD3 register to "0" to select transmission mode. The setting to the serial 4 mode register 3 (SC4MD3) should be executed with one-time MOV instruction in accordance with the setting of each bit. Do not set with BSET/BCLR. Also, do not read out the value of SC4MD3 and write to the specified bit. SC4ACKO flag will be destroyed.
(7) Initialize the monitor flag. SC4STR1(0x03FB7) bp0 :SC4DATA_ERR =0	(7) Set the SC4DATA_ERR flag of the serial 4 status register 1 (SC4STR1) to "0" to initialize the communication error detection flag.
(8) Set the SC4MD0 register. Select the transfer bit count. SC4MD0(0x03FB0) bp2-0 :SC4LNG2-0 =111 Select the start condition. SC4MD0(0x03FB0) bp3 :SC4STE =0 Select the first bit to be transferred. SC4MD0(0x03FB0) bp4 :SC4DIR =0	(8) Set the SC4LNG2-0 flags of the serial 4 mode register 0 (SC4MD0) to "111" to set the transfer bit count to 8 bits. Set the SC4STE flag of the SC4MD0 register to "0" to disable the stand condition (start condition is not added after second communication). Set the SC4DIR flag of the SC4MD0 register to "0" to set the first transfer bit to MSB.
(9) Set the SC4MD1 register. Select the transfer clock. SC4MD1(0x03FB1) bp2 :SC4MST =1 Control the pin function. SC4MD1(0x03FB1) bp4 :SC4SBOS =1 bp5 :SC4SBIS =1 bp6 :SC4SBTS =1 bp7 :SC4IOM =1	(9) Set the SC4MST flag of the SC4MD1 register to "1" to select the clock master (internal clock). Set the SC4SBOS, SC4SBIS, and SC4SBTS flags of the SC4MD1 register to "1" to set the SDA4 (SBO4) pin to serial data output, the SBI4 pin to serial data input, and the SCL4 (SBT4) pin to serial clock I/O. Set the SC4IOM flag to "1" to set the SDA4 (SBO4) pin to serial data input.

Setup Procedure	Description
(10) Set the interrupt level. PSW bp6 :MIE =0 SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10 PERIICR(0x03FFE) bp7-6 :PERILV1-0 =10	(10) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt level by the SL4LV1-0 flags and the PERILV1-0 flags of the serial 4 communication interrupt control register (SC4TICR) and of the peripheral function group interrupt register (PERIICR).
(11) Enable the interrupt. IRQEXPEN(0x03F4E) bp3 :IRQEXPEN3 =1 SC4ICR(0x03FFC) bp1 :SC4IE =1 bp0 :SC4IR =0 PERIICR(0x03FFE) bp1 :PERIIE =1 bp0 :PERIIR =0 PSW bp6 :MIE 1	(11) Set the IRQEXPEN3 flag of the IRQEXPEN register to "1" to enable serial 4 stop condition interrupt. Set the SC4IE flag of the SC4ICR register and the PERIIE flag of the PERIICR register to "1" to enable interrupts. When the interrupt request flags (SC4IR of the SC4ICR register and PERIIR of the PERIICR register) have been already set, clear SC4IR and PERIIR before enabling interrupts. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt. [Chapter 3 3.1.4. Maskable Interrupt Control Register Setup]
(12) <Transmission starts> Start the serial transmission. Confirm that SCL4(P65) is "H". Transmission data→TXBUF4(0x03FB9)	(12) Set the transmission data in the transmission buffer TXBUF4. A transfer clock is generated and transmission starts. After data is transmitted, if ACK bit is received, the communication complete interrupt SC4TIRQ is generated.
(13) <Transmission ends> <Setup for the next data transmission> Determine the monitor flag. SC4STR1(0x03FB7) bp0 :SC4DATA_ERR	(13) Check the SC4DATA_ERR flag of the serial 4 status register 1 (SC4STR1). When the previous transmission is normally completed, SC4DATA_ERR = "0". If SC4DATA_ERR = "1", reexecute the communication.
(14) Determine the ACK bit level. SC4MD3(0x03FB3) bp0 :SC4ACK0	(14) Check the ACK bit level received by the SC4ACK0 flag of the serial 4 mode register 3 (SC4MD3). When SC4ACK0=0, transmission continues. When SC4ACK0=1,the slave side may not receive data. In this case, finish the communication.
(15) Set the SC4MD0 register. Select the transfer bit count. SC4MD0(0x03FB0) bp2-0 :SC4LNG2-0	(15) When changing the transfer bit count, set the transfer bit count by the SC4LNG2-0 flag of the serial 4 mode register (SC4MD0).
(16) <The next data transmission starts.> Serial transmission starts. [→(15)]	(16) Set the transmission data in TXBUF4 to start transmission.[→(15)]
(17) <Transmission ends> <End process of IIC communication> Set the SC4STPC flag. SC4MD3(0x03FB3) bp5 :SC4STPC =1	(17) Set the SC4STPC flag of the serial 4 mode register 3 (SC4MD3) to "1". A stop condition is automatically generated and communication ends.

*(1) and (2) can be set at once.

*Each setup in (8) and (9) can be set at once.

*(10) to (11) can be set at once.

> ⚠ Set each flag in accordance with the order of the setup procedure. Activate the communication after all the control registers (Table:12.2.1, except TXBUF4) are set.

■ Slave Transmission Setup

The following describes the setup examples for slave transmission processing using serial 4 IIC interface function. Table:12.5.7 shows the conditions for transmission processing.

Table:12.5.7 Setup Conditions of Slave IIC Communication

Item	Set to
Serial data input selection	SDA4A
Transfer bit count	8 bits
First transfer bit	MSB
ACK bit	Enabled
IIC communication mode	Standard mode
Clock source	fpll/32
Pin	A system (port 6)
SCL4/SDA4 pin type	Nch open-drain
SCL4 pin pull-up resistor	Added
SDA4 pin pull-up resistor	Added
Address mode	7 bits
Slave address	0110011
Master/slave setup	Master (Multimaster)

An example setup procedure is shown below.

Setup Procedure	Description
(1) Select the prescaler operation. SC4MD2(0x03FB2) bp3: SC4PSCE =1	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select "prescaler count enable".
(2) Select the clock source. SC4MD2(0x03FB2) bp2-0: SC4PSC2-0 =011	(2) Select clock source by the SC4MD2 register. Set bp2-0 to "011" to select fpll/32.
(3) Select the pin. SC4SEL0(0x03FA8) bp3 :OSL4 =0	(3) Set the OSL4 flag of SC4SEL register to "0" to select A system (port 6) for the I/O pin.
(4) Control the pin type. P6ODC(0x03EF4) bp6: P6ODC6 =1 bp7: P6ODC7 =1 P6PLUD(0x03F46) bp6: P6PLUD6 =1 bp7: P6PLUD7 =1	(4) Set the P6ODC6, P6ODC7 flags of the P6ODC register to "1,1" to select Nch open-drain for the SDA4/SCL4 pin type. Set the P6PLUD6, P6PLUD7 flags of the P6PLU Dregister to "1,1" to add pull-up resistor.

Setup Procedure	Description
(5) Control the pin direction. 　　P6DIR(0x03F36) 　　bp6: P6DIR6 =1 　　bp7: P6DIR7 =1	(5) Set the P6DIR6, P6DIR7 flags of the port 6 pin direction control register (P6DIR) to "1,1" to set P66 and P67 to output mode.
(6) Set the SC4MD3 register 　　Set the ACK bit. 　　SC4MD3(0x03FB3) 　　bp0: SC4ACK0 =x 　　bp1 :SC4ACKS =1 　　Set the communication mode. 　　SC4MD3(0x03FB3) 　　bp4 :SC4TMD =0 　　Select the communication type. 　　SC4MD3(0x03FB3) 　　bp2 :SC4CMD =1	(6) Set the SC4ACKS flag of the serial 4 mode register 3 (SC4MD3) to "1" to select "ACK bit enabled". ACK bit is received at transmission and the level setting of ACK bit with the SC4ACKO flag is not needed. Set the SC4TMD flag of SC4MD3 register to "0" to set standard mode, the SC4CMD flag to "1" to select IIC. The setting to the serial 4 mode register 3 (SC4MD3) should be executed with one-time MOV instruction in accordance with the setting of each bit. Do not set with BSET/BCLR. Also, do not read out the value of SC4MD3 and write to the specified bit. SC4ACKO flag will be destroyed.
(7) Initialize the monitor flag. 　　SC4STR1(0x03FB7) 　　bp0 :SC4DATA_ERR =0	(7) Set the SC4DATA_ERR flag of the serial 4 status register 1 (SC4STR1) to "0" to initialize the communication error detection flag.
(8) Set the SC4MD0 register. 　　Select transfer bit count. 　　SC4MD0(0x03FB1) 　　bp2-0 :SC4LNG2-0 =111 　　Select the first transfer bit. 　　SC4MD0(0x03FB0) 　　bp4 :SC4DIR =0	(8) Set the SC4LNG2-0 flags of the serial 4 mode register 0 (SC4MD0) to "111" to set the transfer bit count to 8 bits. Set the SC4DIR flag of the SC4MD0 register to "0" to set the first transfer bit to MSB.
(9) Set the SC4MD1 register. 　　Select the transfer clock. 　　SC4MD1(0x03FB1) 　　bp2 :SC4MST =1 　　Control the pin function. 　　SC4MD1(0x03FB1) 　　bp4 :SC4SBOS =1 　　bp5 :SC4SBIS =1 　　bp6 :SC4SBTS =1 　　bp7 :SC4IOM =1	(9) Set the SC4MST flag of the SC4MD1 register to "1" to select the clock master (internal clock). Set the SC4SBOS, SC4SBIS, and SC4SBTS flags of the SC4MD1 register to "1" to set the SDA4 (SBO4) pin to serial data output, the SBI4 pin to serial data input, and the SCL4 (SBT4) pin to serial clock I/O. Set the SC4IOM flag to "1" to set the SDA4 (SBO4) pin to serial data input.
(10) Set the slave address. 　　SC4AD0(0x03FB4) 　　bp7-1:SC4AD7-1 = 0110011	(10) Set the slave address tin the upper 7 bits (SC4AD7-1) of the SC4AD0 register.
(11) Set the interrupt level. 　　PSW 　　bp6 :MIE =0 　　SC4ICR(0x03FFC) 　　bp7-6 :SC4LV1-0 =10 　　PERIICR(0x03FFE) 　　bp7-6 :PERILV1-0 =10	(11) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt level by the SC4LV1-0 flags and the PERILV1-0 flags of the serial 4 communication interrupt control register (SC4TICR) and of the peripheral function group interrupt register (PERIICR).

Setup Procedure	Description
(12) Enable the interrupt. IRQEXPEN(0x03F4E) bp3 :IRQEXPEN3 =1 SC4ICR(0x03FFC) bp1 :SC4IE =1 bp0 :SC4IR =0 PERIICR(0x03FFE) bp1 :PERIIE =1 bp0 :PERIIR =0 PSW bp6 :MIE =1	(12) Set the IRQEXPEN3 flag of the IRQEXPEN register to "1" to enable serial 4 stop condition interrupt. Set the SC4IE flag of the SC4ICR register and the PERIIE flag of the PERIICR register to "1" to enable interrupts. When the interrupt request flags (SC4IR of the SC4ICR register and PERIIR of the PERIICR register) have been already set, clear SC4IR and PERIIR before enabling interrupts. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt. [Chapter 3 3.1.4. Maskable Interrupt Control Register Setup]
(13) Start IIC communication.	(13) The master on the IIC bus starts communication.
(14) Check the data transmission/reception. SC4STR1(0x03FB7) bp7 :SC4WRS = 0	(14) Communication complete interrupt (SC4IRQ) is generated when the address transmitted from the master matches the slave address set in SC4AD0 register. In the interrupt handling routine, the communication is recognized as the slave transmission by verifying that the SC4WRS flag of the SC4STR1 register is set to "0".
(15) Set the transmission data. TXBUF4(0x03FB9) bp7-0:TXBUF47-0 = 0x55	(15) Set the data in the TXBUF4 register.

*(1) and (2) can be set at once.

*Each setting in (9) to (10) can be set at once.

*(10) to (11) can be set at once.

> ⚠ Set each flag in accordance with the order of the setup procedure. Activate the communication after all the control registers (Table:12.2.1, except TXBUF4) are set.

12.6 Slave Interface

■ Serial Interface 5 Activation and Termination Factors

Setting the SELI2C flag of the SC5AD1 register to "1" activating this serial interface. Setting the SELI2C flag to "0" terminating the serial interface. The ports used in communication can be used as general ports while the serial interface is not operating. If the SELI2C register is set to "0", the SC5AD0 register, SC5TXB register and SC5RXB register are automatically cleared.

■ Slave Address Setup

This serial interface can select either 7- or 10-bit slave address. To set 7-bit slave address, set the I2CADM flag of the SC5AD1 register to "0" to select 7-bit address mode, and set the slave address in upper 7 bits (I2CAD7 to I2CAD1) of the I2CAD0 register. To set 10-bit slave address, set the I2CADM flag of the SC5AD1 register to "1" to select 10-bit address mode, and set the upper 2 bits of the slave address in the lower 2 bits (I2CAD9, I2CAD8) of the I2CAD1 register and set the lower 8 bits of the slave address in SC5AD0 register. When the 10-bit address mode is selected, this serial interface circuit is capable of data reception only.

■ General Call Communication

This serial interface is compatible with general call communication. To operate general call communication, set the I2CGEM flag of the SC5AD1 register to "1" and select general call communication mode. In this mode, the slave address set in the SC5AD0 and SC5AD1 registers are invalid.

■ Data Transmission/Reception

This serial interface performs address determination by automatically obtaining the received data after detecting the start condition on IIC bus. The serial interface 5 interrupt (SC5IRQ) is generated only when the address transmitted from master matches the set slave address. Data transmission and reception are determined by the WRS flag of the SC5STR register. When WRS = "0", slave transmission is selected; when WRS = "1", slave reception is selected. In slave transmission, setting transmission data in the SC5TXB register opens the bus line and data transmission starts by the clock transmitted from master. In slave reception, setting the dummy data in the SC5RXB register opens the bus line and data reception starts by the clock transmitted from master.

■ Start/Restart Condition Detection

If the data (SDA) pin changes from "H" to "L" while the clock (SCL) pin is "H", a start condition is detected and the STRT flag of the SC5STR register is set to "1". The STRT flag is cleared to "0" by setting communication data at the interrupt process right after address reception. If a start condition is detected again during data transfer, the RSTRT flag is set. This flag is cleared to "0" by setting communication data at the interrupt process right after the slave address reception. If the address transmitted from master does not match the slave address, these flags are automatically cleared by hardware as an address miscompare is detected.

■ Busy Flag

This serial interface contains 2 busy flags (SLVBSY, I2CBSY). The SLVBSY flag is set to "1" when the address transmitted from master matches the slave address. The I2CBSY flag is set to "1" during communication on IIC bus. In 10-bit address mode, if the upper 2-bit address firstly transmitted from master matches the I2CAD9-8 of the SC5AD1 register, the SLVBSY flag is set to "1" but SC5IRQ is not generated. If the lower 8-bit address secondly transmitted from master matches the I2CAD7-0 flags of the SC5AD0 register, the SLVBSY flag is remained "1" and SC5IRQ is generated. If these address mismatch, the SLVBSY flag is cleared to "0" and SC5IRQ is not generated.

■ Bus Line Monitor

General call communication can be monitored with the bus line OFF (serial interface 5 is not activated). For monitoring, set the I2CGEM flag of the SC5AD1 register to "1" and set the I2CMON flag to "1" while the SELI2C flag is set to "1". Although the serial 5 interrupt (SC5IRQ) is generated at this time, it has no effect on the communication since it does not output a signal to the data and clock pin.

■ Pin Setup

The following table shows pin setup (SDA, SCL pins) for IIC serial interface 5 data transmission. Nch open drain setup is always necessary for using this serial interface. Set the pull-up resistor control register (PnPLUD) of each port for pull-up resistor setup. Input/output of the transfer data is automatically switched.

Table:12.6.1 Pin Setup

Item	Data I/O pin	Clock output pin
	SDA pin	SCL pins
Port Pin	P73	P74
	P46	P47
Function	Serial data I/O	Serial clock I/O
Nch open-drain setup register	P7ODC P4ODC	
Pull-up resistor control register	P7PLUD P4PLUD	

> This serial interface does not features the function that resets the serial interface circuit by identifying reception data or by changing the slave address. Including general call communication mode, reception data identification should be done by software.

■ Reception Timing
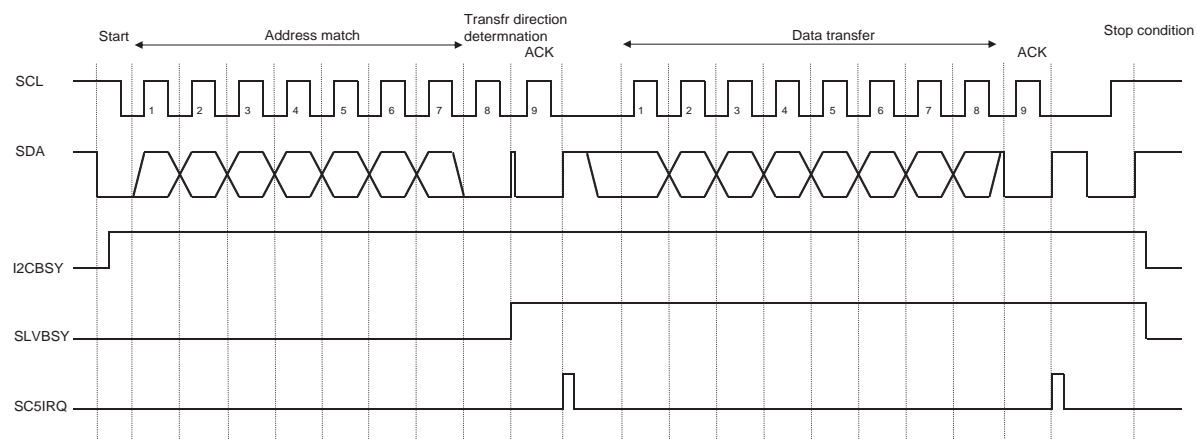
Figure:12.6.1 7-bit Address Reception at Standard Communication Mode
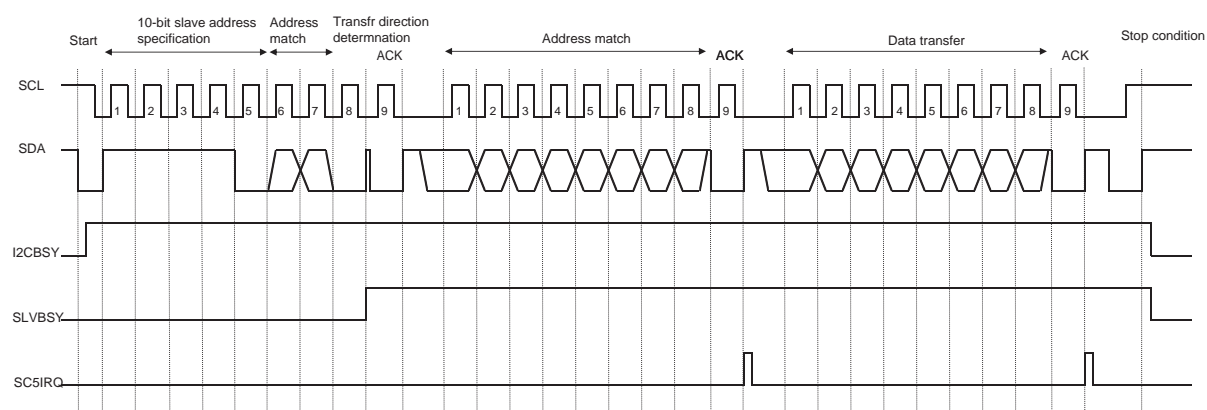
Figure:12.6.2 10-bit Address Reception at Standard Communication Mode

■ Transmission Timing
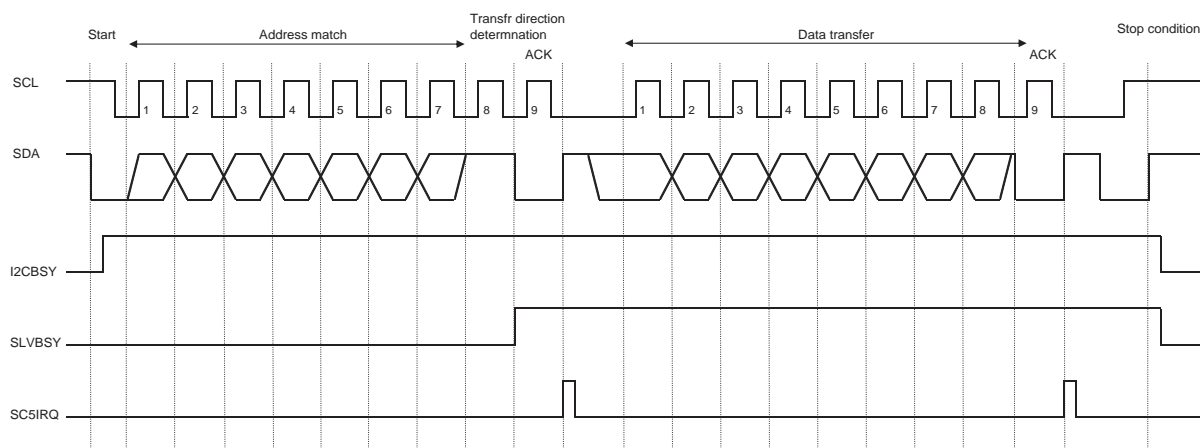
Figure:12.6.3 7-bit Address Transmission at Standard Communication Mode

12.6.1   Setup Example

■ Setup Example for Data Transmission

The setup example for slave transmission with serial 4 is shown. The following table shows the conditions at transmission.

Table:12.6.2 Conditions for Slave IIC Communication

Item	Set to
Data pin (SDA)	P73
Clock pin (SCL)	P74
Addressing mode	7 bits
Slave address	0110011
Transmission data	0x55

Setup Procedure	Description
(1) Control the pin type. P7ODC(0x03FF5) bp4-3 :P7ODC4-3 =11 P7PLUD(0x03F47) bp4-3 :P7PLUD4-3 =11	(1) Set the P7ODC3, P7ODC4 flags of the P7ODC register to "1" to select N-ch open-drain for P73 and P74. Set the P7PLUD3, P7PLUD4 flags of the P7PLUD register to "1" to add pull-up resistor.
(2) Control the pin direction. P7DIR(0x03F37) bp4-3 :P7DIR4-3 =11	(2) Set the P7DIR3, P7DIR4 flags of the port 7 pin direction control register (P7DIR) to "1" to set P73 and P74 to output mode.
(3) Select communication pin. SC5SEL(0x03FC6) bp3 :OSL5 =0	(3) Set the OSL5 flag of the SC5SEL register to "0" to select P73 and P74 for communication pins.
(4) íSelect communication mode, address mode. SC5AD1(0x03FA9) bp3 :I2CGEM =0 bp2 :I2CADM =0	(4) Set the I2CGEM flag to "0" to select standard communication mode, and set I2CADM flag to "0" to select 7-bit address mode.
(5) Activate serial interface 5. SC5AD1(0x03FA9) bp7 :SELI2C =1	(5) Set the SELI2C flag of the SC5AD1 register to "1" to activate the serial interface.
(6) Set the slave address. SC5AD0(0x03FBA) bp7-1 :I2CAD7-1 =0110011	(6) Set the slave address in the upper 7 bits (I2CAD7-1) of the SC5AD1 register.
(7) Start IIC communication	(7) Master on the IIC bus starts communication.
(8) Confirm data transmission/reception. SC5STR(0x03FBE) bp7 :WRS =0	(8) When the address transmitted from the master matches the slave address set in the SC5AD1 register, the serial 5 interrupt (SC5IRQ) is generated. In the interrupt processing routine, when the WRS flag of the SC5MD0 register is "0", this communication is recognized as slave transmission.
(9) Set transmission data. SC5TXB(0x03FBD) bp7-0 :I2CTXB7-0 =0x55	(9) Set the transmission data in the SC5TXB register.

Chapter 13 A/D Converter

13

13.1 Overview

This LSI has an A/D converter with 10 bits resolutions. It contains a built-in sample hold circuit. The channels 0 to 15 (AN0 to AN15) of analog input can be switched by software. When A/D converter is stopped, the power consumption can be reduced by turning the built-in ladder resistance OFF. A/D converter is activated by a register set and an external interrupt.

13.1.1 Functions

Table:13.1.1 shows the A/D converter functions.

Table:13.1.1 A/D Converter Functions

A/D Input Pins	16 pins
Pins	AN15 to AN0
Interrupt	ADIRQ
Resolution	10 bits
Conversion Time (Min.)	13.3 μs(T_{AD}= as 800 ns)
Input range	V_{SS} to V_{REF+}
Power Consumption	Built-in Ladder Resistance (ON/OFF)

This function can't be used ni STOP/HALT mode.

Don't execute mode switching as follows;
- NORMAL mode to SLOW mode
- SLOW mode to IDLE mode to NORMAL mode
If the mode switching is executed, we can't guarantee the result of A/D conversion.

To realize a low power consumption, ladder resistance is turned OFF before STOP/HALT mode switching.

The reference voltage input V_{ref+} pin uses value of $2.0 \text{ V} \leq V_{ref+} \leq V_{DD5}$. When input voltage is $V_{ref+} < 2.0$ V, there is a possibility that the microcontroller malfunctions.

13.1.2   Block Diagram

■   A/D Converter Block Diagram
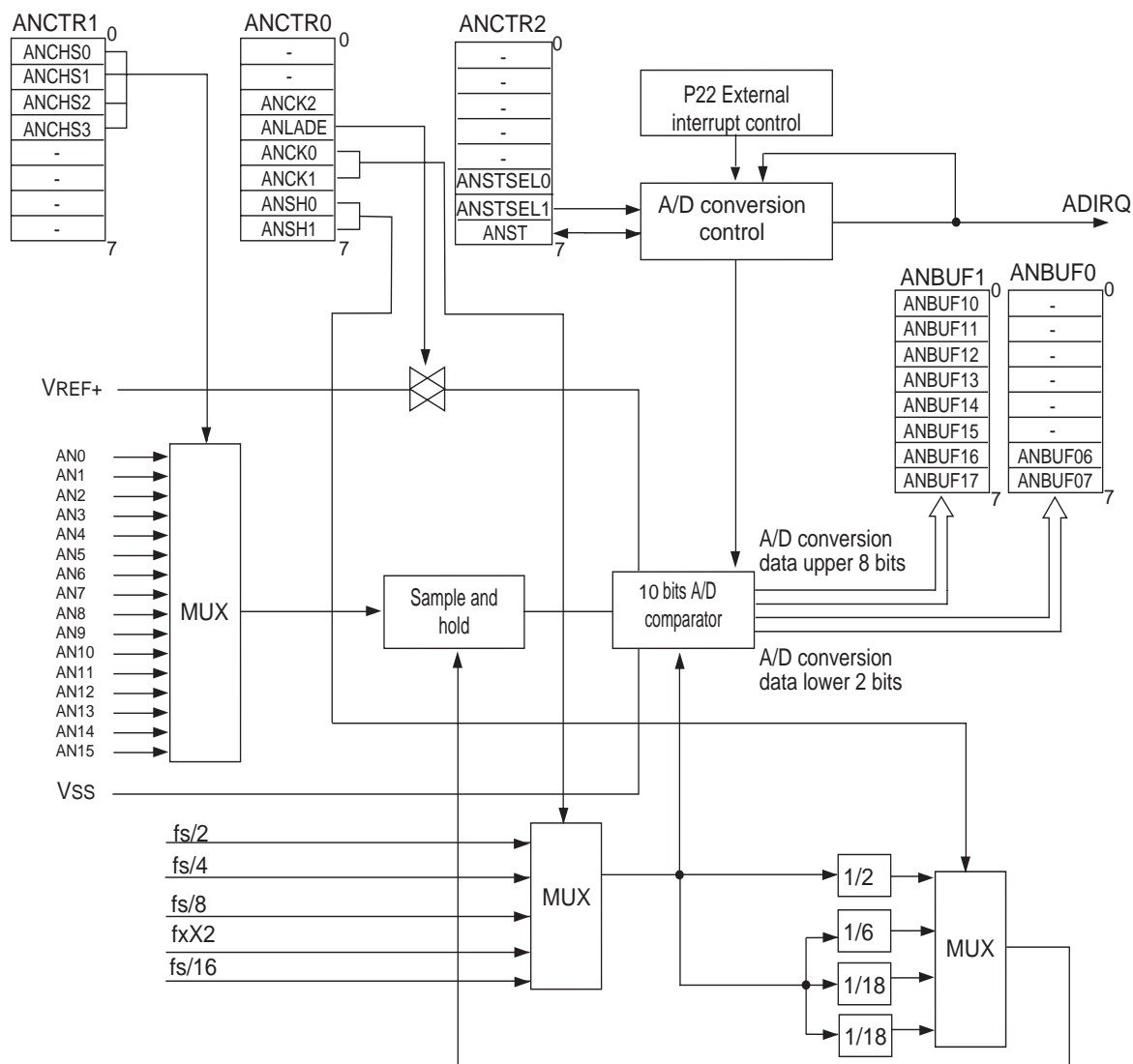
Figure:13.1.1 A/D Converter Block Diagram

13.2 Control Registers

A/D converter consists of the control register (ANCTRn) and the data storage buffer (ANBUFn).

13.2.1 Registers

Table:13.2.1 shows the registers used to control A/D converter.

Table:13.2.1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ANCTR0	0x03FD1	R/W	A/D converter control register 0	XIII-6
ANCTR1	0x03FD2	R/W	A/D converter control register 1	XIII-7
ANCTR2	0x03FD3	R/W	A/D converter control register 2	XIII-8
ANBUF0	0x03FD4	R	A/D converter data storage buffer 0	XIII-9
ANBUF1	0x03FD5	R	A/D converter data storage buffer 1	XIII-9
ADICR	0x03FFD	R/W	A/D converter interrupt control register	III-40
EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-58
PAIMD	0x03EE8	R/W	Port A input mode register	IV-148
PAPLU	0x03F4A	R/W	Port A Pull-up resistor control register	IV-146
PBIMD	0x03EE9	R/W	Port B input mode register	IV-162
PBPLU	0x03F4B	R/W	Port B pull-up resistor control register	IV-161

R/W : Readable/Writable

R : Readable only

13.2.2   Control Registers

■   A/D Converter Control Register0 (ANCTR0:0x03FD1)

bp	7	6	5	4	3	2	1	0
Flag	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	ANCK2	-	-
Reset	0	0	0	0	0	0	-	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	-

bp	Flag	Description
7-6	ANSH1 ANSH0	Sample hold time 00:$T_{AD} \times 2$ 01:$T_{AD} \times 6$ 10:$T_{AD} \times 18$ 11:$T_{AD} \times 18$
2, 5-4	ANCK2-0	A/D conversion clock (ftad=$1/T_{AD}$) 000:fs/2 001:fs/4 010:fs/8 011:fx $\times$ 2 1XX:fs/16 111:Prohibited * as 800 ns $\leq T_{AD} \leq$ 15.26 μs
3	ANLADE	A/D ladder resistance control 0:A/D ladder resistance OFF 1:A/D ladder resistance ON
1-0	-	-

■ A/D Converter Control Register1 (ANCTR1:0x03FD2)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	ANCHS3	ANCHS2	ANCHS1	ANCHS0
Reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3-0	ANCHS3 ANCHS2 ANCHS1 ANCHS0	Analog input channel 0000:AN0 0001:AN1 0010:AN2 0011:AN3 0100:AN4 0101:AN5 0110:AN6 0111:AN7 1000:AN8 1001:AN9 1010:AN10 1011:AN11 1100:AN12 1101:AN13 1110:AN14 1111:AN15

■ A/D Converter Control Register2 (ANCTR2:0x03FD3)

bp	7	6	5	4	3	2	1	0
Flag	ANST	ANSTSEL 1	ANSTSEL 0	-	-	-	-	-
Reset	0	0	0	-	-	-	-	-
Access	R/W	R/W	R/W	-	-	-	-	-

bp	Flag	Description
7	ANST	A/D conversion status 0:Finish, Stop 1:Start, Converting
6-5	ANSTSEL 1-0	A/D conversion starting factor select 00:Set ANST flag to "1" 01:Set ANST flag to "1" 10:P22 external interrupt or Set ANST flag to "1" 11:A/D conversion interrupt or Set ANST flag to "1"
4-0	-	-

13.2.3   Data Buffers

■ A/D Converter Data Storage Buffer0 (ANBUF0:0x03FD4)

The lower 2 bits results from A/D conversion are stored to this register.

bp	7	6	5	4	3	2	1	0
Flag	ANBUF07	ANBUF06	-	-	-	-	-	-
Reset	X	X	-	-	-	-	-	-
Access	R	R	-	-	-	-	-	-

■ A/D Converter Data Storage Buffer1 (ANBUF1:0x03FD5)

The upper 8 bits results from A/D conversion are stored to this register.

bp	7	6	5	4	3	2	1	0
Flag	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Do not word access to ANBUF1 register.

13.3 Operation

Here is a description of A/D converter circuit setup procedure.

1. Set the analog pins.

    Set the analog input pin, set in 2. , to "special function pin" by the port A,B input mode register (PAIMD,PBIMD).

    * Setup of the port A,B input mode register should be done before analog voltage is put to pins.

2. Select the analog input pin.

    Select the analog input pin from AN15 to AN0 by the ANCHS3-0 flag of the A/D converter control register1 (ANCTR1).

3. Select the A/D conversion clock.

    Select the A/D converter clock by the ANCK2, ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0). Setup should be such a way that converter clock (T_{AD}) does not drop less than 800 ns with any resonator.

4. Set the sample hold time.

    Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0). The sample hold time should be based on analog input impedance.

    * 2. to 4. are not in order. 3. and 4. can be operated simultaneously.

5. Set the A/D ladder resistance.

    Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1", and a current flow through the ladder resistance and A/D converter goes into the waiting.

6. Select the A/D converter activation factor, then start A/D conversion.

    Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start A/D converter or set ANSTSEL1, ANSTSEL0 flag of A/D converter control register 2 (ANCTR2) to "11" to start A/D converter by the external trigger factor.

7. A/D conversion.

    A/D conversion is compared and determined sequentially by MSB after the sampling in the sample hold time to be set 4. .

8. Complete the A/D conversion.

    After the A/D conversion is completed, the result of the conversion is stored in the A/D conversion data store buffer (ANBUF0,1), the A/D conversion end interrupt is generated and the ANST flag is cleared to "0".

Set the ANLADE flag to "1" then start A/D conversion after waiting for 12 conversion clock.

When A/D converter is started again after setting the ANST flag to "0" and A/D converter was stopped by force during A/D converter, start A/D converter after waiting for more than (2 system clock) + (2 converter clock) considerable time.

In the A/D conversion starting factor selection, when A/D is converted in the status that the start by the external interrupt is selected and the ANST flag is set to "0" to be completed A/D conversion forcefully during the A/D conversion, be sure to set the A/D conversion starting factor selection to "0" in advance before setting the ANST flag to "0".
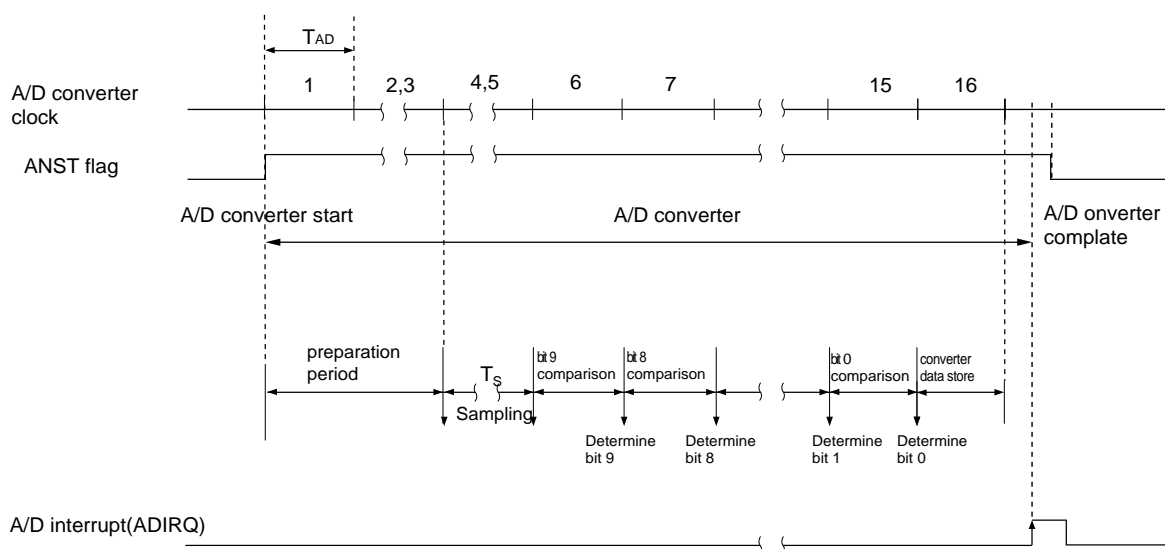
Figure:13.3.1 Operation of A/D conversion(sample hold time at $T_{AD} \times 2$)

To read out the value of the A/D conversion, A/D conversion should be done several times to prevent noise error by confirming the match of level by program, or by using the average value.

If the flags of ANCTR0, ANCTR1 are changed during A/D conversion, we can't guarantee the operation and the result of A/D conversion. When A/D conversion isn't executed or after A/D conversion was stopped by force, must change the flags.

13.3.1　Setup

■　Input Pins of A/D Conversion Setup

Input pins for A/D converter is selected by the ANCH3-0 flag of the ANCTR1 register.

■　A/D Conversion Clock Setup

The A/D conversion clock is set with the ANCK2 to ANCK0 flag of the ANCTR0 register. Set the A/D conversion cycle (T_{AD}) more than 800 ns or less than 15.26 μs. Table:13.3.1 shows the machine clock (fpll, fx, fs) and the A/D conversion cycle (T_{AD}). (calculated as fs = fpll/2, fx/4)

Table:13.3.1 A/D Conversion Clock and A/D Conversion Cycle

ANCK2	ANCK1	ANCK0	A/D conversion clock	A/D conversion cycle (T_{AD})		
				At high speed oscillation		at low speed oscillation
				fpll=10 MHz	fpll=8.38 MHz	fx=32.768 kHz
0	0	0	fs/2	400 ns (no usable)	477.33 ns (no usable)	244.14 μs (no usable)
		1	fs/4	800 ns	954.65 ns	488.28 μs (no usable)
	1	0	fs/8	1.6 μs	1.91 μs	976.56 μs (no usable)
		1	fx × 2	15.26 μs	15.26 μs	15.26 μs
1	-	-	fs/16	3.2 μs	3.82 μs	1953.12 μs (no usable)

For the system clock (fs), refer to [Chapter 2 2.6 Clock Switching].

■　A/D Conversion Sample Hold Time (T_S) Setup

The sample hold time of A/D conversion is set with the ANSH1 to 0 flag of the ANCTR0 register. The sample hold time of A/D conversion depends on external circuit, so set the right value by analog input impedance.

Table:13.3.2 Sample Hold Time of A/D Conversion and A/D Conversion Time

ANSH1	ANSH0	Sample hold time (T_S)	A/D conversion time[μs]				
			at high speed				at low speed
			at T_{AD}=1.6 μs (fs=5 MHz)	at T_{AD}=954.65 ns (fs=4.19 MHz)	at T_{AD}=1.91 μs (fs=4.19 MHz)	at T_{AD}=15.26 μs (fs=4.19 kHz)	at T_{AD}=15.26 μs (fs=8.192 kHz)
0	0	$T_{AD} \times 2$	26.1	15.87	31.16	244.88	610.37
	1	$T_{AD} \times 6$	32.5	19.69	38.8	305.92	671.41
1	0	$T_{AD} \times 18$	51.7	31.15	61.72	488.92	854.53
	1	$T_{AD} \times 18$	51.7	31.15	61.72	488.92	854.53

* Calculated as fs=fpll/2,fx/4.

Table:13.3.3 The method of Calculation of A/D conversion time

ANCK2	ANCK1	ANCK0	A/D conversion clock	The method of Calculation of A/D conversion time
0	0	0	fs/2	$T_S + 14 \times T_{AD} + 2.5/fs$
		1	fs/4	
	1	0	fs/8	
		1	fx × 2	$T_S + 14 \times T_{AD} + 3/fs$
1	-	-	fx × 16	$T_S + 14 \times T_{AD} + 2.5/fs$

Following Table:13.3.3, A/D conversion time may be shortened at most the 1 fs in A/D conversion cycle by the phase difference of fs and A/D conversion clock.

■ Built-in Ladder Register Control

The ANLADE flag to the ANCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. When A/D conversion is stopped, the ANLADE flag of the ANCTR0 register is set to "0" to save the power consumption.

■ A/D Conversion Starting Factor Setup

A/D conversion starting factor is set with the ANSTSEL1,0 flag of the ANCTR2 register. The ANSTSEL1,0 flag of the ANCTR2 register is set to start A/D conversion by the continuous conversion factor. Also, the ANST flag of the ANCTR2 register is set to "1" is possible.

When the continuous conversion is selected as A/D conversion starting factor, the valid edge should be assigned at REDG flag of the external interrupt control register (IRQ2ICR) and EDGSEL flag of the both edge interrupt control register (EDGDT).

The interrupt valid edge assingnment should be done before selecting the interrupt factor at A/D conversion starting factor.

■ A/D Conversion Starting Setup

The A/D conversion start is set with the ANST flag of the ANCTR2 register. The A/D conversion is started by setting the ANST flag of the ANCTR2 register to "1". When the A/D conversion is started by the continuous conversion factor, the ANST flag of the ANCTR2 register is automatically set to "1" after the continuous conversion is generated and the A/D conversion is started. The ANST flag of the ANCTR2 register is cleared to "0" automatically after the conversion data is stored

13.3.2   Setup Example

■ Example of A/D Conversion Setup by Registers

A/D conversion is started by setting registers. The analog input pins are set to AN0, the conversion clock is set to fs/4, and the sample hold time is set to $T_{AD} \times 2$. Then, A/D conversion complete interrupt is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description

(1) Set the analog input pin.
    PAIMD(0x03EE8)
    bp7 :PAIMD7 =1
    PAPLU(0x03F4A)
    bp7 :PAPLU7 =0
	(1) Set the analog input pin to be set (2) to the special function pin by the port A input mode register (PAIMD) and set to the no pull-up resistor by the port 0 pull-up resistor control register (PAPLU).

(2) Select the analog input pin.
    ANCTR1(0x03FD2)
    bp3-0 :ANCHS3-0 =0000
	(2) Select the analog input pin from AN15 to AN0 by setting the ANCHS3-0 flags of the A/D converter control register 1 (ANCTR1) to "0000".

(3) Select the A/D conversion clock.
    ANCTR0(0x03FD1)
    bp2, 5-4 :ANCK2-0 =001
	(3) Select the A/D conversion clock by the ANCK2, ANCK1, ANCK0 flag of the A/D converter control register0 (ANCTR0).

(4) Set the sample hold time.
    ANCTR0(0x03FD1)
    bp7-6 :ANSH1-0 =00
	(4) Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register0 (ANCTR0).

(5) Set the interrupt level.
    ADICR(0x03FFD)
    bp7-6 :ADLV1-0 =00
	(5) Set the interrupt level by the ADLV1-0 flag of the A/D converter complete interrupt control register (ADICR). If any interrupt request flag is already set, clear it. [Chapter 3.1.4 Interrupt Flag Setup]

(6) Enable the interrupt.
    ADICR(0x03FFD)
    bp1 :ADIE =1
	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1".

(7) Set the A/D ladder resistance.
    ANCTR0(0x03FD1)
    bp3 :ANLADE =1
	(7) Set the ANLADE flag of the A/D converter control register0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.

(8) A/D conversion starting factor select.
    ANCTR2(0x03FD3)
    bp6-5 :ANSTSEL1-0 =00
	(8) Clear the ANSTSEL1 to 0 flag of the A/D converter control register2 (ANCTR2) to "00" to set A/D converter starting factor to ANST flag of the A/D converter control register2 (ANCTR2).

(9) Start A/D converter operation.
    ANCTR2(0x03FD3)
    bp7 :ANST =1
	(9) Set the ANST flag of the A/D converter control register2 (ANCTR2) to "1" to start the A/D conversion.

* The above (3) to (4) can be set at the same time.

When the conversion is restarted by changing the setting after the A/D conversion, set the
ANLADE flag of the A/D converter control register 0 (ANCTR0) to "0" to disable the analog to
change the setting.
 The operation is not guaranteed if this procedure fails to be kept.

■ Example of A/D Conversion Setup by the External Interrupt

A/D conversion is started by the external interrupt. The analog input pins are set to AN0, the conversion clock is set to fs/4, and the sample hold time is set to T_{AD} x 2. Then, A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD(0x03EE8) bp7 :PAIMD7 =1 PAPLU(0x03F4A) bp7 :PAPLU7 =0	(1) Set the analog input pin to be set (2) to the special function pin by the port A input mode register (PAIMD) and set to the no pull-up resistor by the port 0 pull-up resistor control register (PAPLU).
(2) Select the analog input pin. ANCTR1(0x03FD2) bp3-0 :ANCHS3-0 =0000	(2) Select the analog input pin from AN15 to AN0 by setting the ANCHAS3-0 flags of the A/D converter control register 1 (ANCTR1) to "0000".
(3) Select the A/D conversion clock. ANCTR0(0x03FD1) bp2, 5-4 :ANCK2-0 =001	(3) Select the A/D conversion clock by the ANCK2-0 flag of the A/D converter control register0 (ANCTR0).
(4) Set the sample hold time. ANCTR0(0x03FD1) bp7-6 :ANSH1-0 =00	(4) Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register0 (ANCTR0).
(5) Set the interrupt level. ADICR(0x03FFD) bp7-6 :ADLV1-0 =10	(5) Set the interrupt level by the ADLV1-0 flag of the A/D converter complete interrupt control register (ADICR). If any interrupt request flag is already set, clear it. [Chapter 3. 3.1.4. Maskable Interrupt Control Register Setup]
(6) Enable the interrupt. ADICR(0x03FFD) bp1 :ADIE =1	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1".
(7) Set the A/D ladder resistance. ANCTR0(0x03FD1) bp3 :ANLADE =1	(7) Set the ANLADE flag of the A/D converter control register0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D converter.
(8) Select the A/D Conversion Starting factor. ANCTR2(0x03FD3) bp6-5 :ANSTSEL1-0 =10	(8) Set the ANSTSEL1 to 0 flag of the A/D converter control register2 (ANCTR2) to "10" , then setup the A/D conversion starting factor to the continuous conversion and the ANST flag of the A/D converter control register2 (ANCTR2).
(9) Start the A/D Conversion Operation. ANCTR2(0x03FD3) bp7 :ANST =1	(9) When the òAë±ïœä² is generated, the ANST flag of the A/D converter control register2 (ANCTR2) is automatically set to "1", then the A/D conversion is started. Also, even if the continuous conversion is not generated, the A/D conversion can be started by setting the ANST flag of the A/D converter control register2 (ANCTR2)

When the conversion is restarted by changing the setting after the A/D conversion is completed, set the ANLADE flag of the A/D coverter control register 0 (ANCTR0) to "0" to disable the analog to change the setting. The operation is not guaranteed if this procedure fails to be kept.

Input the pulse for the external interrupt to be input longer than the system clock period. If the pulse is shorter than the system clock period, the A/D conversion may not be started.

13.3.3   Cautions

A/D conversion can be damaged by noise easily, therefore, anti-noise measures should be taken adequately.

■   Anti-noise measures

To A/D input (analog input pin), add condenser near the Vss pins of micro controller.
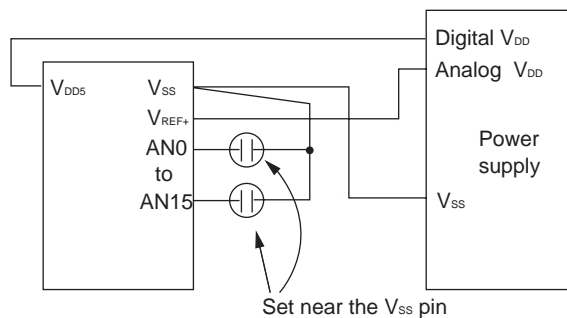
Figure:13.3.2 A/D Converter Recommended Example 1
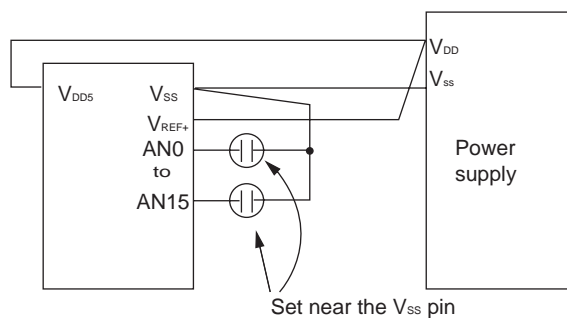
Figure:13.3.3 A/D Converter Recommended Example 2

For high precision of A/D conversion, the following cautions on A/D converter should be kept.
1.The input impedance R of A/D input pin should be under 500 kΩ, and the external capacitor C (more than 1000 pF, under 1 μF) should be connected to it.
2.The A/D conversion frequency should be set in regard to R, C.
3.At the A/D conversion, if the output level of microcontroller is changed, or the peripheral added circuit is switched to ON/OFF, the A/D converter could work wrongly, as the analog input pins and power pins cannot be fixed. At the set checking, confirm the wave form of analog input pins.
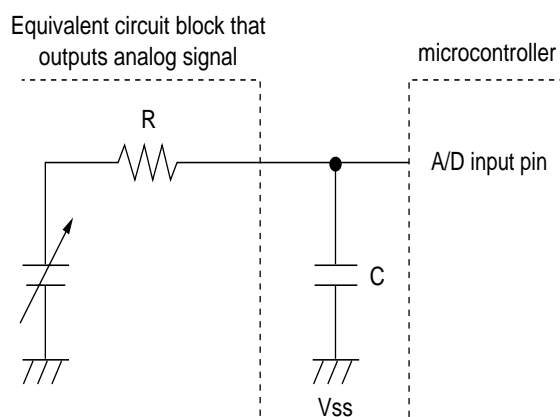
Figure:13.3.4 Recommended Circuit

Chapter 14 D/A Converter

14

14.1 Overview

This LSI has a built-in D/A converter with 8 bits solution. There are 4 output channel and 8-bit data registers for each channel. In D/A conversion mode, there are 3 modes : channel fixed conversion mode, 2 channels conversion mode and 4 channels conversion mode. At 2 and 4 channels conversion mode, the time for switching channels can be programed by the software. When the D/A converter is not used, the built-in ladder resistance can be set to OFF to save the power consumption.

14.1.1 Functions

Here is the list of D/A converter functions.

Table:14.1.1 D/A converter functions

Resolution	8-bit
Pin	DA_A pin, DA_B pin, DA_C pin, DA_D pin
Power consumption saving	Built-in ladder resistance ON/OFF

14.1.2   D/A Converter Block Diagram
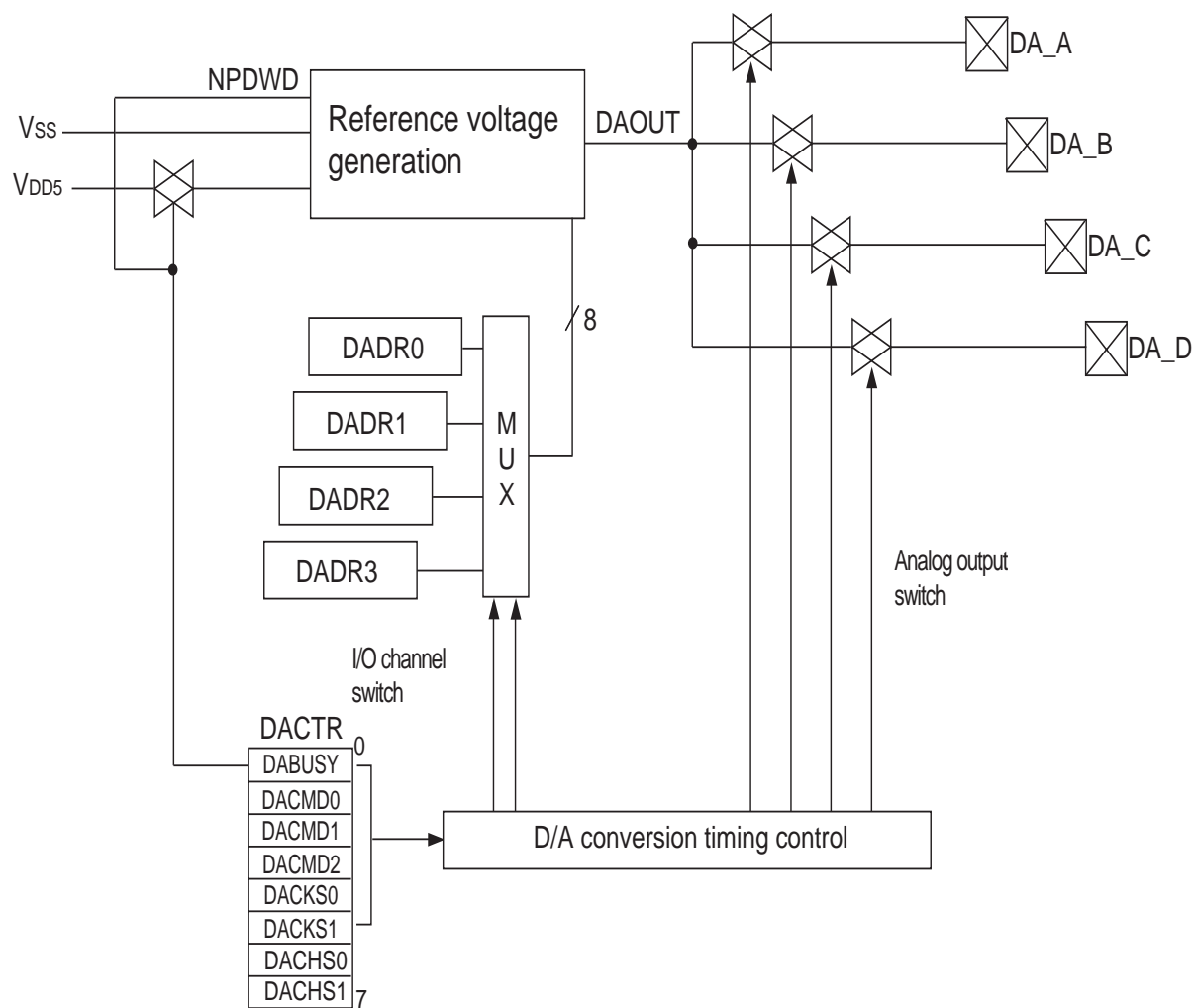
Figure:14.1.1 D/A Converter Block Diagram

14.2 D/A Converter Control Registers

14.2.1 D/A Converter Control Registers

Following table shows the registers to control the D/A converter of this LSI.

Table:14.2.1 D/A Converter Control Registers

Register	Address	R/W	Function	Page
DACTR	0x03FD6	R/W	D/A converter control register	XIV-5
DADR0	0x03FD7	R/W	D/A converter input data register 0	XIV-6
DADR1	0x03FD8	R/W	D/A converter input data register 1	XIV-6
DADR2	0x03FD9	R/W	D/A converter input data register 2	XIV-6
DADR3	0x03FDA	R/W	D/A converter input data register 3	XIV-6
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-10
P0PLUD	0x03F40	R/W	Port 0 pull-up/pull-down resistor control register	IV-10
SELUD	0x03F4C	R/W	Pull-up/down resistor selection register	IV-15
P6DIR	0x03F36	R/W	Port 6 direction control register	IV-93
P6PLUD	0x03F46	R/W	Port 6 pull-up/pull-down resistor control register	IV-93
P9DIR	0x03F39	R/W	Port 9 direction control register	IV-138
P9PLU	0x03F49	R/W	Port 9 pull-up resistor control register	IV-138

R/W : Readable/Writable

14.2.2 D/A Converter Control Register(DACTR)

This is the 8-bit readable/writable register that controls the D/A converter.

■ D/A Converter Control Register(DACTR:0x03FD6)

bp	7	6	5	4	3	2	1	0
Flag	DACHS1	DACHS0	DACKS1	DACKS0	DACMD2	DACMD1	DACMD0	DABUSY
At reset	x	x	x	x	x	x	x	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	DACHS1-0	Monitor flag DA conversion 00:During channel 0 conversion 01:During channel 1 conversion 10:During channel 2 conversion 11:During channel 3 conversion
5-4	DACKS1-0	DA scan clock 00:fs/16 01:fs/32 10:fs/64 11:fs/128
3-1	DACMD2-0	DA conversion mode selection 000:Channel 0 fixed conversion 001:Channel 1 fixed conversion 010:Channel 2 fixed conversion 011:Channel 3 fixed conversion 1*0:2 Channel scan conversion (Channel0, 1) 1*1:4 Channel scan conversion (Channel0, 1,2,3)
0	DABUSY	D/A conversion enable flag 0:Stop D/A converter operation(ladder resistance OFF) 1:Enable D/A converter operation

14.2.3 D/A Converter Input Data Register

This readable/writable register stores the D/A converter data.

■ D/A Converter Input Data Register 0(DADR0:0x03FD7)

This register stores the D/A converter data(for DA0 channel).

bp	7	6	5	4	3	2	1	0
Flag	DA0BUF7	DA0BUF6	DA0BUF5	DA0BUF4	DA0BUF3	DA0BUF2	DA0BUF1	DA0BUF0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ D/A Converter Input Data Register 1(DADR1:0x03FD8)

This register stores the D/A converter data(for DA1 channel).

bp	7	6	5	4	3	2	1	0
Flag	DA1BUF7	DA1BUF6	DA1BUF5	DA1BUF4	DA1BUF3	DA1BUF2	DA1BUF1	DA1BUF0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ D/A Converter Input Data Register 2(DADR2:0x03FD9)

This register stores the D/A converter data(for DA2 channel).

bp	7	6	5	4	3	2	1	0
Flag	DA2BUF7	DA2BUF6	DA2BUF5	DA2BUF4	DA2BUF3	DA2BUF2	DA2BUF1	DA2BUF0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ D/A Converter Input Data Register 3(DADR3:0x03FDA)

This register stores the D/A converter data(for DA3 channel).

bp	7	6	5	4	3	2	1	0
Flag	DA3BUF7	DA3BUF6	DA3BUF5	DA3BUF4	DA3BUF3	DA3BUF2	DA3BUF1	DA3BUF0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.3 Operation

Procedures of D/A converter operation is as follows;

1. Select the D/A conversion mode by the DACMD2 to DACMD1 flag of the D/A control register (DACTR).

2. Set the switching time of analog output channel by the DACKS1 to DACKS0 flag of the DACTR register. When the fixed conversion mode is selected in (1), this setup is not valid.

3. Set the DABUSY flag of the DACTR register to "1" to send a ladder resistance current to start the D/A conversion.

4. The D/A conversion is done to the data that is set to the DADR3 to DADR0 register, and its result output to the DA_A to DA_D in accordance with the setup in (1), (2). If the scan conversion is selected, the pins are high impedance while D/A output is not done.

5. When the D/A conversion is stopped, set the DABUSY flag to "0".

*Tscan is the time set by DACKS1, DACKS0

*Pin for 1/2 of Tscan is high-impedance not to output inadequantly
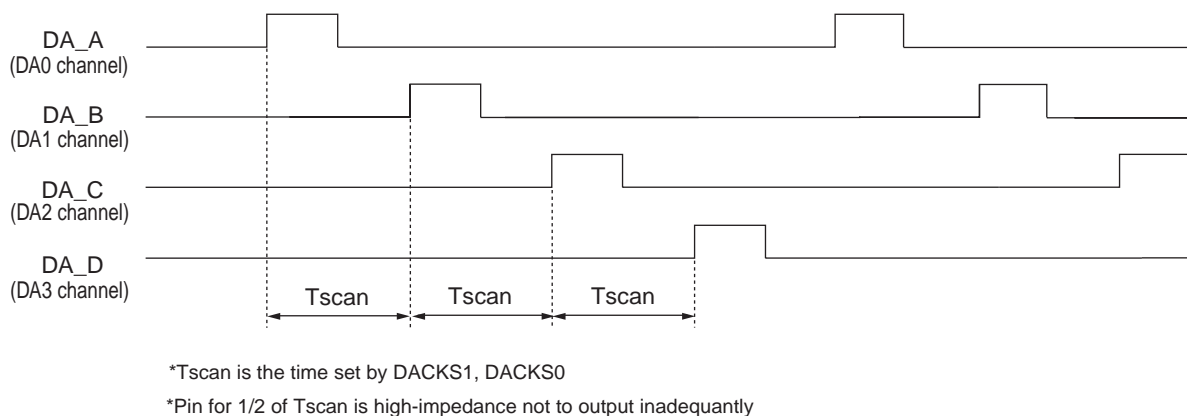
Figure:14.3.1 4 Channel Scan Conversion Mode Timing

⚠ To select D/A scan clock, set more than the settling time.

14.3.1   Setup Example

■ Setup Example by DABUSY0 Flag

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description

(1) Set the port 0 pin.
    P0DIR(0x03F30)
    bp7 :P0DIR7 =0
    SELUD(0x03F4C)
    bp0 :SELUD0 =0
    P0PLUD(0x03F40)
    bp7 :P0PLUD7 =0
	(1) Set the analog output pin to "input mode" by the port 0 output direction control register(P0DIR). Also set the SELUD0 flag of the SELUD register to "0" to select the pull-up registor. And set to the "no pull-up/down registor" by the port 0 pull-up/down registor(P0PLUD).

(2) Set the D/A converter data. DADR0(0x03FD7)	(2) Set the D/A converter data by the D/A converter input data register 0(DADR0).

(3) Start the D/A conversion.
    DACTR(0x03FD6)
    bp0 :DABUSY =1
	(3) Set the DABUSY flag of the D/A converter control register(DACTR) to "1" to start the D/A conversion. The result obtained from the conversion is output to the DA0 pin.

(4) Stop the D/A conversion.
    DACTR(0x03FD6)
    bp0 :DABUSY =0
	(4) Reset the DABUSY flag of the D/A converter control register(DACTR) to "0" to stop the D/A conversion.

Chapter 15 LCD

15

15.1 Functions

This LSI contains an internal LCD driver circuit with 55 segment pins and 4 common pins. The LCD driver contains of a segment output latch, LCD control registers, a prescaler, a timing control circuit, a multiplexer, segment drivers, common drivers and voltage divider resistors.

15.1.1   Functions

Table:15.1.1 shows the functions of the LCD driver circuits.

Table:15.1.1 LCD Functions

	LCD
Duty	Static 1/2 Duty 1/3 Duty 1/4 Duty
Segment Output Pins	SEG0 to SEG54
Common Output Pins	COM0 to COM3
LCD Power Supply	V_{LC1} to V_{LC3}
LCD Voltage Divider Resistor	V_{LC1} input voltage can be divided into 2/3, 1/3. Selectable from high resistance or low resistance.
Clock Source (LCDCLK)	$fpll/2^{11}$ $fpll/2^{12}$ $fpll/2^{13}$ $fpll/2^{14}$ $fpll/2^{15}$ $fpll/2^{16}$ $fpll/2^{17}$ $fpll/2^{18}$ $fx/2^{6}$ $fx/2^{7}$ $fx/2^{8}$ $fx/2^{9}$ Timer 0 to 4 and simple timer A selection
fpll: Machine clock (High speed oscillation) fx: Machine clock (Low speed oscillation) LCDCLK: LCD clock source (selected with LCDCK0 to LCDCK3)	

Use the LCD panel driver voltage V_{LCD} as $V_{LCD} \leq V_{DD5} \leq 5.5$ v

15.1.2   LCD Operation in Standby Mode

Certain LCD driver operation could be limited in standby mode.

Table:15.1.2 shows the LCD operation capabilities in standby mode.

Table:15.1.2 LCD Operation in Standby Mode

CPU Mode		LCD Clock	
		fpll	fx
Operation Mode	NORMAL	√	√
	SLOW	×	√
Standby Mode	HALT0	Δ	Δ
	HALT1	×	Δ
	STOP	×	×
√: LCD Operation is available. Δ: Holding Display is available. ×: LCD Operation is not available.			

For transition to CPU mode in which LCD operation is not available, turn the LCD off and switch segment output to port in advance.

Set bp5 of the low-speed oscillation selection register (XSEL) to "1" before the transition to the slow oscillation mode.

15.1.3   Maximum Pixels

Table:15.1.3 shows the maximum pixels.

Table:15.1.3 Maximum Pixels

Duty	Maximum Pixels (Segment × Common)	8-Segment LCD Panel	Common Pins	Segment Output Latch bits
Static	55 (55 × 1)	6 figures	COM0	bit0, bit4
1/2	110 (55 × 2)	13 figures	COM0 to COM1	bit0 to bit1, bit4 to bit5
1/3	165 (55 × 3)	20 figures	COM0 to COM2	bit0 to bit2, bit4 to bit6
1/4	220 (55 × 4)	27 figures	COM0 to COM3	bit0 to bit3, bit4 to bit7

15.1.4   Switching I/O ports and LCD segment pins

Switching of port output and segment output is controlled with the LCD output control register 1 to 7 (LCCTR1 to LCCTR7). [Chapter 15.2 Control Registers]

Switching of normal port, common pin and V_{LC1} pin to V_{LC3} pin are controlled with the LCD output control register 0 (LCCTR0).

[Chapter 15.2 Control Registers]

   Segment pin, common pin and V_{LC1} pin to V_{LC3} pin are switchable to I/O port in 1-bit unit.

15.1.5   Block Diagram
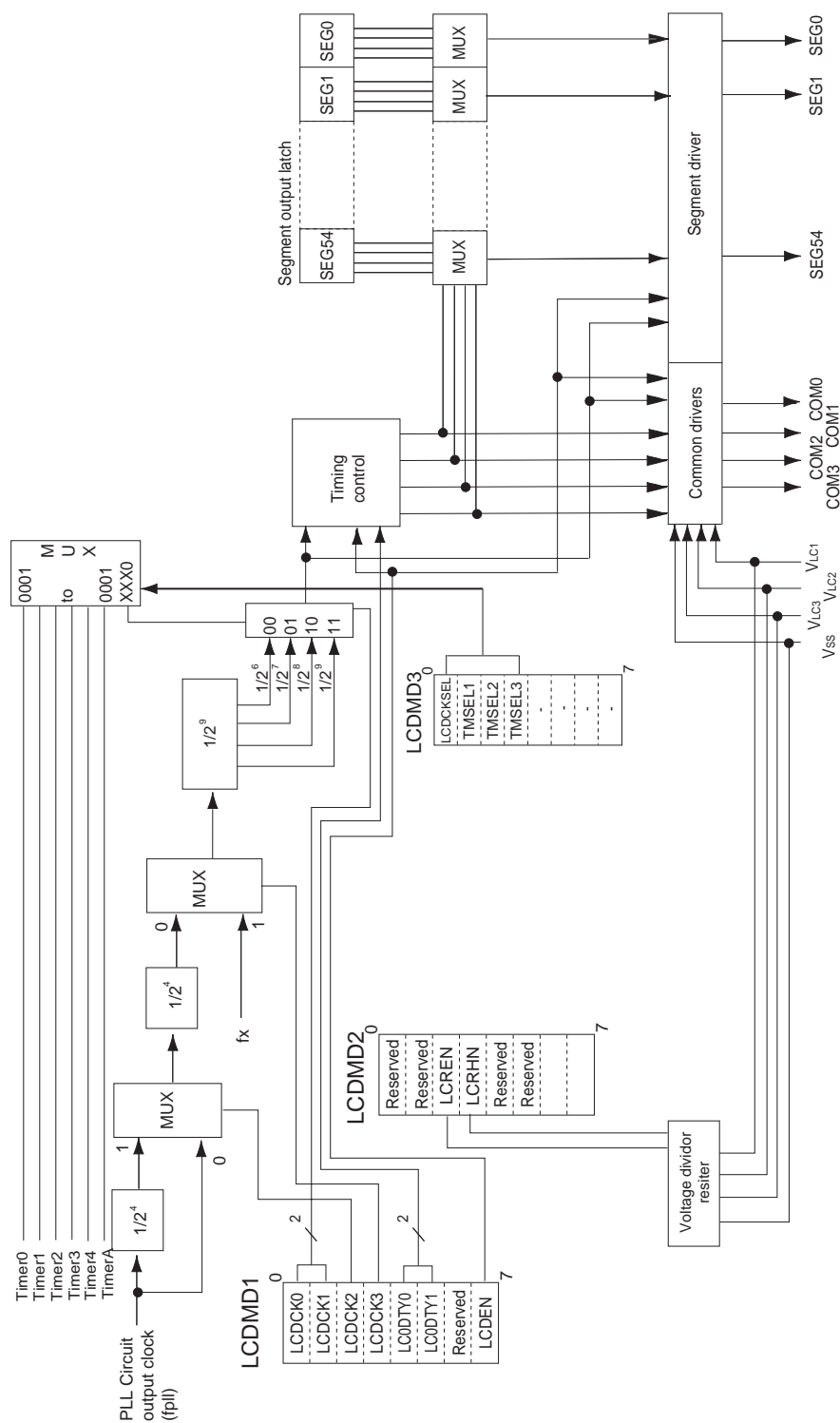
Figure:15.1.1 LCD Driver Circuit Block Diagram

15.2 Control Registers

The LCD is controlled by LCD mode control register 1 to 3 (LCDMD1 to LCDMD3) and LCD output control register 0 to 7 (LCCTR0 to LCCTR7). The LCD display data is stored in the segment output latch.

15.2.1　Registers

Table:15.2.1 shows the LCD control registers.

Table:15.2.1 LCD Control Registers List

Register	Address	R/W	Function	Page
LCDMD1	0x03E90	R/W	LCD mode control register 1	XVI-7
LCDMD2	0x03E91	R/W	LCD mode control register 2	XVI-9
LCDMD3	0x03E92	R/W	LCD mode control register 3	XVI-10
LCCTR0	0x03E93	R/W	LCD output control register 0	XVI-13
LCCTR1	0x03E94	R/W	LCD output control register 1	XVI-13
LCCTR2	0x03E95	R/W	LCD output control register 2	XVI-14
LCCTR3	0x03E96	R/W	LCD output control register 3	XVI-15
LCCTR4	0x03E97	R/W	LCD output control register 4	XVI-16
LCCTR5	0x03E98	R/W	LCD output control register 5	XVI-15
LCCTR6	0x03E99	R/W	LCD output control register 6	XVI-18
LCCTR7	0x03E9A	R/W	LCD output control register 7	XVI-19

R/W: Readable/Writable

* Address 0x03E70 to 0x03E8B are assigned to the segment output latch.

[Chapter 15.2.13 Segment Output Latch]

15.2.2 Mode Control Register 1 (LCDMD1)

The LCD mode control register 1 (LCDMD1) is a 8-bit register that controls LCD clock, LCD panel ON/OFF, and selecting display duty. The value of the LCDMD1 register is initialized at reset.

Table:15.2.2 shows the LCD control registers.

■ Mode Control Register 1 (LCDMD1: 0x03E90, R/W)

Table:15.2.2 LCD Mode Control Register 1

	7	6	5	4	3	2	1	0
Flag	LCDEN	Reserved	LCDTY1	LCDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LCDEN	LCD driver circuit start flag 0: Stop 1: Start
6	Reserved	Always set to "0" *.
5-4	LCDTY1 LCDTY0	LCD display duty selection 00: 1/4 duty 01: 1/3 duty 10: 1/2 duty 11: Static
3-0	LCDCK3 LCDCK2 LCDCK1 LCDCK0	LCD clock source selection 0000: $fpll/2^{11}$ 0001: $fpll/2^{12}$ 0010: $fpll/2^{13}$ 0011: $fpll/2^{14}$ 0100: $fpll/2^{15}$ 0101: $fpll/2^{16}$ 0110: $fpll/2^{17}$ 0111: $fpll/2^{18}$ 1X00: $fx/2^{6}$ 1X01: $fx/2^{7}$ 1X10: $fx/2^{8}$ 1X11: $fx/2^{9}$

Set bp5 of the low-speed oscillation selection register (XSEL) to "1" before the transition to the slow oscillation mode.

When the LCDEN flag of LCDMD1 register being set, do not change other flags of LCDMDn register to prevent malfunction.

Always set "0" to the bp denoted by asterisk.

15.2.3 Mode Control Register 2 (LCDMD2)

The LCD mode control register 2 (LCDMD2) is a 8-bit register that controls internal voltage divider circuit ON/ OFF and selecting of internal voltage booster circuit. The value of the LCDMD2 register is initialized at reset.

Table:15.2.3 shows the LCD control registers.

■ Mode Control Register 2 (LCDMD2: 0x03E91, R/W)

Table:15.2.3 LCD Mode Control Register 2

	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	Reserved	LCRHL	LCREN	UPCK	UPEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7-4	Reserved	Always set to "0" *.
3	LCRHL	Internal partial pressure resistor type selection 0: Low resistance (V_{LC1} to V_{LC2}, V_{LC2} to V_{LC3}, V_{LC3} to V_{SS}, about 10 kΩ) 1: High resistance (V_{LC1} to V_{LC2}, V_{LC2} to V_{LC3}, V_{LC3} to V_{SS}, about 100 kΩ)
2	LCREN	Internal partial pressure circuit connect selection 0: Unconnected 1: Connected
1-0	Reserved	Always set to "0" *.

Always set "0" to the bp denoted by asterisk.

15.2.4 Mode Control Register 3 (LCDMD3)

The LCD mode control register 3 (LCDMD3) is a 4-bit register that switches the oscillation dividing circuit and the selection timer. The value of the LCDMD3 register is initialized at reset.

Table:15.2.4 shows the LCD control registers.

■ Mode Control Register 3 (LCDMD3:0x03E92, R/W)

Table:15.2.4 LCD Mode Control Register 3

	7	6	5	4	3	2	1	0
Flag	-	-	-	-	TMSEL3	TMSEL2	TMSEL1	LCDCKSEL
Reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

	Flag	Description
7-4	-	Always set to "0" *.
3-1	TMSEL3-1	Timer0 to 4, A input selection 000: Timer0 001: Timer1 010: Timer2 011: Timer3 100: Timer4 101: TimerA 11x: Disable
0	LCDCKSEL	Oscillation dividing circuit/selection timer 0: Oscillation dividing circuit 1: Selection timer

Always set "0" to the bp denoted by asterisk.

15.2.5   Output Control Register 0 (LCCTR0)

The LCD output control register 0 (LCCTR0) is a 2-bit register that switches Port I/O (P84 to P87) and VLC pins (COM0 to COM3) and switches Port I/O (P92 to 94) and VLC pins (V_{LC1} to V_{LC3}). The value of the LCCTR0 register is set port at reset.

■   Output Control Register 0(LCCTR0:0x03E93, R/W)

Table:15.2.5 LCD Output Control Register 0

	7	6	5	4	3	2	1	0
Flag	COMSL3	COMSL2	COMSL1	COMSL0	Reserved	VLC3SL	VLC2SL	VLC1SL
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	COMSL3	COM3/Port87 selection 0: Port87 1: COM3
6	COMSL2	COM2/Port86 selection 0: Port86 1: COM2
5	COMSL1	COM1/Port85 selection 0: Port85 1: COM1
4	COMSL0	COM0/Port84 selection 0: Port84 1: COM0
3	Reserved	Always set to "0" *
2	VLC3SL	VLC3/Port92 selection 0: Port92 1: VLC3
1	VLC2SL	VLC2/Port93 selection 0: Port91 1: VLC2
0	VLC1SL	VLC1/Port94 selection 0: Port90 1: VLC1

P94(V_{LC1}), P93(V_{LC2}) and P92(V_{LC3}) can be used as a port when using the internal voltage dividing resistor, but LCD display may not have enough brightness depending on panels you used. Because the stabilization capacity can not be connected to outside.
If LCD display can not have enough brightness, use the exeternal voltage dividing resistor.

Always set "0" to the bp denoted by asterisk.

15.2.6　Output Control Register 1 (LCCTR1)

The LCD output control register 1 (LCCTR1) switches port I/O (P80 to P83, P74 to P77) and segment output (SEG0 to SEG7). At reset, these ports are set to the port.

■　Output Control Register 1(LCCTR1:0x03E94, R/W)

Table:15.2.6 LCD Output Control Register 1

	7	6	5	4	3	2	1	0
Flag	LC1SL7	LC1SL6	LC1SL5	LC1SL4	LC1SL3	LC1SL2	LC1SL1	LC1SL0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LC1SL7	SEG7/Port74 selection 0: Port74 1: SEG7
6	LC1SL6	SEG6/Port75 selection 0: Port75 1: SEG6
5	LC1SL5	SEG5/Port76 selection 0: Port76 1: SEG5
4	LC1SL4	SEG4/Port77 selection 0: Port77 1: SEG4
3	LC1SL3	SEG3/Port80 selection 0: Port80 1: SEG3
2	LC1SL2	SEG2/Port81 selection 0: Port81 1: SEG2
1	LC1SL1	SEG1/Port82 selection 0: Port82 1: SEG1
0	LC1SL0	SEG0/Port83 selection 0: Port83 1: SEG0

15.2.7   Output Control Register 2 (LCCTR2)

The LCD output control register 2 (LCCTR2) switches port I/O (P70 to P73, P64 to P67) and segment output (SEG8 to SEG15). At reset, these ports are set to the port.

■   Output Control Register 2(LCCTR2:0x03E95, R/W)

Table:15.2.7 LCD Output Control Register 2

	7	6	5	4	3	2	1	0
Flag	LC2SL7	LC2SL6	LC2SL5	LC2SL4	LC2SL3	LC2SL2	LC2SL1	LC2SL0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LC2SL7	SEG15/Port64 selection 0: Port64 1: SEG15
6	LC2SL6	SEG14/Port65 selection 0: Port65 1: SEG14
5	LC2SL5	SEG13/Port66 selection 0: Port66 1: SEG13
4	LC2SL4	SEG12/Port67 selection 0: Port67 1: SEG12
3	LC2SL3	SEG11/Port70 selection 0: Port70 1: SEG11
2	LC2SL2	SEG10/Port71 selection 0: Port71 1: SEG10
1	LC2SL1	SEG9/Port72 selection 0: Port72 1: SEG9
0	LC2SL0	SEG8/Port73 selection 0: Port73 1: SEG8

15.2.8 Output Control Register 3 (LCCTR3)

The LCD output control register 3 (LCCTR3) switches port I/O (P60 toP63, P50 to P53) and segment output (SEG16 to SEG23). At reset, these ports are set to the port.

■ Output Control Register 3 (LCCTR3:0x03E96, R/W)

Table:15.2.8 LCD Output Control Register 3

	7	6	5	4	3	2	1	0
Flag	LC3SL7	LC3SL6	LC3SL5	LC3SL4	LC3SL3	LC3SL2	LC3SL1	LC3SL0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LC3SL7	SEG23/Port53 selection 0: Port53 1: SEG23
6	LC3SL6	SEG22/Port52 selection 0: Port52 1: SEG22
5	LC3SL5	SEG21/Port51 selection 0: Port51 1: SEG21
4	LC3SL4	SEG20/Port50 selection 0: Port50 1: SEG20
3	LC3SL3	SEG19/Port60 selection 0: Port60 1: SEG19
2	LC3SL2	SEG18/Port61 selection 0: Port61 1: SEG18
1	LC3SL1	SEG17/Port62 selection 0: Port62 1: SEG17
0	LC3SL0	SEG16/Port63 selection 0: Port63 1: SEG16

15.2.9　Output Control Register 4 (LCCTR4)

The LCD output control register 4 (LCCTR4) switches port I/O (P54 to P57, P44 to P47) and segment output (SEG24 to SEG31). At reset, these ports are set to the port.

■　Output Control Register 4 (LCCTR4:0x03E97, R/W)

Table:15.2.9 LCD Output Control Register 4

	7	6	5	4	3	2	1	0
Flag	LC4SL7	LC4SL6	LC4SL5	LC4SL4	LC4SL3	LC4SL2	LC4SL1	LC4SL0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LC4SL7	SEG31/Port44 selection 0: Port44 1: SEG31
6	LC4SL6	SEG30/Port45 selection 0: Port45 1: SEG30
5	LC4SL5	SEG29/Port46 selection 0: Port46 1: SEG29
4	LC4SL4	SEG28/Port47 selection 0: Port47 1: SEG28
3	LC4SL3	SEG27/Port57 selection 0: Port57 1: SEG27
2	LC4SL2	SEG26/Port56 selection 0: Port56 1: SEG26
1	LC4SL1	SEG25/Port55 selection 0: Port55 1: SEG25
0	LC4SL0	SEG24/Port54 selection 0: Port54 1: SEG24

15.2.10 Output Control Register 5 (LCCTR5)

The LCD output control register 5 (LCCTR5) switches port I/O (P40 to P43, P33 to P36) and segment output (SEG32 to SEG39). At reset, these ports are set to the port.

■ Output Control Register 5 (LCCTR5:0x03E98, R/W)

Table:15.2.10 LCD Output Control Register 5

	7	6	5	4	3	2	1	0
Flag	LC5SL7	LC5SL6	LC5SL5	LC5SL4	LC5SL3	LC5SL2	LC5SL1	LC5SL0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LC5SL7	SEG39/Port33 selection 0: Port33 1: SEG39
6	LC5SL6	SEG38/Port34 selection 0: Port34 1: SEG38
5	LC5SL5	SEG37/Port35 selection 0: Port35 1: SEG37
4	LC5SL4	SEG36/Port36 selection 0: Port36 1: SEG36
3	LC5SL3	SEG35/Port40 selection 0: Port40 1: SEG35
2	LC5SL2	SEG34/Port41 selection 0: Port41 1: SEG34
1	LC5SL1	SEG33/Port42 selection 0: Port42 1: SEG33
0	LC5SL0	SEG32/Port43 selection 0: Port43 1: SEG32

15.2.11 Output Control Register 6 (LCCTR6)

The LCD output control register 6 (LCCTR6) switches port I/O (P30 to P32, P12 to P16) and segment output (SEG40 to SEG47). At reset, these ports are set to the port.

■ Output Control Register 6 (LCCTR6:0x03E99, R/W)

Table:15.2.11 LCD Output Control Register 6

	7	6	5	4	3	2	1	0
Flag	LC6SL7	LC6SL6	LC6SL5	LC6SL4	LC6SL3	LC6SL2	LC6SL1	LC6SL0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7	LC6SL7	SEG47/Port12 selection 0: Port12 1: SEG47
6	LC6SL6	SEG46/Port13 selection 0: Port13 1: SEG46
5	LC6SL5	SEG45/Port14 selection 0: Port14 1: SEG45
4	LC6SL4	SEG44/Port15 selection 0: Port15 1: SEG44
3	LC6SL3	SEG43/Port16 selection 0: Port16 1: SEG43
2	LC6SL2	SEG42/Port30 selection 0: Port30 1: SEG42
1	LC6SL1	SEG41/Port31 selection 0: Port31 1: SEG41
0	LC6SL0	SEG40/Port32 selection 0: Port32 1: SEG40

15.2.12 Output Control Register 7 (LCCTR7)

The LCD output control register 7 (LCCTR7) switches port I/O (P10 to P11, P20 to P24) and segment output (SEG48 to SEG54). At reset, these ports are set to the port.

■ Output Control Register 7 (LCCTR5:0x03E9A, R/W)

Table:15.2.12 LCD Output Control Register 7

	7	6	5	4	3	2	1	0
Flag	-	LC7SL6	LC7SL5	LC7SL4	LC7SL3	LC7SL2	LC7SL1	LC7SL0
Reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
-	-	-
6	LC7SL6	SEG54/Port20 selection 0: Port20 1: SEG54
5	LC7SL5	SEG53/Port21 selection 0: Port21 1: SEG53
4	LC7SL4	SEG52/Port22 selection 0: Port22 1: SEG52
3	LC7SL3	SEG51/Port23 selection 0: Port23 1: SEG51
2	LC7SL2	SEG50/Port24 selection 0: Port24 1: SEG50
1	LC7SL1	SEG49/Port10 selection 0: Port10 1: SEG49
0	LC7SL0	SEG48/Port11 selection 0: Port11 1: SEG48

15.2.13 Segment Output Latch

A 4-bit latch is allocated per segment. Bit0 and bit4 are read out at the timing of COM0, bit1 and bit5 are read out at the timing of COM1, bit2 and bit6 are read out at the timing of COM2, and bit3 and bit7 are read out at the timing of COM3. If a bit points "1", the segment pin outputs the "selected voltage", and if a bit points "0", the segment pin outputs "non-selected voltage".

The assigned address are 0x03E70 to 0x03E8B, and segment output latch value is indefinite at reset.

Figure:15.2.1 shows the matching of the segment output latch and the segment/common pins.

Address	COM3 bit7	COM2 bit6	COM1 bit5	COM0 bit4		COM3 bit3	COM2 bit2	COM1 bit1	COM0 bit0	
X'3E70'					→ SEG 1/P82					→ SEG 0/P83
X'3E71'					→ SEG 3/P80					→ SEG 2/P81
X'3E72'					→ SEG 5/P76					→ SEG 4/P77
X'3E73'					→ SEG 7/P74					→ SEG 6/P75
X'3E74'					→ SEG 9/P72					→ SEG 8/P73
X'3E75'					→ SEG11/P70					→ SEG10/P71
X'3E76'					→ SEG13/P66					→ SEG12/P67
X'3E77'					→ SEG15/P64					→ SEG14/P65
X'3E78'					→ SEG17/P62					→ SEG16/P63
X'3E79'					→ SEG19/P60					→ SEG18/P61
X'3E7A'					→ SEG21/P51					→ SEG20/P50
X'3E7B'					→ SEG23/P53					→ SEG22/P52
X'3E7C'					→ SEG25/P55					→ SEG24/P54
X'3E7D'					→ SEG27/P57					→ SEG26/P56
X'3E7E'					→ SEG29/P46					→ SEG28/P47
X'3E7F'					→ SEG31/P44					→ SEG30/P45
X'3E80'					→ SEG33/P42					→ SEG32/P43
X'3E81'					→ SEG35/P40					→ SEG34/P41
X'3E82'					→ SEG37/P35					→ SEG36/P36
X'3E83'					→ SEG39/P33					→ SEG38/P34
X'3E84'					→ SEG41/P31					→ SEG40/P32
X'3E85'					→ SEG43/P16					→ SEG42/P30
X'3E86'					→ SEG45/P14					→ SEG44/P15
X'3E87'					→ SEG47/P12					→ SEG46/P13
X'3E88'					→ SEG49/P10					→ SEG48/P11
X'3E89'					→ SEG51/P23					→ SEG50/P24
X'3E8A'					→ SEG53/P21					→ SEG52/P22
X'3E8B'										→ SEG54/P20

at static

at 1/2duty

at 1/3duty

at 1/4duty

Figure:15.2.1 Matching of the Segment Output Latch and the Segment/Common Pins

15.3 Operation

15.3.1 Operation

The LCD driver is capable of static display and dynamic display (1/2 duty 1/2 bias, 1/3 duty 1/3 bias, 1/4 duty 1/3 bias) through the segment output pins (SEG0 to SEG54) and the common output pins (COM0 to COM3).

■ The LCD driver circuit operation

The LCD driver circuit generates the timing signals, which are necessary for controlling 1/2 duty, 1/3 duty, 1/4 duty and static, at the timing control circuit, based on the LCD clock divided by the prescaler, and supplies them to the common driver and the multiplexer.

The common driver outputs the common signals which are necessary for the LCD display, based on the voltage from the LCD power supply. When the LCD is OFF Vss is output and the potential difference between the LCD electrodes becomes 0 V.

The multiplexer selects the segment output latched data in response to the signal from the timing control circuit and supplies it to the segment driver. The segment driver converts the content of the segment output latch into the signals, which is capable of driving the LCD, based on the voltage supplied to LCD power supply, then outputs the segment signal.
When the LCD is OFF Vss is output and the potential difference between the LCD electrodes becomes 0 V.

> At reset, common pins and segment pins become high impedance.
> Therefore, when reset input from external sources is long, there could be some adverse effects such as blinks of the LCD display.

> In STOP mode, supplies from the main clocks is stopped, and the LCD drive cannot be operated. Set "0" to the enable flag of the LCD driver circuit before entering STOP mode.

> Set bp5 of the low-speed oscillation selection register (XSEL) to "1" before the transition to the slow oscillation mode.

15.3.2　Power Supply

The driver power pins are V_{LC1}, V_{LC2} and V_{LC3}. The voltage divider resistor to divide voltage for LCD drive. There are four ways to supply voltage to the LCD driver; to supply voltage to the V_{LC1}, V_{LC2} and V_{LC3} pins from external source (when external voltage divider resistor is used) and to supply voltage to V_{LC1} pin from external source and use internal divider resistor,.

The power source for LCD drive and V_{DD5} power supply for the micro controller are separated so that the voltage V_{LCD} for LCD panel drive can be used at higher voltage than the V_{DD5} power supply (usable at $V_{LCD} \leq V_{DD5} \leq$ 5.5 V).

The LCD driver voltage supplied through the LCD driver power pins (V_{LC1}, V_{LC2} and V_{LC3}) is converted by the LCD clock signal and the timing control signal, and then supplied to the segment driver and the common driver.

Table:15.3.1 Supplying LCD drive voltage (In using 1/3 bias)

	Supplying voltage	Reference voltage supplying pin	Description
1	Supply the drive voltage directly	V_{LC1} V_{LC2} V_{LC3}	Supply voltage to VLC1, VLC2, VLC3 pins externally.
2	Use the external dividing resistor	V_{LC1} V_{LC2} V_{LC3}	Supply the reference voltage to VLC1 pin externally and generate VLC2, VLC3 potentials at the external resistor divider, then supply the voltage to each pin.
3	Use the internal dividing resistor	V_{LC1}	Supply the reference voltage to VLC1 externally and generate VLC2, VLC3 potentials by using the internal resistor.,

■ Supplying voltage with the external voltage divider resistor

Supply the voltage as shown in Table:15.3.2.

Table:15.3.2 LCD Power Supply

	Static	1/2 bias	1/3 bias
V_{LC1}	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$
V_{LC2}		$1/2V_{LCD} + V_{SS}$	$2/3V_{LCD} + V_{SS}$
V_{LC3}	V_{SS}		$1/3V_{LCD} + V_{SS}$

V_{LCD}: LCD panel driver voltage (Maximum voltage to the LCD panel)

Use the LCD panel driver voltage at $V_{LCD} \leq V_{DD5} \leq 5.5$ V.

Figure:15.3.1 shows example of the LCD power supply connection.

Stabilization condenser C for LCD power supply is recommended to be C = 0.1 μF.

(a)Static ($V_{DD5}=V_{LCD}$)
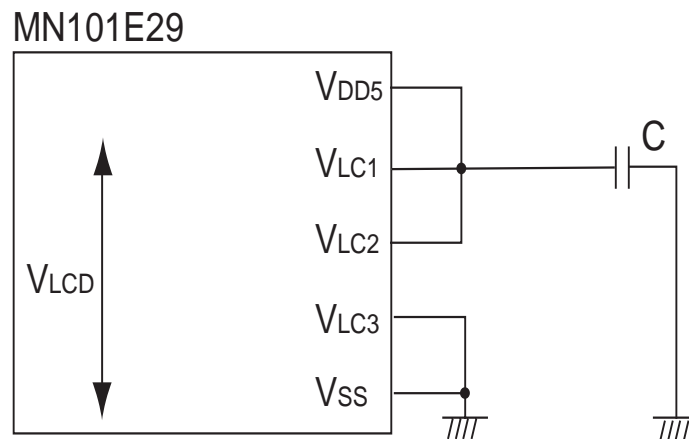
(b)1/3duty 1/3bias, 1/4duty 1/3bias ($V_{DD5}=V_{LCD}$)
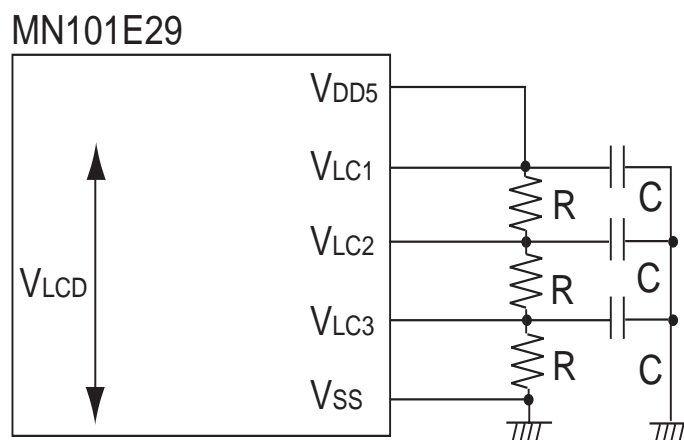
Figure:15.3.1 LCD Power Supply Connection (When using External Voltage Divider Resistors)

1. In Figure:15.3.1, current always flows through the voltage divider resistors.
   The following connection is used to cut the current flowing through these dividing resistors.
   (at $V_{LC1} = V_{DD5}$)
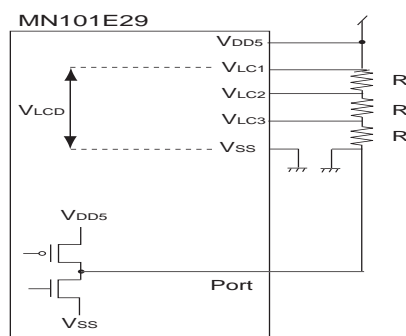
Figure:15.3.2 LCD Power Supply Connection (In external voltage divider)

(1) The voltage difference of the opposite ends of devided resistor R is generated by outputting Port to V_{SS} in LCD driver, and the divided voltage is input to each of V_{LC1} to V_{LC3}.

(2) When LCD driver is stopped, the voltage difference of the opposite ends of devided resistor R become equalized and the current to flow to devided resistor R can be cut.

2. The LCD power supply V_{LC1} to V_{LC3} is supplied as shown in the following Figure:15.3.3.
   V_{LCD} value varies depending on the type of LCD. Refer to the specifications of LCD for the appropriate value.

$$V_{LC1} = V_{LCD} + V_{SS}$$
$$V_{LC2} = 2/3\ V_{LCD} + V_{SS}$$
$$V_{LC3} = 1/3\ V_{LCD} + V_{SS}$$

Usually V_{DD5} - Vss are divided by resistors and supplied to the LCD.

Standard resistance voltage ranges from tens to several hundreds kW.

In Figure:15.3.3, a bypass capacitor C (about 0.1 μF) is used to lower the impedance of power supply.
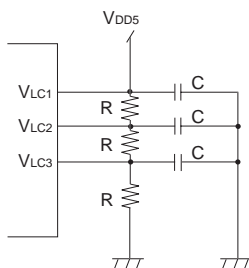
Figure:15.3.3 Supplying Voltage to V_{LC1} to V_{LC3}

■ Supplying voltage when using the internal voltage divider circuit

Supply the voltage as shown in Table:15.3.3.

Table:15.3.3 LCD voltage when using the internal voltage dividing resistor

	Static	1/2 bias	1/3 bias
V_{LC1}	Not used	V_{LCD}	V_{LCD}
V_{LC2}		Connect V_{LC2} to V_{LC3} (1/2 V_{LCD} is output.)	(2/3 V_{LCD} is output.)
V_{LC3}			(1/3 V_{LCD} is output.)

When internal divider resistor is used, voltages of V_{LC1}, V_{LC2} and V_{LC3} could be dropped depending on used LCD panel and that may lower the brightness of LCD display. Use the external divider resistor when this happens.

P94(V_{LC1}), P93(V_{LC2}) and P92(V_{LC3}) can be used as a port when using the internal voltage dividing resistor, but LCD display may not have enough brightness depending on panels you used. Because the stabilization capacity can not be connected to outside.
If LCD display can not have enough brightness, connect the stabilization capacity or use the exeternal voltage dividing resistor.

The internal dividing resistor is formed as connecting to between V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and V_{SS}.
In the selection of the internal dividing resistor type, when low resistor is selected, about 10 kΩ resistor is connected between V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and V_{SS}. When high resistor is selected, about 100 kΩ resistor is connected each pin.

When low resistor is selected   When high resistor is selected

MN101E29   MN101E29

R:Approx.10 kΩ V_{LC1} pin   R:Approx.100 kΩ V_{LC1} pin
                      V_{LC2} pin V_{LC2} pin
R:Approx.10 kΩ V_{LC3} pin   R:Approx.100 kΩ V_{LC3} pin
R:Approx.10 kΩ V_{SS} pin   R:Approx.100 kΩ V_{SS} pin
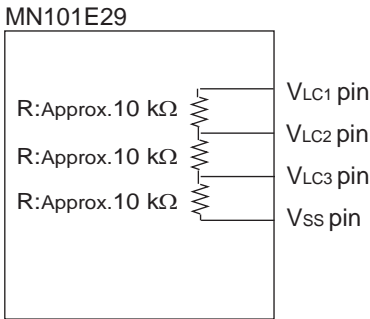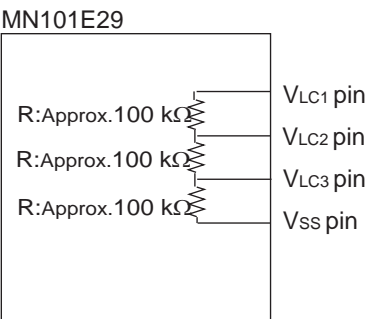
Figure:15.3.4 Configuration and Resistor Value of Internal Dividing Resistor

15.3.3 Frame Cycle

■ Setup of the LCD frame cycle

The clock fpll or fx is divided by the prescaler and supplied as the LCD clock. Set the LCD clock with bit0 to bit3 and set the LCD frame cycle with bit4 to bit5 of the LCDMD1 register. Figure:15.3.5 shows reference input frequencies and the matching of the LCD clock and the LCD frame cycle.

Input cloci LCDCK3 to 0	duty LCDTY1 to 0	10 MHz LCD clock	frame	8 MHz LCD clock	frame	4 MHz LCD clock	frame	2 MHz LCD clock	frame	32.768 kHz LCD ckock	frame
0000 ($OSC1/2^{11}$)	00 (1/4 duty)	4883 Hz	1221 Hz	3906Hz	977 Hz	1953 Hz	488 Hz	977 Hz	244 Hz		
	01 (1/3 duty)		1628 Hz		1302 Hz		651 Hz		326 Hz		
	10 (1/2 duty)		2441 Hz		1953 Hz		977 Hz		488 Hz		
	11 (static)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
0001 ($OSC1/2^{12}$)	00 (1/4 duty)	2441 Hz	610 Hz	1953 Hz	488 Hz	977 Hz	244 Hz	488 Hz	122 Hz		
	01 (1/3 duty)		814 Hz		651 Hz		326 Hz		163 Hz		
	10 (1/2 duty)		1221 Hz		977 Hz		488 Hz		244 Hz		
	11 (static)		2441 Hz		1953 Hz		977 Hz		488 Hz		
0010 ($OSC1/2^{13}$)	00 (1/4 duty)	1221 Hz	305 Hz	977 Hz	244 Hz	488 Hz	122 Hz	244 Hz	61 Hz		
	01 (1/3 duty)		407 Hz		326 Hz		163 Hz		81 Hz		
	10 (1/2 duty)		610 Hz		488 Hz		244 Hz		122 Hz		
	11 (static)		1221 Hz		977 Hz		488 Hz		244 Hz		
0011 ($OSC1/2^{14}$)	00 (1/4 duty)	610 Hz	153 Hz	488 Hz	122 Hz	244 Hz	61 Hz	122 Hz	31 Hz		
	01 (1/3 duty)		203 Hz		163 Hz		81 Hz		41 Hz		
	10 (1/2 duty)		305 Hz		244 Hz		122 Hz		61 Hz		
	11 (static)		610 Hz		488 Hz		244 Hz		122 Hz		
0100 ($OSC1/2^{15}$)	00 (1/4 duty)	305 Hz	76 Hz	244 Hz	61 Hz	122 Hz	31 Hz	61 Hz	15 Hz		
	01 (1/3 duty)		102 Hz		81 Hz		41 Hz		20 Hz		
	10 (1/2 duty)		153 Hz		122 Hz		61 Hz		31 Hz		
	11 (static)		305 Hz		244 Hz		122 Hz		61 Hz		
0101 ($OSC1/2^{16}$)	00 (1/4 duty)	153 Hz	38 Hz	122 Hz	31 Hz	61 Hz	15 Hz	31 Hz	8 Hz		
	01 (1/3 duty)		51 Hz		41 Hz		20 Hz		10 Hz		
	10 (1/2 duty)		76 Hz		61 Hz		31 Hz		15 Hz		
	11 (static)		153 Hz		122 Hz		61 Hz		31 Hz		
0110 ($OSC1/2^{17}$)	00 (1/4 duty)	76 Hz	19 Hz	61 Hz	15 Hz	31 Hz	8 Hz	15 Hz	4 Hz		
	01 (1/3 duty)		25 Hz		20 Hz		10 Hz		5 Hz		
	10 (1/2 duty)		38 Hz		31 Hz		15 Hz		8 Hz		
	11 (static)		76 Hz		61 Hz		31 Hz		15 Hz		
0111 ($OSC1/2^{18}$)	00 (1/4 duty)	38 Hz	10 Hz	31 Hz	8 Hz	15 Hz	4 Hz	8 Hz	2 Hz		
	01 (1/3 duty)		13 Hz		10 Hz		5 Hz		3 Hz		
	10 (1/2 duty)		19 Hz		15 Hz		8 Hz		4 Hz		
	11 (static)		38 Hz		31 Hz		15 Hz		8 Hz		
1X00 ($XI/2^{6}$)	00 (1/4 duty)									512 Hz	128 Hz
	01 (1/3 duty)										171 Hz
	10 (1/2 duty)										256 Hz
	11 (static)										512 Hz
1X01 ($XI/2^{7}$)	00 (1/4 duty)									256 Hz	64 Hz
	01 (1/3 duty)										85 Hz
	10 (1/2 duty)										128 Hz
	11 (static)										256 Hz
1X10 ($XI/2^{8}$)	00 (1/4 duty)									128 Hz	32 Hz
	01 (1/3 duty)										43 Hz
	10 (1/2 duty)										64 Hz
	11 (static)										128 Hz
1X11 ($XI/2^{9}$)	00 (1/4 duty)									64 Hz	16 Hz
	01 (1/3 duty)										21 Hz
	10 (1/2 duty)										32 Hz
	11 (static)										64 Hz

Figure:15.3.5 Input Frequency and the LCD Clock

■ Setup example of the internal voltage dividing resistor

An example of setup procedure to display "23" on a 8 segment type LCD panel in 1/4 duty, 1/3 bias with both segment signals (SEG0 to SEG3) and common signals (COM0 to COM3) by using internal voltage dividing circuit is shown below.

Refer to XV-25. Figure:15.3.2 for the LCD power supply connection. Refer to [Chapter 15 15.4 Display] for connection of LCD panel.

Setup Procedure	Description

(1) Select the internal voltage dividing resistor
    LCDMD2 (0x03E91)
    bp3 : LCRHL = 1
	(1) Set the LCRHL flag of the LCD mode control register 2 (LCDMD2) to "1" to set the internal voltage dividing resistor to "high resistor".

(2) Select the internal voltage dividing resistor connection
    LCDMD2 (0x03E91)
    bp2 : LCREN = 1
	(2) Set the LCREN flag of the LCD mode control register 2 (LCDMD2) to "1" to connect the internal voltage dividing resistor between V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and Vss.

(3) Set the pins
    LCCTR0 (0x03E93)
    bp7-4 : COMSL3-0 = 1111
    LCCTR1 (0x03E94)
    bp3-0 : LC1SL3-0 = 1111
	(3) Set COMSL3 to 0 flags of the LCD mode control register 0 (LCCTR0) to "1111" to set up the common segment 3 to 0.
	Set LC1SL3 to 0 flags of the LCD output control register 1 (LCCTR1) to "1111" to set up the segment pins 3 to 0.

(4) Select the LCD clock source
    LCDMD1 (0x03E90)
    bp3-0 : LCDCK3-0 = 0111
	(4) Select $fpll/2^{18}$ as the LCD clock source by LCDCK3 to 0 flags of the LCD mode control register 1 (LCDMD1).

(5) Select the LCD display duty
    LCDMD1 (0x03E90)
    bp5-4 : LCDTY1-0 = 00
	(5) Set LCDTY1 to 0 flags of the LCD mode control register 1 (LCDMD1) to "00" to set the display duty to 1/4 duty.

(6) Set the LCD panel display data
    0x03E70 = 0x5E
    0x03E71 = 0x7C
	(6) Set up the display data on the address 0x03E70, 0x03E71 of the segment output latch.
	[Chapter 15 15.4 Display]

(7) Start the LCD drive circuit
    LCDMD1 (0x03E90)
    bp7 : LCDEN = 1
	(7) Set the LCDEN flag of the LCD mode control register 1 (LCDMD1) to "1" to start the LCD driver circuit.

If internal voltage booster circuit is used, voltage of V_{LC1}, V_{LC2} and V_{LC3} may be dropped depending on the load of used LCD panel and that may lower the brightness of LCD display. In this case, set the internal voltage dividing resistor selection bit of the LCD mode control register 2 (LCDMD2) to "0" to select the low resistor. By selecting the low resistor, the current supply capability increases.

15.4 Display

15.4.1 to 15.4.8 show example of connections, display and waveforms of the LCD panel in these condition; in 1/2 duty, 1/3 duty, 1/4 duty and static.

15.4.1 Static

■ Static

S:selected voltage N:non-selected voltage

V_{LCD}:LCD driver voltage

On static COM(COM0) always outputs selected voltage.
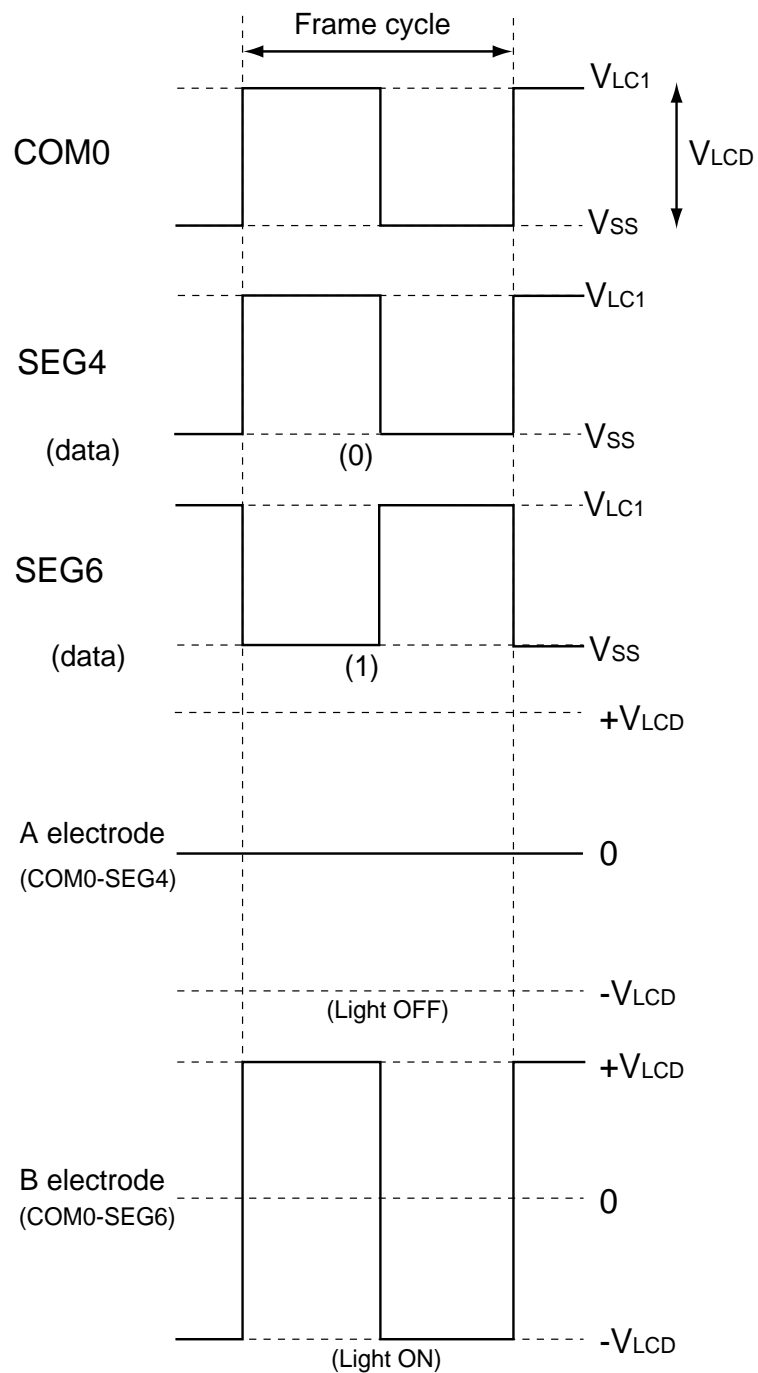
Figure:15.4.1 LCD Display in Static

15.4.2 Setup Example (Static)

■ Setup example of the LCD (static)

An example of setup procedure to display "23" with both segment signals (SEG0 to SEG7) and common signals (COM0), using an external divider resistor is shown below.
[Chapter 15 15.4.1 Static]
Clock source fpll = 4 MHz, a LCD clock source fpll/2^{15} = 122 Hz, and flame cycle = 122 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCDMD1(0x03E90) bp7 :LCDEN = 0	(1) Set "0" to the LCDEN flag of the LCD mode control register (LCDMD1) to stop the LCD operation.
(2) Setup the display duty LCDMD1(0x03E90) bp5-4 :LCDDTY1-0= 11	(2) Set "11" to the LCDTY1 to LCDTY0 flags of the LCD mode control register (LCDMD1) to enter the static drive mode.
(3) Select the LCD clock source LCDMD1(0x03E90) bp3-0 :LCDCK3-0 = 0100	(3) Select fpll/2^{15} as a LCD clock source with LCDCK3 to LCDCK0 flags of the LCD mode control register (LCDMD1).
(4) Select the segment output/port pin Select the common output/port pin LCCTR0(0x03E93) bp4 :COMSL0 = 1 LCCTR1(0x03E94) bp7-0 :LC1SL7-0 = 11111111	(4) Select SEG0 to SEG7 and COM0 with the output control register 0 (LCCTR0) and the output control register 1 (LCCTR1).
(5) Setup the LCD panel display data Segment output latch SEG1-0 (0x03E70) = 0x00 Segment output latch SEG3-2 (0x03E71) = 0x11 Segment output latch SEG5-4 (0x03E72) = 0x10 Segment output latch SEG7-6 (0x03E73) = 0x11	(5) Display "23" on the display panel with the address 0x03E70 to 0x03E73 of the segment output latch SEG7 to SEG0. [Chapter 15 15.4.1 Static]
(6) Start the LCD operation LCDMD1(0x03E90) bp7 :LCDEN = 1	(6) Set "1" to the LCDEN flag of the LCD mode control register (LCDMD1) to start the LCD operation.

15.4.3　1/2 Duty

■　1/2 Duty

MN101E29

LCDPANEL

:Light ON
:Light OFF

A electrode
B electrode

	LCD ON				LCD OFF
	COM=S SEG=S	COM=N SEG=S	COM=S SEG=N	COM=N SEG=N	
LCD clock					uncertain
Data	"1"		"0"		uncertain
COM					
SEG					
COM-SEG					
	Light ON	Light OFF	Light OFF	Light OFF	Light OFF

S:selected voltage　N:non-selected voltage
V_{LCD}:LCD driver voltage

Figure:15.4.2 LCD Display (1/2 Duty)

15.4.4   Setup Example (1/2 duty)

■   Setup example of the LCD (1/2 duty)

An example of setup procedure to display "23" with both segment signals (SEG0 to SEG7) and common signals (COM0 to COM1), using an external divider resistor is shown below.
[Chapter 15 15.4.3 1/2 Duty]

Clock source fpll = 4 MHz, a LCD clock source $fpll/2^{15}$ = 122 Hz, and flame cycle = 61 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation 　　LCDMD1(0x03E90) 　　bp7 :LCDEN = 0	(1) Set "0" to the LCDEN flag of the LCD mode control 　　register (LCDMD1) to stop the LCD operation.
(2) Setup the display duty 　　LCDMD1(0x03E90) 　　bp5-4 :LCDTY1-0= 10	(2) Set the LCDTY1 to LDCTY0 flags of the LCD mode 　　control register (LCDMD1) to "10" to drive 1/2 duty.
(3) Select the LCD clock source 　　LCDMD1(0x03E90) 　　bp3-0 :LCDCK3-0 = 0100	(3) Select $fpll/2^{15}$ as a LCD clock source with LCDCK3 to 　　LCDCK0 flags of the LCD mode control register 　　(LCDMD1).
(4) Select the segment output/port pin 　　Select the common output/port pin 　　LCCTR0(0x03E93) 　　bp5-4 : COMSL1-0 = 11 　　LCCTR1(0x03E94) 　　bp7-0 : LC1SL7-0 = 11111111	(4) Select the SEG7 to SEG0 and COM1 to COM0 with the 　　LCD output control register (LCCTR1).
(5) Setup the LCD panel display data 　　Segment output latch SEG1-0 　　(0x03E70) = 0x31 　　Segment output latch SEG3-2 　　(0x03E71) = 0x22 　　Segment output latch SEG5-4 　　(0x03E72) = 0x30 　　Segment output latch SEG7-6 　　(0x03E73) = 0x32	(5) Display "23" on the display panel with the address 　　0x03E70 to 0x03E73 of the segment output latch SEG7 　　to SEG0. 　　[Chapter 15 15.4.3 1/2 Duty]
(6) Start the LCD operation 　　LCDMD1(0x03E90) 　　bp7 :LCDEN = 1	(6) Set "1" to the LCDEN flag of the LCD mode control 　　register (LCDMD1) to start the LCD operation.

15.4.5 1/3 Duty

■ 1/3 Duty

MN101E29

SegmentLatch
X'3E8B' ·········

	X'3E72'	X'3E72'	X'3E71'	X'3E71'	X'3E70'	X'3E70'		
	0	0	0	0	0	0	bit7/bit3	COM3 open
	0	1	1	0	1	1	bit6/bit2	COM2
	1	1	0	0	1	1	bit5/bit1	COM1
	0	1	0	0	1	0	bit4/bit0	COM0

SEG54 ········· | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 | SEG0

A electrode

B electrode

:Light ON
:Light OFF

LCDPANEL

	LCD ON				LCD OFF
	COM=S SEG=S	COM=N SEG=S	COM=S SEG=N	COM=N SEG=N	
LCD clock					uncertain
Data	"1"		"0"		uncertain
COM V_{LC1} V_{LC2} V_{LC3} V_{SS}					
SEG V_{LC1} V_{LC2} V_{LC3} V_{SS}					
COM-SEG V_{LCD} $1/3V_{LCD}$ 0 $-1/3V_{LCD}$ $-V_{LCD}$					
	Light ON	Light OFF	Light OFF	Light OFF	Light OFF

S:selected voltage N:non-selected voltage
V_{LCD}:LCD driver voltage

Figure:15.4.3 LCD Display (1/3 duty)

15.4.6　Setup Example (1/3 Duty)

■　Setup example of the LCD (1/3 duty)

An example of setup procedure to display "23" with both segment signals (SEG0 to SEG7) and common signals (COM0 to COM2), using an external divider resistor is shown below.
[Chapter 15 15.4.5 1/3 Duty]

Clock source fpll = 4 MHz, a LCD clock source fpll/2^{15} = 122 Hz, and flame cycle = 41 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCDMD1(0x03E90) bp7 :LCDEN = 0	(1) Set "0" to the LCDEN flag of the LCD mode control register (LCDMD1) to stop the LCD operation.
(2) Setup the display duty LCDMD1(0x03E90) bp5-4 :LCDTY1-0= 01	(2) Set the LCDTY1 to LCDTY0 flags of the LCD mode control register (LCDMD1) to "01" to drive 1/3 duty.
(3) Select the LCD clock source LCDMD1(0x03E90) bp3-0 :LCDCK3-0 = 0100	(3) Select fpll/2^{15} as a LCD clock source with LCDCK3 to0 LCDCK0 flags of the LCD mode control register (LCDMD1).
(4) Select the segment output/port pin Select the common output/port pin LCCTR0(0x03E93) bp2-0 :COMSL2-0 = 111 bp6-4 :LC1SL2-0 = 111	(4) Select the SEG5 to SEG0 and COM2 to COM0 with the LCD output control register (LCCTR1).
(5) Setup the LCD panel display data Segment output latch SEG1-0 (0x03E70) = 0x76 Segment output latch SEG3-2 (0x03E71) = 0x40 Segment output latch SEG5-4 (0x03E72) = 0x27	(5) Display "23" on the display panel with the address 0x03E70 to 0x03E72 of the segment output latch SEG7 to SEG0. [Chapter 15 15.4.5 1/3 Duty]
(6) Start the LCD operation LCDMD1(0x03E90) bp7 :LCDEN = 1	(6) Set "1" to the LCDEN flag of the LCD mode control register (LCDMD1) to start the LCD operation.

15.4.7　1/4 duty

■　1/4 duty

MN101E29

SegmentLatch X'3E8B' ·········	X'3E71'	X'3E71'	X'3E70'	X'3E70'		
	0	1	0	1	bit7/bit3	COM3
	1	1	1	1	bit6/bit2	COM2
	1	0	0	1	bit5/bit1	COM1
	1	0	1	0	bit4/bit0	COM0

SEG54 ·········　SEG3　SEG2　SEG1　SEG0

A electrode

B electrode

■ :Light ON
□ :Light OFF

LCDPANEL

	LCD ON				LCD OFF
	COM=S SEG=S	COM=N SEG=S	COM=S SEG=N	COM=N SEG=N	
LCD clock					uncertain
Data	"1"		"0"		uncertain
COM	V_{LC1} V_{LC2} V_{LC3} V_{SS}				
SEG	V_{LC1} V_{LC2} V_{LC3} V_{SS}				
COM-SEG	V_{LCD} $1/3V_{LCD}$ 0 $-1/3V_{LCD}$ $-V_{LCD}$				
	Light ON	Light OFF	Light OFF	Light OFF	Light OFF

S:selected voltage N:non-selected voltage
V_{LCD}:LCD driver voltage

Figure:15.4.4 LCD Display (1/4 Duty)

15.4.8　Setup Example (1/4 duty)

■　Setup example of the LCD (1/4 duty)

An example of setup procedure to display 8-shaped 2figures "23" with both segment signals (SEG0 to SEG4)and common signals (COM0 to COM3) in 1/4 duty, 1/3 bias, using an external divider resistor is shown below.

[Chapter 15 15.4.7 1/4 duty]

Clock source fpll = 4 MHz, LCD clock source $fpll/2^{15}$ = 122 Hz, and flame cycle = 31 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation 　　LCDMD1(0x03E90) 　　bp7 :LCDEN = 0	(1) Set "0" the LCDEN flag of the LCD mode control register (LCDMD1) to stop the LCD operation.
(2) Setup the display duty 　　LCDMD1(0x03E90) 　　bp5-4 :LCDTY1-0= 00	(2) Set the LCDTY1 to LCDTY0 of the LCD mode control register (LCDMD1) to "00" to drive 1/4 duty.
(3) Select the LCD clock source 　　LCDMD1(0x03E90) 　　bp3-0 :LCDCK3-0 = 0100	(3) Select $fpll/2^{15}$ as the LCD clock source with LCDKC3 to LCDCK0 flags of the LCD mode control register (LCDMD1).
(4) Select the segment output/port pin 　　Select the common output/port pin 　　LCCTR0(0x03E93) 　　bp7-4 :COMSL3-0 = 1111 　　LCCTR1(0x03E94) 　　bp3-0 :LC1SL3-0 = 1111	(4) Select SEG0 to SEG3 and COM0 to COM3 with the output control register0 (LCCTR0) and the output control register1 (LCCTR1) .
(5) Setup the LCD panel display data 　　Segment output latch SEG1-0 　　(0x03E70) = 0x5E 　　Segment output latch SEG3-2 　　(0x03E71) = 0x7C	(5) Display "23" on the display panel with the address 0x03E70 to 0x03E71 of the segment output latch SEG0 to SEG7. 　　[Chapter 15 15.4.7 1/4 duty]
(6) Start the LCD operation 　　LCDMD1(0x03E90) 　　bp7:LCDEN = 1	(6) Set "1" to the LCDEN flag of the LCD mode control register (LCDMD1) to start the LCD operation.

Chapter 16 Automatic Transfer Controller

16

16.1 Automatic Transfer Controller

16.1.1 Overview

This LSI contains an automatic transfer controller (ATC) that uses 2 direct memory accesses (DMA) to transfer the contents of the whole memory space (1 MB) using the hardware. This ATC block is called ATC0 or ATC1.

ATCn is activated by an interrupt or a flag set by the software. Once this occurs, even if it is in the middle of executing an instruction, the microcontroller waits for a time when it can release the bus, stops normal operation, and transfers bus control to ATCn. ATCn then uses the released bus for the hardware data transfer.

The software sets the activation factor in ATCn control register 1 (ATnCNT1), then data transfer begins when the ATnACT flag in ATCn control register 0 (ATnCNT0) is set to "1". ATnACT flag is automatically cleared to "0" when ATCn is activated.

The transfer data counter (ATnTRC) determines the number of transfers that ATCn makes, up to a maximum of 255 times. There are also 16 transfer modes, set in ATCn control register 0 (ATnCNT0).

The interrupt enable flag (xxxIE) for interrupt as a trigger factor needs not to be set. This is because the automatic data transfer occurs in the hardware without going through an interrupt service routine. If the interrupt enable flag (xxxIE) is set for the type of interrupt ATCn, hardware handling of a regular interrupt is generated after the automatic transfer ends.

"n" in [Chapter 16 Automatic Transfer Controller] means serial number 0 to 1.

The order of an interrupt acceptace may be changed by software when setting each interrupt is set as a trigger factor of ATC1, a trigger factor interrupt and an interrupt level of ATC1 interrupt (ATC1IRQ) are in same level.
To prevent this, set each interrupt level differently.

ATC1 can't be used in standby mode (HALT mode and STOP mode).
ATC1 starts the data transfer after recovering CPU operation mode when ATC1 actication factor is generated in standby mode

16.1.2   Functions

Table:16.1.1 provides a list of the ATCn trigger factors and transfer modes.

■   ATCn Trigger Factors

Table:16.1.1 ATCn Trigger Factors

Trigger Factors	External interrupt 0
	External interrupt 1
	External interrupt 2
	External interrupt 3
	Timer 0 interrupt
	Timer 1 interrupt
	Timer 2 interrupt
	Timer 3 interrupt
	Timer 7 interrupt
	Timer 7 capture trigger
	Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt *1
	Serial 1 transmission buffer empty, Serial 1 transmission complete interrupt *1
	Serial 2 transmission buffer empty, Serial 2 transmission complete interrupt *1
	Serial 3 transmission buffer empty, Serial 3 transmission complete interrupt *1
	Serial 4 transmission complete interrupt, A/D converter interrupt *1
	Software startup

*1   Only ATC1 can select Serial 0 to 4 transmission complete interrupt.

■ Transfer Modes

Table:16.1.2 Transfer Modes

Transfer Mode	Transfer Direction (*)			Pointer Increment Control		Transfer Operation
	cycle	Source Address	→	Destination Address		
				ATnMAP0	ATnMAP1	
Transfer mode 0		ATnMAP0	→	ATnMAP1 (I/O area)	-	-	1-byte data transfer
Transfer mode 1		ATnMAP1 (I/O area)	→	ATnMAP0	-	-	1-byte data transfer
Transfer mode 2		ATnMAP0	→	ATnMAP1 (I/O area)	ATnMAP0+1	-	1-byte data transfer
Transfer mode 3		ATnMAP1 (I/O area)	→	ATnMAP0	ATnMAP0+1	-	1-byte data transfer
Transfer mode 4	1st 2nd	ATnMAP0 ATnMAP0 [=ATnMAP0+1]	→ →	ATnMAP1 ((I/O area : even ADR) ATnMAP1 (I/O area : odd ADR)	ATnMAP0+1 ATnMAP0+1	- -	1-word data transfer (An even address must be set in ATnMAP1)
Transfer mode 5	1st 2nd	ATnMAP1 (I/O area : even ADR) ATnMAP1 (I/O area : odd ADR)	→ →	ATnMAP0 ATnMAP0 [=ATnMAP0+1]	ATnMAP0+1 ATnMAP0+1	- -	1-word data transfer (An even address must be set in ATnMAP1)
Transfer mode 6	1st 2nd	ATnMAP0 ATnMAP0 [=ATnMAP0+1]	→ →	ATnMAP1 (I/O area) ATnMAP1 (I/O area)	ATnMAP0+1 ATnMAP0+1	- -	Two 1-byte data transfers
Transfer mode 7	1st 2nd	ATnMAP1 (I/O area) ATnMAP0 [=ATnMAP0+1]	→ →	ATnMAP0 ATnMAP1 (I/O area)	ATnMAP0+1 -	- -	Two 1-byte data transfers
Transfer mode 8	1st 2nd	ATnMAP1 (I/O area : even ADR) ATnMAP0 [=ATnMAP0+1]	→ →	ATnMAP0 ATnMAP0 (I/O area : odd ADR)	ATnMAP0+1 ATnMAP0+1	- -	Two 1-byte data transfers (An even address must be set in ATnMAP1)
Transfer mode 9	1st 2nd	ATnMAP1 (I/O area : even ADR) ATnMAP0 [=ATnMAP0+1]	→ →	ATnMAP0 ATnMAP1 (I/O area : odd ADR)	ATnMAP0+1 -	- -	Two 1-byte data transfers (An even address must be set in ATnMAP1)
Transfer mode A		ATnMAP0	→	ATnMAP1	-	-	1-byte data transfer (whole memory area)
Transfer mode B		ATnMAP1	→	ATnMAP0	-	-	1-byte data transfer (whole memory area)
Transfer mode C		ATnMAP0	→	ATnMAP1	ATnMAP0+1	ATnMAP1+1	1-byte data transfer (whole memory area)
Transfer mode D		ATnMAP1	→	ATnMAP0	ATnMAP0+1	ATnMAP1+1	1-byte data transfer (whole memory area)
Transfer mode E		ATnMAP0	→	ATnMAP1	ATnMAP0+1	ATnMAP1+1	Burst transfer (continues until ATnTCR=0)
Transfer mode F		ATnMAP1	→	ATnMAP0	ATnMAP0+1	ATnMAP1+1	Burst transfer (continues until ATnTCR=0)

(*) When a memory pointer points to the I/O space, only the lower 8 bits of the pointer are valid.

Change the ATC1 activation factor and the transfer mode while ATC1 transfer is disabled (AT1EN flag of the AT1CNT register is "0").

16.1.3   Block Diagram
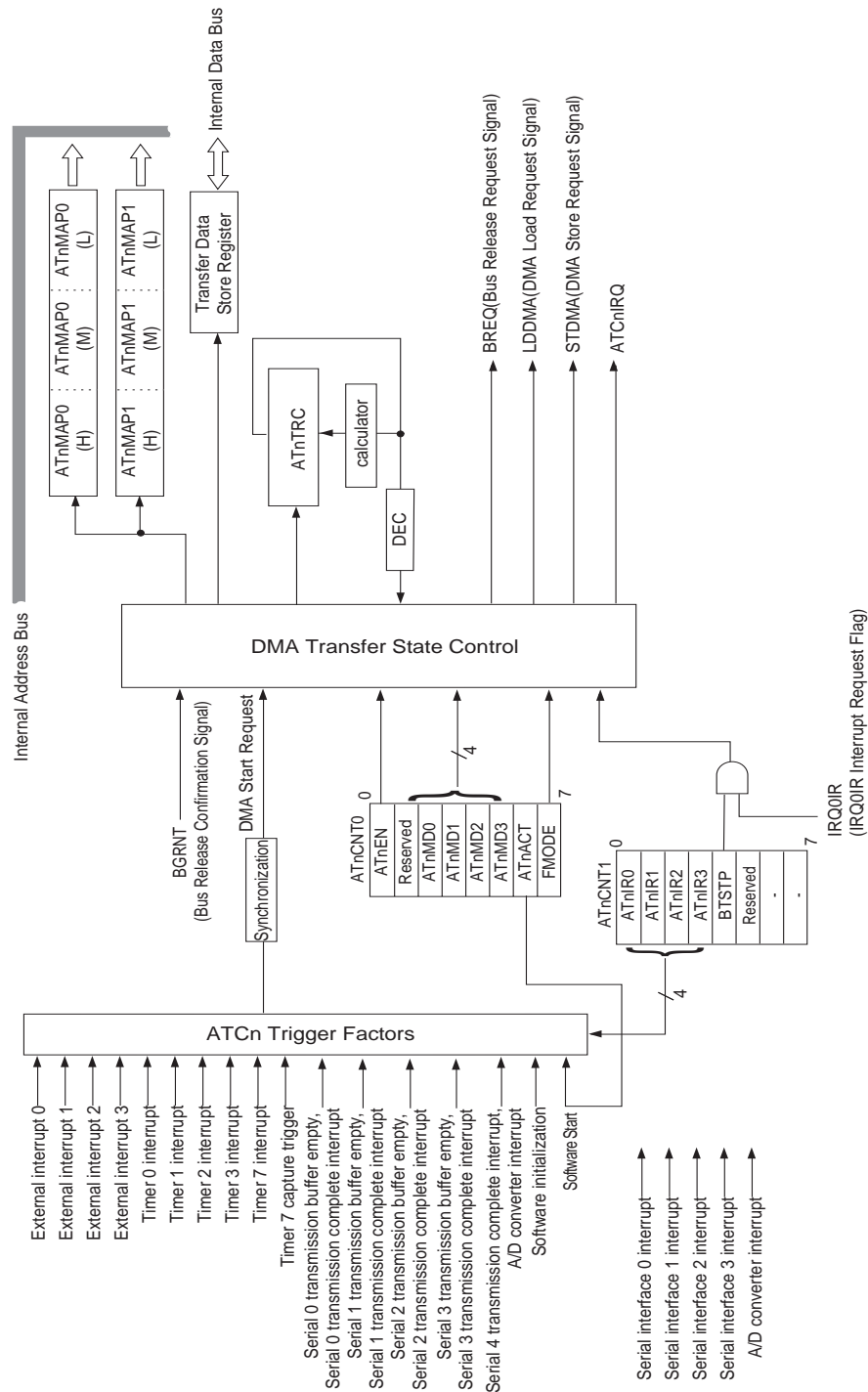
Figure:16.1.1 ATCn Block Diagram

16.2 Control Registers

16.2.1 Registers

Table:16.2.1 shows the registers used to control ATCn.

Table:16.2.1 ATC0 Control Registers

	Register	Address	R/W	Function	Page
ATC0	AT0CNT0	0X03EC0	R/W	ATC0 control register 0	XVII-7
	AT0CNT1	0X03EC1	R/W	ATC0 control register 1	XVII-9
	AT0TRC	0X03EC2	R/W	ATC0 transfer data counter	XVII-10
	AT0MAPOL	0X03EC3	R/W	ATC0 memory pointer 0 (lower 8 bits)	XVII-11
	AT0MAPOM	0X03EC4	R/W	ATC0 memory pointer 0 (middle 8 bits)	XVII-11
	AT0MAPOH	0X03EC5	R/W	ATC0 memory pointer 0 (upper 4 bits)	XVII-11
	AT0MAP1L	0X03EC6	R/W	ATC0 memory pointer 1 (lower 8 bits)	XVII-12
	AT0MAP1M	0X03EC7	R/W	ATC0 memory pointer 1 (middle 8 bits)	XVII-12
	AT0MAP1H	0X03EC8	R/W	ATC0 memory pointer 1 (upper 4 bits)	XVII-12

R/W : Readable / Writable

Table:16.2.2 ATC1 Control Registers

	Register	Address	R/W	Function	Page
ATC1	AT1CNT0	0X03ED0	R/W	ATC1 control register 0	XVII-7
	AT1CNT1	0X03ED1	R/W	ATC1 control register 1	XVII-9
	AT1TRC	0X03ED2	R/W	ATC1 transfer data counter	XVII-10
	AT1MAPOL	0X03ED3	R/W	ATC1 memory pointer 0 (lower 8 bits)	XVII-11
	AT1MAPOM	0X03ED4	R/W	ATC1 memory pointer 0 (middle 8 bits)	XVII-11
	AT1MAPOH	0X03ED5	R/W	ATC1 memory pointer 0 (upper 4 bits)	XVII-11
	AT1MAP1L	0X03ED6	R/W	ATC1 memory pointer 1 (lower 8 bits)	XVII-12
	AT1MAP1M	0X03ED7	R/W	ATC1 memory pointer 1 (middle 8 bits)	XVII-12
	AT1MAP1H	0X03ED8	R/W	ATC1 memory pointer 1 (upper 4 bits)	XVII-12

R/W : Readable / Writable

■ ATCn Control Register 0 (AT0CNT0:0x03EC0, AT1CNT0:0x03ED0)

bp	7	6	5	4	3	2	1	0
Flag	FMODE	ATnACT	ATnMD3	ATnMD2	ATnMD1	ATnMD0	Reserved	ATnEN
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	FMODE	Increment control flag for memory pointer 0 0: Increment depending on transfer mode 1: Disable incrementing of memory pointer 0
6	ATnACT	ATCn software activation flag 0: Do not activate ATCn 1: Activate ATCn
5-2	ATnMD3-0	ATCn data transfer mode 0000 : Transfer mode 0 0001 : Transfer mode 1 0010 : Transfer mode 2 0011 : Transfer mode 3 0100 : Transfer mode 4 0101 : Transfer mode 5 0110 : Transfer mode 6 0111 : Transfer mode 7 1000 : Transfer mode 8 1001 : Transfer mode 9 1010 : Transfer mode A 1011 : Transfer mode B 1100 : Transfer mode C 1101 : Transfer mode D 1110 : Transfer mode E 1111 : Transfer mode F
1	Reserved	Always set to "0". *
0	ATnEN	ATCn transfer enable flag 0: ATCn transfer disable 1: ATCn transfer enable

AT1ACT flag of the ATC1 control register0 (AT1CNT0) is cleared by hardware automatically when the transfer completes.

Always set "0" to the bp denoted by asterisk.

■ ATC0 Control Register 1(AT0CNT1:0x03EC1)

bp	7	6	5	4	3	2	1	0
Flag	-	-	Reserved	BTSTP	AT0IR3	AT0IR2	AT0IR1	AT0IR0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	-	-
5	Reserved	Always set to "0". *
4	BTSTP	Burst transfer stop enable 0: Burst transfer stop disable 1: Burst transfer stop enable (Transfer stops when external interrupt 0 occurs.)
3-0	AT0IR3-0	ATCn trigger factor settings 0000:External interrupt 0 0001:External interrupt 1 0010:External interrupt 2 0011:External interrupt 3 0100:Timer 0 interrupt 0101:Timer 1 interrupt 0110:Timer 2 interrupt 0111:Timer 3 interrupt 1000:Timer 7 interrupt 1001:Timer 7 capture trigger 1010:Serial interface 0 interrupt 1011:Serial interface 1 interrupt 1100:Serial interface 2 interrupt 1101:Serial interface 3 interrupt 1110:A/D converter interrupt 1111:Software initialization

When burst transfer stop is enabled, do not select external interrupt 0 for ATC0 trigger factor.

Always set "0" to the bp denoted by asterisk.

Bp5 of the ATC1 control register1 (AT1CNT1) may be set by hardware automatically.
If automatic setting is operated by hardware, the data automatic transfer function operates normally.

■ ATC1 Control Register 1(AT1CNT1:0x03ED1)

bp	7	6	5	4	3	2	1	0
Flag	AT1IRS	-	Reserved	BTSTP	AT1IR3	AT1IR2	AT1IR1	AT1IR0
At reset	0	-	0	0	0	0	0	0
Access	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	AT1IRS	Trigger factor selection flag 0: Serial 0 to 3 transfer buffer empty, A/D interrupt 1: Serial 0 to 4 transfer interrupt
6	-	-
5	Reserved	Always set to "0". *
4	BTSTP	Burst transfer stop enable 0: Burst transfer stop disable 1: Burst transfer stop enable (Transfer stops when external interrupt 0 occurs.)
3-0	AT1IR3-0	ATC1 trigger factor settings 　　　　　(AT1IRS=0)　　　　　　　　　　(AT1IRS=1) 0000:　External interrupt 0　　　　0000: External interrupt 0 0001:　External interrupt 1　　　　0001: External interrupt 1 0010:　External interrupt 2　　　　0010: External interrupt 2 0011:　External interrupt 3　　　　0011: External interrupt 3 0100:　Timer 0 interrupt　　　　　0100: Timer 0 interrupt 0101:　Timer 1 interrupt　　　　　0101: Timer 0 interrupt 0110:　Timer 2 interrupt　　　　　0110: Timer 0 interrupt 0111:　Timer 3 interrupt　　　　　0111: Timer 0 interrupt 1000:　Timer 7 interrupt　　　　　1000: Timer 0 interrupt 1001:　Timer 7 capture trigger　　1001: Timer 7 capture trigger 1010:　Serial 0 transmission buffer empty　1010: Serial interface 0 interrupt 1011:　Serial 1 transmission buffer empty　1011: Serial interface 1 interrupt 1100:　Serial 2 transmission buffer empty　1100: Serial interface 2 interrupt 1101:　Serial 3 transmission buffer empty　1101: Serial interface 3 interrupt 1110:　A/D converter interrupt　　1110: Serial interface 4 interrupt 1111:　Software initialization　　　1111: Software initialization

When burst transfer stop is enabled, do not select external interrupt 0 for ATC1 trigger factor.

Always set "0" to the bp denoted by asterisk.

■ ATCn Transfer Counter (AT0TRC:0x03EC2, AT1TRC:0x03ED2)

bp	7	6	5	4	3	2	1	0
Flag	ATnTRC7	ATnTRC6	ATnTRC5	ATnTRC4	ATnTRC3	ATnTRC2	ATnTRC1	ATnTRC0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-0	ATnTRC7-0	ATCn Transfer Data Count Setting · For transfer modes 0 to D, set this register to the number of ATC activations. · For transfer modes E and F, set this register to number of burst transfers.

■ ATCn Memory Pointer 0 : Lower 8 bits (AT0MAP0L:0x03EC3, AT1MAP0L:0x03ED3)

bp	7	6	5	4	3	2	1	0
Flag	ATnMAP0L7	ATnMAP0L6	ATnMAP0L5	ATnMAP0L4	ATnMAP0L3	ATnMAP0L2	ATnMAP0L1	ATnMAP0L0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATCn Memory Pointer 0 : Middle 8 bits (AT0MAP0M:0x03EC4, AT1MAP0M:0x03ED4)

bp	7	6	5	4	3	2	1	0
Flag	ATnMAP0M7	ATnMAP0M6	ATnMAP0M5	ATnMAP0M4	ATnMAP0M3	ATnMAP0M2	ATnMAP0M1	ATnMAP0M0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATCn Memory Pointer 0 : Upper 4 bits (AT0MAP0H:0x03EC5, AT1MAP0H:0x03ED5)

bp	7	6	5	4	3	2	1	0
Flag	-	-		-	ATnMAP0H3	ATnMAP0H2	ATnMAP0H1	ATnMAP0H0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

■ ATCn Memory Pointer 1 : Lower 8 bits (AT0MAP1L:0x03EC6, AT1MAP1L:0x03ED6)

bp	7	6	5	4	3	2	1	0
Flag	ATnMAP1L7	ATnMAP1L6	ATnMAP1L5	ATnMAP1L4	ATnMAP1L3	ATnMAP1L2	ATnMAP1L1	ATnMAP1L0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATCn Memory Pointer 1 : Middle 8 bits (AT0MAP1M:0x03EC7, AT1MAP1M:0x03ED7)

bp	7	6	5	4	3	2	1	0
Flag	ATnMAP1M7	ATnMAP1M6	ATnMAP1M5	ATnMAP1M4	ATnMAP1M3	ATnMAP1M2	ATnMAP1M1	ATnMAP1M0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATCn Memory Pointer 1 : Upper 4 bits (AT0MAP1H:0x03EC8, AT1MAP1H:0x03ED8)

bp	7	6	5	4	3	2	1	0
Flag	-	-		-	ATnMAP1H3	ATnMAP1H2	ATnMAP1H1	ATnMAP1H0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

16.3 Operation

16.3.1   Basic Operations and Timing

ATCn is a DMA block that enables the hardware to transfer the whole memory space (1 MB). This section provides a description of and timing for the basic ATCn operations.
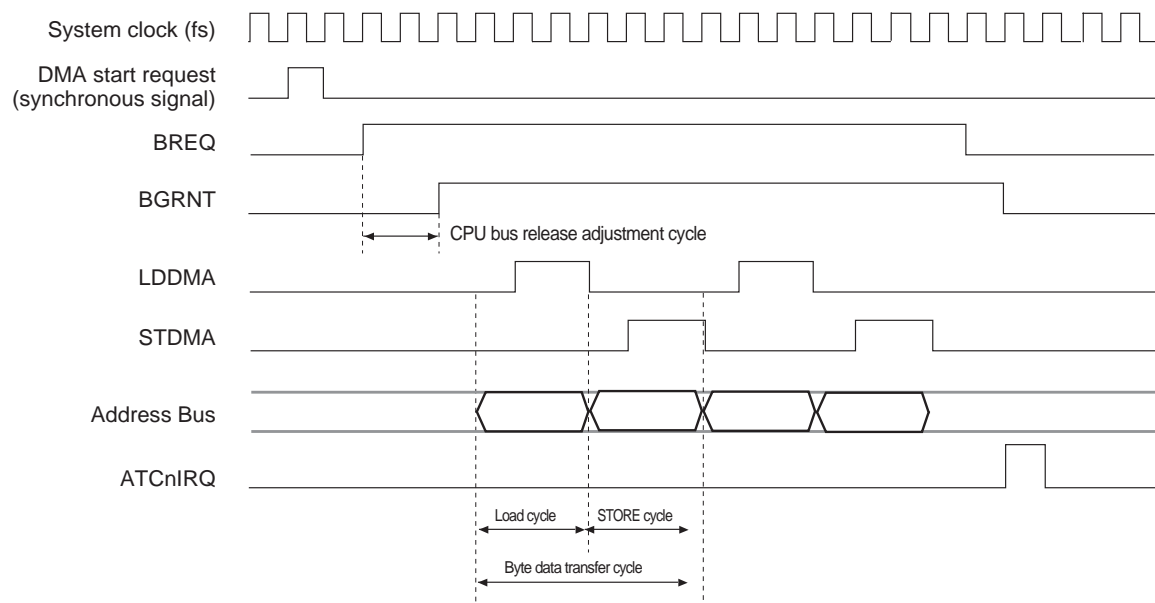
Figure:16.3.1 ATCn Timing Chart

■ ATCn activation and internal bus acquisition

ATCn activates either when the selected interrupt factor occurs or when the software sets the activation flag. Set the ATCn trigger factor in ATCn control register 1 (ATnCNT1). When ATCn starts, the ATCn controller asserts the BREQ signal, which requests the MCU core to release the bus. When the core receives the BREQ signal, it stops all normal executions, even if it is in the middle of executing an instruction, and releases the bus at the next available timing. The core takes a minimum of two cycles from the time it receives the BREQ signal until it actually releases the bus. After it releases the internal bus, the core returns the bus granted signal, BGRNT, to ATCn. ATCn can then begin using the bus to transfer data.

DMA activation request occurs at ATC0 and ATC1, ATC0 gets priority over ATC1.

When an external interrupt is selected as an ATCn trigger factor, specify the activation valid edge by the REDGn flag of the external interrupt control register and the EDGSELn flag of the both edges interrupt control register (EDGDT). [Chapter 3 3.3. External interrupts]

The pulse input which is shorter than the system clock cycle may sometimes be ignored as the external interrupt input is sampled by the system clock.

Set the valid edge for external interrupts before ATCn activates.

When the software activation is selected as an activation factor of ATC1, maximum four instructions are needed from setting of the software activation flag (AT1ACT) until ATC1 transfer activation. And maximum three instructions are needed until ATC1 transfer complete interrupt (ATC1IRQ) generation.

■ Data transfer

The basic ATCn operation cycle is the "byte-data transfer cycle", in which ATCn transfers a single byte of data. This operation consists of two instruction cycles, a load and a store cycle. In the load cycle, ATCn reads the data from the source address of the source memory, and in the store cycle, ATCn stores the read data to the destination address of the destination memory. ATCn transfers word-length data or a multi-byte stream of data by repeating the byte-data transfer cycle as many times as necessary.

■ Transfer end

Once it has transferred all the data, ATCn generates an interrupt (ATCnIRQ) and stop the automatic transfer. In this way, the ATCn block bypasses the software and automatically transfers data in a continuous DMA operation.

In both the load and store cycles, the read and write access occurs to the memory exactly as it does in a normal instruction execution. This means that the access timing is different depending on the memory space. Also, the wait settings for I/O and external memory spaces apply. The following is the access timing for each memory space, assuming no-wait situation.

• Internal ROM/RAM space   2 cycles
• I/O space (special registers) 3 cycles
LOAD cycle and STORE cycle are set as follows.
An access timing corresponding to each memory space + 1 cycle

In Figure:16.3.1 ATCn Timing Chart, the time, from the rising of DMA activation request signal to the starting of LOAD cycle depends on the state of CPU, but it takes minimum of nine cycles.

16.3.2   Memory Address Setting

■   Setting of transfer addresses to the memory pointers

The address of the memory space for an automatic data transfer (ATCn) should be set in the both of memory pointer 0 (ATnMAP0) and memory pointer 1 (ATnMAP1). In each transfer mode, one of those pointer is the source address, and another is the destination address.

■   Memory pointer 0 functions

Memory pointer 0 is consists of three 8-bit registers, ATnMAP0H, ATnMAP0M, and ATnMAP0L. ATnMAP0H holds upper 4bits of the 20-bit address, ATnMAP0M contains the middle 8 bits, and ATnMAP0L contains lower 8 bits. The 20-bit address set in memory pointer 0 points to a specific address in the total memory space of 1 MB. Memory pointer 0 also contains a computational function that enables it to increment the address based on the transfer state. You can disable this function for all transfer modes by setting the FMODE bit of ATCn control register 0 to "1".

■   Memory pointer 1 functions

Memory pointer 1 is consists of three 8-bit registers, ATnMAP1H, ATnMAP1M, and ATnMAP1L. ATnMAP1H holds upper 4 bits of the 20-bit address, ATnMAP1M contains the middle 8 bits, and ATnMAP1L contains lower 8 bits. Depending on the transfer mode, either all 20 bits are valid, or only the least significant 8 bits (in ATnMAP1L) are valid. When only the 8 bits in ATnMAP1L are valid, the value 0x03F is assigned to the 12 bits in ATnMAP1H and ATnMAP1M, and the pointer points to the I/O space (special registers). Memory pointer 1 also contains a computational function that enables it to increment the address based on the transfer state.

Set the memory address while ATCn transfer is disabled (ATnEN flag of the ATnCNT0 register is "0").

16.3.3　Data Transfer Count Setting

■　Transfer data counter (ATnTRC) function

You can preset the data transfer count by ATCn. Set the value in the ATCn transfer counter (ATnTRC). The counter decrements everytime when ATCn transfers one byte of data.

The value in the transfer data counter is 0x00 at reset. Set the data transfer counts before activating ATCn. Note that ATCn cannot be activated if the transfer data counter is set to 0x00.

■　Data transfer operations using the transfer data counter (ATnTRC)

There are two main types of ATCn data transfers, standard and burst transfers. (See section 16.3.4 "Data Transfer Modes Setting"). The transfer counter operates differently depending on the transfer type.

1. Standard transfers [transfer modes 0 to D]

In standard transfers, the transfer counter decrements everytime when ATCn is activated. When the counter reaches 0x00 after a data transfer, ATCn generates an interrupt (ATCnIRQ). This means that for standard transfers, the program must set the counter to the number of times ATCn needs to be activated.

2. Burst transfers [transfer modes E to F]

In burst transfers, one activation of ATCn continuously transfers multiple bytes of data. In this case, the program must set the counter to the number of data bytes contained in the burst transfer. When the burst transfer starts, the transfer counter decrements everytime when one byte of data is transferred. When the counter reaches 0x00, ATCn generates an interrupt (ATCnIRQ). It is also possible to force ATCn to shut down during the burst transfer using the external interrupt 0 by setting the BTSTP flag of the ATCn control register1 (ATnCNT1) to "1". (See section 16.3.4 "Data Transfer Modes Setting").

■　The transfer data counter (ATnTRC)

The transfer data counter can be set to a maximum 255 transfers (for standard transfers) or 255 bytes (for burst transfers). Note that setting the counter to 0x00 disables transfers.

> Set the number of data transfer while ATCn transfer is disabled (ATnEN flag of the ATnCNT0 register is "0").

16.3.4   Data Transfer Modes Setting

■   Data transfer modes

There are two types of ATCn transfers, standard and burst, and sixteen transfer modes. Set the transfer mode in ATCn control register 0 (ATnCNT0). [Table:16.1.2 Transfer Modes]

■   Standard and burst transfers

The ATCn transfer modes are divided into standard transfer modes and burst transfer modes. There are fourteen standard modes, 0 to D, and two burst modes, E and F.

In standard modes, the operation specified for that mode executes everytime when ATCn is activated. When the transfer ends, the value set in the transfer counter (ATnTRC) decrements and bus control returns to the MCU core. This operation repeats until the transfer counter reaches 0x00. When this happens, ATCn completes the final data transfer, then generates an interrupt (ATCnIRQ).

For instance, if the initial transfer counter value is 0x05, and the ATCn activation factor is set to a timer 0 interrupt, ATCn is activated everytime when interrupt request of timer 0 interrupt generates and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 interrupt request generation) is completed, the transfer counter value becomes 0x00, an ATCn interrupt occurs, and the operation ends. Timer 0 overflows occurring after this point do not activate ATCn. For standard transfers, the program must set the transfer counter to the number of ATCn activations required.

In burst modes, once ATCn is activated, it transfers in one operation the number of bytes set in the transfer counter (ATnTRC). After the burst transfer begins, the transfer counter decrements everytime when ATCn transfers one byte of data. When the counter reaches 0x00, ATCn generates an interrupt (ATCnIRQ) and the burst transfer ends. For burst transfers, the program must set the transfer counter to the number of data bytes in the burst transfer.

The external interrupt 0 can also be used to shut down ATCn during a burst transfer. To enable this function, set the burst transfer stop enable bit (BTSTP) in ATCn control register 1 (ATnCNT1) to 1. When BTSTP = 1, ATCn data transfers stop when the external interrupt 0 interrupt request flag (IRQ0IR flag in the IRQ0ICR register) is set. In an emergency shutdown, the transfer counter and memory pointer save the values prior to the shutdown. When the interrupt service routine ends, a new activation factor restarts ATCn, and the burst transfer begins transferring data from the point at which it stopped.

> When burst transfer stop is enabled, do not select external interrupt 0 for ATCn trigger factor.

> Set the data transfer mode while ATCn transfer is disabled (ATnEN flag of the ATnCNT0 register is "0").

16.3.5   Transfer Mode 0

In transfer mode 0, ATCn automatically transfers one byte of data from any memory space to the I/O space (special registers : 0x03F00 - 0x03FFF) everytime an ATCn activation request occurs.

```
Memory pointer 0              Memory pointer 1
 00000 to FFFFF                03F00 to 03FFF
┌──────────────┐             ┌──────────────┐
│              │        ┌───►│   ATMAP1     │
├──────────────┤        │    └──────────────┘
│    ATMAP0    │────────┘
├──────────────┤            [Only lower 8 bits are valid]
│  ATMAP0 + 1  │
├──────────────┤
│  ATMAP0 + 2  │
├──────────────┤
│  ATMAP0 + 3  │
├──────────────┤
│              │
├──────────────┤
│              │
└──────────────┘
```
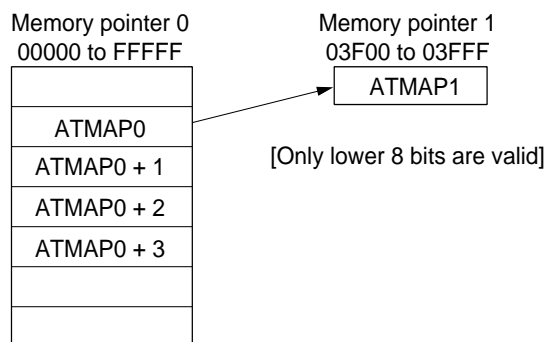
Figure:16.3.2 Transfer Mode 0

Set the source address in 20-bit memory pointer 0 (ATnMAP0H, M, L), and set the destination I/O address in lower 8 bits of memory pointer 1(ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H and ATnMAP1M.

Transfer mode 0 does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.6   Transfer Mode 1

In transfer mode 1, ATCn automatically transfers one byte of data from the I/O space (special registers : 0x03F00-0x03FFF) to any memory space everytime an ATCn activation request occurs.

Memory pointer 0
00000 to FFFFF

Memory pointer 1
03F00 to 03FFF

ATMAP1

ATMAP0

ATMAP0 + 1

ATMAP0 + 2

ATMAP0 + 3

[Only lower 8 bits are valid]
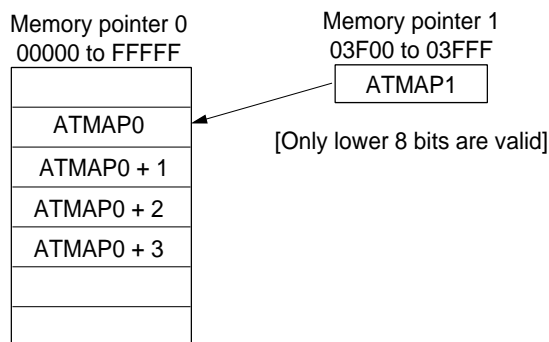
Figure:16.3.3 Transfer Mode 1

Set the source I/O address in lower 8 bits of memory pointer 1 (ATnMAP1L), and set the destination address in 20-bit memory pointer 0 (ATnMAP0H, M, L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H and ATnMAP1M.

Transfer mode 1 does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.7   Transfer Mode 2

In transfer mode 2, ATCn automatically transfers one byte of data from any memory space to the I/O space (special registers : 0x03F00 - 0x03FFF) everytime an ATCn activation request occurs.

Memory pointer 0
00000 to FFFFF

Memory pointer 1
03F00 to 03FFF

(1)

ATMAP1

[Only lower 8 bits are valid]

ATMAP0

(2)

ATMAP0 + 1

ATMAP0 + 2

ATMAP0 + 3
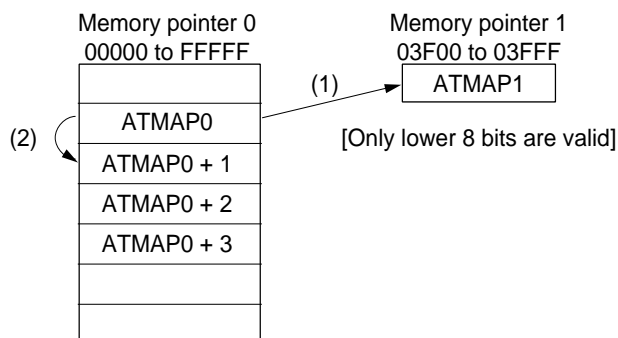
Figure:16.3.4 Transfer Mode 2

Set the source address in 20-bit memory pointer 0 (ATnMAP0H, M, L), and set the destination I/O address in lower 8 bits of memory pointer 1(ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H and ATnMAP1M.

In transfer mode 2, the value in memory pointer 0 increments everytime a byte-length data transfer ends. As a result, the source address for the next transfer is one address higher than that for the previous transfer.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.8   Transfer Mode 3

In transfer mode 3, ATCn automatically transfers one byte of data from the I/O space (special registers : 0x03F00 - 0x03FFF) to any memory space everytime an ATCn activation request occurs.
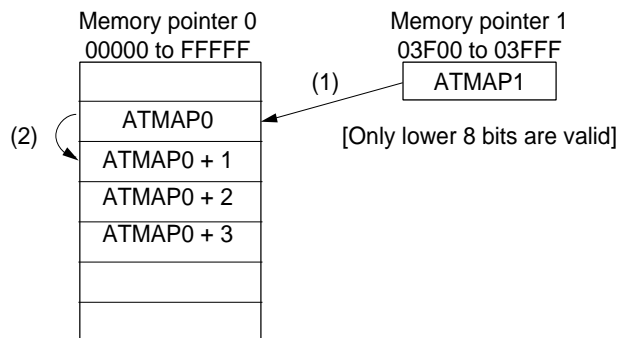
Figure:16.3.5 Transfer Mode 3

Set the source I/O address in lower 8 bits of memory pointer 1 (ATnMAP1L), and set the destination address in 20-bit memory pointer 0 (ATnMAP0H, M, L). You do not have to set the upper 12 bits of the I/O space address (0x3F) in ATnMAP1H and ATnMAP1M.

In transfer mode 3, the value in memory pointer 0 increments everytime a byte-length data transfer ends. As a result, the destination address for the next transfer is one address higher than that for the previous transfer.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.9   Transfer Mode 4

In transfer mode 4, ATCn automatically transfers two bytes (one word) of data from any memory space to the I/O space (special registers : 0x03F00 - 0x03FFF) everytime an ATCn activation request occurs.
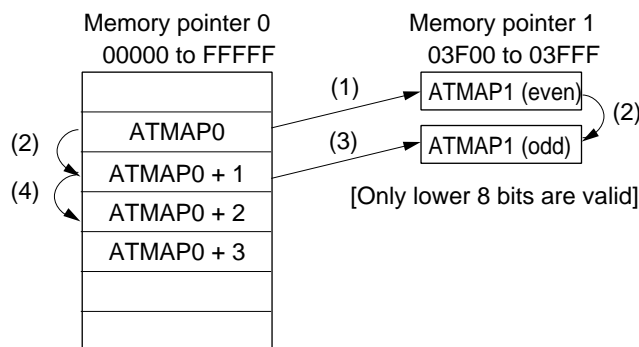
Figure:16.3.6 Transfer Mode 4

Set the source address in 20-bit memory pointer 0 (ATnMAP0H, M, L), and set the destination I/O address in the lower 8 bits of memory pointer 1(ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H and ATnMAP1M.

Always set an even address as the destination I/O address in memory pointer 1. When ATCn transfers one word to the I/O space, ATCn can transfer the even address set in memory pointer 1 and the consecutive odd address.

In transfer mode 4, ATCn executes a data byte transfer twice to send one data word everytime when activated. The value in memory pointer 0 increments everytime a byte-length data transfer ends. As a result, the source address for the next ATCn operation is two addresses higher than that for the previous operation.

In this word-length transfer, ATCn transfers the first data byte to an even address in the I/O space and the second data byte to an odd address in the I/O space.

Set the data transfer data count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime ATCn is activated (after each word transfer). When it reaches x'00', an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.10 Transfer Mode 5

In transfer mode 5, ATCn automatically transfers two bytes (one word) of data from the I/O space (special registers : 0x03F00' - 0x03FFF') to any memory space everytime an ATCn activation request occurs.
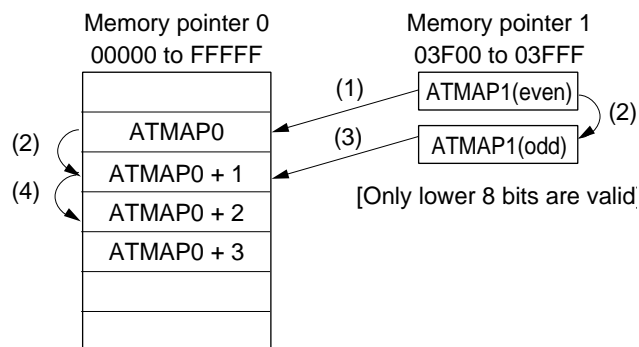
Figure:16.3.7 Transfer Mode 5

Set the source I/O address in lower 8 bits of memory pointer 1 (ATnMAP1L), and set the destination address in 20-bit memory pointer 0 (ATnMAP0H, M, L). You do not have to set the upper 12 bits of the I/O space address (0x3F) in ATnMAP1H and ATnMAP1M.

Always set an even address as the source I/O address in memory pointer 1. When ATCn transfers one word from the I/O space, ATCn can transfer the even address set in memory pointer 1 and the consecutive odd address.

In transfer mode 5, ATCn executes a data byte transfer twice to send one data word everytime when activated. The value in memory pointer 0 increments by one each time a byte-length data transfer ends. As a result, the destination address for the next ATCn operation is two addresses higher than that for the previous operation.

In this word-length transfer, ATCn transfers the first data byte from an even address in the I/O space and the second data byte from an odd address in the I/O space.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC).Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated (after each word transfer). When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.11 Transfer Mode 6

In transfer mode 6, ATCn automatically transfers one byte of data two times everytime an ATCn activation request occurs.
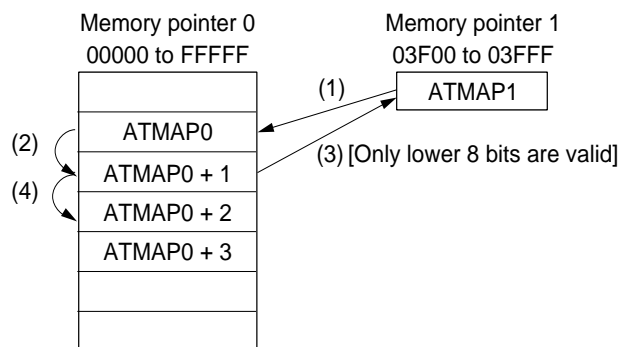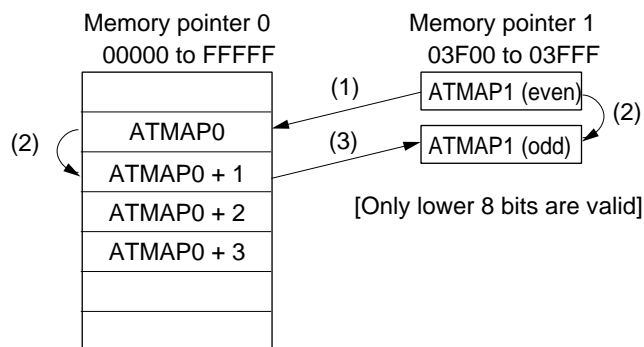

Figure:16.3.8 Transfer Mode 6

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. The adsdress in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set the I/O address in lower 8 bits of memory pointer 1 (ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H, ATnMAP1M.

In transfer mode 6, ATCn executes a data byte transfer twice everytime when activated. The value in memory pointer 0 increments by one everytime a byte-length data transfer ends. As a result, the source address for the next ATCn operation is two addresses higher than that for the previous operation.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated (after one byte of data is transferred twice). When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.12 Transfer Mode 7

In transfer mode 7, ATCn automatically transfers one byte of data two times everytime an ATCn activation request occurs.
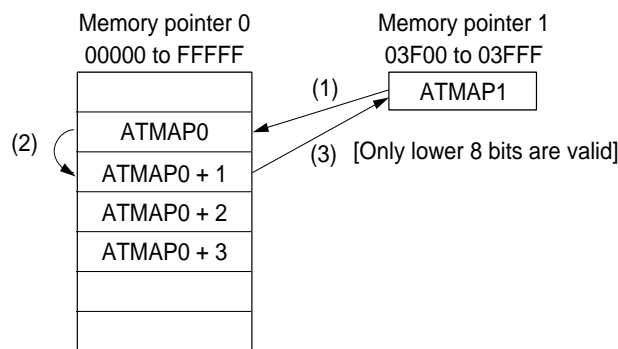
Figure:16.3.9 Transfer Mode 7

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FF') in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. The address in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set the I/O address in lower 8 bits of memory pointer 1 (ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H, ATnMAP1M.

In transfer mode 7, ATCn executes a data byte transfer twice everytime when activated. However, the value in memory pointer 0 increments by one only after the first transfer ends. As a result, the source address for the next ATCn operation is one address higher than that for the previous operation.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated (after one byte of data has been transferred twice). When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.13 Transfer Mode 8

In transfer mode 8, ATCn automatically transfers one byte of data two times everytime an ATCn activation request occurs.
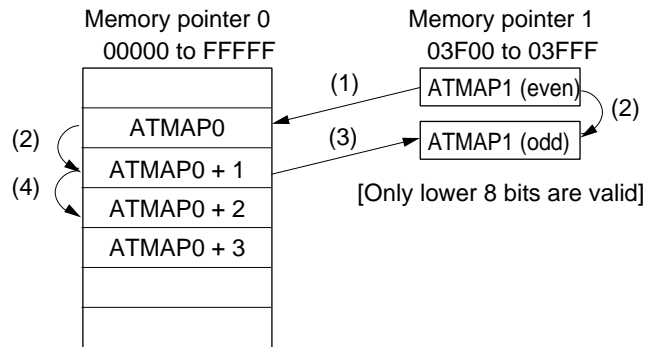
Figure:16.3.10 Transfer Mode 8

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. When the second data byte transfer ends, the address in memory pointer 0 increments again.

Set an even I/O address in the lower 8 bits of memory pointer 1 (ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H, ATnMAP1M.

Always set an even I/O address in memory pointer 1. In this double transfer of a data byte from and to the I/O space, ATCn targets the even I/O address set in memory pointer 1 and the consecutive odd address. In this mode, the first data byte transfer accesses an even I/O address and the second data byte transfer accesses an odd I/O address.

Transfer mode 8 can be used to support continuous transmission/ reception for serial interface 0,1, 2 and 3. Set the memory pointer 1 to point to the serial reception buffer (RXBUF0, RXBUF1) and select serial interrupts as the ATCn trigger factor. In this way, everytime the serial communication ends, the MCU continuously reads the reception data (first data byte transfer), then writes the transmission data to the transmission buffer (TXBUF0, TXBUF1) (second data byte transfer) up to 255 times, entirely through the hardware.

Before execute a continuous serial transaction, store the serial transmission data in the memory space that memory pointer 0 points, the transmission data must fill every other address in the space. Once the serial transaction ends, the received data is stored in empty (skipped) addresses and the transmission and reception data at stored in an alternative pattern.

In transfer mode 8, ATCn executes a data byte transfer twice each time it is activated. The value in memory pointer 0 increments by one everytime a byte-length data transfer ends. As a result, the source address for the next ATCn operation is two addresses higher than that for the previous operation.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated (after one byte of data is transferred twice). When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.14 Transfer Mode 9

In transfer mode 9, ATCn automatically transfers one byte of data two times everytime an ATCn activation request occurs.

Figure:16.3.11 Transfer Mode 9

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 is the source address, and the address in memory pointer 0 for any memory space is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. The address in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set an even I/O address in lower 8 bits of memory pointer 1 (ATnMAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in ATnMAP1H, ATnMAP1M.

Always set an even I/O address in memory pointer 1. In this double transfer of a data byte from and to the I/O space, ATCn targets the even I/O address set in memory pointer 1 and the consecutive odd address. In this mode, the first data byte transfer accesses an even I/O address and the second data byte transfer accesses an odd I/O address.

Transfer mode 9 can be used to support continuous transmission/ reception for serial interface 0,1, 2 and 3. Set the memory pointer 1 to point to the serial reception buffer (RXBUF0, RXBUF1) and select serial interrupts as the ATCn trigger factor. In this way, everytime a serial communication ends, the MCU continuously reads the reception data (first data byte transfer), then writes the transmission data to the transmission buffer (TXBUF0, TXBUF1) (second data byte transfer) up to 255 times, entirely through the hardware.

Before execute a continuous serial transaction, store the serial transmission data in the memory space that memory pointer 0 points, once the serial communication ends, the MCU has written to the reception data over the transmission data, so that only reception data remains in the memory.

In transfer mode 9, ATCn executes a data byte transfer twice everytime when activated. However, the value in memory pointer 0 increments by one only after the first transfer ends. As a result, the source address for the next ATCn operation is one address higher than that for the previous operation.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated (after one byte of data is transferred twice). When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.15 Transfer mode A

In transfer mode A, ATCn automatically transfers one byte of data from any memory space to any other memory space everytime an ATCn activation request occurs.

Memory pointer 0 00000 to FFFFF		Memory pointer 1 00000 to FFFFF
AT1MAP0	→	AT1MAP1
AT1MAP0 + 1		AT1MAP1 + 1
AT1MAP0 + 2		AT1MAP1 + 2
AT1MAP0 + 3		AT1MAP1 + 3
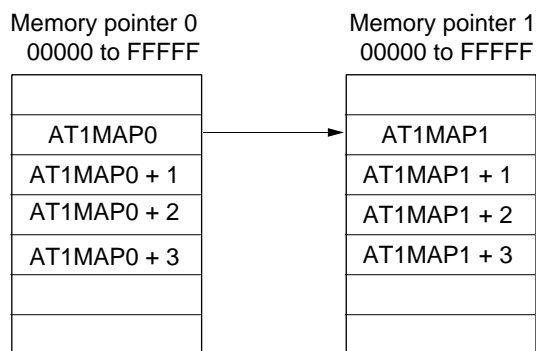
Figure:16.3.12 Transfer Mode A

Set the source address in 20-bit memory pointer 0 (ATnMAP0H, M, L), and set the destination address in 20-bit memory pointer 1 (ATnMAP0H, M, L).

Transfer mode A does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.16 Transfer Mode B

In transfer mode B, ATCn automatically transfers one byte of data from any memory space to any other memory space everytime an ATCn activation request occurs.

Memory pointer 0 00000 to FFFFF	Memory pointer 1 00000 to FFFFF
AT1MAP0	AT1MAP1
AT1MAP0 + 1	AT1MAP1 + 1
AT1MAP0 + 2	AT1MAP1 + 2
AT1MAP0 + 3	AT1MAP1 + 3
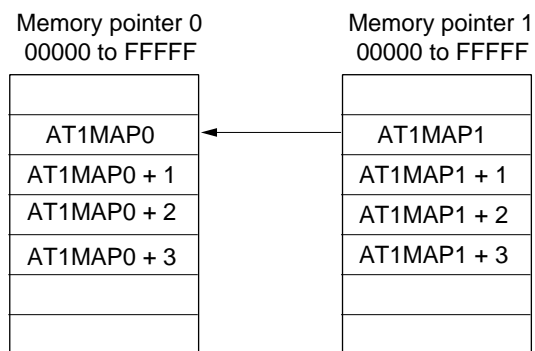
Figure:16.3.13 Transfer Mode B

Set the source address in 20-bit memory pointer 1 (ATnMAP1H, M, L), and set the destination address in 20-bit memory pointer 0 (ATnMAP0H, M, L).

Transfer mode B does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.17 Transfer Mode C

In transfer mode C, ATCn automatically transfers one byte of data from any memory space to any other memory space everytime an ATCn activation request occurs.
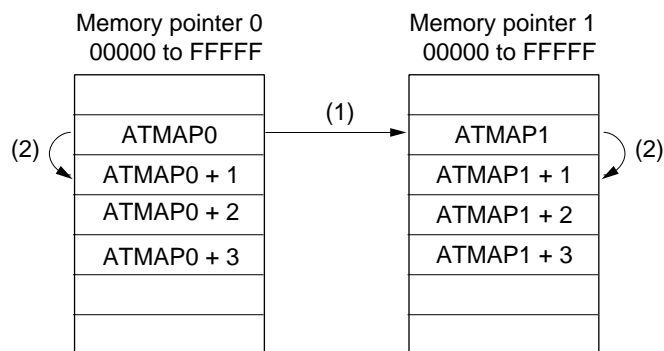
Figure:16.3.14 Transfer Mode C

Set the source address in 20-bit memory pointer 0 (ATnMAP0H, M, L), and set the destination address in 20-bit memory pointer 1 (ATnMAP1H, M, L).

In transfer mode C, the values in memory pointers 0 and 1 increment everytime a byte-length data transfer ends. As a result, the source and destination addresses for the next transfer are one address higher than those for the original transfer.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.18 Transfer Mode D

In transfer mode D, ATCn automatically transfers one byte of data from any memory space to any other memory space everytime an ATCnATCn activation request occurs.

ATCn
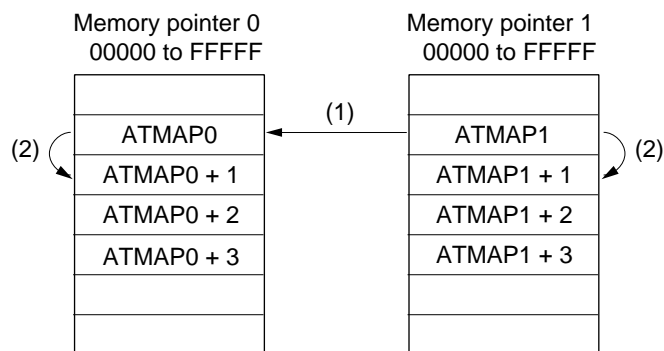
Figure:16.3.15 Transfer Mode D

Set the source address in 20-bit memory pointer 1 (ATnMAP1H, M, L), and set the destination address in 20-bit memory pointer 0 (ATnMAP0H, M, L).

In transfer mode D, the values in memory pointers 0 and 1 increment everytime a byte-length data transfer ends. As a result, the source and destination addresses for the next transfer are one address higher than those for the original transfer.

Set the data transfer count for ATCn in the transfer data counter (ATnTRC). Up to 255 transfers can be set. The counter decrements everytime an ATCn is activated. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the automatic transfer ends.

16.3.19 Transfer Mode E

Transfer mode E is a burst mode. In this mode, when ATCn is activated, it automatically transfers the number of data bytes set in the transfer data counter (ATnTRC) in one continuous operation.
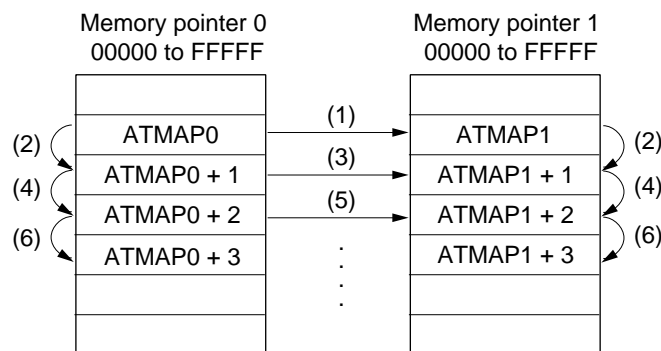
Figure:16.3.16 Transfer Mode E

Set the source address in 20-bit memory pointer 0 (ATnMAP0H, M, L), and set the destination address in 20-bit memory pointer 1 (ATnMAP1H, M, L). Once ATCn is activated, memory pointers 0 and 1 increment everytime a byte-length data transfer ends.

For burst transfers, set the number of data bytes to be transferred in the transfer data counter (ATnTRC). Up to 255 transfers can be set. Once the burst transfer starts, the counter decrements everytime ATCn transfers one byte of data. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the burst transfer ends.

You can shut down ATCn during burst transfers using external interrupt 0. You can enable or disable ATCn shutdown with the burst transfer stop enable flag (BSTP) of ATCn control register 1 (ATnCNT1).

When BTSTP=1 and the interrupt request flag for external interrupt 0 (the IRQ0IR flag in the IRQ0ICR register) is set, the ATCn data automatic transfer shuts down immediately after one byte transfer completed. During this shutdown, the transfer counter and the memory pointers save the values they contained prior to the shutdown. When the interrupt service routine ends and a new ATCn trigger factor occurs, the burst transfer restarts from the point at which it stopped.ATCn

When burst transfer stop is enabled, do not select external interrupt 0 for ATCn trigger factor.

16.3.20 Transfer Mode F

Transfer mode F is a burst mode. In this mode, when ATCn is activated, it automatically transfers the number of data bytes set in the transfer data counter (ATnTRC) in one continuous operation.
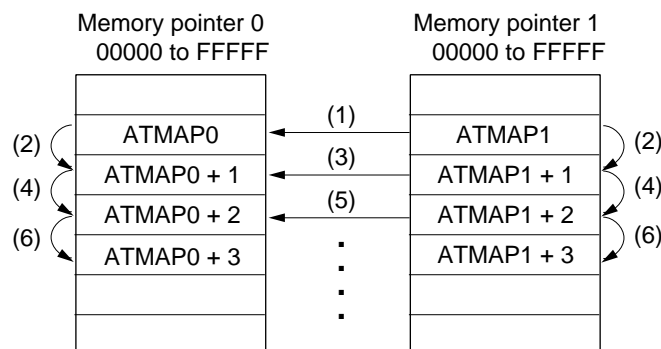
Figure:16.3.17 Transfer Mode F

Set the source address in 20-bit memory pointer 1 (ATnMAP1H, M, L), and set the destination address in 20-bit memory pointer 0 (ATnMAP0H, M, L). Once ATCn is activated, memory pointers 0 and 1 increment everytime a byte-length data transfer ends.

For burst transfers, set the number of data bytes to be transferred in the transfer data counter (ATnTRC). Up to 255 transfers can be set. Once the burst transfer starts, the counter decrements everytime ATCn transfers one byte of data. When it reaches 0x00, an interrupt (ATCnIRQ) occurs and the burst transfer ends.

You can shut down ATCn during burst transfers using external interrupt 0. You can enable or disable ATCn shut-down with the burst transfer stop enable flag (BSTP) of ATCn control register 1 (ATnCNT1).

When BTSTP=1 and the interrupt request flag for external interrupt 0 (the IRQ0IR flag in the IRQ0ICR register) is set, the ATCn data automatic transfer shuts down immediately after one byte transfer completed. During this shutdown, the transfer counter and the memory pointers save the values they contained prior to the shutdown. When the interrupt service routine ends and a new ATCn trigger factor occurs, the burst transfer restarts from the point at which it stopped.ATCn

When burst transfer stop is enabled, do not select external interrupt 0 for ATCn trigger factor.

16.4　Setup Example

An example setup procedure, with a description of each step is as follows ;

Setup Procedure	Description
(1) Disable the data automatic transfer 　　ATnCNT0 　　(AT0CNT0:0x03EC0,AT1CNT0:0x03ED0) 　　bp0 :ATnEH = 0	(1) Set the ATnEN flag of ATnCNT0 register to "0" to disable ATCn data automatic transfer.
(2) Set the data transfer mode. 　　ATnCNT0 　　(AT0CNT0:0x03EC0,AT1CNT0:0x03ED0) 　　bp7 :FMODE = 0 　　bp6 :ATnACT = 0 　　bp5-2 :ATnMD3-0 　　bp0 :ATnEN = 0	(2) Select the data transfer mode with the ATnMD flag in the ATnCNT0 register. No matter which mode you select, setting the FMODE flag disables the increment function in memory pointer 0.Normally set this flag to 0.Note that you must set the ATCn enable flag, ATnEN, to 0 at this step.Only enable ATCn after setting all the other registers.
(3) Set memory pointer 0. 　　ATnMAP0L 　　(AT0MAP0L:0x03EC3,AT1MAP0L:0x03ED3) 　　ATnMAP0M 　　(AT0MAP0M:0x03EC4,AT1MAP0M:0x03ED4) 　　ATnMAP0H 　　(AT0MAP0H:0x03EC5,AT1MAP0H:0x03EC5)	(3) Set the source or destination address in the ATnMAP0 registers depending on the transfer mode you select.
(4) Set memory pointer 1. 　　ATnMAP1L 　　(AT0MAP1L:0x03EC6,AT0MAP1L:0x03ED6) 　　ATnMAP1M 　　(AT0MAP0M:0x03EC7,AT1MAP0M:0x03ED7) 　　ATnMAP1H 　　(AT0MAP1H:0x03EC8,AT1MAP1H:0x03EC8)	(4) Set the source or destination address in the ATnMAP1 registers depending on the transfer mode you select.
(5) Set the transfer data counter. 　　ATnTRC 　　(AT0TRC:0x03EC2,AT1TRC:0x03ED2)	(5) Set the ATCn data transfer count in the ATnTRC register.
(6) Select the ATCn activation factor. 　　ATnCNT1 　　(AT0CNT1:0x03EC1,AT1CNT1:0x03ED1) 　　bp4 :BTSTP 　　bp3-0 :ATnIR3-0	(6) Select the ATCn activation factor with the ATnIR flag in the ATnCNT1 register. If you select a burst-type transfer mode, then you must also enable or disable ATCn shutdown at this step, by setting the BTSTP.
(7) Enable ATC operation. 　　ATnCNT0 　　(AT0CNT0:0x03EC0,AT1CNT0:0x03ED0) 　　bp0 :ATnEN = 1	(7) Enable ATCn data transfers with the ATnEN flag in the ATnCNT0 register.

To activate ATCn in the software, first complete steps (1) to (6), then set the ATnACT flag in the ATnCNT0 register. After the ATnACT flag is set, ATCn is started and data transfer is started. The hardware automatically clears ATnACT flag when ATCn is activated. In standard transfer mode, set a program that sets flags as many as necessary for the the data transfer.

Set the ATCn data automatic transfer while ATCn transfer is disabled (ATnEN flag of the ATnCNT0 register is "0").

Chapter 17 AC Timing Variable

17

17.1 Overview

In the memory expansion mode, the AC timing of the control signal to the external connected device can be changed by the software. This function can set each of the AC timing of the data strobe signal (P72/NWE) at writing and the data strobe signal (P73/NRE) at reading. The hold time is set to the AC timing control register (ACTMD) by the software.

17.2 Control Register

17.2.1 Register

Table:17.2.1 shows the register that controls AC timing.

Table:17.2.1 AC Timing Control Register

Register	Address	R/W	Functions	Page
ACTMD	0x03F06	R/W	AC timing control register	XVIII-4

R/W:Readable/Writable

17.2.2　AC Timing Control Register

■　AC Timing Control Register (ACTMD:0x03F06, R/W)

At wtrite

	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	WTHLD1	WTHLD0	Reserved	Reserved	RDHLD1	RDHLD0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

At Read

	7	6	5	4	3	2	1	0
Flag	Reserved	WTHLD1	WTHLD0	Reserved	Reserved	Reserved	RDHLD1	RDHLD0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	Flag	Description
7-6	Reserved	Always set to "0". *
5-4	WTHLD1-0	2 bits field that specify the hold time at writing 00:No expanded cycle 01:fs × (+1) cycle expanded 10:fs × (+2) cycle expanded 11:reserved
3-2	Reserved	Always set to "0". *
1-0	RDHLD1-0	2 bits field that specify the hold time at writing 00:No expanded cycle 01:fs × (+1) cycle expanded 10:fs × (+2) cycle expanded 11:reserved

Do not word access to ACTMD register.

Always set "0" to the bp denoted by *.

17.3 Operation

17.3.1 Setup

■ AC Timing Setup

AC timing variable function can set the timing of the data strobe signal (P72/NWE) at writing and the data strobe signal (P73/NRE) at reading. The hold time is set to the AC timing control register (ACTMD) by the software. The AC timing control register (ACTMD) has a field that sets the hold time at writing (the cycle for writing data to the external device) and at reading (the cycle for reading data to the external device).

WTHLD:2 bits field that specify the hold time at writing.

RDHLD:2 bits field that specify the hold time at reading.

On field above, the expanded cycle count is specified with 1 unit:1 cycle of system clock (fs). "the set value of field" and "the expanded cycle count" are shown on 17.2.2.

■ Caution 1 on AC Timing Variable Function

When AC timing variable function is used, the external wait count that sets at the memory control register (MEMCTR) should be set more than "the hold time". If the external wait count is set less than "the hold time", the operation is not guaranteed.

> Set the external wait count of the memory control register (MEMCTR) more than "the hold time".
> The external wait count > WTHLD, RDHLD

■ Caution 2 on AC Timing Variable Function

When the memory control register (MEMCTR) specified the hand shake mode, AC timing variable function can not be operated. At hand shake mode, even if the setup time and the hold time are set, AC timing variable function is not valid and the operation is at normal hand shake mode. Use it at the fixed wait mode.

> In hand shake mode, AC timing variable function cannot be used.
> Select the fixed wait mode.

> To use AC timing variable function, set the EXW1-0 of the memory control register (MEMCTR) to "01" (1 wait) or "10" (2 wait).
> If set to "11" (3 wait), the operation is not guaranteed.

17.3.2   Operation

■   AC Timing Characteristic of Data Strobe Signal

AC timing of data strobe signal that sets the setup time and the hold time to the external device with AC timing variable function, is shown as follows.
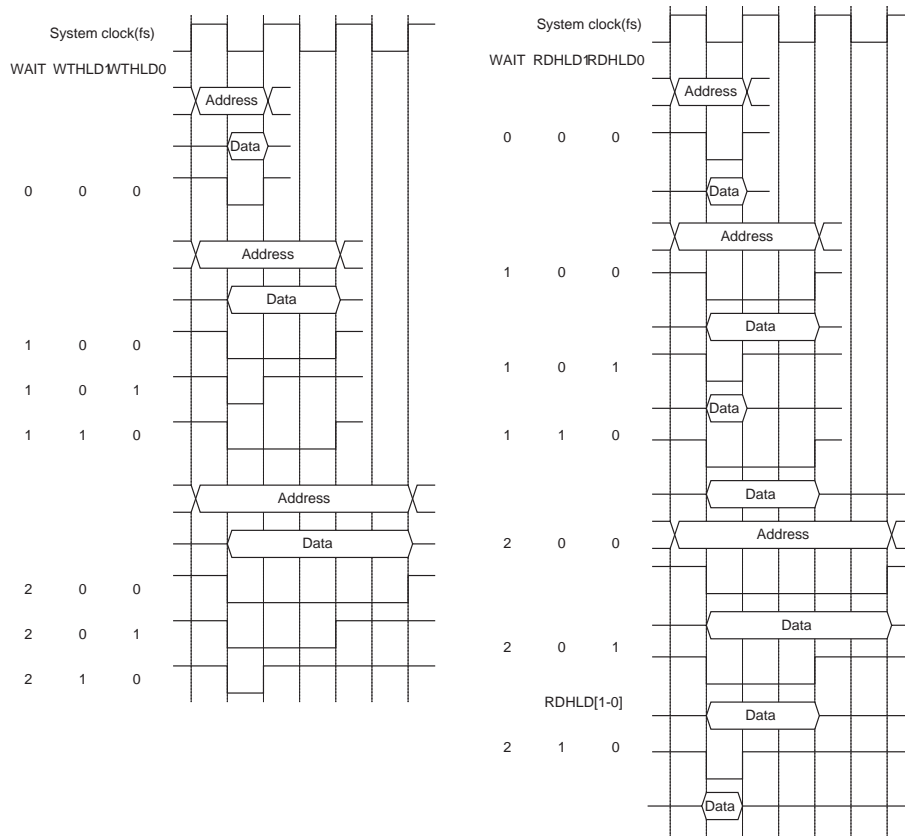
Figure:17.3.1 AC Timing Characteristic of Data Strobe Signal

In Figure:17.3.1, those values are the expanded counts as 1 unit is 1 cycle of system clock (fs). "Wait" means the external wait count that specifies by the memory control register (MEMCTR), "WTHLD0" and "WTHLD1" means the expanded cycle of the hold time.

In order to prevent through current, please fix the level of the extension bus line to the extension bus line (address and data) by disabling pull-up resistor, pull-down resistor or level hold circuit etc., .
(Please take special caution in the standby mode.)

This function is for rerererence and does not guarantee AC timing. Please contact us if you consider using this function.

17.3.3   Setup Example

■   AC Timing Variable Function Setup Example

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description

(1) Set the external wait count
    MEMCTR (0x03F01)
    bp3 : EXWH = 1
    bp1-0 : EXW1-0 = wait count
	(1) Set the wait count by the EXW1-0 flag of the MEMCTR register. At this time, set the EXWH flag to "1", and select the fixed wait mode.
	    [Chapter2 2.4.2. Control Registers]

(2) Set the ACTMD register
    ACTMD (0x03F06)
    bp5-4 : WTHLD1-0 = 01
	(2) Set the setup time and the hold time by the ACTMD register.
	    The set timing is valid from the next cycle after writing the setup value to the ACTMD register.

Chapter 18 Appendix

18

18.1 Flash EEPROM

18.1.1 Overview

The MN101EF29G is equivalent to MN101E29G except its Mask ROM is substituted with 128 KB of flash EEPROM.

-PROM writer mode, which uses a dedicated PROM writer for a microcontroller's stand-alone programming.

-Onboard serial D-Wire Rewriting Mode, which the CPU controls programming of a microcontroller on
 a target board.

-User program area (128 KB)

This area stores an user program. It is overwritten in both programming modes.

-Data area (4 KB)

This area stores various setting information to be stored before in external EEPROM.

-BOOT area (4 Kyte)

This area stores BOOT program.
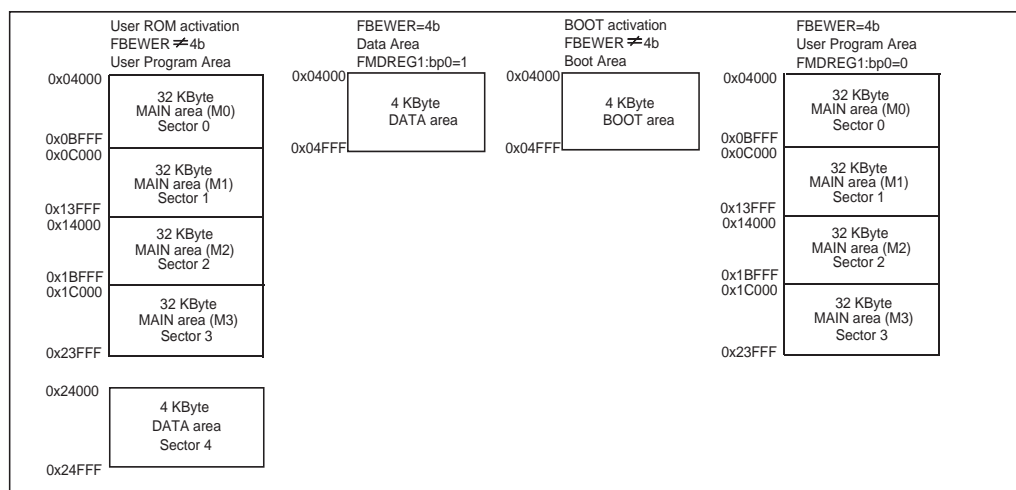
Figure:18.1.1 Memory Map in Internal Flash EEPROM

One cycle of "erase-write" process is counted as 1 programming in every block. When several blocks are programmed separately, programming count is added by just the number of programming cycle. (For instance, when block 1 and 2 are programmed separately, 2 programming count is added.) Therefore, program several blocks together to reduce the programming count.

Table:18.1.1 Difference between ROM and EEPROM

	MN101EF29G (Flash EEPROM)	MN101E29G (Mask ROM)
Data area	O (4 KByte)	X

Writer Maker	Programming method	Programming area		
		Main 128KB	Data 4KB	Boot 4KB
Panasonic Corporation PX-FW2	PROM writer programming mode	O	O	O
	On-board programming mode	O	O	O
OBJECT Co., Ltd. AM1 Flash On-Board Programmer DWire	On-board programming mode	O	O	O
Ando electric Co., Ltd. Flash support Group:AF9709B	PROM writer programming mode	O	O	O
Yokogawa Digital Computer Corporation Inpress module (AF220B)	D-Wire Rewriting Mode	O	O	-

18.2 PROM Writer Mode

18.2.1 Overview

In PROM writer mode, the CPU is halted for the internal flash EEPROM to be programmed. The microcntroller is inserted into a dedicated adaptor socket, which connects to a PROM writer. When the microcontroller connects to the adaptor socket, it automatically enters PROM writer mode.

The programming adaptor differs depending on the writer and the package type.

Table:18.2.1 Programming Adaptor List

Programming Writer	Product Number
By Ando Electric Co., Ltd. By Panax	TEF009-101EF29G100 TEF009-101EF29G100 LQFP

Matching information of the dedicated writer is posted on our semiconductor website, which is listed on the last page of this manual.

■ Fixing a Device on the Adapter Socket and the Position of No.1 Pin
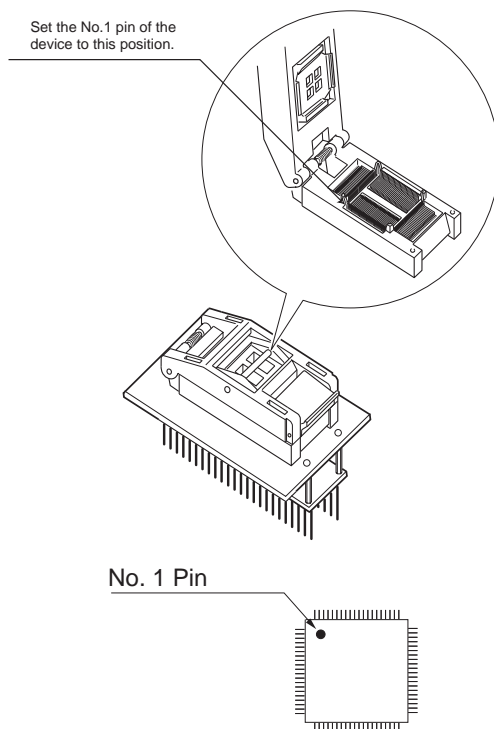
Figure:18.2.1 Fixing a Device on the Adapter Socket and the Position of No.1 Pin

18.3 Onboard Serial D-Wire Rewriting Mode

18.3.1 Overview

The onboard serial D-Wire Rewriting Mode is primarily used to program the flash EEPROM in devices that are already installed on a PCB board with internal dedicated circuit. Use the dedicated serial writer for programming controlled by the load program.

■ Hardware and software requirements

Hardware and software products required for onboard serial D-Wire programming are as follows.

Hardware requirements

-Onboard serial D-Wire writer

-Flash programming connectors or pins for target board

Software requirements

-Programming algorithm for operating onboard serial D-Wire writer

■ Internal hardware for onboard serial D-Wire Rewriting Mode

Use this LSI's dedicated circuit for programming the flash EEPROM in onboard serial D-Wire Rewriting Mode.

> Serial interface I/O pins (P01, P02), used for onboard serial D-Wire programming should be reserved as dedicated pins to prevent other user circuits from communicating with the device. Alternatively, design your target board to be capable of normal communication with serial D-Wire writer.

■ Onboard serial programming writer

The onboard serial D-Wire writer supports the following model.

- YDC AF220/B

  http://www.yokogawa-digital.com/emb/downroad

- Panasonic Corporation   PanaX-FW2

  http://www.semicon.panasonic.co.jp/micom/flash_writer/index.html

- OBJECT Co., Ltd. AM1 Flash On-Board Programmer DWire

  http://www.object.jp/am-obp/am/obp.html

18.3.2   Circuit Requirements for the Target Board
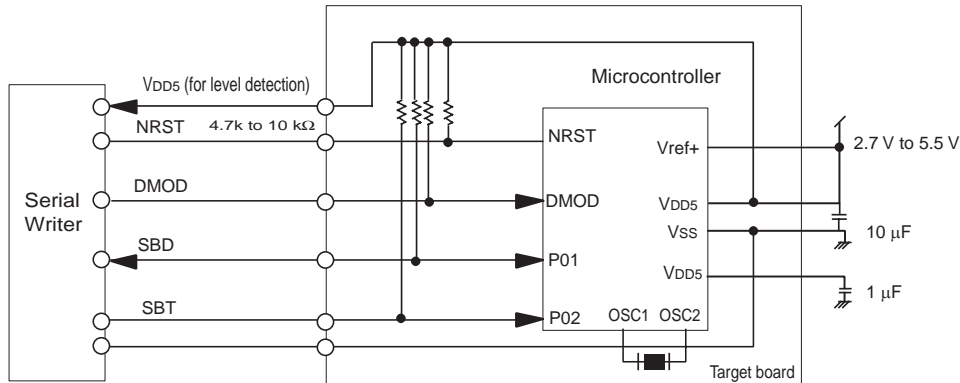
Figure:18.3.1 Circuit Requirements for the Target Board

Pins

-V_{DD5} (18 pin), Vref+ (9 pin)	2.7 V to 5.5 V power supply
-NRST (12 pin)	Reset
-P01 (23 pin)	Data supply pin
-P02 (24 pin)	Clock supply pin
-GND (15 pin)	Ground
-OSC1 (16 pin)	Clock input pin
-OSC2 (17 pin)	Clock input pin
-DMOD (21 pin)	Serial writer mode setting pin (At the user mode=H)

-V_{DD} should be 2.7 V$\leq V_{DD} \leq$5.5 V. When V_{DD} level (2.7 V to 5.5 V) is too low, serial writer generates error message.

-Connect pull-up resistors to NRST, P01, P02 and DMOD pins on the target board. The pull-up resistor value should be 4.7 k$\Omega \pm$ 10 % to 10 k$\Omega \pm$ 10 %

Design NRST, P01, P02 and DMOD pins at serial writer programming and NRST at operation to be able to toggle by a switch. Alternatively, install a wired-OR connection. (For a wired-OR connection, disable NRST and DMOD from the target board during serial writer programming.

-NRST, P01, P02 and DMOD pins are output from the serial writer through an open-drain.

-To prevent the other user circuits on the target board from communicating, the circuit of the target board should be designed for NRST, P01, P02, and DMOD pins to communicate with the serial writer.

-To prevent noise malfunction of Mask ROM, design the circuit of the target board carefully for the signal used for the serial writer.

Please note that though the lower limit of microcontroller operation power voltage is 2.2V, in programming it is 2.7V.

18.3.3   Built-in Hardware for Onboard Serial D-Wire Rewriting

1. I/F

   The following built-in hardware is used as the I/F for serial programming of Flash EEPROM.

   - Dedicated circuit: 1

   - I/O pins: 2

                -P01 and P02 serve for both dedicated circuit and I/O port.

To prevent the other user circuits on the target board, shown on the Figure:18.3.1, from communicating, P01 and P02 pins should be reserved for serial programming, or the circuit of the target board should be designed for normal communication with serial writer.

18.3.4   Clock on the Target Board

-Use the existing clock on the target board for the clock supply to the MN101EF29G on the target board.

Therefore, the clock frequency of the MN101EF29G differs depending on each user.

-The guaranteed clock frequency for the MN101EF29G during serial programming is shown below.

Frequency	Operating voltage
2.0 to 20MHz	2.7 V to 5.5 V

⚠ Do not set the relation between microcontroller clock pin frequency and communication clock frequency to 1/20 or less.

18.4 Microcontroller Rewriting Mode

18.4.1 Setting of Microcontroller Rewriting Mode

Microcontroller Rewriting Mode is used to overwrite the internal flash memory by executing the overwriting program on the microcontroller. This makes it possible to overwrite the internal flash memory while the microcontroller is still mounted on board.

> We are preparing the sample program that achieves microcontroller rewriting mode. Please the customer who consider the use of this function inquire our company (user support URL in end of the LSI User's Manual).

■ Microcontroller Rewriting Mode (on-board rewriting by microcontroller mode)

This mode is used to overwrite the internal flash memory by user's boot program (internal flash overwriting program).

To overwrite the internal flash memory by microcontroller rewriting mode, the boot program needs to be written by one way of the following two.

1. Built the boot program in user's program (part of the MAIN area) in advance.

2. Write the boot program in the BOOT area by using the parallel programmer.

Data to be written in the internal flash memory can be transferred (down-loaded) by using serial incorporated in microcontroller, DMA, and the external bus. Flash memory writing is also possible in the LSI.

The area to be overwritten is only the MAIN/DATA area.

Table:18.4.1 On-board Rewriting Mode Setting by External Pin

Mode	Start space	Microcontroller memory mode	Rewriting area	External pin setting					
				NRST	ATRST	DMOD	OCD_SCL	OCD_SDA	MMOD
D-wire mode	-	Single chip	MAIN/DATA/ BOOT	*2)	L	*2)	*2)	*2)	L
Microcontroller rewriting mode	BOOT	Single chip	MAIN/DATA	↑ *1)	L	H	open or H		H

*1) Mode is determined by the pin condition when NRST is released. (L→H)
*2) It is controlled by the dedicated on-board programmer.

> In microcontroller rewriting mode, the BOOT area can not be overwritten. Use the parallel programmer for the BOOT writing.

> The microcontroller rewriting mode can not be used to security-set chip in MN101EF29G.

18.4.2   On-board rewriting by Microcontroller Mode

on-board rewriting by the microcontroller mode can be done by executing the boot program (the internal flash memory writing program) placed on the internal RAM. Data for writer can be down-loaded by using the peripheral functions incorporated in the microcontroller (serial, DMA and external bus).

The features of the on-board rewriting by the BOOT program startup are shown below.

■   Features of Rewrite by the BOOT Program

- The BOOT area can not be written from the Microcontroller Rewriting Mode, so there is no rewrite by mistake and it has high safety during the microcontroller rewriting mode.

- Approved as an independent program which is independent of user's program

- Be suitable for rewriting of user's program, etc. of the MAIN/DATA area.

Rewriting with BOOT program is not available in security-set chip in MN101EF29G.
When rewriting ROM area with security, rewrite by using on-board serial D-wire rewriting or parallel writer.

At first, it is necessary that the BOOT program is written by Parallel programmer and On-board programmer.

18.4.3   On-board Rewriting Control Registers

To overwrite the internal flash memory with the on-board rewriting mode, the on-board rewriting needs to be enabled by operating the flash on-board rewriting enable register.

Execute the operation of the flash on-board rewriting enable register by executing the instructions placed on the internal RAM. The operation is not assured when the instructions are executed placed on the internal flash memory after the on-board rewriting is enabled.

Settings of the sector protect is executed by the flash rewriting command, however, the writing to the Sector Protect Bit needs to be enabled by operating the flash on-board Sector Protect Bit writer enable register,

If the writing command of the Sector Protect Bit is executed in the status of the writing disabled, the Sector Protect Bit is not written.

MN101E series is bank system that accessed to data memory at each 64 KB. When address space is over the 64 KB, need to set the Bank register for source address (SBNKR) and Bank register for destination address.[2.2.5 Bank Function]

Table:18.4.2 shows on-board rewriting control registers

Table:18.4.2 Control Registers

Address	Register	Symbol	Bit number	Initial value	Access size	Page
0x03FC9	Flash on-board rewriting enable register	FBEWER	8	x'00	8	XVIII-10
0x03FCA	Sector Protect/Security command enable register	FSKPBPER	8	x'00	8	XVIII-11
0x03FC8	Flash mode register	FMDREG1	8	x'00	8	XVIII-11
0x03F0A	Bank register for source address	SBNKR	8	x'00	8	II-22
0x03F0B	Bank register for destination address	DBNKR	8	x'00	8	II-23

■   Flash on-board Rewriting Enable Register (FBEWER: 0x03FC9)

This register is used to specify enable/disable of the flash memory rewriting during on-board rewriting mode.

Bit No.	7	6	5	4	3	2	1	0
Bit name	BEW7	BEW6	BEW5	BEW4	BEW3	BEW2	BEW1	BEW0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Bit name	Description
7-0	BEW7-0	on-board rewriting enable 01001011: on-board rewriting enable Other than the above: on-board rewriting disable

■ Flash On-board Sector Protect/Security Command Enable Register (FSKPBPER: 0x03FCA)

This register is used to specify enable/disable of the access to the sector protect/security command bit.

Bit No.	7	6	5	4	3	2	1	0
Bit name	SEW7	SEW6	SEW5	SEW4	SEW3	SEW2	SEW1	SEW0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Bit name	Description
7-0	SEW7-0	Sector Protect/Security command enable 01011011: Sector Protect/Security command enable Other than the above: Sector Protect/Security command disable

■ Flash Mode Register (FMDREG1: 0x03FC8)

This register is used to specify sector area in on-board rewriting modes.
The initial value at reset is different in MN101EF29G and ICE

-In MN101EF29G

Bit No.	7	6	5	4	3	2	1	0
Bit name	Reserved	Reserved	Reserved	-	Reserved	Reserved	Reserved	DATA
At reset	0	0	0	-	1	1	0	0
Access	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

bp	Bit name	Description
7-5	Reserved	Always set to "0". *1)
4	-	-
3-2	Reserved	Always set to "1". *2)
1	Reserved	Always set to "0". *1)
0	DATA	0: Main area 1: DATA area

-In ICE

The following table shows the initial value of ICE

Bit No.	7	6	5	4	3	2	1	0
Bit name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
At reset	0	0	0	0	0	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	bp	Description
7-3	Reserved	Always set to "0". *1)
2	Reserved	Always set to "1". *2).
1	Reserved	Always set to "0". *1)
0	Reserved	Always set to "1". *2)

When the BOOT area starts, 4 KB of the boot area is mapping in the internal ROM space of the microcontroller (0x4000 to 0x23FFF). However, when it is set to FBEWER=0x4b, the area to be mapped changes from the BOOT area to the MAIN area. Therefore, operation of the FBEWER register should be done by executing the instructions placed on the internal RAM.

The Sector Protect/Security command enable register (FSKPBPER) is valid when the on-board rewriting enable register (FBEWER) is set to the on-board rewriting enable.

Always set "0" to the bp denoted by *1).
Always set "1" to the bp denoted by *2).

18.4.4　Control Command

Flash memory incorporated in this LSI can be executed each operation by inputting address and data supporting command sequence described in Table:18.4.3

Table:18.4.3 Flash Memory Control Command

Command sequence	Cycle	Bus cycle											
		First		Second		Third		Fourth		Fifth		Last	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXh	F0h										
Auto Select	3	AAAh	AAh	555h	55h	AAAh	90h						
Program	4	AAAh	AAh	555h	55h	AAAh	A0h	PA	PD				
Program to Buffer	WC+4	AAAh	AAh	555h	55h	SA	25h	SA	WC	PA	PD	SA	PD
Program to Buffer Abort Reset	3	AAAh	AAh	555h	55h	AAAh	F0h						
Program Buffer to Flash	1	SA	29h										
Sector Erase	6 *1) (+SA(n))	AAAh	AAh	555h	55h	AAAh	80h	AAAh	AAh	555h	55h	SA	30h
Security Key Check	19	AAAh	AAh	555h	55h	AAAh	45h	100h	KD	...	...	10Fh	KD
Security Key Program	20	AAAh	AAh	555h	55h	AAAh	35h	100h	KD	...	...	100h	29h
Sector Protect Bit Program	6	AAAh	AAh	555h	55h	AAAh	80h	AAAh	AAh	555h	55h	SLA	C0h

* 1) The Sector Address to be erased can be continuously input at 6 cycles or later.
　　(input the Sector Address to erased and Data 30h in pairs.)

Symbol description:
　　　Addr: Command address (An[11:0])
　　　Data: Command data (Dn[7:0])
　　　PA: Program address
　　　PD: Program data
　　　SA: Sector address
　　　SLA: Protected sector address
　　　KDn: Security key data (8bit, n=1 to 16)
　　　WC: Word count number
　　　X: H or L

Set the command address An issued by microcontroller to the following.

Command address An = 0x4000 + Addr

However, address recognized as a command address is an address in the internal ROM space (0x4000 to 0x23FFF) and it will be An[11:0].

Specify the first address of the corresponding sector as a sector address. (Refer to Figure:18.1.1)

In the same way, address recognized as a sector address is an address in the internal ROM space (0x4000 to 0x23FFF) and it is 7 bits of A[18:12].

In addition, specify the address in the internal ROM space (0x4000 to 0x23FFF) as a program address. The operation is not assured if addresses any other than the above are specified.

18.4.5   Operation

Table:18.4.4 describes the operation of the flash memory control command.

■   Read/Reset

This is a command to input when it is recovered from the status of transiting to Auto Select mode (return to the normal Read mode of the memory space) after the Auto Select command is input. It is used with the Auto Select command as a set when the protect is executed.

■   Auto Select

This is used to confirm whether the command is operating normally or not when the security and protect are executed. When Auto Select command is input, it is transited to the Auto Select mode and when the Read operation is executed with the transition status, the special register for operation confirmation is read. The contents of the register is shown below.

(In addition, with the transition status to the Auto Select mode, command input other than Read/Reset are not accepted. Command should be executed after pulling out of the Auto Select mode with Read/Reset command once.)

Table:18.4.4 Special Register Address and Data at Auto Select Mode (EF31G)

	Sector	BOOT pin	Special register address specification	Output data		
			Address register An	Code *1		
Sector Protect Verify	SA0	L	0x04004	Data	Data	Data
	SA1	L	0x0C004	Data	Data	Data
	SA2	L	0x14004	Data	Data	Data
	SA3	L	0x1C004	Data	Data	Data

*1   DQ1: Protect status confirmation bit (Protect: 1, No protect: 0)j   ; Select the Sector Address to be confirmed

DQ3: Security set status confirmation bit (Security set: 1, No security set: 0)   ; Data is output whichever Sector Address is selected.

DQ4: Security release status confirmation bit (Security release NG: 1, Security release OK: 0)   ; Data is output whichever Sector Address is selected.

■   Program

This is a data writing mode. For writing, command input is executed every 1 byte. After the command input, writing is automatically executed inside. As any command input can not be accepted during the automatic writing operation, execute the next command input after the writing is completed.

■   Program to Buffer

This is a command to store writing data to Buffer. Data to store is maximum 64 KB (when it is 8-bit). Data volume to store is specified with BC. If it is 32 Byte, input 1Fh (writing byte - 1) to BC. In addition, addresses to write data are automatically internally incremented, so input the only first address.

After data is stored, writing starts by the Program Buffer to Flash command.

■   Program to Buffer Abort Reset

Writing by Program to Buffer command is limited within the same Sector and can not write by two Sectors. If writing by two sectors is set, this memory core will be Program to buffer abort status and does not accept the command other than Program to Buffer Abort Reset. So, to execute the next command, input of this command and

recovery from Abort status are needed. In addition, other than this command, the recovery from the Abort status by the hard reset (set the P27 pin to L) is possible.

■ Program to Buffer to Flash

This is a command to write data stored by Program to Buffer command to memory. It is used with Program to Buffer as a set, and this command is input continuously after the Program to Buffer is input.

■ Sector Erase

Sector Erase is the function to erase by the sector. The Sector Erase function executes the erase of the sector corresponded with SA which is specified by the 6th cycle of command input. In order to erase multiple sectors, input sector Address and Data 30h in a pair after the 6th cycle of the command input. To confirm the state during the erase, execute with data polling. During automatic erase, any command will not be accepted. Please execute the next command input after completion of the erase.

■ Security Key Program

This LSI has a security function to prevent from reading and rewriting data without anthorization (through SECURITY KEY CHECK command to examine a security key code match). This function is enabled by programming a security key code, using SECURITY KEY PROGRAM command. The security key code is 128-bit length and the SECURITY KEY PROGRAM command inputs security key data (in a byte or word) in turn with fixed key address 100h. A security key address in SECURITY KEY PROGRAM command is incremented automatically inside the memory modules. After the SECURITY KEY PROGRAM command, Security Lock state is established by Hardware Reset or SECURITY KEY CHECK command with wrong security key data. During Security Lock state, other commands are not acceptable except AUTO SELECT and READ/RESET commands. Therefore, read program and erase operations for all sectors are inhibited. Please perform the following SECURITY KEY CHECK command to cancel Lock state. It is possible to confirm Lock state by the above AUTO SELECT command. In addition, SECURITY KEY PROGRAM command can be executed only once and the security key data (includes erase) cannot be changed.

■ Security Key Check

SECURITY KEY CHECK is a command to unlock Security Lock state that is activated by SECURITY KEY PROGRAM operation. Once Security Lock state is set by the operation, security function will be valid after RESET. It is always to required after Hardware Reset to unlock Lock state with SECURITY KEY CHECK command.

■ Sector Protect Bit Program

This LSI flash memory has the protect operation not to write data of specified sector. This operation disables write/erase of sector executed by Sector Protect Bit Program. When protect is set up by Sector Protect Bit Program command, it can not be released.

Protect can not be cancelled once it is set. Be careful of it in setting.

18.4.6   Program Flow Chart

Automatic program flow chart of this memory core is shown below.

■   Program Flow Chart
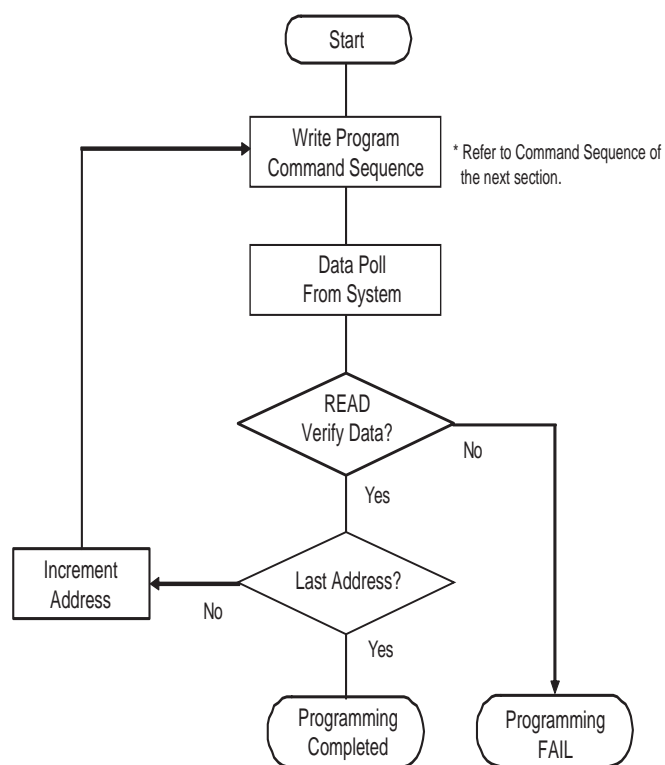
Figure:18.4.1 Program Flow Chart

Write Program Command Sequence (Address/Command)
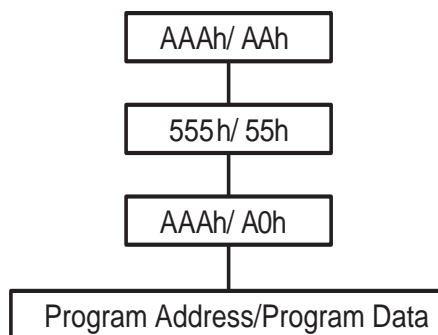
Figure:18.4.2 Write Program Command Sequence

■ Program Buffer Program Flow Chart

*1) Polling is conducted for data of the last address stored in Program Buffer.
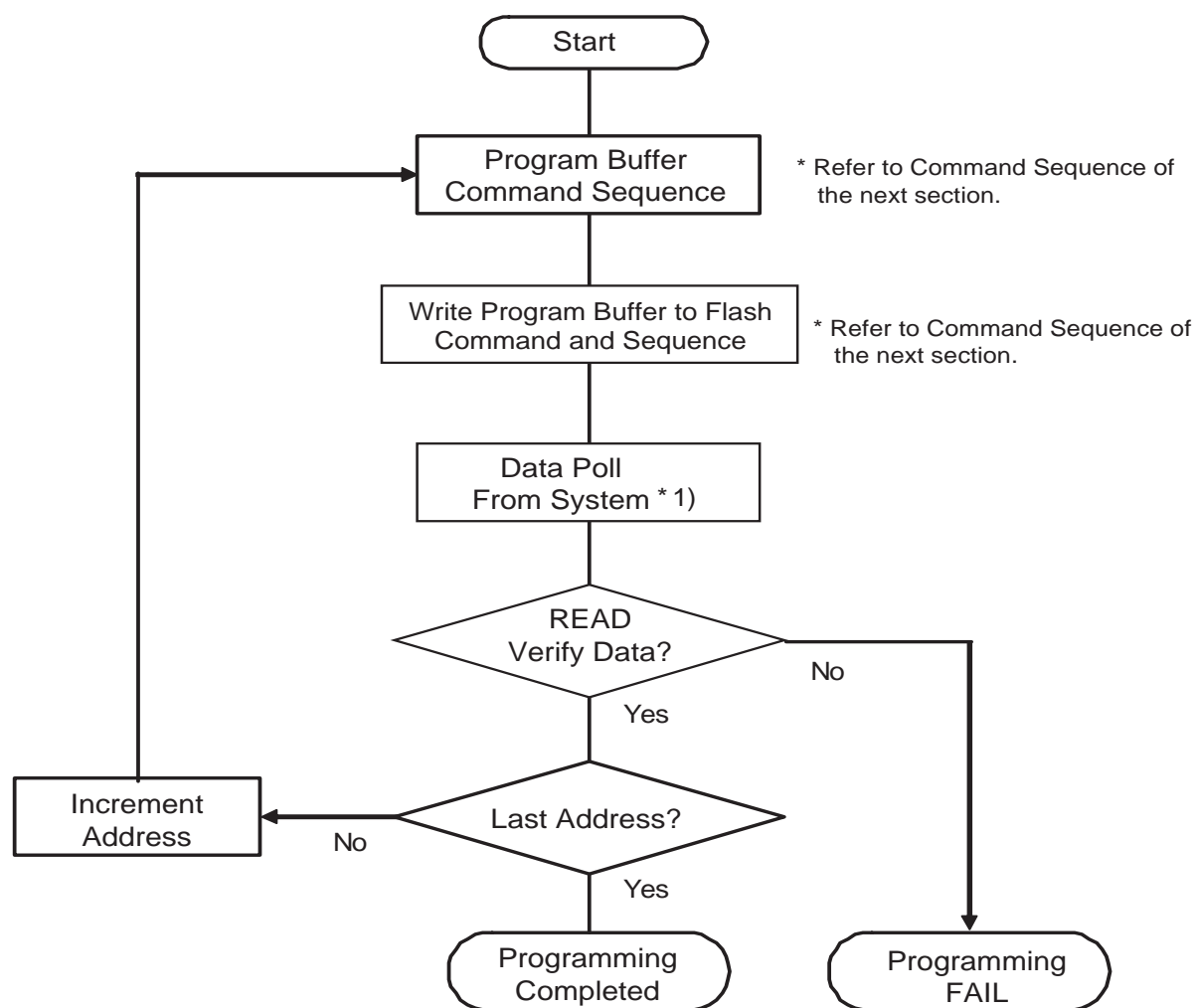
Figure:18.4.3 Program Buffer Program Flow Chart

Program to Buffer Command Sequence (Address/Command)

```
AAAh/AAh
555h/55h
Sector Address/25h
Sector Address/Word Count
Program Address/Program Data(0)
Sector Address/Program Data(1)
Sector Address/Program Data(2)
            ⋮
Sector Address/Program Data(n')
```

n'="Word Count"
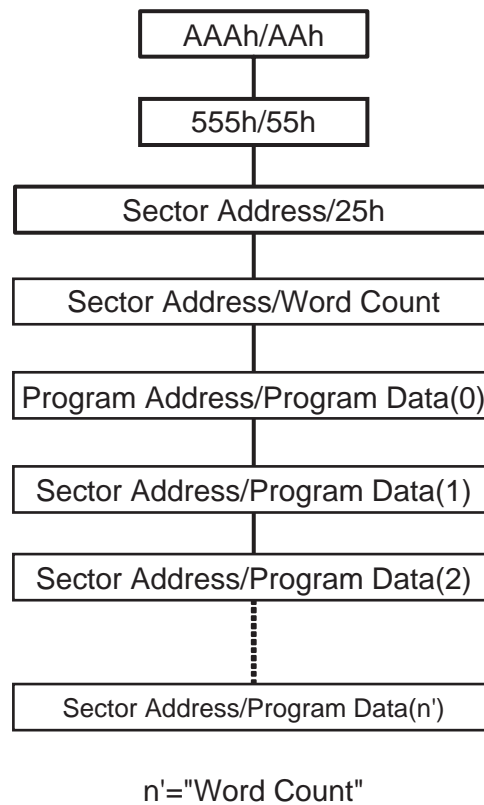
Figure:18.4.4 Program to Buffer Command Sequence

Write Program Buffer to Flash Command Sequence (Address/Command)

Byte Mode

```
Sector Address/29h
```
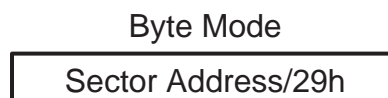
Figure:18.4.5 Write Program Buffer to Flash Command Sequence

18.4.7   Protect Set-up

The following shows the flow chart for protect set-up to protect write data of this memory core.

■   Protect Set-up Flow Chart

Start

Hardware RESET *1)   * Input "L" to the NRESET pin

Sector Protect Bit Program
Command Sequence   * Refer to Command Sequence of the next section.

Toggle bit From System

Auto Select
Command Sequence   * Refer to Command Sequence of the previous section.

DQ1=1?   No

Yes

Read/Reset
Command Sequence   * Refer to Command Sequence of the previous section.

Next Sector
Protect?

Yes

No

Sector Protect Bit Programming
Completed

Sector Protect Bit Programming
Error (FAIL)

Figure:18.4.6 Protect Set-up Flow Chart

*1) Support by commands when not executing hardware reset.

Input dummy
(1) Program to Buffer command
 (2) Program to Buffer Abort Reset command

(Address/Command)

| AAAh/ AAh |

| 555h/ 55h |
| AAAh/ 25h |
| 000h/ 00h | (1)
| 000h/ FFFFh |
| 000h/FFFFh |

| AAAh/ AAh |
| 555h/ 55h | (2)
| AAAh/ F0h |

| Sector Protect Program Sequence |
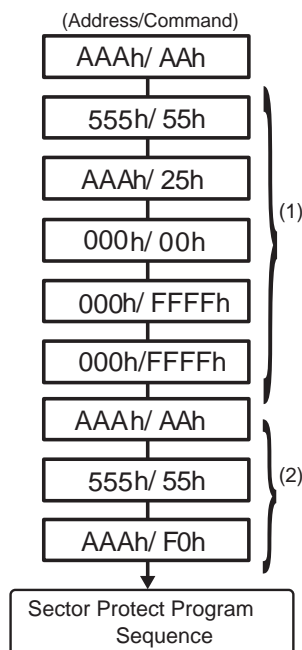
* Set the comand Address published form the microcontroller core as follows.

Command Address = 0x4000 + Address

Sector Protect Bit Program Command Sequence (Address/Command)

Word Mode

| AAAh/ AAh |
| 555h/ 55h |
| AAAh/ 80h |
| AAAh/ AAh |
| 555h/ 55h |

| Protect Sector Address/C0h |
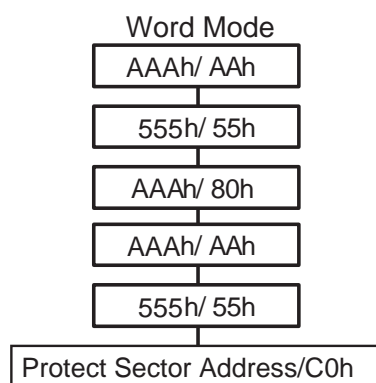
Figure:18.4.7 Sector Protect Bit Program Command Sequence

18.4.8   Erase Flow Chart

Automatic erase flow chart of this memory core is shown below.

■   Sector Erase Flow Chart
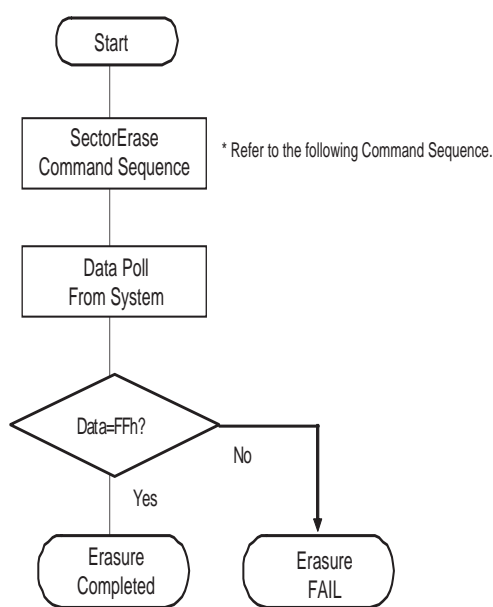
Figure:18.4.8 Sector Erase Flow Chart

Sector Erase Command Sequence (Address/Command)

[Sector Erase]
Word Mode

AAAh/ AAh
555h/ 55h
AAAh/ 80h
AAAh/ AAh
555h/ 55h
Sector(1) Address/ 30h
Sector(2) Address/ 30h
Sector(3) Address/ 30h
Sector(n) Address/ 30h
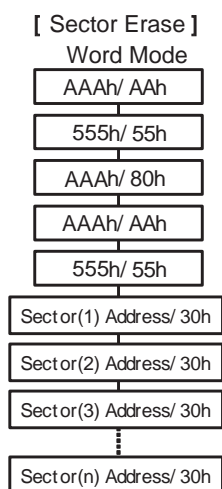
Figure:18.4.9 Sector Erase Command Sequence

18.4.9　Data Polling Flow Chart

■　Data Polling Flow Chart

As a way to know whether the execution of the automatic program is in process or completion status, there is a data polling function. When the reading operation is executed while the automatic writing /erasing algorithm is executed, this memory core is output the reverse data of the written to DQ7 last. When the automatic writing / erasing algorithm is completed, this memory core is output the proper data written to DQ7 last.
The flow chart of data polling confirming the automatic algorithm execution status is shown below.
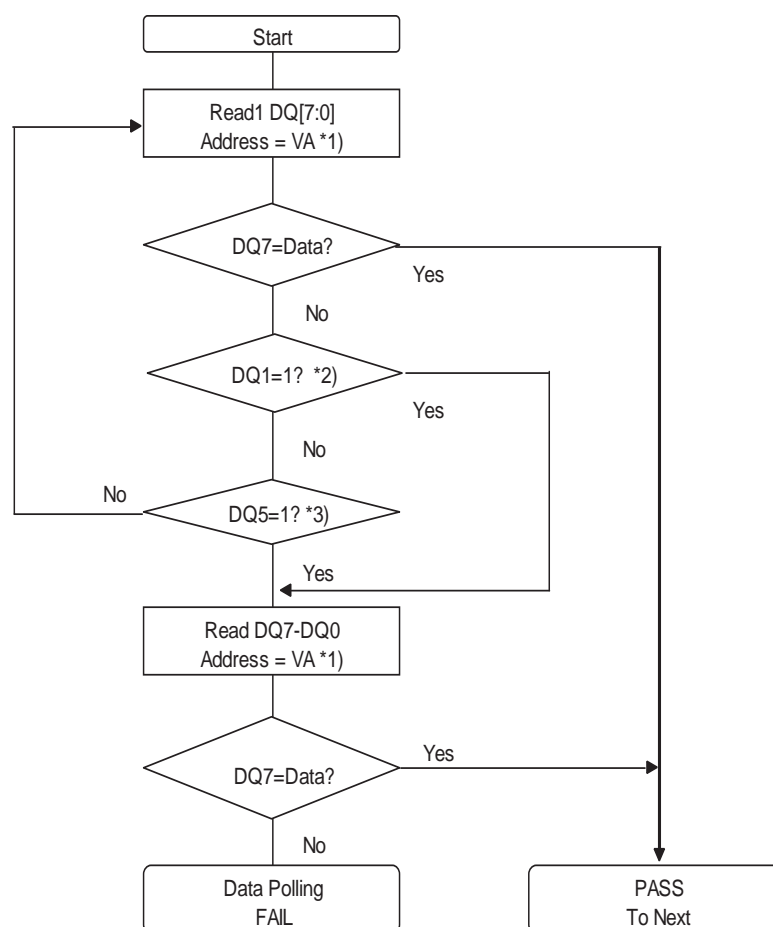
*1)VA:　Address at Byte/Word PROGRAM mode, a last address at WRITE PROGRAM BUFFER
　　　　to FLASH mode,0000h at CHIP ERASE mode, and an address specifying the last
　　　　erase sector at SECTOR ERASE mode.

*2)DQ1:　As for writing with Write to Buffer, '1' is output to DQ1 in case of problems
　　　　"BC does not agree with the amout of stored data(the number of byte). " or " write
　　　　operation ranging two Sectors" . This function is valid as far as data polling is
　　　　operating(DQ7 outputs the invert value of data).

*3)DQ5:　In case that program or erase operation is proceeding beyond the specified time
　　　　(number of an internal pulses for program/erase), '1' is output to DQ5 as time-out.
　　　　This function is valid as far as data polling is opetating(DQ7 outputs the invert
　　　　value of data).

Figure:18.4.10　Data Polling Flow Chart

18.4.10 Toggle Bit Flow Chart

■ Toggle Bit Flow Chart

The flow chart of the toggle bit confirmed the automatic algorithm execution status of this memory core is shown below.

```
                    ┌─────────────────────┐
                    │        Start        │
                    └─────────────────────┘
                              │
                    ┌─────────────────────┐
                    │   Read1 DQ[7:0]     │
                    │   Address = VA *1)  │
                    └─────────────────────┘
                              │
                    ┌─────────────────────┐
          ┌────────▶│   Read2 DQ[7:0]     │
          │         │   Address = VA *1)  │
          │         └─────────────────────┘
          │                   │
          │               ◇─────────◇        No
          │          Toggle Bit(DQ6)  ─────────────────┐
          │          =Toggle? *2)                       │
          │               ◇─────────◇                   │
          │                   │ Yes                      │
          │      No       ◇─────────◇                    │
          └──────────────    DQ5=1?                      │
                         ◇─────────◇                     │
                              │ Yes                       │
                    ┌─────────────────────┐              │
                    │   Read DQ7-DQ0      │              │
                    │   Address = VA *1)  │              │
                    └─────────────────────┘              │
                              │                           │
                          ◇─────────◇       No            │
                     Toggle Bit(DQ6) ───────────────────▶│
                     =Toggle? *2)                         │
                          ◇─────────◇                     ▼
                              │ Yes              ┌─────────────────────┐
                    ┌─────────────────────┐      │        PASS         │
                    │ Toggle Bit Confirming│     │      To Next        │
                    │    Error(FAIL)      │      └─────────────────────┘
                    └─────────────────────┘
```
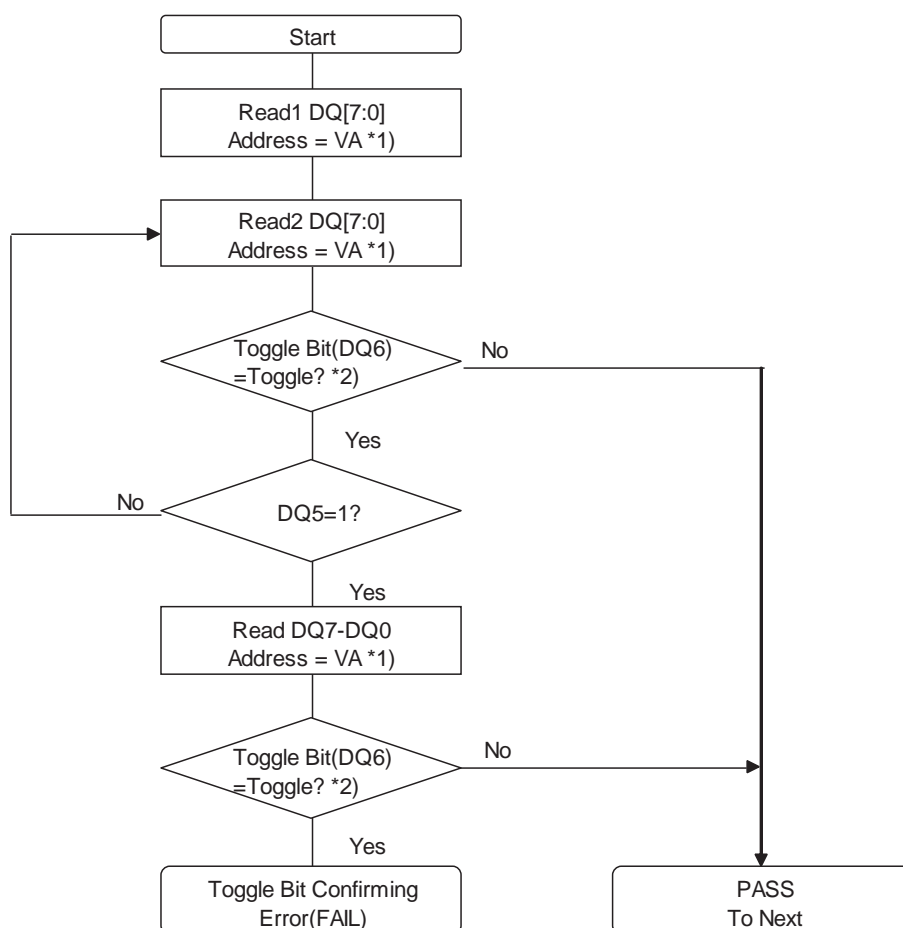
*1)VA: Address 4100h at SECURITY KEY PROGRAM mode, Address of Sector to be protected
        at SECTOR PROTECT BIT PROGRAM mode.

*2)Toggle: In Toggle Bit operation, data are read from DQ6 twice and state is judged by whether the
            read data are alternating each other. In case former read data exists(i.e. read for the second
            time or third time and so on), toggle judge is done by whether read data is same with the previous one.

*3)DQ5: In case that program or erase operation is proceeding beyond the specified time
         (number of an internal pulses for program/erase), '1' is output to DQ5 as time-out.
         This function is valid during Toggle Bit opetation(DQ6 toggles).

Figure:18.4.11 Toggle Bit Flow Chart

18.4.11 Security Key Unlock Flow Chart

■ Security Key Unlock Flow Chart

The flow chart of the security key unlock of this memory core is shown below.
When security is set (security key code is written), the following flow chart always must be executed after reset release. (Writing command will not be executed when security key code is written.)
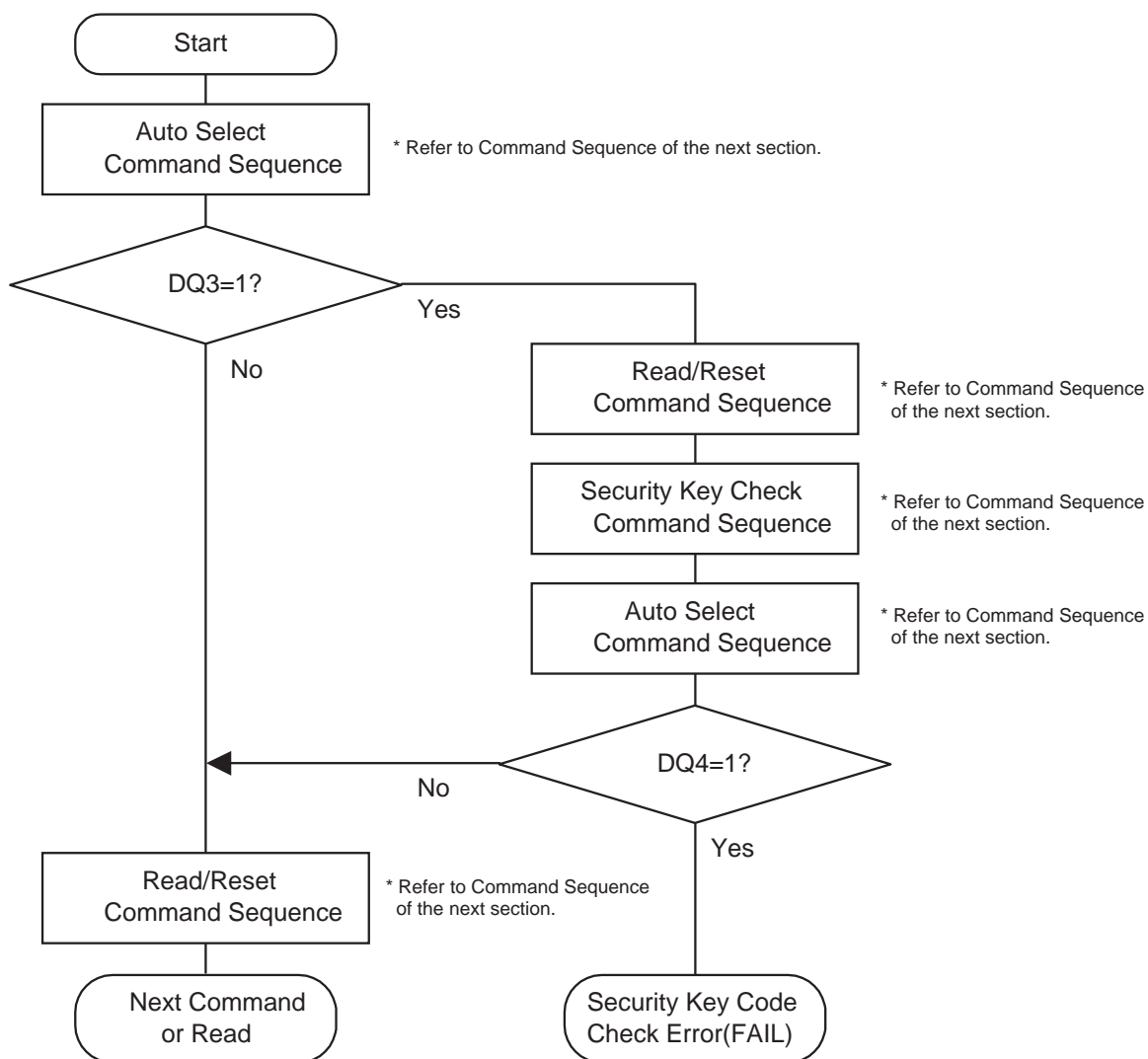
Figure:18.4.12 Security Key Unlock Flow Chart

Security Key Check Command Sequence (Address/Data(Command))

Byte Mode

```
┌─────────────────┐
│    AAAh/AAh      │
└─────────────────┘
         │
┌─────────────────┐
│    555h/55h      │
└─────────────────┘
         │
┌─────────────────┐
│    AAAh/45h      │
└─────────────────┘
         │
┌─────────────────┐
│   100h/KD(0)     │
└─────────────────┘
         ┊
┌─────────────────┐
│   10Fh/KD(15)    │
└─────────────────┘
```

<Explanation>
Relationship between Key Address of security and Key Data

Byte Mode

Key Address	100h	101h	102h	103h	···	10Fh
Key Data	KD(0)	KD(1)	KD(2)	KD(3)	···	KD(15)

* Key Data is little endian system.

Figure:18.4.13 Security Key Check Command Sequence

Security Key Program Command Sequence (Address/Data(Command))

Byte Mode

```
┌─────────────────┐
│    AAAh/AAh      │
└─────────────────┘
         │
┌─────────────────┐
│    555h/55h      │
└─────────────────┘
         │
┌─────────────────┐
│    AAAh/35h      │
└─────────────────┘
         │
┌─────────────────┐
│   100h/KD(0)     │
└─────────────────┘
         ┊
┌─────────────────┐
│   100h/KD(15)    │
└─────────────────┘
         │
┌─────────────────┐
│    100h/29h      │
└─────────────────┘
```
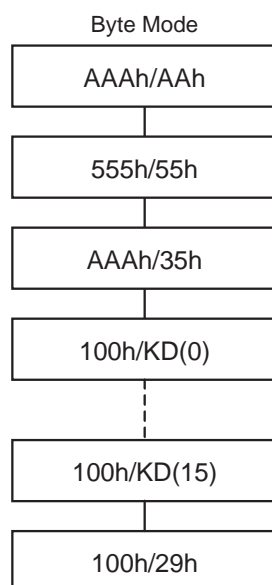
* Key Address is not incremented.
  It is fixed value input of 100h.

Figure:18.4.14 Security Key Program Command Sequence

Auto Select Command Sequence (Address/Data(Command))

Byte Mode

AAAh/AAh
555h/55h
AAAh/90h
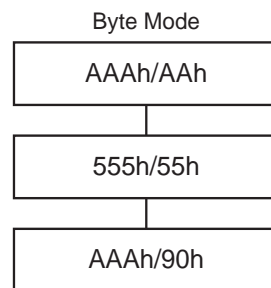
Figure:18.4.15 Auto Select Command Sequence

Read/Reset Command Sequence (Address/Data(Command))

Byte Mode

XXXh/F0h
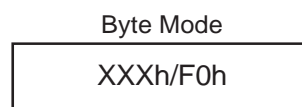
Figure:18.4.16 Read/Reset Command Sequence

18.4.12 Security Key Set Flow Chart

■ Security Key Set Flow Chart

The flow chart of the security key code set of this memory core is shown below.

```
                    ┌─────────────┐
                    │    Start    │
                    └─────────────┘
                           │
              ┌─────────────────────────┐
              │ Security Key Program     │    * Refer to Command Sequence
              │ Command Sequence         │      of the previous section.
              └─────────────────────────┘
                           │
              ┌─────────────────────────┐
              │ Toggle bit From System   │    * Refer to 15.5.2 Toggle bit flow chart.
              └─────────────────────────┘
                           │
              ┌─────────────────────────┐
              │        RESET             │    * Input "L" to the NRESET pin.
              └─────────────────────────┘
                           │
              ┌─────────────────────────┐
              │ Auto Select Command      │    * Refer to Command Sequence
              │ Sequence                 │      of the previous section.
              └─────────────────────────┘
                           │
                     ╱─────────╲
                    ╱   DQ3=1?   ╲────── No ──────┐
                    ╲           ╱                  │
                     ╲─────────╱                   │
                          │ Yes                     │
              ┌─────────────────────────┐          │
              │ Read/Reset Command       │    * Refer to Command Sequence
              │ Sequence                 │      of the previous section.
              └─────────────────────────┘          │
                          │                         │
             ┌─────────────────┐        ┌─────────────────┐
             │ Security Key     │        │ Security Key     │
             │ Setting          │        │ Setting          │
             │ Completed        │        │ Error(FAIL)      │
             └─────────────────┘        └─────────────────┘
```

Figure:18.4.17 Security Key Set Flow Chart

18.5 Connecting the PX-FW2

The MN101EF29G includes an on-chip 128KB flash EEPROM that can be erased and written electrically. The Panasonic PX-FW2 is used to program this on-chip flash EEPROM with the MN101EF29G in the onboard state. This chapter describes the procedure for connection the MN101EF29G to the PX-FW2.

18.5.1 PX-FW2 Connecting Signals

To connect the MN101EF29G to the PX-FW2, a total of 6 lines must be connected: three communication signal lines, reset, VDD, and VSS. The MN101EF29G is connected to the PX-FW2 using a 10-conductor flat cable. The PX-FW2 can be connected to the target board easily if a connector for a 10-conductor flat cable is mounted on the target board. If a connector cannot be mounted on the target board, the 10-conductor flat cable can be directly soldered to the board.

> The length of the cable must not exceed 50 cm. The serial communication system may not work correctly with cables longer than 50 cm.

Table:18.5.1 MN101EF29G and PX-FW2 Pin Correspondence

MN101EF29G signals (pin number)	PX-FW2 connector signals (pin number)	I/O	Notes
NRST (12)	NRST (1)	MN101EF29G <-- PX-FW2	RESET
P01 (23)	TD0 (3)	MN101EF29G <-- PX-FW2	DATA
P02 (24)	TCLK (9)	MN101EF29G <-- PX-FW2	CLOCK
DMOD (21)	OP1 (8)	MN101EF29G <-- PX-FW2	MODE
VDD5	VDD (4)	MN101EF29G <-- PX-FW2	POWER SUPPLY
VSS	GND (2,10)	-	GND

> If a flash programmer other than the Panasonic PX-FW2 is used, the connection pins may differ from those shown in Table:18.5.1

18.5.2　The example of a connection circuit with PX-FW2

If at all possible, all other circuits should be disconnected when the MN101EF29G is connected to the PX-FW2 with this connection circuit. If disconnecting other circuits is difficult, design the connection circuit so that communication is performed reliably by selecting optimal component values based on the instructions in this manual.

Recommended connector: Hirose Electric Co., Ltd., straight type pin header
Product No.: HIF3FC-10PA-2.54DSA
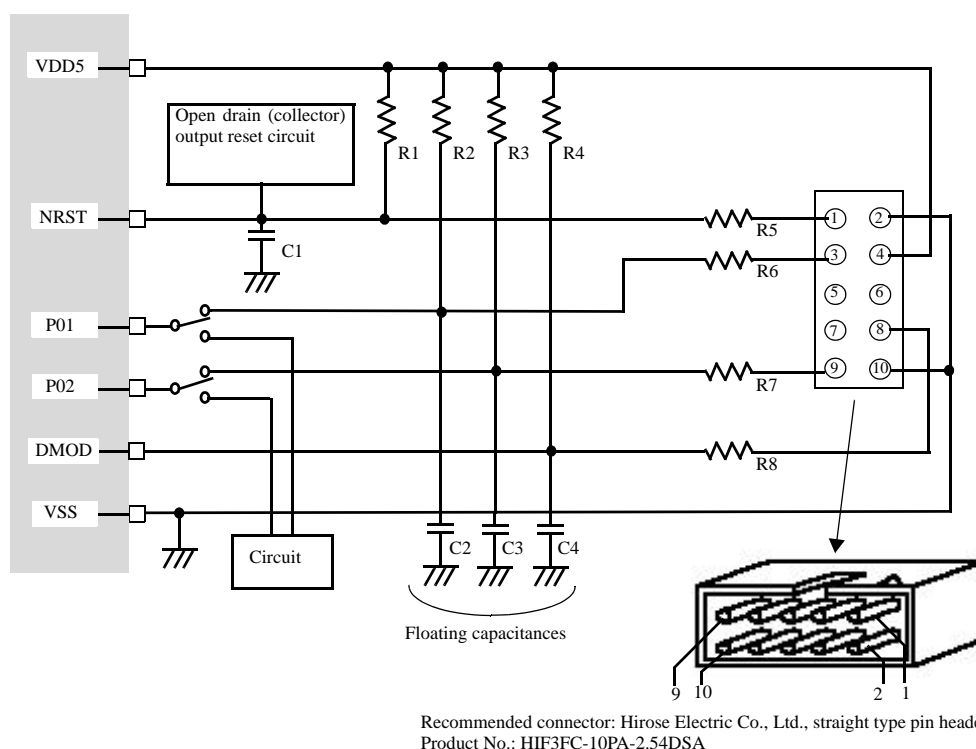
Figure:18.5.1　Sample Connection Circuit Using a 10-Conductor Flat Cable

⚠ Be careful not to mistake the pin numbers on the 10-conductor flat cable connector. The pin numbers on this connector are set up so that, when the connector is viewed from the connection target side with the cutout pointing, the upper right pin is pin 1, and the lower right pin is pin 2. Similarly, the upper left pin is pin 9 and the lower left pin is pin 10.

Use an open collector (or similar) reset circuit, and design the circuit so that signals do not collide.

18.6 Component Value Calculations

This section presents the calculations for each of the components used for connection with the PX-FW2.

18.6.1 Component Values

The table shows the values of the components used in figure 18.5.1.

-The value of the resistor R1 must be greater than RupRst.
-The values of the resistors R2,R3 and R4 must be greater than RupMin and greater than 1 k ohm.
-The value of the resistor R5 must be less than 1/10 that of R1 and less than RsMax.
-The value of the resistor R6 must be less than 1/10 that of R2 and less than RsMax.
-The value of the resistor R7 must be less than 1/10 that of R3 and less than RsMax.
-The value of the resistor R8 must be less than 1/10 that of R4 and less than RsMax.
-C1 must be less than Crst and less than 100 uF.
-C2,C3 and C4 must be under 50 pF.
-Except for the VDD and VSS lines, the line length of the signal from the connector to the microcomputer must be less than 50 cm.

[18.5.2 The example of a connection circuit with PX-FW2]

! This document is written assuming that the clock and data outputs used from the PX-FW2 are the push-pull outputs. The required component values will differ from those shown here if the PX-FW2 open-drain outputs are used.

18.6.2 Reset Signal Capacitor (C1) Maximum Value Calculation

Writing to MN101EF29G, it uses the oscillator stabilization time after the microcomputer resets. The rise time of the reset must beless than 1/3 of the oscillator stabilization time (Twait). The maximum value, C_{rst}, of the reset signal capacitor is determined from the equation (1).

$$C_{rst} = \frac{\text{The oscillator stabilization time}}{3 * \text{ Pull-up resistor R1}} \qquad \text{... Equation (1)}$$

18.6.3 Pull-up Resistor (R1) Minimum Value Calculation

The maximum output current from the PX-FW2 is 12 mA. Since this value is the maximum load current available for outputting a low level, R_{upMin} can be determined from equation (2).

$$R_{upMin} = \frac{\text{Operating supply voltage (VDD)}}{12mA} \quad .... \text{Equation (2)}$$

18.6.4 Relationship Between R_{upRst} and R_{sRt}

If you want to insert a resistor with a large value in series with the reset pin, the pull-up resistor (R_{upRst}) and the series resistor (R_{sRst}) must meet the condition in equation (3) so that the signal level falls all the way to the low level.

$$R_{upRst} * \frac{1}{10} = R_{sRst} \quad ... \text{Equation (3)}$$

18.6.5 Pull-up Resistor (R2, R3 and R4) Minimum Value Calculations

Find the maximum output current, I_{OH}, for the pins used for communication from 1.5.3 "DC Characteristic".
Since that value is the maximum load current available for outputting a high level, R_{upMin} can be determined from equation (4).

$$R_{upMin} = \frac{\text{Operating supply voltage (}V_{DD}\text{)}}{\text{Pin maximum output current (}I_{OH}\text{)}} \quad ... \text{Equation (4)}$$

18.6.6   Communication Pin Series Resistor (R6, R7 and R8) Maximum Value Calculations

If series resistors are inserted in the communication pin lines, the signal transmission speed will be slowed due to the influence of the load capacitors (C2, C3). To assure reliable communication, the time for the signal voltage to change by 63% of the supply voltage (i.e. the time constant) must be held to under 1/8 of the communication period.

If we assume that the load capacitance is 50 pF and the communication frequency is 1 MHz, then the maximum resistor value (R_{sMax}) allowable for reliable communication will be, from equation (5), 2.5 k ohm.

$$R_{sMax} = \frac{1}{8 * \text{Communication frequency (f)} * \text{Load capacitance (C)}} \quad ... \text{Equation (5)}$$
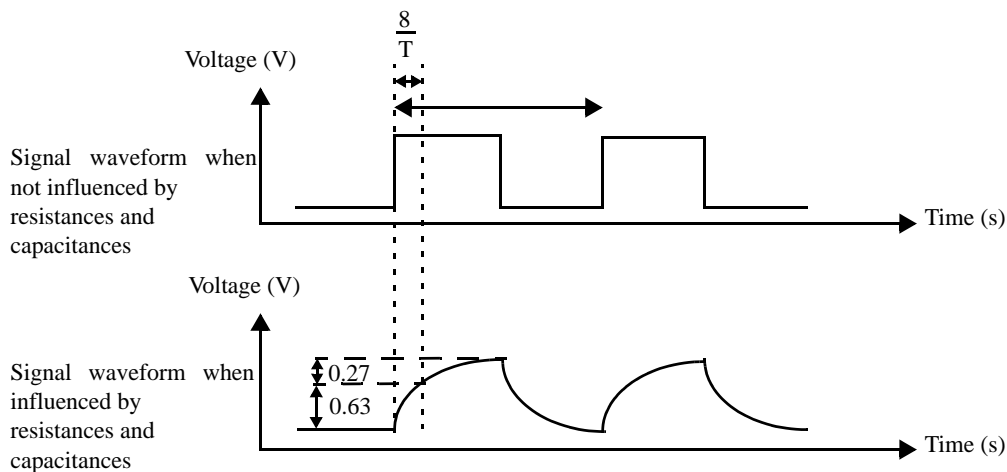
Figure:18.6.1 Relationship Between Communication Frequency, R, and C

When it is used an on board debugger, please make resistance value to classify into series on a communication terminal less than 100 ohm

18.6.7　Relationship Between R_{upMin} and R_{sMax}

It will be possible to insert resistors with large values in series in the communication lines if the communication speed is lowered. However, even in that case, the pull-up resistor (R_{upMin}) and the series resistor (R_{sMax}) must meet the condition in equation (6) so that the signals fall to the low level.

$$R_{upMin} * \frac{1}{10} \geq R_{sMax} \qquad \text{... Equation (6)}$$

18.7 Flash Memory Programming Procedure

This section describes the procedures for onboard serial programming using the PX-FW2.

18.7.1 Overview of the Flash Memory Programming Procedure

This program runs on the microcomputer and is used to control programming the MN101EF29G
on-chip flash EEPROM using the Panasonic PX-FW2.
Using PX-FW2 to opearate on-board serial writing of MN101EF29G, micon program that is called boot program
is not needed.

> ! Using on-board serial writer other than PX-FW2, boot program may be needed

18.7.2 KeyCode

The security method used in the MN101EF29G is the dedicated area storage method (128-bit fixed length).
See the PX-FW2 User's Manual for details on the security functions and the KeyCodes.

18.7.3 Protection Function

The MN101EF29G is supported the protection functions.
See the PX-FW2 User's Manual for details on the protection functions.

18.7.4 Flash Programming Control Program

The programming control program is loaded in RAM in the target microcomputer and implements the flash memory write control algorithm. This program includes functions for erasing flash memory, for writing the user program to flash memory, and for reading out data from flash memory.This program is loaded into RAM from the programmer using serial communication between the PX-FW2 and the boot program.
Note that the file MN101EF29G.exe is included in the additional product information pack. Executing this file registers both MN101EF29G product information and the programming control program with Flash Commander.
Note that the file MN101EF29G.exe is included in the additional product information pack. Executing this file registers both MN101EF29G product information and the programming control program with Flash Commander.

18.8 Boot Area Programming Procedure

This section describes the procedures of onboard serial programming for the boot area using the PX-FW2.

18.8.1 Overview of the Flash Memory Programming Procedure

This program runs on the microcomputer and is used to control programming the MN101EF29G
on-chip flash EEPROM using the Panasonic PX-FW2.
Using PX-FW2 to opearate on-board serial writing of MN101EF29G, micon program that is called boot program
is not needed.

> ⚠ Using on-board serial writer other than PX-FW2, boot program may be needed

18.8.2 KeyCode

The security method used in the MN101EF29G is the dedicated area storage method (128-bit fixed length).
See the PX-FW2 User's Manual for details on the security functions and the KeyCodes.

18.8.3 Protection Function

The MN101EF29G is supported the protection functions.
See the PX-FW2 User's Manual for details on the protection functions.

18.8.4 Flash Programming Control Program

The programming control program is loaded in RAM in the target microcomputer and implements the flash memory write control algorithm. This program includes functions for erasing flash memory, for writing the user program to flash memory, and for reading out data from flash memory.This program is loaded into RAM from the programmer using serial communication between the PX-FW2 and the boot program.
MN101EF29G.exe is attached for the additional product information pack.
Note that the file MN101EF29G.exe for MN101EF29G(Boot) is included in the additional product information pack. Executing this file registers both MN101EF29G(Boot) product information and the programming control program with Flash Commander.

18.9 ROM Programming Service

Panasonic Corporation provides ROM programming service.
This LSI can be produced in which the arbitrary data has been written in advance.
The protect information to prevent writing/erasing errors and the security key code to prevent alteration or leakage of the program can be set.
Request it from our ROM order service.
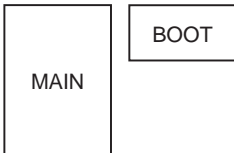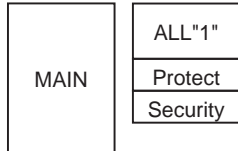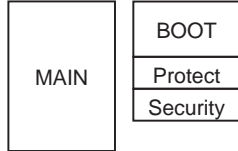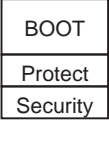
18.9.1 ROM Data Configuration

For your ROM structure, select one among six configurations of ROM data according to your usage.
Table:18.9.1 shows ROM data configuration.

Table:18.9.1 ROM Data Configuration

		BOOT Mode Microcontroller Rewriting Method		
		Unused	Used	
Protect/ Security Function	Unused	Configuration 1 MAIN	Configuration 2 MAIN / BOOT	Configuration 3 BOOT
	Used	Configuration 4 MAIN / ALL"1" Protect Security	Configuration 5 MAIN / BOOT Protect Security	Configuration 6 BOOT Protect Security

MAIN: Data for MAIN area
BOOT: Data for BOOT area
ALL"1": 0xFF padding data
Protect: Protect information
Security: Key code for security

Configuration 1

    BOOT mode microcontroller rewriting method: Unused
    Protect / Security function   : Unused
        Prepare only the data file for MAIN area.
        The size of the data file for MAIN area should be adjusted to less than 132 KB.

Configuration 2, 3

    BOOT mode microcontroller rewriting method: Used
    Protect / Security function   : Unused
        Prepare the data file for MAIN area and the data file for BOOT area. (Configuration 2)
        The size of the data file for MAIN area should be adjusted to less than 132 KB.
        The size of the data file for BOOT area should be adjusted to less than 4 KB.
        Prepare only the data file for BOOT area. (Configuration 3)

Configuration 4

    BOOT mode microcontroller rewriting method: Unused
    Protect / Security function   : Used
        Prepare the data file for MAIN area and the data file for protect / security.
        The size of the data file for MAIN area should be adjusted to less than 132 KB.
        For the data file for protect/security, refer to [Chapter 18 18.9.2 File for Protect / Security].

Configuration 5 and 6

    BOOT mode microcontroller rewriting method: Used
    Protect / Security function   : Used
        Prepare the data file for MAIN area and the data file for BOOT area/ protect/ security. (Configuration 5)
        The size of the data file for MAIN area should be adjusted to less than 132 KB.
        For the data file for BOOT area/ protect/ security, refer to [Chapter 18 18.9.2 File for Protect / Security].
        Prepare only the data file for BOOT area/ protect/ security. (Configuration 6).

18.9.2　File for Protect / Security

When using protect / security function, prepare the data for BOOT area and the data for protect / security with one file. Figure:18.9.1 shows the configuration of the file for protect / security. Figure:18.9.2 shows the protect information.

Figure:18.9.1　File for Protect / Security

Figure:18.9.2　Protect Information

The following description shows precautions for creation of the file for protect / security.

- Compose the file for protect/security of 4 KB + 64 byte.
- When the data for BOOT area is less than 4 KB, perform padding by "0xFF".
- When BOOT mode microcontroller rewriting method is not used, perform padding by "0xFF" to BOOT area.
- When the protect function is not used, set all the data of the protect information to "0xFF".
- When the security function is not used, set all the data of the security key code to "0xFF".
- Even when the protect or the security function is not used, allocate the ID code.

18.9.3   ROM Order Service

For the ROM order service, consult our sales offices.

18.10 Special Function Registers List

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03E30	TM9BCL	TM9BCL7	TM9BCL6	TM9BCL5	TM9BCL4	TM9BCL3	TM9BCL2	TM9BCL1	TM9BCL0	VII-19
		X	X	X	X	X	X	X	X	
		Timer 9 Binary Counter Lower 8 Bit								
0x03E31	TM9BCH	TM9BCH7	TM9BCH6	TM9BCH5	TM9BCH4	TM9BCH3	TM9BCH2	TM9BCH1	TM9BCH0	VII-19
		X	X	X	X	X	X	X	X	
		Timer 9 Binary Counter Upper 8 Bit								
0x03E32	TM9OC1L	TM9OC1L7	TM9OC1L6	TM9OC1L5	TM9OC1L4	TM9OC1L3	TM9OC1L2	TM9OC1L1	TM9OC1L0	VII-17
		X	X	X	X	X	X	X	X	
		Timer 9 Compare Register 1 Lower 8 Bit								
0x03E33	TM9OC1H	TM9OC1H7	TM9OC1H6	TM9OC1H5	TM9OC1H4	TM9OC1H3	TM9OC1H2	TM9OC1H1	TM9OC1H0	VII-17
		X	X	X	X	X	X	X	X	
		Timer 9 Compare Register 1 Upper 8 Bit								
0x03E34	TM9PR1L	TM9PR1L7	TM9PR1L6	TM9PR1L5	TM9PR1L4	TM9PR1L3	TM9PR1L2	TM9PR1L1	TM9PR1L0	VII-18
		X	X	X	X	X	X	X	X	
		Timer 9 Preset Register 1 Lower 8 Bit								
0x03E35	TM9PR1H	TM9PR1H7	TM9PR1H6	TM9PR1H5	TM9PR1H4	TM9PR1H3	TM9PR1H2	TM9PR1H1	TM9PR1H0	VII-18
		X	X	X	X	X	X	X	X	
		Timer 9 Preset Register 1 Upper 8 Bit								
0x03E36	TM9ICL	TM9ICL7	TM9ICL6	TM9ICL5	TM9ICL4	TM9ICL3	TM9ICL2	TM9ICL1	TM9ICL0	VII-19
		X	X	X	X	X	X	X	X	
		Timer 9 Input Capture Lower 8 Bit								
0x03E37	TM9ICH	TM9ICH7	TM9ICH6	TM9ICH5	TM9ICH4	TM9ICH3	TM9ICH2	TM9ICH1	TM9ICH0	VII-19
		X	X	X	X	X	X	X	X	
		Timer 9 Input Capture Upper 8 Bit								
0x03E38	TM9MD1	Reserved	T9ICEDG1	TM9CL	TM9EN	TM9PS1	TM9PS0	TM9CK1	TM9CK0	VII-28
		0	0	1	0	0	0	0	0	
		Always set to "0"	Capture trigger edge selection	Timer output reset signal	Timer count control	Count clock selection		Clock source selection		
0x03E39	TM9MD2	T9ICEDG0	T9PWMSL	TM9BCR	TM9PWM	TM9IRS1	T9ICEN	T9ICT1	T9ICT0	VII-29
		0	0	0	0	0	0	0	0	
		Capture trigger edge selection	PWM mode selection	Timer count clear source selection	Timer output waveform selection	Timer interrupt source selection	Input Capture operation enable selection	Capture trigger selection		
0x03E3A	TM9OC2L	TM9OC2L7	TM9OC2L6	TM9OC2L5	TM9OC2L4	TM9OC2L3	TM9OC2L2	TM9OC2L1	TM9OC2L0	VII-17
		X	X	X	X	X	X	X	X	
		Timer 9 Compare Register 2 Lower 8 Bit								
0x03E3B	TM9OC2H	TM9OC2H7	TM9OC2H6	TM9OC2H5	TM9OC2H4	TM9OC2H3	TM9OC2H2	TM9OC2H1	TM9OCHL0	VII-17
		X	X	X	X	X	X	X	X	
		Timer 9 Compare Register 2 Upper 8 Bit								
0x03E3C	TM9PR2L	TM9PR2L7	TM9PR2L6	TM9PR2L5	TM9PR2L4	TM9PR2L3	TM9PR2L2	TM9PR2L1	TM9PR2L0	VII-18
		X	X	X	X	X	X	X	X	
		Timer 9 Preset Register 2 Lower 8 Bit								
0x03E3D	TM9PR2H	TM9PR2H7	TM9PR2H6	TM9PR2H5	TM9PR2H4	TM9PR2H3	TM9PR2H2	TM9PR2H1	TM9PR2H0	VII-18
		X	X	X	X	X	X	X	X	
		Timer 9 Preset Register 2 Upper 8 Bit								
0x03E3E	TM9MD3	TM9CKSMP	-	-	-	-	-	-	-	VII-30
		0	-	-	-	-	-	-	-	
		Input Capture sampling selection	-	-	-	-	-	-	-	
0x03E42	TMCKSEL1	-	-	-	TM4IOSEL	TM3IOSEL	TM2IOSEL	TM1IOSEL	TM0IOSEL	V-21
		-	-	-	0	0	0	0	0	
		-	-	-	Timer4 input selection	Timer3 input selection	Timer2 input selection	Timer1 input selection	Timer0 input selection	

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03E43	TMCKSEL2	-	-	-	-	-	TM9IOSEL	TM81OSEL	TM07OSEL	VII-31
		-	-	-	-	-	0	0	0	
		-	-	-	-	-	Timer 9 input selection	Timer 8 input selection	Timer 7 input selection	
0x03E44	TMINSEL1	TMINSEL17	TMINSEL16	TMINSEL15	TMINSEL14	TMINSEL13	TMINSEL12	TMINSEL11	TMINSEL10	V-22
		0	0	0	0	0	0	0	0	
		Timer 3 input selection		Timer 2 input selection		Timer 1 input selection		Timer 0 input selection		
0x03E45	TMINSEL2	TMINSEL27	TMINSEL26	TMINSEL25	TMINSEL24	TMINSEL23	TMINSEL22	TMINSEL21	TMINSEL20	V-23, VII-32
		0	0	0	0	0	0	0	0	
		Timer 9 input selection		Timer 8 input selection		Timer 7 input selection		Timer4 input selection		
0x03E70	LC00BUF	LC00BUF7	LC00BUF6	LC00BUF5	LC00BUF4	LC00BUF3	LC00BUF2	LC00BUF1	LC00BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E71	LC01BUF	LC01BUF7	LC01BUF6	LC01BUF5	LC01BUF4	LC01BUF3	LC01BUF2	LC01BUF1	LC01BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E72	LC02BUF	LC02BUF7	LC02BUF6	LC02BUF5	LC02BUF4	LC02BUF3	LC02BUF2	LC02BUF1	LC02BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E73	LC03BUF	LC03BUF7	LC03BUF6	LC03BUF5	LC03BUF4	LC03BUF3	LC03BUF2	LC03BUF1	LC03UF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E74	LC04BUF	LC04BUF7	LC04BUF6	LC04BUF5	LC04BUF4	LC04BUF3	LC04BUF2	LC04BUF1	LC04BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E75	LC05BUF	LC05BUF7	LC05BUF6	LC05BUF5	LC05BUF4	LC05BUF3	LC05BUF2	LC05BUF1	LC05BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E76	LC06BUF	LC06BUF7	LC06BUF6	LC06BUF5	LC06BUF4	LC06BUF3	LC06BUF2	LC06BUF1	LC06BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E77	LC07BUF	LC07BUF7	LC07BUF6	LC07BUF5	LC07BUF4	LC07BUF3	LC07BUF2	LC07BUF1	LC07BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E78	LC08BUF	LC08BUF7	LC08BUF6	LC08BUF5	LC08BUF4	LC08BUF3	LC08BUF2	LC08BUF1	LC08BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E79	LC09BUF	LC09BUF7	LC09BUF6	LC09BUF5	LC09BUF4	LC09BUF3	LC09BUF2	LC09BUF1	LC09BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E7A	LC0ABUF	LC0ABUF7	LC0ABUF6	LC0ABUF5	LC0ABUF4	LC0ABUF3	LC0ABUF2	LC0ABUF1	LC0ABUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E7B	LC0BBUF	LC0BBUF7	LC0BBUF6	LC0BBUF5	LC0BBUF4	LC0BBUF3	LC0BBUF2	LC0BBUF1	LC0BBUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E7C	LC0CBUF	LC0CBUF7	LC0CBUF6	LC0CBUF5	LC0CBUF4	LC0CBUF3	LC0CBUF2	LC0CBUF1	LC0CBUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E7D	LC0DBUF	LC0DBUF7	LC0DBUF6	LC0DBUF5	LC0DBUF4	LC0DBUF3	LC0DBUF2	LC0DBUF1	LC0DBUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E7E	LC0EBUF	LC0EBUF7	LC0EBUF6	LC0EBUF5	LC0EBUF4	LC0EBUF3	LC0EBUF2	LC0EBUF1	LC0EBUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E7F	LC0FBUF	LC0FBUF7	LC0FBUF6	LC0FBUF5	LC0FBUF4	LC0FBUF3	LC0FBUF2	LC0FBUF1	LC0FBUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E80	LC10BUF	LC10BUF7	LC10BUF6	LC10BUF5	LC10BUF4	LC10BUF3	LC10BUF2	LC10BUF1	LC10BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E81	LC11BUF	LC11BUF7	LC11BUF6	LC11BUF5	LC11BUF4	LC11BUF3	LC11BUF2	LC11BUF1	LC11BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03E82	LC12BUF	LC12BUF7	LC12BUF6	LC12BUF5	LC12BUF4	LC12BUF3	LC12BUF2	LC12BUF1	LC12BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E83	LC13BUF	LC13BUF7	LC13BUF6	LC13BUF5	LC13BUF4	LC13BUF3	LC13BUF2	LC13BUF1	LC13BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E84	LC14BUF	LC14BUF7	LC14BUF6	LC14BUF5	LC14BUF4	LC14BUF3	LC14BUF2	LC14BUF1	LC14BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E85	LC15BUF	LC15BUF7	LC15BUF6	LC15BUF5	LC15BUF4	LC15BUF3	LC15BUF2	LC15BUF1	LC15BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E86	LC16BUF	LC16BUF7	LC16BUF6	LC16BUF5	LC16BUF4	LC16BUF3	LC16BUF2	LC16BUF1	LC16BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E87	LC17BUF	LC17BUF7	LC17BUF6	LC17BUF5	LC17BUF4	LC17BUF3	LC17BUF2	LC17BUF1	LC17BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E88	LC18BUF	LC18BUF7	LC18BUF6	LC18BUF5	LC18BUF4	LC18BUF3	LC18BUF2	LC18BUF1	LC18BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E89	LC19BUF	LC19BUF7	LC19BUF6	LC19BUF5	LC19BUF4	LC19BUF3	LC19BUF2	LC19BUF1	LC19BUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E8A	LC1ABUF	LC1ABUF7	LC1ABUF6	LC1ABUF5	LC1ABUF4	LC1ABUF3	LC1ABUF2	LC1ABUF1	LC1ABUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segment output latch data								
0x03E8B	LC1BBUF	LC1BBUF7	LC1BBUF6	LC1BBUF5	LC1BBUF4	LC1BBUF3	LC1BBUF2	LC1BBUF1	LC1BBUF0	XV-20
		X	X	X	X	X	X	X	X	
		Segmentoutput latch data								
0x03E90	LCDMD1	LCDEN	Reserved	LCDTY1	LCDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	XV-7
		0	0	0	0	0	0	0	0	
		LCD driver circuit start flag	Always set to "0"	LCD display duty selection		LCD Clock source selection				
0x03E91	LCDMD2	Reserved	Reserved	Reserved	Reserved	LCRHL	LCREN	Reserved	Reserved	XV-9
		0	0	0	0	0	0	0	0	
		Always set to "0"				Internal partial pressure type selection	Internal partial pressure connect selection	Always set to "0"		
0x03E92	LCDMD3	-	-	-	-	TMSEL3	TMSEL2	TMSEL1	LCDCKSEL	XV-10
		-	-	-	-	0	0	0	0	
		-	-	-	-	Timer0 to 4, A input selection			Oscillation dividing circuit/ selection timer selection	
0x03E93	LCCTR0	COMSL3	COMSL2	COMSL1	COMSL0	Reserved	VLC3SL	VLC2SL	VLC1SL	XV-11
		0	0	0	0	0	0	0	0	
		COM3/ port 87 selection	COM2/ port 86 selection	COM1/ port 85 selection	COM0/ port 84 selection	Always set to "0"	VLC3/ port 92 selection	VLC2/ port 93 selection	VLC1/ port 94 selection	
0x03E94	LCCTR1	LC1SL7	LC1SL6	LC1SL5	LC1SL4	LC1SL3	LC1SL2	LC1SL1	LC1SL0	XV-13
		0	0	0	0	0	0	0	0	
		SEG7/ port 74 selection	SEG6/ port 75 selection	SEG5/ port 76 selection	SEG4/ port 77 selection	SEG3/ port 80 selection	SEG2/ port 81 selection	SEG1/ port 82 selection	SEG0/ port 83 selection	
0x03E95	LCCTR2	LC2SL7	LC2SL6	LC2SL5	LC2SL4	LC2SL3	LC2SL2	LC2SL1	LC2SL0	XV-14
		0	0	0	0	0	0	0	0	
		SEG15/ port 64 selection	SEG14/ port 65 selection	SEG13/ port 66 selection	SEG12/ port 67 selection	SEG11/ port 70 selection	SEG10/ port 71 selection	SEG9/ port 72 selection	SEG8/ port 73 selection	
0x03E96	LCCTR3	LC3SL7	LC3SL6	LC3SL5	LC3SL4	LC3SL3	LC3SL2	LC3SL1	LC3SL0	XV-15
		0	0	0	0	0	0	0	0	
		SEG23/ port 53 selection	SEG22/ port 52 selection	SEG21/ port 51 selection	SEG20/ port 50 selection	SEG19/ port 60 selection	SEG18/ port 61 selection	SEG17/ port 62 selection	SEG16/ port 63 selection	

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03E97	LCCTR4	LC4SL7	LC4SL6	LC4SL5	LC4SL4	LC4SL3	LC4SL2	LC4SL1	LC4SL0	XV-16
		0	0	0	0	0	0	0	0	
		SEG31/ port 44 selection	SEG30/ port 45 selection	SEG29/ port 46 selection	SEG28/ port 47 selection	SEG27/ port 57 selection	SEG26/ port 56 selection	SEG25/ port 55 selection	SEG24/ port 54 selection	
0x03E98	LCCTR5	LC5SL7	LC5SL6	LC5SL5	LC5SL4	LC5SL3	LC5SL2	LC5SL1	LC5SL0	XV-17
		0	0	0	0	0	0	0	0	
		SEG39/ port 33 selection	SEG38/ port 34 selection	SEG37/ port 35 selection	SEG36/ port 36 selection	SEG35/ port 40 selection	SEG34/ port 41 selection	SEG33/ port 42 selection	SEG32/ port 43 selection	
0x03E99	LCCTR6	LC6SL7	LC6SL6	LC6SL5	LC6SL4	LC6SL3	LC6SL2	LC6SL1	LC6SL0	XV-18
		0	0	0	0	0	0	0	0	
		SEG47/ port 12 selection	SEG46/ port 13 selection	SEG45/ port 14 selection	SEG44/ port 15 selection	SEG43/ port 16 selection	SEG42/ port 30 selection	SEG41/ port 31 selection	SEG40/ port 32 selection	
0x03E9A	LCCTR7	-	LC7SL6	LC7SL5	LC7SL4	LC7SL3	LC7SL2	LC7SL1	LC7SL0	XV-19
		-	0	0	0	0	0	0	0	
		-	SEG54/ port 20 selection	SEG53/ port 21 selection	SEG52/ port 22 selection	SEG51/ port 2 3 selection	SEG50/ port 24 selection	SEG49/ port 10 selection	SEG48/ port 11 selection	
0x03EC0	AT0CNT0	FM0DE	AT0ACT	AT0MD3	AT0MD2	AT0MD1	AT0MD0	Reserved	AT0EN	XVI-7
		0	0	0	0	0	0	0	0	
		Increment control flag for memory pointer 0	ATC0 software activation flag	ATC0 data transfer mode				Always set to "0"	ATC0 transfer enable flag	
0x03EC1	AT0CNT1	-	-	Reserved	BTSTP	AT0IR3	AT0IR2	AT0IR1	AT0IR0	XVI-9
		-	-	0	0	0	0	0	0	
		-	-	Always set to "0"	Burst transfer stop enable flag	ATC0 trigger factor setup flag				
0x03EC2	AT0TRC	AT0TRC7	AT0TRC6	AT0TRC5	AT0TRC4	AT0TRC3	AT0TRC2	AT0TRC1	AT0TRC0	XVI-10
		0	0	0	0	0	0	0	0	
		ATC0 data transfer count setup								
0x03EC3	AT0MAP0L	AT0MAP0L7	AT0MAP0L6	AT0MAP0L5	AT0MAP0L4	AT0MAP0L3	AT0MAP0L2	AT0MAP0L1	AT0MAP0L0	XVI-11
		0	0	0	0	0	0	0	0	
		ATC0 Memory Pointer 0 Lower 8 Bit								
0x03EC4	AT0MAP0M	AT0MAP0M7	AT0MAP0M6	AT0MAP0M5	AT0MAP0M4	AT0MAP0M3	AT0MAP0M2	AT0MAP0M1	AT0MAP0M0	XVI-11
		0	0	0	0	0	0	0	0	
		ATC0 Memory Pointer 0 Middle 8 Bit								
0x03EC5	AT0MAP0H	-	-	-	-	AT0MAP0H3	AT0MAP0H2	AT0MAP0H1	AT0MAP0H0	XVI-11
		-	-	-	-	0	0	0	0	
		-	-	-	-	ATC0 Memory Pointer 0 Upper 4Bit				
0x03EC6	AT0MAP1L	AT0MAP1L7	AT0MAP1L6	AT0MAP1L5	AT0MAP1L4	AT0MAP1L3	AT0MAP1L2	AT0MAP1L1	AT0MAP1L0	XVI-12
		0	0	0	0	0	0	0	0	
		ATC0 Memory Pointer 1 Lower 8 Bit								
0x03EC7	AT0MAP1M	AT0MAP1M7	AT0MAP1M6	AT0MAP1M5	AT0MAP1M4	AT0MAP1M3	AT0MAP1M2	AT0MAP1M1	AT0MAP1M0	XVI-12
		0	0	0	0	0	0	0	0	
		ATC0 Memory Pointer 1 Middle 8 Bit								
0x03EC8	AT0MAP1H	-	-	-	-	AT0MAP1H3	AT0MAP1H2	AT0MAP1H1	AT0MAP1H0	XVI-12
		-	-	-	-	0	0	0	0	
		-	-	-	-	ATC0 Memory Pointer 1 Upper 4Bit				
0x03ED0	AT1CNT0	FM0DE	AT1ACT	AT1MD3	AT1MD2	AT1MD1	AT1MD0	Reserved	AT1EN	XVI-7
		0	0	0	0	0	0	0	0	
		Increment control flag for memory pointer 0	ATC1 software activation flag	ATC1 data transfer mode				Always set to "0"	ATC1 transfer enable flag	
0x03ED1	AT1CNT1	AT1IRS	-	Reserved	BTSTP	AT1IR3	AT1IR2	AT1IR1	AT1IR0	XVI-8
		0	-	0	0	0	0	0	0	
		Trigger factor selection flag	-	Always set to "0"	Burst transfer stop enable flag	ATC1Trigger factor setup flag				
0x03ED2	AT1TRC	AT1TRC7	AT1TRC6	AT1TRC5	AT1TRC4	AT1TRC3	AT1TRC2	AT1TRC1	AT1TRC0	XVI-10
		0	0	0	0	0	0	0	0	
		ATC1 data transfer count setup								
0x03ED3	AT1MAP0L	AT1MAP0L7	AT1MAP0L6	AT1MAP0L5	AT1MAP0L4	AT1MAP0L3	AT1MAP0L2	AT1MAP0L1	AT1MAP0L0	XVI-11
		0	0	0	0	0	0	0	0	
		ATC1 Memory Pointer 0 Lower 8 Bit								

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03ED4	AT1MAP0M	AT1MAP0M7	AT1MAP0M6	AT1MAP0M5	AT1MAP0M4	AT1MAP0M3	AT1MAP0M2	AT1MAP0M1	AT1MAP0M0	XVI-11
		0	0	0	0	0	0	0	0	
		ATC1 Memory Pointer 0 Middle 8 Bit								
0x03ED5	AT1MAP0H	-	-	-	-	AT1MAP0H3	AT1MAP0H2	AT1MAP0H1	AT1MAP0H0	XVI-11
		-	-	-	-	0	0	0	0	
		-	-	-	-	ATC1 Memory Pointer 0 Upper 4Bit				
0x03ED6	AT1MAP1L	AT1MAP1L7	AT1MAP1L6	AT1MAP1L5	AT1MAP1L4	AT1MAP1L3	AT1MAP1L2	AT1MAP1L1	AT1MAP1L0	XVI-12
		0	0	0	0	0	0	0	0	
		ATC1 Memory Pointer 1 Lower 8 Bit								
0x03ED7	AT1MAP1M	AT1MAP1M7	AT1MAP1M6	AT1MAP1M5	AT1MAP1M4	AT1MAP1M3	AT1MAP1M2	AT1MAP1M1	AT1MAP1M0	XVI-12
		0	0	0	0	0	0	0	0	
		ATC1 Memory Pointer 1 Middle 8 Bit								
0x03ED8	AT1MAP1H	-	-	-	-	AT1MAP1H3	AT1MAP1H2	AT1MAP1H1	AT1MAP1H0	XVI-12
		-	-	-	-	0	0	0	0	
		-	-	-	-	ATC1 Memory Pointer 1 Upper 4Bit				
0x03EE0	P0OMD	-	-	-	P0OMD4	P0OMD3	P0OMD2	P0OMD1	P0OMD0	IV-11
		-	-	-	0	0	0	0	0	
		-	-	-	P03 special function selection	I/O port TM0IOB/ TM2IOB/ RMOUTB selection	I/O port TM9IOB selection	I/O port TM8IOB selection	I/O port TM7IOB selection	
0x03EE1	P1OMD	-	P1OMD6	P1OMD5	P1OMD4	P1OMD3	P1OMD2	P1OMD1	P1OMD0	IV-27
		-	0	0	0	0	0	0	0	
		-	I/O port timer/ buzzer output selection	I/O port timer/ buzzer output selection	I/O port TM4IOC selection	I/O port TM3IOC selection	I/O port TM1IOC selection	I/O port TM2IOC selection	I/O port TM0IOC/ RMOUTC selection	
0x03EE2	BUZSEL	-	-	-	BUZSEL4	BUZSEL3	BUZSEL2	BUZSEL1	-	IV-29
		-	-	-	0	0	0	0	-	
		-	-	-	Buzzer (Reverse) output selection	Buzzer output selection	Buzzer (Reverse) output selection *Control with P1OMD6	Buzzer output selection *Control with P1OMD5	-	
0x03EE3	P0LED	P0LED7	P0LED6	P0LED5	P0LED4	P0LED3	P0LED2	P0LED1	P0LED0	IV-13
		0	0	0	0	0	0	0	0	
		LED7 (Large current output) selection	LED6 (Large current output) selection	LED5 (Large current output) selection	LED4 (Large current output) selection	LED3 (Large current output) selection	LED2 (Large current output) selection	LED1 (Large current output) selection	LED0 (Large current output) selection	
0x03EE4	P6OMD	-	-	-	P6OMD4	P6OMD3	P6OMD2	-	-	IV-94
		-	-	-	0	0	0	-	-	
		-	-	-	I/O port, TM4IOB selection	I/O port, TM3IOB selection	I/O port, TM1IOB selection	-	-	
0x03EE5	P8OMD1	-	-	P8OMD15	P8OMD14	P8OMD13	P8OMD12	P8OMD11	P8OMD10	IV-124
		-	-	0	0	0	0	0	0	
		-	-	I/O port, timer output selection	I/O port, timer output selection	I/O port, timer output selection	I/O port, timer output selection	I/O port, timer output selection	I/O port, timer output selection	
0x03EE6	PAOMD	PAOMD7	PAOMD6	PAOMD5	PAOMD4	PAOMD3	PAOMD2	PAOMD1	PAOMD0	IV-147
		0	0	0	0	0	0	0	0	
		I/O port, TM9IOA selection	I/O port, TM8IOA selection	I/O port, TM7IOA selection	I/O port, TM4IOA selection	I/O port, TM3IOA selection	I/O port, TM2IOA selection	I/O port, TM1IOA selection	I/O port, TM1IOA/ RMOUTA selection	
0x03EE7	P9OMD	-	-	-	Reserved	-	-	-	-	IV-139
		-	-	-	0	-	-	-	-	
		-	-	-	Always set to "0"	-	-	-	-	
0x03EE8	PAIMD	PAIMD7	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0	IV-148
		0	0	0	0	0	0	0	0	
		I/O port, AN7 analog input selection	I/O port, AN6 analog input selection	I/O port, AN5 analog input selection	I/O port, AN4 analog input selection	I/O port, AN3 analog input selection	I/O port, AN2 analog input selection	I/O port, AN1 analog input selection	I/O port, AN0 analog input selection	

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03EE9	PBIMD	PBIMD7	PBIMD6	PBIMD5	PBIMD4	PBIMD3	PBIMD2	BAIMD1	PBIMD0	IV-162
		0	0	0	0	0	0	0	0	
		I/O port, AN15 analog input selection	I/O port, AN14 analog input selection	I/O port, AN13 analog input selection	I/O port, AN12 analog input selection	I/O port, AN11 analog input selection	I/O port, AN10 analog input selection	I/O port, AN9 analog input selection	I/O port, AN8 analog input selection	
0x03EEA	SCHMIT1	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10	IV-14
		0	0	0	0	0	0	0	0	
		Port 7 Schmit switching	Port 6 Schmit switching	Port 5 Schmit switching	Port 4 Schmit switching	Port 3 Schmit switching	Port 2 Schmit switching	Port 1 Schmit switching	Port 0 Schmit switching	
0x03EEB	NF0CTR	NF0SCK2	NF0SCK1	NF0SCK0	NF0EN1	Reserved	Reserved	Reserved	Reserved	III-56
		0	0	0	0	0	0	0	0	
		IRQ0 noize sampling frequencys			Noize filter ON/OFF control	Always set to "0"				
0x03EEC	NF1CTR	NF1SCK2	NF1SCK1	NF1SCK0	NF1EN1	Reserved	Reserved	Reserved	Reserved	III-56
		0	0	0	0	0	0	0	0	
		IRQ1 noize sampling frequency			Noize filter ON/OFF control	Always set to "0"				
0x03EED	NF2CTR	NF2SCK2	NF2SCK1	NF2SCK0	NF2EN1	Reserved	Reserved	Reserved	Reserved	III-56
		0	0	0	0	0	0	0	0	
		IRQ2 noize sampling frequency			Noize filter ON/OFF control	Always set to "0"				
0x03EEE	NF3CTR	NF3SCK2	NF3SCK1	NF3SCK0	NF3EN1	Reserved	Reserved	Reserved	Reserved	III-56
		0	0	0	0	0	0	0	0	
		IRQ3 noize sampling frequency			Noize filter ON/OFF control	Always set to "0"				
0x03EEF	NF4CTR	NF4SCK2	NF4SCK1	NF4SCK0	NF4EN1	Reserved	Reserved	Reserved	Reserved	III-56
		0	0	0	0	0	0	0	0	
		IRQ4 noize sampling frequency			Noize filter ON/OFF control	Always set to "0"				
0x03EF0	P0ODC	-	P0ODC6	-	P0ODC4	-	P0ODC2	P0ODC1	-	IV-12
		-	0	-	0	-	0	0	-	
		-	Nch open-drain output selection	-	Nch open-drain output selection	-	Nch open-drain output selection	Nch open-drain output selection	-	
0x03EF1	P3ODC	-	-	-	P3ODC4	P3ODC3	P3ODC2	-	P3ODC0	IV-53
		-	-	-	0	0	0	-	0	
		-	-	-	Nch open-drain output selection	Nch open-drain output selection	Nch open-drain output selection		Nch open-drain output selection	
0x03EF2	P4ODC	P4ODC7	P4ODC6	P4ODC5	-	P4ODC3	P4ODC2	-	P4ODC0	IV-67
		0	0	0	-	0	0	-	0	
		Nch open-drain output selection	Nch open-drain output selection	Nch open-drain output selection	-	Nch open-drain output selection	Nch open-drain output selection	-	Nch open-drain output selection	
0x03EF3	P5ODC	-	-	-	-	-	P5ODC2	-	P5ODC0	IV-81
		-	-	-	-	-	0	-	0	
		-	-	-	-	-	Nch open-drain output selection	-	Nch open-drain output selection	
0x03EF4	P6ODC	P6ODC7	P6ODC6	-	-	-	-	-	-	IV-94
		0	0	-	-	-	-	-	-	
		Nch open-drain output selection	Nch open-drain output selection	-	-	-	-	-	-	
0x03EF5	P7ODC	P7ODC7	-	P7ODC5	P7ODC4	P7ODC3	P7ODC2	-	P7ODC0	IV-109
		0	-	0	0	0	0	-	0	
		Nch open-drain output selection	-	Nch open-drain output selection	Nch open-drain output selection	Nch open-drain output selection	Nch open-drain output selection	-	Nch open-drain output selection	
0x03EF6	PACNT	-	-	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0	IV-149
		-	-	0	0	0	0	0	0	
		-	-	PA5 real time control (IRQ0 event)		PA2 real time control (IRQ0 event)		PA0 real time control (IRQ0 event)		
0x03EF7	P8SYO	P8SYO7	P8SYO6	P8SYO5	P8SYO4	P8SYO3	P8SYO2	P8SYO1	P8SYO0	IV-126
		0	0	0	0	0	0	0	0	
		Synchronous output selection								
0x03EF8	P8SEV	-	-	-	-	-	-	P8SEV1	P8SEV0	IV-127
		-	-	-	-	-	-	0	0	
		-	-	-	-	-	-	Synchronous output event selection		

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03EFA	SCHMIT2	-	-	-	-	SCHMIT2B	SCHMIT2A	SCHMIT29	SCHMIT28	IV-127
		-	-	-	-	0	0	0	0	
		-	-	-	-	Port B Schmit level switching	Port A Schmit level switching	Port 9 Schmit level switching	Pport 8 Schmit level switching	
0x03EFB	P8CNT1	P8CNT17	P8CNT16	P8CNT15	P8CNT14	P8CNT13	P8CNT12	P8CNT11	P8CNT10	IV-125
		0	0	0	0	0	0	0	0	
		P83 real time control (IRQ0 event)		P82 real time control (IRQ0 event)		P81 real time control (IRQ0 event)		P80 real time control (IRQ0 event)		
0x03EFC	P8CNT2	-	-	-	-	P8CNT23	P8CNT22	P8CNT21	P8CNT20	IV-126
		-	-	-	-	0	0	0	0	
		-	-	-	-	P85 real time control (IRQ0 event)		P84 real time control (IRQ0 event)		
0x03F00	CPUM	Reserved	OSCSEL1	OSCSEL0	OSCDBL	STOP	HALT	OSC1	OSC0	II-45, II-51
		0	0	0	0	0	0	0	0	
		Always set to "0"	Division ratio		Internal system clock(fs)	Operation mode control				
0x03F01	MEMCTR	IOW1	IOW0	IVBM	EXMEM	EXWH	IRWE	EXW1	EXW0	II-36
		1	1	0	0	1	0	1	1	
		Wait cycles when accessing special register area		Base address specification for interrupt vector table	External memory expansion mode	External memory fixed wait cycle mode/ handshake mode switching	Software write setup for the interrupt request flag	Fixed wait cycles setup		
0x03F02	WDCTR	-	-	Reserved	Reserved	Reserved	WDTS1	WDTS0	WDEN	X-5
		-	-	0	0	0	1	1	0	
		-	-	Always set to "0"			Runaway detect cycles setup		Watchdog Timer enable	
0x03F03	DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-	II-60, X-6
		0	0	0	0	0	0	-	-	
		Output selection	Buzzer output frequency selection			Oscillation stabilization wait selection		-	-	
0x03F06	ACTMD	Reserved	Reserved	WTHLD1	WTHLD0	Reserved	Reserved	RDHLD1	RDHLD0	XVII-4
		0	0	0	0	0	0	0	0	
		Always set to "0"		2-bit field to specify hold time at write		Always set to "0"		2-bit field to specify hold time at read		
0x03F07	AUCTR	-	-	-	-	-	AUDIVU	AUMUL	AUMULU	II-70
		-	-	-	-	-	0	0	0	
		-	-	-	-	-	Unsigned division execution	Signed multiplication execution	Unsigned multiplication execution	
0x03F0A	SBNKR	-	-	-	-	SBA3	SBA2	SBA1	SBA0	II-22
		-	-	-	-	0	0	0	0	
		-	-	-	-	Bank for source address selection				
0x03F0B	DBNKR	-	-	-	-	DBA3	DBA2	DBA1	DBA0	II-23
		-	-	-	-	0	0	0	0	
		-	-	-	-	Bank for destination address selection				
0x03F10	P0OUT	P0OUT7	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0	IV-9
		X	X	X	X	X	X	X	X	
		Output data								
0x03F11	P1OUT	-	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	IV-25
		-	X	X	X	X	X	X	X	
		-	Output data							
0x03F12	P2OUT	P2OUT7	-	-	P2OUT4	P2OUT3	P2OUT2	P2OUT1	P2OUT0	IV-39
		1	-	-	X	X	X	X	X	
		Output data	-	-	Output data					
0x03F13	P3OUT	-	P3OUT6	P3OUT5	P3OUT4	P3OUT3	P3OUT2	P3OUT1	P3OUT0	IV-51
		-	X	X	X	X	X	X	X	
		-	Output data							
0x03F14	P4OUT	P4OUT7	P4OUT6	P4OUT5	P4OUT4	P4OUT3	P4OUT2	P4OUT1	P4OUT0	IV-65
		X	X	X	X	X	X	X	X	
		Output data								
0x03F15	P5OUT	P5OUT7	P5OUT6	P5OUT5	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0	IV-79
		X	X	X	X	X	X	X	X	
		Output data								
0x03F16	P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	IV-92
		X	X	X	X	X	X	X	X	
		Output data								

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F17	P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	IV-107
		X	X	X	X	X	X	X	X	
		Output data								
0x03F18	P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	IV-122
		X	X	X	X	X	X	X	X	
		Output data								
0x03F19	P9OUT	-	P9OUT6	P9OUT5	P9OUT4	P9OUT3	P9OUT2	P9OUT1	P9OUT0	IV-137
		-	X	X	X	X	X	X	X	
		-	Output data							
0x03F1A	PAOUT	PAOUT7	PAOUT6	PAOUT5	PAOUT4	PAOUT3	PAOUT2	PAOUT1	PAOUT0	IV-145
		X	X	X	X	X	X	X	X	
		Output data								
0x03F1B	PBOUT	PBOUT7	PBOUT6	PBOUT5	PBOUT4	PBOUT3	PBOUT2	PBOUT1	PBOUT0	IV-160
		X	X	X	X	X	X	X	X	
		Output data								
0x03F1D	EXADV	EXADV3	EXADV2	EXADV1	-	-	-	-	-	II-38
		0	0	0	-	-	-	-	-	
		"A19 to 16" address output enable during memory expansion mode.	"A15 to 12" address output enable during memory expansion mode	"A11 to 8" address output enable during memory expansion mode.	-	-	-	-	-	
0x03F1E	EDGDT	EDGSEL7	-	EDGSEL3	-	EDGSEL2	EDGSEL1	-	EDGSEL0	III-58
		0	-	0	-	0	0	-	0	
		IRQ5 Key interrupt both edges operation selection	-	IRQ4 both edge interrupt operation setup	-	IRQ3 both edge interrupt operation setup	IRQ2 both edge interrupt operation setup	-	External interrupt 5 enable selection	
0x03F1F	LVLMD	-	-	EXLVL4	LVLEN4	EXLVL43	LVLEN3	EXLVL2	LVLEN2	III-60
		-	-	0	0	0	0	0	0	
		-	-	External interrupt 4 enable input level setup	External interrupt 4 enable input setup	External interrupt 3 enable input level setup	External interrupt 3 enable input setup	External interrupt 2 enable input level setup	External interrupt 2 enable input setup	
0x03F20	P0IN	P0IN7	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0	IV-10
		X	X	X	X	X	X	X	X	
		Input data								
0x03F21	P1IN	-	P1IN	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	IV-26
		-	X	X	X	X	X	X	X	
		-	Input data							
0x03F22	P2IN	-	-	-	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0	IV-40
		-	-	-	X	X	X	X	X	
		-	-	-	Input data					
0x03F23	P3IN	-	P3IN6	P3IN5	P3IN4	P3IN3	P3IN2	P3IN1	P3IN0	IV-52
		-	X	X	X	X	X	X	X	
		-	Input data							
0x03F24	P4IN	P4IN7	P4IN6	P4IN5	P4IN4	P4IN3	P4IN2	P4IN1	P4IN0	IV-65
		X	X	X	X	X	X	X	X	
		Port 4 input data								
0x03F25	P5IN	P5IN7	P5IN6	P5IN5	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0	IV-80
		X	X	X	X	X	X	X	X	
		Port 5 input data								
0x03F26	P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	IV-93
		X	X	X	X	X	X	X	X	
		Port 6 input data								
0x03F27	P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	IV-107
		X	X	X	X	X	X	X	X	
		Port 7 input data								
0x03F28	P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	IV-123
		X	X	X	X	X	X	X	X	
		Port 8 input data								
0x03F29	P9IN	-	P9IN6	P9IN5	P9IN4	P9IN3	P9IN2	P9IN1	P9IN0	IV-138
		-	X	X	X	X	X	X	X	
		-	Port 9 input data							

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F2A	PAIN	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	IV-146
		X	X	X	X	X	X	X	X	
		Port A input data								
0x03F2B	PBIN	PBIN7	PBIN6	PBIN5	PBIN4	PBIN3	PBIN2	PBIN1	PBIN0	IV-160
		X	X	X	X	X	X	X	X	
		Port B input data								
0x03F2E	ACZCTR	P21IM	-	-	-	P20IM	-	-	-	III-57
		0	-	-	-	0	-	-	-	
		IRQ1 ACZ input enable	-	-	-	IRQ0 ACZ input enable	-	-	-	
0x03F2F	XSEL	-	-	XSEL	-	-	ROMHND	Reserved	Reserved	II-54
		-	-	0	-	-	0	0	0	
		-	-	Port/Slow oscillation selection	-	-	Built-in ROM area access selection	Always set to "0"		
0x03F30	P0DIR	P0DIR7	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0	IV-10
		0	0	0	0	0	0	0	0	
		Port 0 input/output direction control								
0x03F31	P1DIR	-	P1DIR6	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	IV-26
		-	0	0	0	0	0	0	0	
		-	Port 1 input/output direction control							
0x03F32	P2DIR	-	-	-	P2DIR4	P2DIR3	P2DIR2	P2DIR1	P2DIR0	IV-40
		-	-	-	0	0	0	0	0	
		-	-	-	Port 2 input/output direction control					
0x03F33	P3DIR	-	P3DIR6	P3DIR5	P3DIR4	P3DIR3	P3DIR2	P3DIR1	P3DIR0	IV-52
		-	0	0	0	0	0	0	0	
		-	Port 3 input/output direction control							
0x03F34	P4DIR	P4DIR7	P4DIR6	P4DIR5	P4DIR4	P4DIR3	P4DIR2	P4DIR1	P4DIR0	IV-66
		0	0	0	0	0	0	0	0	
		Port 4 input/output direction control								
0x03F35	P5DIR	P5DIR7	P5DIR6	P5DIR5	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0	IV-80
		0	0	0	0	0	0	0	0	
		Port 5 input/output direction control								
0x03F36	P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	IV-93
		0	0	0	0	0	0	0	0	
		Port 6 input/output direction control								
0x03F37	P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	IV-108
		0	0	0	0	0	0	0	0	
		Port 7 input/output direction control								
0x03F38	P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	IV-123
		0	0	0	0	0	0	0	0	
		Port 8 input/output direction control								
0x03F39	P9DIR	-	P9DIR6	P9DIR5	P9DIR4	P9DIR3	P9DIR2	P9DIR1	P9DIR0	IV-138
		-	0	0	0	0	0	0	0	
		-	Port 9 input/output direction control							
0x03F3A	PADIR	PADIR7	PADIR6	PADIR5	PADIR4	PADIR3	PADIR2	PADIR1	PADIR0	IV-146
		0	0	0	0	0	0	0	0	
		Port A input/output direction control								
0x03F3B	PBDIR	PBDIR7	PBDIR6	PBDIR5	PBDIR4	PBDIR3	PBDIR2	PBDIR1	PBDIR0	IV-161
		0	0	0	0	0	0	0	0	
		Port B input/output direction control								
0x03F3D	IRQCNT	-	-	-	P24EN	P23EN	P22EN	P21EN	P20EN	III-55
		-	-	-	0	0	0	0	0	
		-	-	-	External interrupt enable					
0x03F3E	KEYT3_1IMD	KEYT3SEL	-	-	-	KEYT3_1EN3	KEYT3_1EN2	KEYT3_1EN1	KEYT3_1EN0	III-61
		0	-	-	-	0	0	0	0	
		Interrupt source selection	-	-	-	KEY3 interrupt selection	KEY2 interrupt selection	KEY1 interrupt selection	KEY0 interrupt selection	
0x03F3F	KEYT3_2IMD	-	-	-	-	KEYT3_2EN3	KEYT3_2EN2	KEYT3_2EN1	KEYT3_2EN0	III-62
		-	-	-	-	0	0	0	0	
		-	-	-	-	KEY7 interrupt selection	KEY6 interrupt selection	KEY5 interrupt selection	KEY4 interrupt selection	

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F40	P0PLUD	P0PLUD7	P0PLUD6	P0PLUD5	P0PLUD4	P0PLUD3	P0PLUD2	P0PLUD1	P0PLUD0	IV-10
		0	0	0	0	0	0	0	0	
		Port 0 pull-up/pull-down resistor selection								
0x03F41	P1PLUD	-	P1PLUD6	P1PLUD5	P1PLUD4	P1PLUD3	P1PLUD2	P1PLUD1	P1PLUD0	IV-26
		-	0	0	0	0	0	0	0	
		-	Port 1 pull-up/pull-down resistor selection							
0x03F42	P2PLUD	-	-	-	P2PLUD4	P2PLUD3	P2PLUD2	P2PLUD1	P2PLUD0	IV-40
		-	-	-	0	0	0	0	0	
		-	-	-	Port 2 pull-up/pull-down resistor selection					
0x03F43	P3PLUD	-	P3PLUD6	P3PLUD5	P3PLUD4	P3PLUD3	P3PLUD2	P3PLUD1	P3PLUD0	IV-52
		-	0	0	0	0	0	0	0	
		-	Port 3 pull-up/pull-down resistor selection							
0x03F44	P4PLUD	P4PLUD7	P4PLUD6	P4PLUD5	P4PLUD4	P4PLUD3	P4PLUD2	P4PLUD1	P4PLUD0	IV-66
		0	0	0	0	0	0	0	0	
		Port 4 pull-up/pull-down resistor selection								
0x03F45	P5PLUD	P5PLUD7	P5PLUD6	P5PLUD5	P5PLUD4	P5PLUD3	P5PLUD2	P5PLUD1	P5PLUD0	IV-80
		0	0	0	0	0	0	0	0	
		Port 5 pull-up/pull-down resistor selection								
0x03F46	P6PLUD	P6PLUD7	P6PLUD6	P6PLUD5	P6PLUD4	P6PLUD3	P6PLUD2	P6PLUD1	P6PLUD0	IV-93
		0	0	0	0	0	0	0	0	
		Port 6 pull-up/pull-down resistor selection								
0x03F47	P7PLUD	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0	IV-109
		0	0	0	0	0	0	0	0	
		Port 7 pull-up/pull-down resistor selection								
0x03F48	P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	IV-123
		0	0	0	0	0	0	0	0	
		Port 8 pull-up resistor selection								
0x03F49	P9PLU	-	P9PLU6	P9PLU5	P9PLU4	P9PLU3	P9PLU2	P9PLU1	P9PLU0	IV-138
		-	0	0	0	0	0	0	0	
		-	Port 9 pull-up resistor selection							
0x03F4A	PAPLU	PAPLU7	PAPLU6	PAPLU5	PAPLU4	PAPLU3	PAPLU2	PAPLU1	PAPLU0	IV-146
		0	0	0	0	0	0	0	0	
		Port A pull-up resistor selection								
0x03F4B	PBPLU	PBPLU7	PBPLU6	PBPLU5	PBPLU4	PBPLU3	PBPLU2	PBPLU1	PBPLU0	IV-161
		0	0	0	0	0	0	0	0	
		Port B pull-up resistor selection								
0x03F4C	SELUD	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0	IV-15
		0	0	0	0	0	0	0	0	
		Pull-up/down selection								
0x03F4E	IRQEXPEN	Reserved	IRQEXPEN6	IRQEXPEN5	IRQEXPEN4	IRQEXPEN3	IRQEXPEN2	IRQEXPEN1	IRQEXPEN0	III-42
		0	0	0	0	0	0	0	0	
		Always set to "0"	ATC1 interrupt enable	ATC0 interrupt enable	Serial5 interrupt enable	Serial4 stop condition interrupt enable	Serial3 UART reception interrupt enable	Serial1 UART reception interrupt enable	Serial0 UART reception interrupt enable	
0x03F4F	IRQEXPDT	Reserved	IRQEXPDT6	IRQEXPDT5	IRQEXPDT4	IRQEXPDT3	IRQEXPDT2	IRQEXPDT1	IRQEXPDT0	III-43
		0	0	0	0	0	0	0	0	
		Always set to "0"	ATC1 interrupt request	ATC0 interrupt request	Serial5 interrupt request	Serial4 stop condition interruptrequest	Serial3 UART reception interrupt request	Serial1 UART reception interrupt request	Serial0 UART reception interrupt request	
0x03F50	TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	V-15
		0	0	0	0	0	0	0	0	
		Timer 0 Binary Counter								
0x03F51	TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	V-15
		0	0	0	0	0	0	0	0	
		Timer 1 Binary Counter								
0x03F52	TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	V-13
		X	X	X	X	X	X	X	X	
		Timer 0 Compare Register								
0x03F53	TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	V-13
		X	X	X	X	X	X	X	X	
		Timer 1 Compare Register								

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F54	TM0MD	-	TM0POP	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0	V-16
		-	0	0	0	0	0	0	0	
		-	Output signal start polarity selection	Pulse width measurement control	Timer0 operation mode selection	Timer0 count control	Clock source selection			
0x03F55	TM1MD	Reserved	Reserved	TM1CAS1	TM1CAS0	TM1EN	TM1CK2	TM1CK1	TM1CK0	V-17
		0	0	0	0	0	0	0	0	
		Always set to "0"		Timer1 operation mode selection		Timer 1 count control	Clock source selection			
0x03F56	CK0MD	-	TM0ADD1	TM0ADD0	TM0ADDEN	TM0PSC2	TM0PSC1	TM0PSC0	TM0BAS	V-10
		-	0	0	0	0	0	0	0	
		-	Position of additional pulses		Additional pulses PWM output control	Clock source selection				
0x03F57	CK1MD	-	-	-	-	TM1PSC2	TM1PSC1	TM1PSC0	TM1BAS	V-11
		-	-	-	-	0	0	0	0	
						Clock source selection				
0x03F58	TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	V-15
		0	0	0	0	0	0	0	0	
		Timer 2 Binary Counter								
0x03F59	TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	V-15
		0	0	0	0	0	0	0	0	
		Timer 3 Binary Counter								
0x03F5A	TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	V-13
		X	X	X	X	X	X	X	X	
		Timer 2 Compare Register								
0x03F5B	TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	V-13
		X	X	X	X	X	X	X	X	
		Timer 3 Compare Register								
0x03F5C	TM2MD	-	TM2POP	TM2MOD	TM2PWM	TM2EN	TM2CK2	TM2CK1	TM2CK0	V-18
		-	0	0	0	0	0	0	0	
		-	Output signal start polarity selection	Pulse width measurement control	Timer 2 operation mode selection	Timer 2 count control	Clock source selection			
0x03F5D	TM3MD	-	-	-	TM3CAS	TM3EN	TM3CK2	TM3CK1	TM3CK0	V-19
		-	-	-	0	0	0	0	0	
		-	-	-	Timer 3 operation mode selection	Timer 3 count control	Clock source selection			
0x03F5E	CK2MD	-	TM2ADD1	TM2ADD0	TM2ADDEN	TM2PSC2	TM2PSC1	TM2PSC0	TM2BAS	V-11
		-	0	0	0	0	0	0	0	
		-	Positions of additional pulses		Additional pulses PWM output control	Clock source selection				
0x03F5F	CK3MD	-	-	-	-	TM3PSC2	TM3PSC1	TM3PSC0	TM3BAS	V-12
		-	-	-	-	0	0	0	0	
		-	-	-	-	Clock source selection				
0x03F60	TM4BC	TM4BC7	TM4BC6	TM4BC5	TM4BC4	TM4BC3	TM4BC2	TM4BC1	TM4BC0	V-15
		0	0	0	0	0	0	0	0	
		Timer 4 Binary Counter								
0x03F61	TMABC	TMABC7	TMABC6	TMABC5	TMABC4	TMABC3	TMABC2	TMABC1	TMABC0	VI-5
		0	0	0	0	0	0	0	0	
		Timer A Binary Counter								
0x03F62	TM4OC	TM4OC7	TM4OC6	TM4OC5	TM4OC4	TM4OC3	TM4OC2	TM4OC1	TM4OC0	V-14
		X	X	X	X	X	X	X	X	
		Timer 4 Compare Register								
0x03F63	TMAOC	TMAOC7	TMAOC6	TMAOC5	TMAOC4	TMAOC3	TMAOC2	TMAOC1	TMAOC0	VI-5
		X	X	X	X	X	X	X	X	
		Timer A Compare Register								
0x03F64	TM4MD	-	TM4POP	TM4MOD	TM4PWM	TM4EN	TM4CK2	TM4CK1	TM4CK0	V-20
		-	0	0	0	0	0	0	0	
		-	Output signal start polarity selection	Pulse width measurement control	Timer 4 operation mode selection	Timer 4 count control	Clock source selection			

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x03F65	TMAMD1	-	-	-	-	TMAEN	TMACK2	TMACK1	TMACK0	VI-6
		-	-	-	-	0	0	0	0	
		-	-	-	-	TimerA count control	Prescaler operation control			
0x03F66	CK4MD	-	TM4ADD1	TM4ADD0	TM4ADDEN	TM4PSC2	TM4PSC1	TM4PSC0	TM4BAS	V-12
		-	0	0	0	0	0	0	0	
		-	Positions of additional pulses		Additional pulses PWM output control	Clock source selection				
0x03F67	TMAMD2	Reserved	PSCEN	-	-	-	-	-	-	VI-7
		0	0	-	-	-	-	-	-	
		Always set to "0"	Timer A count control	-	-	-	-	-	-	
0x03F68	TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	VIII-5
		0	0	0	0	0	0	0	0	
		Timer 6 Binary Counter								
0x03F69	TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	VIII-5
		X	X	X	X	X	X	X	X	
		Timer 6 Compare Register								
0x03F6A	TM6MD	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0	VIII-7
		0	0	0	0	0	0	0	0	
		Timer6 binary counter clear selection	Time base timer interrupt cycle selection			Timer6 Clock source selection			Time base timer Clock source selection	
0x03F6B	TBCLR	TMBCLR7	TMBCLR6	TMBCLR5	TMBCLR4	TMBCLR3	TMBCLR2	TMBCLR1	TMBCLR0	VIII-5
		-	-	-	-	-	-	-	-	
		Time base timer clear control Register								
0x03F6C	TM6BEN	-	-	-	-	-	Reserved	TBEN	TM6EN	VIII-6
		-	-	-	-	-	0	0	0	
		-	-	-	-	-	Always set to "0"	Time base timer operation control	Timer 6 operation control	
0x03F6D	RMCTR	TM0RMC	TM0RMB	Reserved	TM0RMA	RM0EN	RMDTY1	RMDTY0	RMBTMS	IX-5
		0	0	0	0	0	0	0	0	
		P10 special function output selection	P03 special function output selection	Always set to "0"	PA0 special function output selection	Remote control carrier output enable	Remote control carrier duty selection		Remote control carrier base timer selection	
0x03F6E	TM7MD4	Reserved	T7IGBTSFT	T7IGBTCNT	T7ONESHOT	T7NODED	-	T7ICT2	T7CAPCLR	VII-23
		0	0	0	0	0	-	0	0	
		Always set to "0"	IGBT software startup	When IGBT is disable, BC operation	One shot pulse selection	Dead time selection	-	Capture trigger selection	BC clear at capture	
0x03F6F	TM8MD4	Reserved	Reserved	Reserved	TM8SEL_C	TM8SEL_B	TM8SEL_A	T8ICT2	T8CAPCLR	VII-27
		0	0	0	0	0	0	0	0	
		Always set to "0"			C port Timer 8/IGBT selection	B port Timer 8/IGBT selection	A port Timer 8/IGBT selection	Capture trigger selection	BC clear at Capture	
0x03F70	TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	VII-12
		0	0	0	0	0	0	0	0	
		Timer 7 Binary Counter Lower 8 Bit								
0x03F71	TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	VII-12
		0	0	0	0	0	0	0	0	
		Timer 7 Binary Counter Upper 8 Bit								
0x03F72	TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 1 Lower 8 Bit								
0x03F73	TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 1 Upper 8 Bit								
0x03F74	TM7PR1L	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 1 Lower 8 Bit								
0x03F75	TM7PR1H	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 1 Upper 8 Bit								

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F76	TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 7 Input Capture Register Lower 8 Bit								
0x03F77	TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 7 Input Capture Register Upper 8 Bit								
0x03F78	TM7MD1	Reserved	T7ICEDG1	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0	VII-20
		0	0	1	0	0	0	0	0	
		Always set to "0"	Capture trigger edge selection	Timer output reset signal	Timer count control	Count clock selection		Clock source selection		
0x03F79	TM7MD2	T7ICEDG0	TM7PWMSL	TM7BCR	TM7PWM	TM7IRS1	T7ICEN	T7ICT1	T7ICT0	VII-21
		0	0	0	0	0	0	0	0	
		Capture trigger edge selection	PWM mode selection	Timer 7 count clear source selection	Timer output waveform selection	Timer 7 interrupt source selection	Input Capture operation enable selection	Capture trigger selection		
0x03F7A	TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 2 Lower 8 Bit								
0x03F7B	TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 2 Upper 8 Bit								
0x03F7C	TM7PR2L	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 2 Lower 8 Bit								
0x03F7D	TM7PR2H	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 2 Upper 8 Bit								
0x03F7E	TM7DPR1	TM7DPR17	TM7DPR16	TM7DPR15	TM7DPR14	TM7DPR13	TM7DPR12	TM7DPR11	TM7DPR10	VII-13
		X	X	X	X	X	X	X	X	
		Timer 7 Dead time Preset Register 1								
0x03F7F	TM7DPR2	TM7DPR27	TM7DPR26	TM7DPR25	TM7DPR24	TM7DPR23	TM7DPR22	TM7DPR21	TM7DPR20	VII-13
		X	X	X	X	X	X	X	X	
		Timer 7 Dead time Preset Register 2								
0x03F80	TM8BCL	TM8BCL7	TM8BCL6	TM8BCL5	TM8BCL4	TM8BCL3	TM8BCL2	TM8BCL1	TM8BCL0	VII-16
		X	X	X	X	X	X	X	X	
		Timer 8 Binary Counter Lower 8 Bit								
0x03F81	TM8BCH	TM8BCH7	TM8BCH6	TM8BCH5	TM8BCH4	TM8BCH3	TM8BCH2	TM8BCH1	TM8BCH0	VII-16
		X	X	X	X	X	X	X	X	
		Timer 8 Binary Counter Upper 8 Bit								
0x03F82	TM8OC1L	TM8OC1L7	TM8OC1L6	TM8OC1L5	TM8OC1L4	TM8OC1L3	TM8OC1L2	TM8OC1L1	TM8OC1L0	VII-14
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 1 Lower 8 Bit								
0x03F83	TM8OC1H	TM8OC1H7	TM8OC1H6	TM8OC1H5	TM8OC1H4	TM8OC1H3	TM8OC1H2	TM8OC1H1	TM8OC1H0	VII-14
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 1 Upper 8 Bit								
0x03F84	TM8PR1L	TM8PR1L7	TM8PR1L6	TM8PR1L5	TM8PR1L4	TM8PR1L3	TM8PR1L2	TM8PR1L1	TM8PR1L0	VII-15
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 1 Lower 8 Bit								
0x03F85	TM8PR1H	TM8PR1H7	TM8PR1H6	TM8PR1H5	TM8PR1H4	TM8PR1H3	TM8PR1H2	TM8PR1H1	TM8PR1H0	VII-15
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 1 Upper 8 Bit								
0x03F86	TM8ICL	TM8ICL7	TM8ICL6	TM8ICL5	TM8ICL4	TM8ICL3	TM8ICL2	TM8ICL1	TM8ICL0	VII-16
		X	X	X	X	X	X	X	X	
		Timer 8 Input Capture Register Lower 8 Bit								
0x03F87	TM8ICH	TM8ICH7	TM8ICH6	TM8ICH5	TM8ICH4	TM8ICH3	TM8ICH2	TM8ICH1	TM8ICH0	VII-16
		X	X	X	X	X	X	X	X	
		Timer 8 Input Capture Register Upper 8 Bit								
0x03F88	TM8MD1	Reserved	T8ICEDG1	TM8CL	TM8EN	TM8PS1	TM8PS0	TM8CK1	TM8CK0	VII-24
		0	0	1	0	0	0	0	0	
		Always set to "0"	Capture trigger edge selection	Timer output reset signal	Timer count control	Count clock selection		Clock source selection		

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F89	TM8MD2	T8ICEDG0	TM8PWMSL	TM8BCR	TM8PWM	TM8IRS1	T8ICEN	T8ICT1	T8ICT0	VII-25
		0	0	0	0	0	0	0	0	
		Capture trigger edge selection	PWM mode selection	Timer 8 count clear source selection	Timer output waveform selection	Timer 8 interrupt source selection	Input Capture operation enable selection	Capture trigger selection		
0x03F8A	TM8OC2L	TM8OC2L7	TM8OC2L6	TM8OC2L5	TM8OC2L4	TM8OC2L3	TM8OC2L2	TM8OC2L1	TM8OC2L0	VII-17
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 2 Lower 8 Bit								
0x03F8B	TM8OC2H	TM8OC2H7	TM8OC2H6	TM8OC2H5	TM8OC2H4	TM8OC2H3	TM8OC2H2	TM8OC2H1	TM8OC2H0	VII-17
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 2 Upper 8 Bit								
0x03F8C	TM8PR2L	TM8PR2L7	TM8PR2L6	TM8PR2L5	TM8PR2L4	TM8PR2L3	TM8PR2L2	TM8PR2L1	TM8PR2L0	VII-18
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 2 Lower 8 Bit								
0x03F8D	TM8PR2H	TM8PR2H7	TM8PR2H6	TM8PR2H5	TM8PR2H4	TM8PR2H3	TM8PR2H2	TM8PR2H1	TM8PR2H0	VII-18
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 2 Upper 8 Bit								
0x03F8E	TM7MD3	TM7CKSMP	TM7BUFSEL	TM7CKEDG	TM7IGBTTR	T7IGBTDT	T7IGBTEN	T7IGBT1	T7IGBT0	VII-22
		0	0	0	0	0	0	0	0	
		Capture sampling selection	Buffer selection	TM7I0 count edge selection	IGBT trigger level selection	IGBT dead time insert timeing	IGBT operation enable	IGBT/Timer trigger factor selection capture		
0x03F8F	TM8MD3	TM8CKSMP	TM8BUFSEL	-	TM8CKEDG	-	TM8PWMF	TM8PWMO	TM8CAS	VII-26
		0	0	-	0	-	0	0	0	
		Capture sampling selection	Buffer selection	-	TM8I0 count edge selection	-	PWM output control when timer 8 is stopped	Timer 8PWM output polarity selection	Cascade selection	
0x03F90	SC0SEL	SBO0SEL	SC0BRP2	SC0BRP1	SC0BRP0	OSL0	SC0SEL2	SC0SEL1	SC0SEL0	XII-17
		0	0	0	0	0	0	0	0	
		UART reverse output selection	Timer clock output selection			Serial output port selection	Timer selection			
0x03F91	SC0MD0	SC0CE1	-	-	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0	XII-24
		0	-	-	0	0	1	1	1	
		Transmission/ reception data input/output edge	-	-	Transfer bit specification	Start condition selection	Synchronous serial transfer bit count selection			
0x03F92	SC0MD1	SC0IOM	SC0SBTS	SC0SBIS	SC0SBOS	SC0CKM	SC0MST	SC0DIV	SC0CMD	XII-25
		0	0	0	0	0	0	0	0	
		Serial data input pin selection	SBT0 pin function selection	Serial input control selection	SBO0 (TXD0) pin function selection	Transfer clock devide selection	Clock master slave selection	Transfer clock devide selection	Synchronous Serial /duplex UART selection	
0x03F93	SC0MD2	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	-	SC0BRKF	SC0BRKE	XII-27
		0	0	0	0	0	-	0	0	
		Frame mode specification		Additional bit specification		Parity enable	-	Break status reception monitor	Break status transmit control	
0x03F94	SC0MD3	SC0FDC1	SC0FDC0	-	-	SC0PSCE	SC0PSC2	SC0PSC1	SC0PSC0	XII-28
		0	0	-	-	0	0	0	0	
		Output selection after SBO0 final data is transmitted		-	-	Prescaler count control	Selection clock			
0x03F95	SC0STR	SC0TBSY	SC0RBSY	SC0TEMP	SC0REMP	SC0FEF	SC0PEK	SC0ORE	SC0ERE	XII-29
		0	0	0	0	0	0	0	0	
		Serial bus transmission status	Serial bus reception status	transmission buffer empry	Reception buffer empry	Frame error detection	Parity error detection	Overrun error detection	Error monitor flag	
0x03F96	RXBUF0	RXBUF07	RXBUF06	RXBUF05	RXBUF04	RXBUF03	RXBUF02	RXBUF01	RXBUF00	XII-23
		X	X	X	X	X	X	X	X	
		Serial interface 0 reception data buffer								
0x03F97	TXBUF0	TXBUF07	TXBUF06	TXBUF05	TXBUF04	TXBUF03	TXBUF02	TXBUF01	TXBUF00	XII-23
		X	X	X	X	X	X	X	X	
		Serial interface 0 transmission data buffer								

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03F98	SC3SEL	SBO3SEL	SC3BRP2	SC3BRP1	SC3BRP0	OSL3	SC3SEL2	SC3SEL1	SC3SEL0	XII-20
		0	0	0	0	-	-	0	0	
		UART reverse output selection	Timer clock output selection			Serial output port selection	Timer selection			
0x03F99	SC1MD0	SC1CE1	-	-	SC1DIR	SC1STE	SC1LNG2	SC1LNG1	SC1LNG0	XII-24
		0	-	-	0	0	1	1	1	
		Transmission/ reception data input/output edge	-	-	Transfer bit specification	Start condition selection	Synchronous serial transfer bit count selection			
0x03F9A	SC1MD1	SC1IOM	SC1SBTS	SC1SBIS	SC1SBOS	SC1CKM	SC1MST	SC1DIV	SC1CMD	XII-25
		0	0	0	0	0	0	0	0	
		Serial data input selection	SBT1 pin function selection	Serial input control selection	SBO1(TXD1) pin function selection	Transfer clock divide selection	Clock master slave selection	Transfer clock devide selection	Synchronous serial /duplexUART selection	
0x03F9B	SC1MD2	SC1FM1	SC1FM0	SC1PM1	SC1PM0	SC1NPE	-	SC1BRKF	SC1BRKE	XII-27
		0	0	0	0	0	-	0	0	
		Frame mode specification		Additional bit specification		Parity enable	-	Break status reception monitor	Break status transmit control	
0x03F9C	SC1MD3	SC1FDC1	SC1FDC0	-	-	SC1PSCE	SC1PSC2	SC1PSC1	SC1PSC0	XII-28
		0	0	-	-	0	0	0	0	
		Output selection after SBO1 final data is transmitted		-	-	Prescaler count control	Selection clock			
0x03F9D	SC1STR	SC1TBSY	SC1RBSY	SC1TEMP	SC1REMP	SC1FEF	SC1PEK	SC1ORE	SC1ERE	XII-29
		0	0	0	0	0	0	0	0	
		Serial bus transmission status	Serial bus reception status	Transmission buffer empry	Reception buffer empry	Frame error detection	Parity error detection	Overrun error detection	Error monitor flag	
0x03F9E	RXBUF1	RXBUF17	RXBUF16	RXBUF15	RXBUF14	RXBUF13	RXBUF12	RXBUF11	RXBUF10	XII-23
		X	X	X	X	X	X	X	X	
		Serial interface 1 reception data buffer								
0x03F9F	TXBUF1	TXBUF17	TXBUF16	TXBUF15	TXBUF14	TXBUF13	TXBUF12	TXBUF11	TXBUF10	XII-23
		X	X	X	X	X	X	X	X	
		Serial interface 1 transmission data buffer								
0x03FA0	SC1SEL	SBO1SEL	SC1BRP2	SC1BRP1	SC1BRP0	OSL1	SC1SEL2	SC1SEL1	SC1SEL0	XII-18
		0	0	0	0	-	-	0	0	
		UART reverse output selection	Timer clock output selection			Serial output port selection	Timer selection			
0x03FA1	SC2MD0	SC2CE1	-	-	SC2DIR	SC2STE	SC2LNG2	SC2LNG1	SC2LNG0	XII-24
		0	-	-	0	0	1	1	1	
		Transmission/ reception data input/output edge	-	-	Transfer bit specification	Start condition selection	Synchronous serial transfer bit count selection			
0x03FA2	SC2MD1	SC2IOM	SC2SBTS	SC2SBIS	SC2SBOS	SC2CKM	SC2MST	SC2DIV	SC2CMD	XII-25
		0	0	0	0	0	0	0	0	
		Serial data input selection	SBT2 pin function selection	Serial input control selection	SBO2(TXD2) pin function selection	transfer clock divide selection	Clock master slave selection	Transfer clock devide selection	Synchronous serial / duplex UART selection	
0x03FA3	SC2MD2	SC2FM1	SC2FM0	SC2PM1	SC2PM0	SC2NPE	-	SC2BRKF	SC2BRKE	XII-27
		0	0	0	0	0	-	0	0	
		Frame mode specification		Additional bit specification		Parity enable	-	Break status reception monitor	Break status transmit control	
0x03FA4	SC2MD3	SC2FDC1	SC2FDC0	-	-	SC2PSCE	SC2PSC2	SC2PSC1	SC2PSC0	XII-28
		0	0	-	-	0	0	0	0	
		Output selection after SBO2 final data transmmision		-	-	Prescaler count control	Selection clock			
0x03FA5	SC2STR	SC2TBSY	SC2RBSY	SC2TEMP	SC2REMP	SC2FEF	SC2PEK	SC2ORE	SC2ERE	XII-29
		0	0	0	0	0	0	0	0	
		Serial bus transmission status	Serial bus reception status	Transmission buffer empry	Reception buffer empry	Frame error detection	Parity error detection	Overrun error detection	Error monitor flag	
0x03FA6	RXBUF2	RXBUF27	RXBUF26	RXBUF25	RXBUF24	RXBUF23	RXBUF22	RXBUF21	RXBUF20	XII-23
		X	X	X	X	X	X	X	X	
		Serial interface 2 reception data buffer								

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x03FA7	TXBUF2	TXBUF27	TXBUF26	TXBUF25	TXBUF24	TXBUF23	TXBUF22	TXBUF21	TXBUF20	XII-23
		X	X	X	X	X	X	X	X	
		Serial interface 2 transmission data buffer								
0x03FA8	SC4SEL	Reserved	SC4BRP2	SC4BRP1	SC4BRP0	OSL4	SC4SEL2	SC4SEL1	SC4SEL0	XII-21
		0	0	0	0	0	-	0	0	
		Always set to "0"	Timer clock output selection			Serial output port selection	Timer selection			
0x03FA9	SC3MD0	SC3CE1	-	-	SC3DIR	SC3STE	SC3LNG2	SC3LNG1	SC3LNG0	XII-24
		0	-	-	0	0	1	1	1	
		Transmission/ reception data input/output edge	-	-	Transfer bit specification	Start condition selection	Synchronous serial transfer bit count selection			
0x03FAA	SC3MD1	SC3IOM	SC3SBTS	SC3SBIS	SC3SBOS	SC3CKM	SC3MST	SC3DIV	SC3CMD	XII-25
		0	0	0	0	0	0	0	0	
		Serial data input pin selection	SBT3 pin function selection	Serial input control selection	SBO3(TXD3) pin function selection	Transfer clock divide selection	Clock master slave selection	Transfer clock divide value selection	Synchronous serial /duplex UART selection	
0x03FAB	SC3MD2	SC3FM1	SC3FM0	SC3PM1	SC3PM0	SC3NPE	-	SC3BRKF	SC3BRKE	XII-27
		0	0	0	0	0	-	0	0	
		Frame mode specification		Additional bit specification		Parity enable	-	Break status reception monitor	Break status transmit control	
0x03FAC	SC3MD3	SC3FDC1	SC3FDC0	-	-	SC3PSCE	SC3PSC2	SC3PSC1	SC3PSC0	XII-28
		0	0	-	-	0	0	0	0	
		Output selection after SBO3 final data transmit		-	-	Prescaler count control	Selection clock			
0x03FAD	SC3STR	SC3TBSY	SC3RBSY	SC3TEMP	SC3REMP	SC3FEF	SC3PEK	SC3ORE	SC3ERE	XII-29
		0	0	0	0	0	0	0	0	
		Serial bus transmission status	Serial bus reception status	Transmission buffer empry	Reception buffer empry	Frame error detection	Parity error detection	Overrun error detection	Error monitor flag	
0x03FAE	RXBUF3	RXBUF37	RXBUF36	RXBUF35	RXBUF34	RXBUF33	RXBUF32	RXBUF31	RXBUF30	XII-23
		x	x	x	x	x	x	x	x	
		Serial interface 3 reception data buffer								
0x03FAF	TXBUF3	TXBUF37	TXBUF36	TXBUF35	TXBUF34	TXBUF33	TXBUF32	TXBUF31	TXBUF30	XII-23
		x	x	x	x	x	x	x	x	
		Serial interface 3 transmission data buffer								
0x03FB0	SC4MD0	SC4CE1	-	-	SC4DIR	SC4STE	SC4LNG2	SC4LNG1	SC4LNG0	XII-31
		0	-	-	0	0	1	1	1	
		Transmission/ reception data input/output input/output edge	-	-	Transfer bit specification	Start condition selection	Transfer bit count			
0x03FB1	SC4MD1	SC4IOM	SC4SBTS	SC4SBIS	SC4SBOS	-	SC4MST	-	-	XII-32
		0	0	0	0	-	0	-	-	
		Serial data input pin selection	SBT4 pin function selection	Serial input control selection	SB04(SDA4) pin function selection	-	Clock master / slave selection	-	-	
0x03FB2	SC4MD2	SC4FDC1	SC4FDC0	-	-	SC4PSCE	SC4PSC2	SC4PSC1	SC4PSC0	XII-33
		0	0	-	-	0	0	0	0	
		Output selectionafter SB04 final data transmission		-	-	Prescaler count control	Selection clock			
0x03FB3	SC4MD3	Reserved	Reserved	SC4STPC	SC4TMD	SC4REX	SC4CMD	SC4ACKS	SC4ACK0	XII-34
		0	0	0	0	0	0	0	0	
		Always set to "0"		Stop condition generation flag in IIC com- munication	Communication mode selection in IIC communication	Transmission/ reception mode selection in IIC master communication	Synchronous serial/IIC selection	ACK bit enable	ACK bit selection at Transmission/ reception mode	
0x03FB4	SC4AD0	SC4AD7	SC4AD6	SC4AD5	SC4AD4	SC4AD3	SC4AD2	SC4AD1	Reserved	XII-35
		0	0	0	0	0	0	0	0	
		Serial interface 4 address setup Register 0								

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x03FB6	SC4STR0	SC4BSY	-	SC4TEMP	SC4REMP	-	-	-	SC4ORE	XII-36
		0	-	0	0	-	-	-	0	
		Clock synchronous communication serial bus status	-	Transmission buffer empty flag	Reception buffer empty flag	-	-	-	Overrun error detection	
0x03FB7	SC4STR1	SC4WSR	SC4ABT_LST	SC4ADD_ACC	SC4STRT	SC4BUSBSY	SC4IICBSY	SC4GCALL	SC4DATA_ERR	XII-37
		0	0	0	0	0	0	0	0	
		Data transfer direction determine flag in slave communication	Arbitration lost detection flag	Slave address compare flag	Start condition detection flag	Bus busy flag	Serial bus status in IIC communication	General call detection flag	Communication abnormal detection flag	
0x03FB8	RXBUF4	RXBUF47	RXBUF46	RXBUF45	RXBUF44	RXBUF43	RXBUF42	RXBUF41	RXBUF40	XII-30
		x	x	x	x	x	x	x	x	
		Serial interface 4 reception data buffer								
0x03FB9	TXBUF4	TXBUF47	TXBUF46	TXBUF45	TXBUF44	TXBUF43	TXBUF42	TXBUF41	TXBUF40	XII-30
		x	x	x	x	x	x	x	x	
		Serial interface 4 transmission data buffer								
0x03FBA	SC5AD0	I2CAD7	I2CAD6	I2CAD5	I2CAD4	I2CAD3	I2CAD2	I2CAD1	I2CAD0	XII-40
		0	0	0	0	0	0	0	0	
		Serial interface 5 address setup Register0								
0x03FBB	SC5AD1	SELI2C	I2CMON	-	-	I2CGEM	I2CADM	I2CAD9	I2CAD8	XII-40
		0	0	-	-	0	0	0	0	
		Reset control	Monitor mode selection	-	-	Communication mode selection	Address mode selection	Address setup		
0x03FBC	SC5RXB	I2CRXB7	I2CRXB6	I2CRXB5	I2CRXB4	I2CRXB3	I2CRXB2	I2CRXB1	I2CRXB0	XII-39
		0	0	0	0	0	0	0	0	
		Serial interface 5 reception data buffer								
0x03FBD	SC5TXB	I2CTXB7	I2CTXB6	I2CTXB5	I2CTXB4	I2CTXB3	I2CTXB2	I2CTXB1	I2CTXB0	XII-39
		0	0	0	0	0	0	0	0	
		Serial interface 5 transmission data buffer								
0x03FBE	SC5STR	WRS	I2CINT	STRT	RSTRT	I2CBSY	SLVBSY	ACKVALID	-	XII-41
		1	0	0	0	0	0	0	-	
		Data transfer direction determine flag at communication	Interrupt detection flag	Start condition detection flag	Restart condition detection flag	Bus busy flag	Slave busy flag	ACK detection flag	-	
0x03FBF	SC2SEL	SBO2_SEL	SC2BRP2	SC2BRP1	SC2BRP0	OSL2	SC2SEL2	SC2SEL1	SC2SEL0	XII-19
		0	0	0	0	0	0	0	0	
		UART reverse output selection	Timer clock output selection			Serial output port selection	Timer selection			
0x03FC0	RCAPL	RCAPL7	RCAPL6	RCAPL5	RCAPL4	RCAPL3	RCAPL2	RCAPL1	RCAPL0	II-30
		0	0	0	0	0	0	0	0	
		ROM correction address Lower 8 Bit								
0x03FC1	RCAPM	RCAPM7	RCAPM6	RCAPM5	RCAPM4	RCAPM3	RCAPM2	RCAPM1	RCAPM0	II-30
		0	0	0	0	0	0	0	0	
		ROM correction address Middle 8 Bit								
0x03FC2	RCAPH	-	-	-	-	RCAPH3	RCAPH2	RCAPH1	RCAPH0	II-30
		-	-	-	-	0	0	0	0	
		-	-	-	-	ROM correction address Upper 4 Bit				
0x03FC3	RCPSR	-	-	-	-	Reserved	RCPSR2	RCPSR1	RCPSR0	II-28
		-	-	-	-	0	0	0	0	
		-	-	-	-	Always set to "0"	ROM correction pointer specification			
0x03FC4	RCCTR0	Reserved	RC6EN	RC5EN	RC4EN	RC3EN	RC2EN	RC1EN	RC0EN	II-29
		0	0	0	0	0	0	0	0	
		Always set to "0"	The 6th address ROM correction control	The 5th address ROM correction control	The 4th address ROM correction control	The 3rd address ROM correction control	The 2nd address ROM correction control	The 1st address ROM correction control	The 0th address ROM correction control	
0x03FC6	SC5SEL	Reserved	Reserved	Reserved	Reserved	OSL5	Reserved	Reserved	Reserved	XII-22
		0	0	0	0	0	0	0	0	
		Always set to "0"				Serial output port selection	Always set to "0""			

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03FC8	FMDREG1	Reserved	Reserved	Reserved	-	Reserved	Reserved	Reserved	DATA	XVIII-11
		0	0	0	-	1	1	0	0	
		Always set to "0"			-	Always set to "1"		Always set to "0"	Rewritable area selection	
0x03FC9	FBEWER	BEW7	BEW6	BEW5	BEW4	BEW3	BEW2	BEW1	BEW0	XVIII-10
		0	0	0	0	0	0	0	0	
		On-board rewriting enable								
0x03FCA	FSKPBPER	SEW7	SEW6	SEW5	SEW4	SEW3	SEW2	SEW1	SEW0	XVIII-11
		0	0	0	0	0	0	0	0	
		Sector Protect/Security command enable								
0x03FD1	ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	ANCK2	-	-	XIII-7
		0	0	0	0	0	0	-	-	
		Sample-hold time		A/D conversion clock		A/D ladder resistance control	A/D conversion clock	-	-	
0x03FD2	ANCTR1	-	-	-	-	ANCHS3	ANCHS2	ANCHS1	ANCHS0	XIII-7
		-	-	-	-	0	0	0	0	
		-	-	-	-	Analogue input channel				
0x03FD3	ANCTR2	ANST	ANSTSEL1	ANSTSEL0	-	-	-	-	-	XIII-8
		0	0	0	-	-	-	-	-	
		A/D conversion status	A/D conversion Start source selection		-	-	-	-	-	
0x03FD4	ANBUF0	ANBUF07	ANBUF06	-	-	-	-	-	-	XIII-9
		X	X	-	-	-	-	-	-	
		Conversion data strage buffer		-	-	-	-	-	-	
0x03FD5	ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	XIII-9
		X	X	X	X	X	X	X	X	
		Conversion data strage buffer								
0x03FD6	DACTR	DACHS1	DACHS0	DACKS1	DACKS0	DACMD2	DACMD1	DACMD0	DABUSY	XIV-5
		X	X	X	X	X	X	X	0	
		Channel monitor flag during D/A conversion		D/A scan clock		D/A conversion mode selection			D/A conversion operation enable flag	
0x03FD7	DADR0	DA0BUF7	DA0BUF6	DA0BUF5	DA0BUF4	DA0BUF3	DA0BUF2	DA0BUF1	DA0BUF0	XIV-6
		X	X	X	X	X	X	X	X	
		D/A conversion input data register 0								
0x03FD8	DADR1	DA1BUF7	DA1BUF6	DA1BUF5	DA1BUF4	DA1BUF3	DA1BUF2	DA1BUF1	DA1BUF0	XIV-6
		X	X	X	X	X	X	X	X	
		D/A conversion input data register 1								
0x03FD9	DADR2	DA2BUF7	DA2BUF6	DA2BUF5	DA2BUF4	DA2BUF3	DA2BUF2	DA2BUF1	DA2BUF0	XIV-6
		X	X	X	X	X	X	X	X	
		D/A conversion input data data Register 2								
0x03FDA	DADR3	DA3BUF7	DA3BUF6	DA3BUF5	DA3BUF4	DA3BUF3	DA3BUF2	DA3BUF1	DA3BUF0	XIV-6
		X	X	X	X	X	X	X	X	
		D/A conversion input data Register 3								
0x03FDF	PLLCNT	PLLCK3	PLLCK2	PLLCK1	PLLCK0	-	-	PLLEN	PLLSTART	II-59
		0	0	0	0	-	-	0	0	
		Multiply number specification				-	-	PLL clock enable	PLL operation control	
0x03FE1	NMICR	-	-	-	-	-	IRQNPG	IRQNWDG	Reserved	III-24
		-	-	-	-	-	0	0	0	
		-	-	-	-	-	Program Interrupt request flag	Watchdog Interrupt request flag	Always set to "0"	
0x03FE2	IRQ0ICR	IRQ0LV1	IRQ0LV0	REDG0	-	-	-	IRQ0IE	IRQ0IR	III-25
		0	0	0	-	-	-	0	0	
		Interrupt level specification flag		Interrupt enable edge specification flag	-			External Interrupt enable flag	External Interrupt request flag	
0x03FE3	IRQ1ICR	IRQ1LV1	IRQ1LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR	III-25
		0	0	0	-	-	-	0	0	
		Interrupt level specification flag		Interrupt enable edge specification Ãþ³	-			External Interrupt enable flag	External Interrupt request flag	

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03FE4	IRQ2ICR	IRQ2LV1	IRQ2LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR	III-25
		0	0	0	-	-	-	0	0	
		Interrupt level specification flag		Interrupt enable edge specification flag	-	-	-	External Interrupt enable flag	External Interrupt request flag	
0x03FE5	IRQ3ICR	IRQ3LV1	IRQ3LV0	REDG3	-	-	-	IRQ3IE	IRQ3IR	III-25
		0	0	0	-	-	-	0	0	
		Interrupt level specification flag		Interrupt enable edge specification flag	-	-	-	External Interrupt enable flag	External Interrupt request flag	
0x03FE6	IRQ4ICR	IRQ4LV1	IRQ4LV0	REDG4	-	-	-	IRQ4IE	IRQ4IR	III-25
		0	0	0	-	-	-	0	0	
		Interrupt level specification flag		Interrupt enable edge specification flag	-	-	-	External Interrupt enable flag	External Interrupt request flag	
0x03FE7	IRQ5ICR	IRQ5LV1	IRQ5LV0	REDG5	-	-	-	IRQ5IE	IRQ5IR	III-25
		0	0	0	-	-	-	0	0	
		Interrupt level specification flag		Interrupt enable edge specification flag	-	-	-	External Interrupt enable flag	External Interrupt request flag	
0x03FE8	TM0ICR	TM0LV1	TM0LV0	-	-	-	-	TM0IE	TM0IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FE9	TM1ICR	TM1LV1	TM1LV0	-	-	-	-	TM1IE	TM1IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FEA	TM2ICR	TM2LV1	TM2LV0	-	-	-	-	TM2IE	TM2IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FEB	TM3ICR	TM3LV1	TM3LV0	-	-	-	-	TM3IE	TM3IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FEC	TM4ICR	TM4LV1	TM4LV0	-	-	-	-	TM4IE	TM4IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FED	TM6ICR	TM6LV1	TM6LV0	-	-	-	-	TM6IE	TM6IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FEE	TBICR	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR	III-27
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FEF	TM7ICR	TM7LV1	TM7LV0	-	-	-	-	TM7IE	TM7IR	III-28
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF0	TM7OC2ICR	TM7OC2LV1	TM7OC2LV0	-	-	-	-	TM7OC2IE	TM7OC2IR	III-29
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF1	TM8ICR	TM8LV1	TM8LV0	-	-	-	-	TM8IE	TM8IR	III-30
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF2	TM8OC2ICR	TM8OC2LV1	TM8OC2LV0	-	-	-	-	TM8OC2IE	TM8OC2IR	III-31
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	

Address	Register	Bit Symbol								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x03FF3	TM9ICR	TM9LV1	TM9LV0	-	-	-	-	TM9IE	TM9IR	III-32
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF4	TM9OC2ICR	TM9OC2LV1	TM9OC2LV0	-	-	-	-	TM9OC2IE	TM9OC2IR	III-33
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF7	SC0TICR	SC0TLV1	SC0TLV0	-	-	-	-	SC0TIE	SC0TIR	III-35
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF8	SC1TICR	SC1TLV1	SC1TLV0	-	-	-	-	SC1TIE	SC1TIR	III-35
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FF9	SC2RICR	SC2RLV1	SC2RLV0	-	-	-	-	SC2RIE	SC2RIR	III-36
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FFA	SC2TICR	SC2TLV1	SC2TLV0	-	-	-	-	SC2TIE	SC2TIR	III-37
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FFB	SC3TICR	SC3TLV1	SC3TLV0	-	-	-	-	SC3TIE	SC3TIR	III-38
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FFC	SC4ICR	SC4LV1	SC4LV0	-	-	-	-	SC4IE	SC4IR	III-39
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FFD	ADICR	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR	III-40
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	
0x03FFE	PERIICR	PERILV1	PERILV0	-	-	-	-	PERIIE	PERIIR	III-41
		0	0	-	-	-	-	0	0	
		Interrupt level specification flag		-	-	-	-	Interrupt enable flag	Interrupt request flag	

18.11 Instruction Set

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Ext.	1	2	3	4	5	6	7	8	9	10	11	Notes
			— Flag								— Machine Code											

Data Move Instructions

Group	Mnemonic	Operation	VF	NF	CF	ZF	Size	Cycle	Repeat	Ext.	Machine Code	Notes
MOV	MOV Dn,Dm	Dn→Dm	--	--	--	--	2	1			1010 DnDm	
	MOV imm8,Dm	imm8→Dm	--	--	--	--	4	2			1010 DmDm <#8. ...>	
	MOV Dn,PSW	Dn→PSW	●	●	●	●	3	3			0010 1001 01Dn	
	MOV PSW,Dm	PSW→Dm	--	--	--	--	3	2			0010 0001 01Dm	
	MOV (An),Dm	mem8(An)→Dm	--	--	--	--	2	2			0100 1ADm	
	MOV (d8,An),Dm	mem8(d8+An)→Dm	--	--	--	--	4	2			0110 1ADm <d8. ...>	*1
	MOV (d16,An),Dm	mem8(d16+An)→Dm	--	--	--	--	7	4			0010 0110 1ADm <d16 ....>	
	MOV (d4,SP),Dm	mem8(d4+SP)→Dm	--	--	--	--	3	2			0110 01Dm <d4>	*2
	MOV (d8,SP),Dm	mem8(d8+SP)→Dm	--	--	--	--	5	3			0010 0110 01Dm <d8. ...>	*3
	MOV (d16,SP),Dm	mem8(d16+SP)→Dm	--	--	--	--	7	4			0010 0110 00Dm <d16 ....>	
	MOV (io8),Dm	mem8(IOTOP+io8)→Dm	--	--	--	--	4	2			0110 00Dm <io8 ...>	
	MOV (abs8),Dm	mem8(abs8)→Dm	--	--	--	--	4	2			0100 01Dm <abs 8..>	
	MOV (abs12),Dm	mem8(abs12)→Dm	--	--	--	--	5	2			0100 00Dm <abs 12.. ...>	
	MOV (abs16),Dm	mem8(abs16)→Dm	--	--	--	--	7	4			0010 1100 00Dm <abs 16.. ....>	
	MOV Dn,(Am)	Dn→mem8(Am)	--	--	--	--	2	2			0101 1aDn	
	MOV Dn,(d8,Am)	Dn→mem8(d8+Am)	--	--	--	--	4	2			0111 1aDn <d8. ...>	*1
	MOV Dn,(d16,Am)	Dn→mem8(d16+Am)	--	--	--	--	7	4			0010 0111 1aDn <d16 ....>	
	MOV Dn,(d4,SP)	Dn→mem8(d4+SP)	--	--	--	--	3	2			0111 01Dn <d4>	*2
	MOV Dn,(d8,SP)	Dn→mem8(d8+SP)	--	--	--	--	5	3			0010 0111 01Dn <d8. ...>	*3
	MOV Dn,(d16,SP)	Dn→mem8(d16+SP)	--	--	--	--	7	4			0010 0111 00Dn <d16 ....>	
	MOV Dn,(io8)	Dn→mem8(IOTOP+io8)	--	--	--	--	4	2			0111 00Dn <io8 ...>	
	MOV Dn,(abs8)	Dn→mem8(abs8)	--	--	--	--	4	2			0101 01Dn <abs 8..>	
	MOV Dn,(abs12)	Dn→mem8(abs12)	--	--	--	--	5	2			0101 00Dn <abs 12.. ...>	
	MOV Dn,(abs16)	Dn→mem8(abs16)	--	--	--	--	7	4			0010 1101 00Dn <abs 16.. ....>	
	MOV imm8,(io8)	imm8→mem8(IOTOP+io8)	--	--	--	--	6	3			0000 0010 <io8 ...> <#8. ...>	
	MOV imm8,(abs8)	imm8→mem8(abs8)	--	--	--	--	6	3			0001 0100 <abs 8..> <#8. ...>	
	MOV imm8,(abs12)	imm8→mem8(abs12)	--	--	--	--	7	3			0001 0101 <abs 12.. ...> <#8. ...>	
	MOV imm8,(abs16)	imm8→mem8(abs16)	--	--	--	--	9	5			0011 1101 1001 <abs 16.. ....> <#8. ...>	
	MOV Dn,(HA)	Dn→mem8(HA)	--	--	--	--	2	2			1101 00Dn	
MOVW	MOVW (An),DWm	mem16(An)→DWm	--	--	--	--	2	3			1110 00Ad	
	MOVW (An),Am	mem16(An)→Am	--	--	--	--	3	4			0010 1110 10Aa	*4
	MOVW (d4,SP),DWm	mem16(d4+SP)→DWm	--	--	--	--	3	3			1110 011d <d4>	*2
	MOVW (d4,SP),Am	mem16(d4+SP)→Am	--	--	--	--	3	3			1110 010a <d4>	*2
	MOVW (d8,SP),DWm	mem16(d8+SP)→DWm	--	--	--	--	5	4			0010 1110 011d <d8. ...>	*3
	MOVW (d8,SP),Am	mem16(d8+SP)→Am	--	--	--	--	5	4			0010 1110 010a <d8. ...>	*3
	MOVW (d16,SP),DWm	mem16(d16+SP)→DWm	--	--	--	--	7	5			0010 1110 001d <d16 ....>	
	MOVW (d16,SP),Am	mem16(d16+SP)→Am	--	--	--	--	7	5			0010 1110 000a <d16 ....>	
	MOVW (abs8),DWm	mem16(abs8)→DWm	--	--	--	--	4	3			1100 011d <abs 8..>	
	MOVW (abs8),Am	mem16(abs8)→Am	--	--	--	--	4	3			1100 010a <abs 8..>	
	MOVW (abs16),DWm	mem16(abs16)→DWm	--	--	--	--	7	5			0010 1100 011d <abs 16.. ....>	
	MOVW (abs16),Am	mem16(abs16)→Am	--	--	--	--	7	5			0010 1100 010a <abs 16.. ....>	
	MOVW DWn,(Am)	DWn→mem16(Am)	--	--	--	--	2	3			1111 00aD	
	MOVW An,(Am)	An→mem16(Am)	--	--	--	--	3	4			0010 1111 10aA	*4
	MOVW DWn,(d4,SP)	DWn→mem16(d4+SP)	--	--	--	--	3	3			1111 011D <d4>	*2
	MOVW An,(d4,SP)	An→mem16(d4+SP)	--	--	--	--	3	3			1111 010A <d4>	*2
	MOVW DWn,(d8,SP)	DWn→mem16(d8+SP)	--	--	--	--	5	4			0010 1111 011D <d8. ...>	*3
	MOVW An,(d8,SP)	An→mem16(d8+SP)	--	--	--	--	5	4			0010 1111 010A <d8. ...>	*3
	MOVW DWn,(d16,SP)	DWn→mem16(d16+SP)	--	--	--	--	7	5			0010 1111 001D <d16 ....>	
	MOVW An,(d16,SP)	An→mem16(d16+SP)	--	--	--	--	7	5			0010 1111 000A <d16 ....>	
	MOVW DWn,(abs8)	DWn→mem16(abs8)	--	--	--	--	4	3			1101 011D <abs 8..>	
	MOVW An,(abs8)	An→mem16(abs8)	--	--	--	--	4	3			1101 010A <abs 8..>	
	MOVW DWn,(abs16)	DWn→mem16(abs16)	--	--	--	--	7	5			0010 1101 011D <abs 16.. ....>	
	MOVW An,(abs16)	An→mem16(abs16)	--	--	--	--	7	5			0010 1101 010A <abs 16.. ....>	
	MOVW DWn,(HA)	DWn→mem16(HA)	--	--	--	--	2	3			1001 010D	
	MOVW An,(HA)	An→mem16(HA)	--	--	--	--	2	3			1001 011A	
	MOVW imm8,DWm	sign(imm8)→DWm	--	--	--	--	4	2			0000 110d <#8. ...>	*5
	MOVW imm8,Am	zero(imm8)→Am	--	--	--	--	4	2			0000 111a <#8. ...>	*6
	MOVW imm16,DWm	imm16→DWm	--	--	--	--	6	3			1100 111d <#16 ....>	

*1 d8 sign-extension *4 A=An, a=Am
*2 d4 zero-extension *5 #8 sign-extension
*3 d8 zero-extension *6 #8 zero-extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	VF	NF	CF	ZF	Code Size	Cycle	Re-peat	exten-sion	Machine Code	Notes
	MOVW imm16,Am	imm16→Am	--	--	--	--	6	3			1101 111a <#16 ....>	
	MOVW SP,Am	SP→Am	--	--	--	--	3	3			0010 0000 100a	
	MOVW An,SP	An→SP	--	--	--	--	3	3			0010 0000 101A	
	MOVW DWn,DWm	DWn→DWm	--	--	--	--	3	3			0010 1000 00Dd	*1
	MOVW DWn,Am	DWn→Am	--	--	--	--	3	3			0010 0100 11Da	
	MOVW An,DWm	An→DWm	--	--	--	--	3	3			0010 1100 11Ad	
	MOVW An,Am	An→Am	--	--	--	--	3	3			0010 0000 00Aa	*2
PUSH	PUSH Dn	SP-1→SP,Dn→mem8(SP)	--	--	--	--	2	3			1111 10Dn	
	PUSH An	SP-2→SP,An→mem16(SP)	--	--	--	--	2	5			0001 011A	
POP	POP Dn	mem8(SP)→Dn,SP+1→SP	--	--	--	--	2	3			1110 10Dn	
	POP An	mem16(SP)→An,SP+2→SP	--	--	--	--	2	4			0000 011A	
EXT	EXT Dn,DWm	sign(Dn)→DWm	--	--	--	--	3	3			0010 1001 000d	*3

Arithmetic manupulation instructions

Group	Mnemonic	Operation	VF	NF	CF	ZF	Code Size	Cycle	Re-peat	exten-sion	Machine Code	Notes
ADD	ADD Dn,Dm	Dm+Dn→Dm	●	●	●	●	3	2			0011 0011 DnDm	
	ADD imm4,Dm	Dm+sign(imm4)→Dm	●	●	●	●	3	2			1000 00Dm <#4>	*6
	ADD imm8,Dm	Dm+imm8→Dm	●	●	●	●	4	2			0000 10Dm <#8. ...>	
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	●	●	●	●	3	2	○		0011 1011 DnDm	
ADDW	ADDW DWn,DWm	DWm+DWn→DWm	●	●	●	●	3	3	○		0010 0101 00Dd	*1
	ADDW DWn,Am	Am+DWn→Am	●	●	●	●	3	3	○		0010 0101 10Da	
	ADDW imm4,Am	Am+sign(imm4)→Am	●	●	●	●	3	2			1110 110a <#4>	*6
	ADDW imm8,Am	Am+sign(imm8)→Am	●	●	●	●	5	3			0010 1110 110a <#8. ...>	*7
	ADDW imm16,Am	Am+imm16→Am	●	●	●	●	7	4			0010 0101 011a <#16 ....>	
	ADDW imm4,SP	SP+sign(imm4)→SP	--	--	--	--	3	2			1111 1101 <#4>	*6
	ADDW imm8,SP	SP+sign(imm8)→SP	--	--	--	--	4	2			1111 1100 <#8. ...>	*7
	ADDW imm16,SP	SP+imm16→SP	--	--	--	--	7	4			0010 1111 1100 <#16 ....>	
	ADDW imm16,DWm	DWm+imm16→DWm	●	●	●	●	7	4			0010 0101 010d <#16 ....>	
ADDUW	ADDUW Dn,Am	Am+zero(Dn)→Am	●	●	●	●	3	3	○		0010 1000 1aDn	*8
ADDSW	ADDSW Dn,Am	Am+sign(Dn)→Am	●	●	●	●	3	3	○		0010 1001 1aDn	
SUB	SUB Dn,Dm(when Dn≠Dm)	Dm-Dn→Dm	●	●	●	●	3	2	○		0010 1010 DnDm	
	SUB Dn,Dn	Dn-Dn→Dn	0	0	0	1	2	1			1000 01Dn	
	SUB imm8,Dm	Dm-imm8→Dm	●	●	●	●	5	3			0010 1010DmDm <#8. ...>	
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	●	●	●	●	3	2	○		0010 1011 DnDm	
SUBW	SUBW DWn,DWm	DWm-DWn→DWm	●	●	●	●	3	3			0010 0100 00Dd	*1
	SUBW DWn,Am	Am-DWn→Am	●	●	●	●	3	3			0010 0100 10Da	
	SUBW imm16,DWm	DWm-imm16→DWm	●	●	●	●	7	4			0010 0100 010d <#16 ....>	
	SUBW imm16,Am	Am-imm16→Am	●	●	●	●	7	4			0010 0100 011a <#16 ....>	
MULU	MULU Dn,Dm	Dm*Dn→DWk	0	●	●	●	3	8			0010 1111 111D	*4
DIVU	DIVU DWn,Dwm	DWm/Dn→DWm-I...DWm-h	●	●	●	●	3	9			0010 1110 111d	*5
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2			0011 0010 DnDm	
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2			1100 00Dm <#8. ...>	
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3			0000 0100 <abs 8..> <#8. ...>	
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3			0000 0101 <abs 12.. ...> <#8. ...>	
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5			0011 1101 1000 <abs 16.. ....> <#8. ...>	
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3			0010 1000 01Dd	*1
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3			0010 0101 11Da	
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3			0010 0000 01Aa	*2
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3			1100 110d <#16 ....>	
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3			1101 110a <#16 ....>	

Logical manipulation instructions

Group	Mnemonic	Operation	VF	NF	CF	ZF	Code Size	Cycle	Re-peat	exten-sion	Machine Code	Notes
AND	AND Dn,Dm	Dm&Dn→Dm	0	●	0	●	3	2			0011 0111 DnDm	
	AND imm8,Dm	Dm&imm8→Dm	0	●	0	●	4	2			0001 11Dm <#8. ...>	
	AND imm8,PSW	PSW&imm8→PSW	●	●	●	●	5	3			0010 1001 0010 <#8. ...>	
OR	OR Dn,Dm	DmIDn→Dm	0	●	0	●	3	2			0011 0110 DnDm	
	OR imm8,Dm	DmIimm8→Dm	0	●	0	●	4	2			0001 10Dm <#8. ...>	
	OR imm8,PSW	PSWIimm8→PSW	●	●	●	●	5	3			0010 1001 0011 <#8. ...>	
XOR	XOR Dn,Dm	Dm^Dn→Dm	0	●	0	●	3	2			0011 1010 DnDm	*9
	XOR imm8,Dm	Dm^imm8→Dm	0	●	0	●	5	3			0011 1010DmDm <#8. ...>	

*1 D=DWn, d=DWm   *5 D=DWm   *9 m≠n
*2 A=An, a=Am   *6 #4 sign-extension
*3 d=DWm   *7 #8 sign-extension
*4 D=DWk   *8 Dn zero extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	1	2	3	4	5	6	7	8	9	10	11	Notes
NOT	NOT Dn	‾Dn→Dn=	0	●	0	●	3	2			0010 0010 10Dn											
ASR	ASR Dn	Dn.msb→temp,Dn.lsb→CF Dn>>1→Dn,temp→Dn.msb	0	--	●	●	3	2	○		0010 0011 10Dn											
LSR	LSR Dn	Dn.lsb→CF,Dn>>1→Dn 0→Dn.msb	0	0	●	●	3	2	○		0010 0011 11Dn											
ROR	ROR Dn	Dn.lsb→temp,Dn>>1→Dn CF→Dn.msb,temp→CF	0	●	●	●	3	2	○		0010 0010 11Dn											
Bit manipulation instructions																						
BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1→mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011 1000 0bp. <io8 ...>											
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1→mem8(abs8)bp	0	●	0	●	4	4				1011 0bp. <abs 8..>										
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1→mem8(abs16)bp	0	●	0	●	7	6			0011 1100 0bp. <abs 16.. ....>											
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0→mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011 1000 1bp. <io8 ...>											
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0→mem8(abs8)bp	0	●	0	●	4	4				1011 1bp. <abs 8..>										
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0→mem8(abs16)bp	0	●	0	●	7	6			0011 1100 1bp. <abs 16.. ....>											
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	●	0	●	5	3			0010 0000 11Dm <#8. ...>											
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	●	0	●	7	5			0011 1101 0bp. <abs 16.. ....>											
Branch instructions																						
Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H→PC if(ZF=0), PC+3→PC	--	--	--	--	3	2/3			1001 000H <d4>											*1
	BEQ label	if(ZF=1), PC+4+d7(label)+H→PC if(ZF=0), PC+4→PC	--	--	--	--	4	2/3			1000 1010 <d7. ...H											*2
	BEQ label	if(ZF=1), PC+5+d11(label)+H→PC if(ZF=0), PC+5→PC	--	--	--	--	5	2/3			1001 1010 <d11 ....H											*3
	BNE label	if(ZF=0), PC+3+d4(label)+H→PC if(ZF=1), PC+3→PC	--	--	--	--	3	2/3			1001 001H <d4>											1
	BNE label	if(ZF=0), PC+4+d7(label)+H→PC if(ZF=1), PC+4→PC	--	--	--	--	4	2/3			1000 1011 <d7. ...H											*2
	BNE label	if(ZF=0), PC+5+d11(label)+H→PC if(ZF=1), PC+5→PC	--	--	--	--	5	2/3			1001 1011 <d11 ....H											*3
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H→PC if((VF^NF)=1),PC+4→PC	--	--	--	--	4	2/3			1000 1000 <d7. ...H											*2
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H→PC if((VF^NF)=1),PC+5→PC	--	--	--	--	5	2/3			1001 1000 <d11 ....H											*3
	BCC label	if(CF=0),PC+4+d7(label)+H→PC if(CF=1), PC+4→PC	--	--	--	--	4	2/3			1000 1100 <d7. ...H											*2
	BCC label	if(CF=0),PC+5+d11(label)+H→PC if(CF=1), PC+5→PC	--	--	--	--	5	2/3			1001 1100 <d11 ....H											*3
	BCS label	if(CF=1),PC+4+d7(label)+H→PC if(CF=0), PC+4→PC	--	--	--	--	4	2/3			1000 1101 <d7. ...H											*2
	BCS label	if(CF=1),PC+5+d11(label)+H→PC if(CF=0), PC+5→PC	--	--	--	--	5	2/3			1001 1101 <d11 ....H											*3
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H→PC if((VF^NF)=0),PC+4→PC	--	--	--	--	4	2/3			1000 1110 <d7. ...H											*2
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H→PC if((VF^NF)=0),PC+5→PC	--	--	--	--	5	2/3			1001 1110 <d11 ....H											*3
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H→PC if((VF^NF)|ZF=0),PC+4→PC	--	--	--	--	4	2/3			1000 1111 <d7. ...H											*2
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H→PC if((VF^NF)|ZF=0),PC+5→PC	--	--	--	--	5	2/3			1001 1111 <d11 ....H											*3
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H→PC if((VF^NF)|ZF=1),PC+5→PC	--	--	--	--	5	3/4			0010 0010 0001 <d7. ...H											*2

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Exten-sion	1	2	3	4	5	6	7	8	9	10	11	Notes
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H→PC if((VF^NF)|ZF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0001	<d11	....	...H						*3
	BHI label	if(CF|ZF=0),PC+5+d7(label)+H→PC if(CF|ZF=1), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0010	<d7.	...H							*2
	BHI label	if(CF|ZF=0),PC+6+d11(label)+H→PC if(CF|ZF=1), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0010	<d11	....	...H						*3
	BLS label	if(CF|ZF=1),PC+5+d7(label)+H→PC if(CF|ZF=0), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0011	<d7.	...H							*2
	BLS label	if(CF|ZF=1),PC+6+d11(label)+H→PC if(CF|ZF=0), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0011	<d11	....	...H						*3
	BNC label	if(NF=0),PC+5+d7(label)+H→PC if(NF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0100	<d7.	...H							*2
	BNC label	if(NF=0),PC+6+d11(label)+H→PC if(NF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0100	<d11	....	...H						*3
	BNS label	if(NF=1),PC+5+d7(label)+H→PC if(NF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0101	<d7.	...H							*2
	BNS label	if(NF=1),PC+6+d11(label)+H→PC if(NF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0101	<d11	....	...H						*3
	BVC label	if(VF=0),PC+5+d7(label)+H→PC if(VF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0110	<d7.	...H							*2
	BVC label	if(VF=0),PC+6+d11(label)+H→PC if(VF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0110	<d11	....	...H						*3
	BVS label	if(VF=1),PC+5+d7(label)+H→PC if(VF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0111	<d7.	...H							*2
	BVS label	if(VF=1),PC+6+d11(label)+H→PC if(VF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0111	<d11	....	...H						*3
	BRA label	PC+3+d4(label)+H→PC	--	--	--	--	3	3				1110	111H	<d4>									*1
	BRA label	PC+4+d7(label)+H→PC	--	--	--	--	4	3				1000	1001	<d7.	...H								*2
	BRA label	PC+5+d11(label)+H→PC	--	--	--	--	5	3				1001	1001	<d11	....	...H							*3
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H→PC if(Dm≠imm8),PC+6→PC	●	●	●	●	6	3/4				1100	10Dm	<#8.	...>	<d7.	...H					*2
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H→PC if(Dm≠imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1100	10Dm	<#8.	...>	<d11	....	...H				*3
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H→PC if(mem8(abs8)≠imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1100	<abs 8.>	<#8.	...>	<d7.	...H				*2
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H→PC if(mem8(abs8)≠imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1101	<abs 8.>	<#8.	...>	<d11	....	...H			*3
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H→PC if(mem8(abs16)≠imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1100	<abs 16..	....	...>	<#8.	...>	<d7.	...H		*2
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H→PC if(mem8(abs16)≠imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1101	<abs 16..	....	...>	<#8.	...>	<d11	....	...H	*3
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H→PC if(Dm=imm8),PC+6→PC	●	●	●	●	6	3/4				1101	10Dm	<#8.	...>	<d7.	..H>					*2
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H→PC if(Dm=imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1101	10Dm	<#8.	...>	<d11	....	...H				*3
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H→PC if(mem8(abs8)=imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1110	<abs 8.>	<#8.	...>	<d7.	...H				*2
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H→PC if(mem8(abs8)=imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1111	<abs 8.>	<#8.	...>	<d11	....	...H			*3
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H→PC if(mem8(abs16)=imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1110	<abs 16..	....	...>	<#8.	...>	<d7.	...H		*2
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H→PC if(mem8(abs16)=imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1111	<abs 16..	....	...>	<#8.	...>	<d11	....	...H	*3
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H→PC if(mem8(abs8)bp=1),PC+7→PC	0	●	0	●	7	6/7			0011	0000	0bp.	<abs 8.>	<d7.	...H						*2
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H→PC if(mem8(abs8)bp=1),PC+8→PC	0	●	0	●	8	6/7			0011	0000	1bp.	<abs 8.>	<d11	....	...H					*3

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Exten-sion 1	2	3	4	5	6	7	8	9	10	11	Notes
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+7→PC	0	●	0	●	7	6/7		0011 0100 0bp. <io8 ...> <d7. ...H											*1
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+8→PC	0	●	0	●	8	6/7		0011 0100 1bp. <io8 ...> <d11 ....H											*2
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H→PC if(mem8(abs16)bp=1),PC+9→PC	0	●	0	●	9	7/8		0011 1110 0bp. <abs 16.. ....> <d7. ...H											*1
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC if(mem8(abs16)bp=1),PC+10→PC	0	●	0	●	10	7/8		0011 1110 1bp. <abs 16.. ....> <d11 ....H											*2
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H→PC if(mem8(abs8)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011 0001 0bp. <abs 8..> <d7. ...H											*1
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H→PC if(mem8(abs8)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011 0001 1bp. <abs 8..> <d11 ....H											*2
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H→PC if(mem8(io)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011 0101 0bp. <io8 ...> <d7. ...H											*1
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H→PC if(mem8(io)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011 0101 1bp. <io8 ...> <d11 ....H											*2
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H→PC if(mem8(abs16)bp=0),PC+9→PC	0	●	0	●	9	7/8		0011 1111 0bp. <abs 16.. ....> <d7. ...H											*1
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC if(mem8(abs16)bp=0),PC+10→PC	0	●	0	●	10	7/8		0011 1111 1bp. <abs 16.. ....> <d11 ....H											*2
JMP	JMP (An)	0→PC.17-16,An→PC.15-0,0→PC.H	---	---	---	---	3	4		0010 0001 00A0											
	JMP label	abs18(label)+H→PC	---	---	---	---	7	5		0011 1001 0aaH <abs 18.b p15~ 0..>											*5
	JMP label	abs20(label)+H→PC	---	---	---	---	9	6		0011 1101 1010 000B bbbH <abs 20.b p15~ 0..>											*6 *7
JSR	JSR (An)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+3).bp19-16→mem8(SP+2).bp3-0 0→PC.bp19-16 An→PC.bp15-0,0→PC.H	---	---	---	---	3	7		0010 0001 00A1											
	JSR label	SP-3→SP,(PC+5).bp7-0→mem8(SP) (PC+5).bp15-8→mem8(SP+1) (PC+5).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+5).bp19-16→mem8(SP+2).bp3-0 PC+5+d12(label)+H→PC	---	---	---	---	5	6		0001 000H <d12 ....>											*3
	JSR label	SP-3→SP,(PC+6).bp7-0→mem8(SP) (PC+6).bp15-8→mem8(SP+1) (PC+6).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+6).bp19-16→mem8(SP+2).bp3-0 PC+6+d16(label)+H→PC	---	---	---	---	6	7		0001 001H <d16 ....>											*4
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+7).bp19-16→mem8(SP+2).bp3-0 abs18(label)+H→PC	---	---	---	---	7	8		0011 1001 1aaH <abs 18.b p15~ 0..>											*5
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+7).bp19-16→mem8(SP+2).bp3-0 abs20(label)+H→PC	---	---	---	---	9	9		0011 1101 1011 000B bbbH <abs 20.b p15~ 0..>											*6 *7
	JSRV (tbl4)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7 0→mem8(SP+2).bp6-4, (PC+3).bp19-16→mem8(SP+2).bp3-0 mem8(x'004080+tbl4<<2)→PC.bp7-0 mem8(x'004080+tbl4<<2+1)→PC.bp15-8 mem8(x'004080+tbl4<<2+2).bp7→PC.H mem8(x'004080+tbl4<<2+2).bp3-0→ PC.bp19-16	---	---	---	---	3	9		1111 1110 <t4>											
NOP	NOP	PC+2→PC	---	---	---	---	2	1	○	0000 0000											

*1 d7 sign-extension
*2 d11 sign-extension
*3 d12 sign-extension
*4 d16 sign-extension
*5 aa=abs18.17 - 16
*6 B=abs20.19
*7 bbb=abs20.18 - 16

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Exten-sion	1	2	3	4	5	Machine Code 6	7	8	9	10	11	Notes
RTS	RTS	mem8(SP)→(PC).bp7-0	---	---	---	---	2	7		0000 0001												
		mem8(SP+1)→(PC).bp15-8																				
		mem8(SP+2).bp7→(PC).H																				
		mem8(SP+2).bp3-0→(PC).bp19-16																				
		SP+3→SP																				
RTI	RTI	mem8(SP)→PSW	●	●	●	●	2	11		0000 0011												
		mem8(SP+1)→(PC).bp7-0																				
		mem8(SP+2)→(PC).bp15-8																				
		mem8(SP+3).bp7→(PC).H																				
		mem8(SP+3).bp3-0→(PC).bp19-16																				
		mem8(SP+4)→HA-l																				
		mem8(SP+5)→HA-h																				
		SP+6→SP																				
Contorl instructions																						
REP	REP imm3	imm3-1→RPC	---	---	---	---	3	2		0010 0001 1rep												*1
BE	BE	PSW & x'3F'→PSW	---	---	---	---	3	3		0010 0010 0000												
BD	BD	PSW | x'c0'→PSW	---	---	---	---	3	3		0010 0011 0000												

*1 no repeat whn imm3=0, (rep: imm3-1)

Other than the instruction of MN101E Series,the assembler of this Series has the following instructions as macro instructions.
The assembler will interpret the macro instructions below as the assembler instructions.

macro instructions		replaced instructions		remarks
INC	Dn	ADD	1,Dn	
DEC	Dn	ADD	-1,Dn	
INC	An	ADDW	1,An	
DEC	An	ADDW	-1,An	
INC2	An	ADDW	2,An	
DEC2	An	ADDW	-2,An	
CLR	Dn	SUB	Dn,Dm	n=m
ASL	Dn	ADD	Dn,Dm	n=m
LSL	Dn	ADD	Dn,Dm	n=m
ROL	Dn	ADDC	Dn,Dm	n=m
NEG	Dn	NOT	Dn	
		ADD	1,Dn	
NOPL		MOVW	DWn,DWm	n=m
MOV	(SP),Dn	MOV	(0,SP),Dn	
MOV	Dn,(SP)	MOV	Dn,(0,SP)	
MOVW	(SP),DWn	MOVW	(0,SP),DWn	
MOVW	DWn,(SP)	MOVW	DWn,(0,SP)	
MOVW	(SP),An	MOVW	(0,SP),An	
MOVW	An,(SP)	MOVW	An,(0,SP)	

Ver3.3(2002.01.31)

18.12 Instruction Map

MN101E SERIES INSTRUCTION MAP

1st nibble\2nd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the exension code is b'oo10'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nibble\3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2	BE	BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3	BD	BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

Extension code: b'0011'

2nd nibble\ 3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TBZ (abs8)bp,d7								TBZ (abs8)bp,d11							
1	TBNZ (abs8)bp,d7								TBNZ (abs8)bp,d11							
2	CMP Dn,Dm															
3	ADD Dn,Dm															
4	TBZ (io8)bp,d7								TBZ (io8)bp,d11							
5	TBNZ (io8)bp,d7								TBNZ (io8)bp,d11							
6	OR Dn,Dm															
7	AND Dn,Dm															
8	BSET (io8)bp								BCLR (io8)bp							
9	JMP abs18(label)								JSR abs18(label)							
A	XOR Dn,Dm / XOR #8,Dm															
B	ADDC Dn,Dm															
C	BSET (abs16)bp								BCLR (abs16)bp							
D	BTST (abs16)bp								cmp #8,(abs16)	mov #8,(abs16)	JMP abs20(label)	JSR abs20(label)	CBEQ #8,(abs16),d7/11		CBNE #8,(abs16),d7/11	
E	TBZ (abs16)bp,d7								TBZ (abs16)bp,d11							
F	TBNZ (abs16)bp,d7								TBNZ (abs16)bp,d11							

Ver2.1(2001.03.26)

Record of Changes

The following shows the changes in the publication of "MN101E29G/F29G LSI User's Manual" (From 1st Edition 4th Printing dated in January, 2008 to the 2nd Edition 1st Printing dated in March, 2012.)

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-2	16	Error correction	High speed mode has the normal mode which is based on 2-cycle clock (<u>fosc/2</u>) and the double speed mode which is based on <u>the same cycle clock with fosc</u>.	High speed mode has the normal mode which is based on 2-cycle clock (<u>fpll/2</u>) and the double speed mode which is based on <u>the not-devided clock with fpll</u>.
I-4,5		Specification addition	-	Add the description as (Peripheral function group interrupt)
From I-5 to the last		Error correction	<u>fosc</u>	<u>fpll</u>
I-6	Timer 3	Error correction	16bit cascade connected (timer2<u>, 3</u>), 32-bit cascade connected (timer0, 1, 2<u>, 3</u>)	16bit cascade connected (timer2), 32-bit cascade connected (timer0, 1, 2)
I-8	2 from the bottom	Error correction	Port <u>4</u> outputs the latched data, on the event timing of the synchronous output signal of timer	Port <u>8</u> outputs the latched data, on the event timing of the synchronous output signal of timer
I-11	10	Error correction	Serial4 -7-bit <u>or 10-bit</u> of slave address can be set.	Serial4 -7-bit of slave address can be set.
	1 from the bottom	Error correction	1/4 duty, <u>1/4</u> bias	1/4 duty, <u>1/3</u> bias
I-12	9-12	Description change	<u>VDD</u>, <u>VLC1</u>, <u>VLC2</u>, <u>VLC3</u>	<u>V_{DD5}</u>, <u>V_{LC1}</u>, <u>V_{LC2}</u>, <u>V_{LC3}</u>
	16	Error correction	Port -I/O ports LCD driver for segment : <u>54</u> pins	Port -I/O ports LCD driver for segment : <u>55</u> pins
I-13	Figure 1.3.1	Description change	<u>VDD</u> (1.8 capacity)	<u>VDD18</u> (1.8 capacity)
I-18	V_{DD5}	Description change	Apply 2.2 V to 5.5 V to <u>V_{DD}</u> and 0 V to V_{SS}.	Apply 2.2 V to 5.5 V to <u>V_{DD5}</u> and 0 V to V_{SS}.
	V_{DD18}	Description change	<u>V_{DD}</u> (Capacity 1.8V)	<u>V_{DD18}</u> (Capacity 1.8V)
	XI, XO	Description change	Other Function <u>-</u>	Other Function <u>P90, P91</u>
	NRST	Error correction	NO <u>19</u>	NO <u>12</u>
	NRST	Error correction	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. <u>30</u> kΩ)...	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. <u>50</u> kΩ)...
I-19	P27	Error correction	NO <u>19</u>	NO <u>12</u>
I-20,21		Error correction	<u>COMS</u> push-pull	<u>CMOS</u> push-pull

<Record of Changes - 1>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-22	BUZZERx NBUZZERx	Error correction	P1OMD and PA5MD	P1OMD and P5OMD
I-23	V_{REF+}	Error correction	Normally, tha values of $V_{REF+} = V_{DD}$ is used.	The values of $2.0\ V \le V_{REF+} \le V_{DD5}$ is used.
I-25	V_{LC1}	Description change	$V_{LC1}=V_{DD}$	$V_{LC1}=V_{DD5}$
I-26	SEGx	Description change	... Comect to the segment pins of the LCD panel.	... Comect to the segment pins of the LCD display panel.
I-27	DMOD	Description change	Set always to V_{DD}.	Set always to V_{DD5}.
I-29	From 1.5.1 to the last page	Error correction	V_{DD}	V_{DD5}
	1.5.1	Description change	(table)	(table)
	*3	Description change	V_{DD18} V_{DD5}	V_{DD18} V_{DD5}
	*4	Description change	The absolute maximum ratings are the limit values beyond which the LSI may be damaged and proper operation is not assured.	The absolute maximum ratings are the limit values beyond which the LSI may be damaged.
I-31	Table	Error correction	Crystal Oscillator [NORMAL mode:fs=fosc/2] Crystal Oscillator [Slow mode:fs=fx/2]	Crystal Oscillator [NORMAL mode] Crystal Oscillator [Slow mode]
	Figure 1.5.1	Description addition	(figure)	(figure)
	Figure 1.5.2	Description addition	(figure)	(figure)
I-32	Table	Error correction	(table)	(table)

Embedded table (I-29, 1.5.1) — Former Edition:

Vss=0 V

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	-0.3 to +7.0	V
2	Input clamp current(ACZ)		I_C	-500 to +500	µA
3	Input pin voltage		V_I	-0.3 to V_{DD}+0.3	
4	output pin voltage		V_O	-0.3 to V_{DD}+0.3	V
5	I/O pin voltage		V_{IO1}	-0.3 to V_{DD}+0.3	
6		P0	I_{OL1} (peak)	30	
7	Pointed output current	Other than P0	I_{OL2} (peak)	20	
8		All pins	I_{OH} (peak)	-10	mA
9		P0	I_{OL1} (avg)	20	
10	Average output current *1	Other than P0	I_{OL2} (avg)	15	

Embedded table (I-29, 1.5.1) — New Edition:

Vss=0 V

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD5}	-0.3 to + 7.0	V
2	Capacity connect pin voltage		V_{DD18}	-0.3 to + 2.5	
3	Input clamp current(ACZ)		I_C	-500 to + 500	µA
4	Input pin voltage		V_I	-0.3 to V_{DD5} + 0.3 (up to 7)	
5	output pin voltage		V_O	-0.3 to V_{DD5} + 0.3 (up to 7)	V
6	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} + 0.3 (up to 7)	
7		P0	I_{OL1} (peak)	30	
8	Pointed output current	Any other than P0	I_{OL2} (peak)	20	
9		All pins	I_{OH} (peak)	-10	mA
10		P0	I_{OL1} (avg)	20	

Embedded table (I-32) — Former Edition:

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
	External clock input 1 OSC1(OSC2 is unconnected)						
16	Clock frequency	fOSC1		1.0		10	MHz
17	High level pulse width *6	tWH1	Fig. 1-5-3	45			
18	Low level pulse width *6	tWL1		45			
19	Rising time *7	tAR1	Fig. 1-5-3	0		5.0	ns
20	Falling time *7	tAF1		0		5.0	
	External clock input 2 XI(XO is unconnected)						
21	Clock frequency	fOSC2		32.768		100	kHz
22	High level pulse width *6	tWH2	Fig. 1-5-4	4.5			ms
23	Low level pulse width *6	tWL2		4.5			
24	Rising time *7	tAR2	Fig. 1-5-4	0		20	ns
25	Falling time *7	tAF2		0		20	

Embedded table (I-32) — New Edition:

V_{DD5}=2.3 V to 5.5 V   Vss=0 V
Ta=-40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
	External clock input 1 OSC1(OSC2 is unconnected)						
16	Clock frequency	fOSC1		1.0		10	MHz
17	High level pulse width *6	tWH1	Fig. 1-5-3	45			
18	Low level pulse width *6	tWL1		45			
19	Rising time *7	tAR1	Fig. 1-5-3	0		5.0	ns
20	Falling time *7	tAF1		0		5.0	
	External clock input 2 XI(XO is unconnected)						
21	Clock frequency	fOSC2			32.768		kHz
22	High level pulse width *6	tWH2	Fig. 1-5-4		4.5		µs
23	Low level pulse width *6	tWL2			4.5		
24	Rising time *7	tAR2	Fig. 1-5-4	0		20	ns
25	Falling time *7	tAF2		0		20	

Figures 1.5.1: OSC1, with Rf10 (Former); OSC1 with Rf10 and fxtal1 label (New).

Figures 1.5.2: XI, with Rf20 (Former); XI with Rf20 and fxtal2 label (New).

<Record of Changes - 2>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-34	1	Description deletion	<u>The below current is a targeted specification. Please contact us for the latest specification.</u>	-
	Table	Description change	-	Change the each characteristics and add conents 6
	*8	Description deletion	Measured under conditions without load, <u>Ta=25°C.</u> (pull-up / pull-down resistors are unconnected.)	Measured under conditions without load. (pull-up / pull-down resistors are unconnected.)
I-35	Parameter 11,12,17,18	Description Change	Input high voltage <u>1</u> Input low voltage <u>1</u> Input high voltage <u>2</u> Input low voltage <u>2</u>	Input high voltage Input low voltage Input high voltage Input low voltage
	Parameter 19	Error correction	<u>±5</u>	<u>±2</u>
	Parameter 21	Error correction	V_{IN}=<u>V_{SS}</u>	V_{IN}=<u>V_{DD5}</u>
I-36	Parameter 30,31	Description change	Input high voltage <u>1</u> Input low voltage <u>1</u>	Input high voltage Input low voltage
	Parameter 37	Error correction	LED output <u>OFF</u>	LED output <u>ON</u>
I-37	Parameter 41	Description deletion	<u>41 : Input leak current</u>	-
	Parameter 38,39,40,41	Description addition	Condition <u>-</u>	Condition <u>Figure:1.5.5</u>
	Parameter 43,44,45,46	Description change	-	Parameter 43,44,45,46 changed.
I-38	Figure 1.5.5	Description change	V_{DD}	V_{DD5}
I-39	Table	Error correction		
	*12	Description deletion	T_{AD} is A/D conversion clock cycle. The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{ref+}=5 V, V_{SS}=0 V. <u>Note) The voltage difference between V_{ref+} and V_{SS} should be set to more than 2 V.</u>	T_{AD} is A/D conversion clock cycle. The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{ref+}=5 V, V_{SS}=0 V.
	Note	Description addition	-	<u>The reference voltage input V_{ref+} pin uses value of 2.0 V $\leq V_{ref+} \leq V_{DD5}$. When input voltage is V_{ref+} < 2.0 V, there...</u>
I-41	1.5.8	Specification addtion	-	1.5.8 Flash EEPROM Programmig Condition

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-44	1	Description change	V_{DD}	V_{DD5}
	2	Description change	V$\underline{DD}$	V_{DD5}
	5	Description addition	-	-$\underline{V_{ref+}}$ Pin Connection
I-45	Table1.7.1	Error correction	-	Table 1.7.1 is changed
I-46	First Note	Description addition	-	Oscillation between E29 series and E30 series which is added audio function to E29 is different.
	Table1.7.2	Description addition	-	Table 1.7.2 added.
	Second & Third Note	Description change	-	Second and Third Note moved from I-45 of Former Edition.
I-50	The last line	Description addition	-	[In using auto reset] - Microcontroller Power On in using Auto Reset (V_{DD5}=5V) Fig.1.7.8 Microcontroller Power On in using Auto Reset (V_{DD5}=5V)
II-4	Table 2.1.3	Description addition	-	AUCTR
		Error correction	CPUM R/W *1	CPUM R/W
	3	Error correction	*1 a part of bit is for read only	-
II-8	PSW	Description addition	bp 7 ... Flag BKD ... At reset 0 ...	bp 7 ... Flag BKD ... At reset 0 ... Access R/W ...
II-9	Square	Description change	-Maskable Interrupt Enalbe (MIE) ... A '1' enables maskable interrupts; a '0' disables all maskable interrupts	-Maskable Interrupt Enalbe (MIE) ... The setting the flag to "1" enables maskable interrupts; the setting to "0" disables all maskable interrupts
II-10	Second Note	Description addition	-	Make mascable interrutp enable flag (MIE) of processore status word (PSW) of prohibited all mascable interrupts ...
II-12	First Key	Description addition	This LSI is designed for 8-bit data access. It is possible to tranfer data in 16-bit increments with odd or all even addresses.	This LSI is designed for 8-bit data access. When 16-bit data access is carried out, 8-bit data access is performed twice from the lower address. It is possible to tranfer data in 16-bit increments with odd or all even addresses.
II-15	Note	Description deletion	Fix the MMOD pin always to "L" or "H" level. Do not change the settings of this pin also after reset release.	Fix the MMOD pin always to "L" level. Do not change the settings of this pin also after reset release.
II-24	1	Description change	The MN101E series locates the special function registers...	This LSI locates the special function registers...
	Figure: 2.2.5	Error correction	SC4TICR	SC4ICR

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-28	RCPSR	Error correction	110:Address pointer 6 (RC6AP (L/M/H))	110:Address pointer 6 (RC6AP (L/M/H)) <u>111:Setting Prohibited</u>
II-29	First Note	Description addition	-	<u>ROM correction address is set for 4th or later command from command that enable the ROM correction control.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
II-30	Second Note	Description addition	-	<u>ROM correction address is set for 4th or later command from command that enable the ROM correction control.</u>
II-34	18	Description change	After <u>the main program is started,</u> the instruciton fetched address and the set address to ROM...	After <u>4th or later command from command that enable the ROM correction control,</u> the instruciton fetched address and the set address to ROM...
II-37	Third Note	Description addition	-	<u>Alway set IRWE flag of memory control register (MEMCTR) to "0"…</u>
	Fourth Note	Description addition	-	<u>External expansion memory function does not guarantee AC timing. When using this function, refer to [Chapter 17 AC Timing Variable] and recommend the AC timing to be filled.</u>
	Fifth Note	Description addition	-	<u>If accessing the external expansion memory area, execute with 5 MHz or less of access rate.</u>
II-38	First Note	Description change	<u>Key</u> In the memory expansion mode, unused ...	<u>Note</u> In the memory expansion mode, unused ...
II-39	First Note	Description change	<u>Key</u> During single-chip mode, do not set the...	<u>Note</u> During single-chip mode, do not set the...
II-42	1	Change	This LSI has <u>three</u> sets of system clock oscillator (high speed oscillation, <u>multiplied high speed oscillation,</u> low speed oscillation) for <u>two</u> CPU operating modes (NORMAL and SLOW), ...	This LSI has <u>two</u> sets of system clock <u>(fs)</u> oscillator (high speed oscillation, low speed oscillation) <u>and PLL circuit to multiply high speed oscillation,</u> for <u>three</u> CPU operating modes (NORMAL<u>, PLL</u> and SLOW), ...
II-43	2	Description change	<u>The CPU stops operating. But both of the oscillators remain operational in HALT0 and only the high-frequency oscillator stops operating in HALT1. An interrupt returns the CPU to the previous CPU operating mode that is, to NORMAL from HALT0 or to SLOW from HALT1 or to PLL from HALT2.</u>	<u>The CPU stops operation. The oscillator or PLL are operating. An interrupt allows the CPU to operate. The high and low-frequency oscillators operate in HALT0. When an interrupt occurs, HALT0 enters into the normal operation state (NORMAL). ... Both of the oscillators and PLL operate in HALT2. When an interrupt occurs, HALT2 enters into PLL modes.</u>
	18	Description change	The PLL-IDLE allows time for <u>the multiplied high-frequency oscillator</u> to stabilize when the software is changing from NORMAL to PLL mode.	The PLL-IDLE allows time for the <u>clock from PLL</u> to stabilize when the software is changing from NORMAL to PLL mode.
	23	Description addition	This LSI has <u>two</u> system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and...	This LSI has <u>three</u> system clock oscillation circuits. OSC <u>or PLL</u> is for high-frequency operation (NORMAL<u>, PLL</u> mode) and
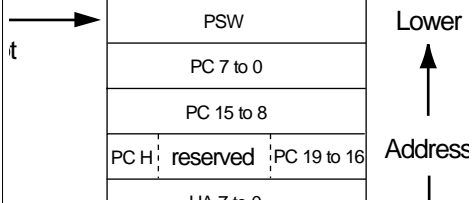
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-44	Second Note	Description change	In <u>idle</u> state, the clock of the oscillator for ...	In <u>OSC-IDLE</u> state, the clock of the oscilla-tor for ...
	Third Note	Description addition	-	<u>When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand...</u>
II-45		Description deletion	-	Page II-42 of the former edition deleted.
	Figure 2.5.2	Description change	Operation mode HALT0 OSCI/OSCO Oscillation System clock OSCI	Operation mode HALT0 <u>(HALT2)</u> OSCI/OSCO Oscillation<u>(PLL Oscillation)</u> System clock OSCI<u>(PLL)</u>
	3	Description change	1. <u>If the return factor is a maskable ...</u> 2. <u>Clear the interrupt request flag ...</u>	1. <u>Clear the interrupt request flag ...</u> 2. <u>If the return factor is a maskable ...</u>
II-46	First Note	Error correction	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock swiching function (OSCDBL, OSCSEL1 and <u>OSCSEL2</u> flags) at the same time.	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock swiching function (OSCDBL, OSCSEL1 and <u>OSCSEL0</u> flags) at the same time.
	Second Key	Description addition	... to clear interrupt request flag by software.	... to clear interrupt request flag by soft-ware. <u>After clear interrupt request flag, must clear the IRWE flag.</u>
	Second Note	Description addition	<u>-</u>	<u>The STOP, the HALT, the OSC1 or the OSC0 flags of the CPUM mode control ...</u>
II-47	1	Error correction	This LSI has <u>two</u> CPU operating modes, NORMAL and SLOW.	This LSI has <u>three</u> CPU operating modes, NORMAL, <u>PLL</u> and SLOW.
	First Note	Description addition	-	<u>We recommend selecting the oscillation stabilization time of slow oscillation after consulting with oscillator manufacturers.</u>
	Third Note	Description addition	-	<u>When SLOW mode, don't operate the peripheral circuits by a hihg-speed oscilla-tion. A high-speed oscillation has stopped at the SLOW mode.</u>
II-48	1	Error correction	This LSI has <u>two PLL</u> operating modes, <u>NOR-MAL and PLL</u>.	This LSI has <u>three CPU</u> operating modes, <u>NORMAL, PLL and SLOW</u>.
	Program 1 line 2	Description addition	Program 1 BCLR (PLLCNT) 1...	Program 1 <u>BSET (XSEL)2 ; Built-in ROM accsess method setting</u> BCLR (PLLCNT) 1...
	First Note	Description addition	-	<u>When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand...</u>

	Program 3 line 2	Error correction	Program 3
			    MOV x'<u>03</u>', D0 ; A loop ...
				Program 3
				    MOV x'<u>43</u>', D0 ; A loop ...

	Second Note	Description addition	-	<u>Necessary time for steady operation of PLL is 100 μs. The stabilization waiting time is inserted by software.</u>
	Third Note	Description addition	-	<u>Do neither multiplication setting of PLL nor oscilattion start of PLL at the same time.</u>

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-49	Figure 2.5.3	Error correction		
II-50	Second Note	Description change	Set bp5 of XSEL register (0x03F2F) before the transition to slow oscillation mode.	When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).
II-51	First Note	Description change	Key	Note
	Second Note	Description change	Key	Note
	Third Note	Description change	Set bp5 of XSEL register (0x03F2F) before the transition to slow oscillation mode.	When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).
	Fourth Note	Description addition	-	When can't ensure to generate the return interrupt sources after transmition request for standby mode (HALT/STOP) by setting to CPUM register, refer to [2.5.6 Attention of Transition to Standby Mode].
II-52	Chapter	Description addition	-	2.5.6 Attention of Transition to Standby Mode
II-53	5,9	Description change	low-fregency oscillation selection register (XSEL)	low-speed oscillation selection register (XSEL)
	Program 6 line 2	Description addition	Program 6 MOV x'20', (XSEL) ; Set... MOV x'02', (TM0MD) ; Select ...	Program 6 MOV x'20', (XSEL) ; Set... MOV x'FF', D0 LOOP ADD -1, D0 BNE LOOP ; Loop to ... MOV x'02', (TM0MD) ; Select...
II-54	Page	Description addition	-	Low-speed oscillation is also ... - Low-speed oscillation selection register (XSEL) ...
II-55	Chapter	Description addition	-	2.5.8 Method for Accessing to Internal ROM
II-57	CPUM bp7	Description change	Description Set always to "0"	Description Always set to "0" *
	First Note	Description addition	-	Always set "0" to the bp denoted by asterisk.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-58	First Note	Error correction	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock swiching function (OSCDBL, OSCSEL1 and OSCSEL2 flags) at the same time.	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock swiching function (OSCDBL, OSCSEL1 and OSCSEL0 flags) at the same time.
	Second Note	Error correction	Set the dividing ratio of oscillation clock to meet the operating condition (refer to Chapter 1 "Electrical Characteristics"). When the dividing ratio is 1, the frequency of fosc should not exceed the maximum frequency of fs (fosc: high-speed oscillation clock, fs: system clock)....	Set the dividing ratio of oscillation clock and transition to the operation mode to meet the operating condition (refer to Chapter 1 "Electrical Characteristics").
	Third Note	Description change	When system clock is over 10 MHz, set bp2 of XSEL register (0x03F2F) before the setting of PLLCNT	When system clock is over 10 MHz, set bp2 of XSEL register (0x03F2F) and change the access method to built-in ROM area to handshake
II-59	1	Description change	Hgh-speed oscillation clock multiply function is to generate a clock , 2-fold, 3-fold, 4-fold, 5-fold, 6-fold, 8-fold and 10-fold of high-speed oscillation input from OSC1/OSC2.	High-speed oscillation clock multiply function is to generate a clock , 2/ 3/ 4/ 5/ 6/ 8/ 10-multiply of high-speed oscillation input from OSC1/OSC2.
	Figure 2.7.1	Description change	fold	multiply
	PLLCNT bp7-4	Description change	Flag desciption 4' h0: 2-fold (Input frequency 4-7.5 MHz) 4' h1: 2-fold (Input frequency 7.5-10 MHz) 4' h2: 3-fold (Input frequency 4-5 MHz) 4' h3: 4-fold (Input frequency 4-7.5 MHz) 4' h4: 4-fold (Input frequency 7.5-10 MHz) 4' h5: 5-fold (Input frequency 4-6 MHz) 4' h6: 5-fold (Input frequency 6-8 MHz) 4' h7: 6-fold (Input frequency 4-5 MHz) 4' h8: 8-fold (Input frequency 4-5 MHz) 4' h9: 10-fold (Input frequency 4 MHz)	Flag desciption 4' h0: 2-multiply (Input frequency 4-7.5 MHz) 4' h1: 2-multiply (Input frequency 7.5-10 MHz) 4' h2: 3-multiply (Input frequency 4-5 MHz) 4' h3: 4-multiply (Input frequency 4-7.5 MHz) 4' h4: 4-multiply (Input frequency 7.5-10 MHz) 4' h5: 5-multiply (Input frequency 4-6 MHz) 4' h6: 5-multiply (Input frequency 6-8 MHz) 4' h7: 6-multiply (Input frequency 4-5 MHz) 4' h8: 8-multiply (Input frequency 4-5 MHz) 4' h9: 10-multiply (Input frequency 4 MHz)
	PLLCNT bp7-4	Error correction	Flag description ... 4' h9: 10-fold (Input frequency 4 MHz)	Flag description ... 4' h9: 10-multiply (Input frequency 4 MHz) 4' h10-15: Setting prohibited
	First Note	Description deletion	When system clock is over 10 MHz, set bp 2 of XSEL register (0x03F2F) before the setting of PLLCNT.	-
II-60	2 Setup procedure(1)(4)	Description change	2-fold	2-multiply
	Setup procedure	Description addition	-	(3) MOV 0x43, D0 LOOP ADD -1, D0 BNE LOOP
	Description	Description addition	-	(3) Wait PLL operation waiting time 100 μs by software.(4 MHz)

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-61	First Note	Description addition	The setup described above can not be done at the same time.	The setup described above can not be done at the same time. When set PLL, has to switch by above setting.
	Second Note	Description change	Set in order of (3) and (2) for transition to NORMAL mode.	Switch in the bit order of (4) and (2) for transition to NORMAL mode.
	Fifth Note	Description addition	-	Don't set PLLSTART flag by the state of PLLEN flag = "0" of PLLCNT register.
	First Key	Description addition	Refer to [2.5 Standby Function] for operation mode trasition.	Refer to [2.5 Standby Function] for operation mode trasition. The direct transition from the slow mode to the Pll mode can not be enabled...
	Sixth Note	Description addition	-	When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand...
	Seventh Note	Description addition		The operation does not guaranteed if the system clock operates over 20MHz. Set the multiply number in 20MHz or...
II-62	First Note	Description change	This LSI is activated in NORMAL mode in which the base clock is high frequency.	This LSI is activated in NORMAL mode in which the base clock is external high-speed oscillation.
	Third Note	Description addition	In this LSI, the oscillation (High-speed oscillation and Low speed oscillation) is stopped.	In this LSI, the oscillation (High-speed oscillation and Low speed oscillation) is stopped at reset.
II-63	Square	Description addition	-	- Reset Sequence at the time of Power Supply Injection.
II-65	Figure 2.8.4	Error correction		
II-66	First Note	Description change	Please set the value by which on oscillation circuit is stabilized enough to the waiting cycle for oscillation stability.	For the oscillation stabilization wait cycle required for high-speed/low-speed oscillation, which is set by DLYS 1-0 flags, it is recommended to consult the oscillator manufacturer for determining appropriate values.
	Second Note	Description addition	-	When recovering from STOP mode, more than 100 µs of oscillation stabilization wait cycle must be set for internal regulator output stabilization wait.
	2 from the bottom	Description Deletion	*1 Do not use at the high-speed operation (NORMAL mode, PLL mode). Use at the low-speed operation (SLOW mode.	-

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-68	2	Description addition	-	Auto reset function can be selected with ATRST pin (11 pin) - In using auto reset --- ATRST pin (11 pin) : V_{DD5} level fixed - In not using auto reset --- ATRST pin (11 pin) : V_{SS} level fixed
	5	Description change	After detecting a low voltage, NRST pin automatically becomes "L" level and reset operation is executed. When power supply voltage reaches reset cancellation voltage (VRST), NRST pin automatically becomes "H" and reset is cancelled.	When detecting a low voltage at auto reset function, NRST pin automatically becomes "L" level and reset operation is executed. When power supply voltage reaches reset cancellation voltage (VRST), NRST pin automatically becomes "H" and reset is cancelled.
	Figure 2.9.1	Error correction	Figure:2.9.1 V_{DD} RST	Figure:2.9.1 Auto Reset Detection Voltage V_{DD5} NRST
	First Key	Description addition	-	Refer to [Chapter I 1.5.7 Auto Reset Characteristics] for VRST.
	First Note	Description addition	-	When use the auto reset function, "L" level input to NRST pin has to keep at least 100 μs or more. Connect ...
II-70	First Note	Description addition	-	Don't set a number of bits at the same time.
III-3	Table 3.1.1	Description addition	-	IVBM=0 IVBM=1 0x00104 0x00108 to 0x00178
III-5	Figure 3.1.2	Description addition	Save PC, PSW, etc Restore PSW, PC, etc	Save PC, PSW, HA, etc Restore PSW, PC, HA, etc
III-6	Table 3.1.2	Description addition	Vector Addresses 0x04000 | 0x04078	Vector Addresses IVBM = 0 IVBM = 1 0x04000 0x00100 | | 0x04078 0x00178
III-7	5	Error correction	For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupt simultaneously, vector 3 will be accepted.	For example, if a vector 3 set to level 1 and a vector 4 set to level 1 request interrupt simultaneously, vector 3 will be accepted.
	Figure 3.1.3	Error correction	Level1 Vector 3 Level2 Vector 4, 8	Level1 Vector 3, 4 Level2 Vector 8
III-8	Square	Error correction	1. The interrupt request flag (xxxR)	1. The interrupt request flag (xxxIR)
	Square	Description change	-	2. to 3. in Determination of Maskable Interrupt Acceptance changed
	Note	Description addition	-	After accept of an interrupt, interrupt of same source is disregarded until ...
III-9	8	Error correction	BE instruction is executed. (BKD is set and MIE is set	BD instruction is executed. (BKD is set and MIE is set
	16	Error correction	Non-Maskable interrupt is accepted (it to 0 (oob)).	Non-Maskable interrupt is accepted (it to 0 (00b)).
	Note	Description change	The MN101C series does not reset the maskable interrupt enable (MIE) flag of the processor status word (PSW) to "0" when accepting interrupts.	The maskable interrupt enable (MIE) flag of the processor status word (PSW) is not set to "0" when accepting interrupts.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)

III-10	8	Error correction	2. The contents of the handy addressing...
			   Upper ...
			   Lower...
			 3. The contents of the program counter...
			   PC bits 20 to 17...
			   PC bits 16 to 9...
			   PC bits 8 to 1...
				2. The contents of the program counter...
				   PC bits 7 to 0...
				   PC bits 15 to 8...
				   PC bits 19 to 16...
				 3. The contents of the handy addressing
				   Lower...
				   Upper ...

	Figure 3.1.5	Error correction		
III-11	Second Note	Error correction	The address bp6 to bp4, when program counter (PC [bit20 to bit17, bit0]) are...	The address bp6 to bp4, when program counter (PC [bit19 to bit16, bitH]) are ...
III-17	First Note	Description addition	-	Interrupt request flag of interrupt control register is set by interrupt generation, the edge ...
	Second Note	Description addition	-	Alway set IRWE flag of memory control register (MEMCTR) to "0" except in writing IR with ...
	Third Note	Description addition	-	Make processore status word (PSW) and mascable interrutp enable flag (MIE) of prohibited ...
III-19	Third Note	Description addition	-	When interrupt request of same bit and above-mentioned request flag by the software is generated ...
III-20	Description	Description addition	(5) ... contents to clear the flags.	(5) ... contents to clear the flags. It clears by this method because there is a possibility that internal interrupt ...
	Description	Description addition	(6) ... interrupt control register (PERIIRQ).	(6) ... interrupt control register (PERIIRQ). It clears by this method because there is a possibility that interrupt request flag has already been set.
	Setup procedure	Description addition	-	(7) Disable writing of the interrupt request flag. MEMCTR(0x03F01) bp2:IRWE =0
	Description	Description addition	-	(7) Clear the IRWE flag to disable writing of the interrupt request flag by software.
	Setup procedure	Description deletion	(9) Clear the extended interrupt request flag IRQEXPDT(0x03F4F) bp x:IRQEXPDTx=1	-
	Description	Description deletion	(9) Write "1" in the appropriate flags of the internal interrupt extended interrupt factor holding register (IRQEXPDT) to clear the request flags.	-
	First Note	Description addition	-	Extended interrupt request flag (IRQEXPDT) is set by interrupt generation regardless of setting

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-21	Square	Description addition	-	- Example of Internal Interrupt Extended Interrupt Processing Program
III-23	Second Note	Description addition	Writing to the interrupt control register should be done after that all maskable interrupts are set to be disable by the MIE flag of the PSW register.	Make processore status word (PSW) and mascable interrupt enable flag (MIE) of prohibited all mascable interrupts (Set MIE flag to "0") before writing to interrupt control register (xxxICR). If writing to interrupt control register with setting MIE flag to "1", we can not guarantee normal operation.
III-24	1,5	Error correction	NMICTR	NMICR
	3	Description addition	the external interrupt control register	the external interrupt control register(IRQnICR)
	10	Description deletion	Setting IRQNPG or IRQNWDG flag to be "1" enables non-maskable interrupt request to be set compulsory.	-
	NMICR bp0	Description change	Description Set always to "0"	Description Always set to "0" *
	Second Note	Description addition	-	Always set "0" to the bp denoted by asterisk.
III-26	bp1 bp0	Error correction	Flag TM0IE TM0IR	Flag TMnIE TMnIR
III-43	IRQEXPDT bp7	Description addition	Description Always set to "0"	Description Always set to "0" *
III-44	First Note	Description addition	-	Peripheral Function Group Interrupt can not be used as a returning source from the standby mode.
	Second Note	Description addition	-	Always set "0" to the bp denoted by asterisk.
	Third Note	Description addition	-	When interrupt request of same bit and above-mentioned request flag by the software is generated ...
III-45	Chapter 3.2.3	Description addition	-	3.2.3 Internal Interrupt Extended Interrupt Interface Block Diagram
III-47 to 52	Figure 3.3.1 3.3.2 3.3.3 3.3.4 3.3.5	Error correction	fosc	fpll
	Figure 3.3.1 3.3.2 3.3.3 3.3.4 3.3.5 3.3.6	Description addition	"Stanby mode signal reverse" in "External Interrupt 1-4 Block Diagram" : AND	"Standby mode signal" in "External interrupt 1 to 4 block diagram" : Delete

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-49	Figure 3.3.3	Error correction	*(circuit diagram: EDGSEL7 7, Standby mode signal, IRQ2, Noise filter, MUX, Level detection circuit, MUX, Match detection circuit, fs, D C, fx, fosc, Counter, NF2CTR, PS2CNT0, PS2CNT1, PS2CNT2, NF2EN0, NF2EN1, NF2SCK0, NF2SCK1, LVLMD, LVLEN2, EXLVL2, LVLEN3, EXLVL3, LVLEN4, EXLVL4, IRQ2ICR, ICR2IR, ICR2IE, REDG2, ICR2LV0, ICR2LV1)*	*(circuit diagram: EDGSEL7 7, Standby mode signal, IRQ2, Noise filter, MUX, Level detection circuit, MUX, Match detection circuit, fs, D CK S, fx, fpll, Counter, NF2CTR, NF2EN1, NF2SCK0, NF2SCK1, NF2SCK2, LVLMD, LVLEN2, EXLVL2, LVLEN3, EXLVL3, LVLEN4, EXLVL4, IRQ2ICR, ICR2IR, ICR2IE, REDG2, ICR2LV0, ICR2LV1)*
III-50	Figure 3.3.4	Error correction	*(circuit diagram: EDGSEL7 7, Standby mode signal, IRQ4, Noise filter, MUX, Level detection circuit, MUX, Match detection circuit, fs, D C, fx, fosc, Counter, NF4CTR, PS4CNT0, PS4CNT1, PS4CNT2, NF4EN0, NF4EN1, NF4SCK0, LVLMD, LVLEN2, EXLVL2, LVLEN3, EXLVL3, LVLEN4, EXLVL4, IRQ4ICR, ICR4IR, ICR4IE, REDG4, ICR4LV0, ICR4LV1)*	*(circuit diagram: EDGSEL7 7, Standby mode signal, IRQ4, Noise filter, MUX, Level detection circuit, MUX, Match detection circuit, fs, D C, fx, fpll, Counter, NF4CTR, NF4EN1, NF4SCK0, NF4SCK1, LVLMD, LVLEN2, EXLVL2, LVLEN3, EXLVL3, LVLEN4, EXLVL4, IRQ4ICR, ICR4IR, ICR4IE, REDG4, ICR4LV0, ICR4LV1)*
III-51	Figure 3.3.5	Error correction	*(circuit diagram: EDGSEL7 7, Standby mode signal, IRQ4, Noise filter, MUX, Level detection circuit, MUX, Match detection circuit, fs, D C, fx, fosc, Counter, NF4CTR, PS4CNT0, PS4CNT1, PS4CNT2, NF4EN0, NF4EN1, NF4SCK0, LVLMD, LVLEN2, EXLVL2, LVLEN3, EXLVL3, LVLEN4, EXLVL4, IRQ4ICR, ICR4IR, ICR4IE, REDG4, ICR4LV0, ICR4LV1)*	*(circuit diagram: EDGSEL7 7, Standby mode signal, IRQ4, Noise filter, MUX, Level detection circuit, MUX, Match detection circuit, fs, D C, fx, fpll, Counter, NF4CTR, NF4EN1, NF4SCK0, NF4SCK1, LVLMD, LVLEN2, EXLVL2, LVLEN3, EXLVL3, LVLEN4, EXLVL4, IRQ4ICR, ICR4IR, ICR4IE, REDG4, ICR4LV0, ICR4LV1)*
III-52	Figure 3.3.6	Error correction	*(large circuit block diagram)*	*(large circuit block diagram)*
III-56	NF0CTR to NF4CTR	Error correction	Flag, Description bp3: NFnEN0, ... bp2-0: PSnCNT2-0, ...	Flag, Description bp3-0: Reserved, Always set to "0".
	2 from the bottom	Description Deletion	*1 Sampling function is incorporated only in IRQ2, 3. *2 bp3-0 is only NF2CTR,NF3CTRÇ	-

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-58	2	Description change	Both edges interrupt control register (EDGDT) select interrupt edges of IRQ2 to 5. With this register, the edge to generate the interrupts is selected; both edges or the edge which is specified by the external interrupt control register (IRQ2ICR, IRQ3ICR, IRQ4ICR).	Bp 2,3,5 of both edges interrupt control register (EDGDT) select interrupt edges of IRQ2 to 4. With this register, the edge to generate the interrupts is selected; both edges or the edge which is specified by the external interrupt control register (IRQ2ICR, IRQ3ICR, IRQ4ICR). When the edge detection circuit in the key interrupt block is used with bit common/bit independant or bit independant, the edge to generate the interrupt is selected; both edges or the edge which is specified by the external interrupt control register (IRQ5ICR) with the register selecting IRQ5 key interrupt edge.
	EDGDT	Description change	bp7 Description Key interrupt both edges operation selection 1 0:Programmable active edge interrupt selection 1:Both edges interrupt selection	bp7 Description IRQ5 Key interrupt both edges operation selection (Enable at bp:0 EDGSEL0 ="1") 0:Programmable active edge interrupt selection (Specified with IRQ5ICR bp:5 REDG5) 1:Both edges interrupt selection
		Description change	bp5 Description 0:Programmable active edge interrupt selection	bp5 Description 0:Programmable active edge interrupt selection (Specified with IRQ4ICR bp:5 REDG4)
		Description change	bp3Description 0:Programmable active edge interrupt selection	bp3 Description 0:Programmable active edge interrupt selection (Specified with IRQ3ICR bp:5 REDG3)
		Description change	bp2 Description 0:Programmable active edge interrupt selection	bp2 Description 0:Programmable active edge interrupt selection (Specified with IRQ2ICR bp:5 REDG2)
		Description change	bp0 Description Key interrupt both edges operation selection 2 0:Falling edge ("L" level) 1:Rising edge ("H" level)	bp0 Description IRQ5 Key interrupt selection 0:Key input Edge detection circuit bit common * 1:Key input Edge detection circuit bit independant
	Last line	Description addition	-	* Detail of operation refers to [3.3.7 Key Input Interrupt].
III-59	First Key	Description addition	-	If the key input edge detection circuit is selected bit common with EDGSEL0 flag, the ...
	Second Key	Description addition	-	If the key input edge detection circuit is selected bit independant with EDGSEL0 flag ...
	First Note	Description addition	-	EDGSEL7 flag is enable only when the key input edge detection circuit is selected bit independant with EDGSEL0 flag ...

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-60	LVLMD	Description addition	bp5 Description External interrupt 4 Enable Input Level setup 0:L level 1:H level	bp5 Description External interrupt 4 Enable Input Level setup (Enable at bp:4 LVLEN4="1") 0:L level 1:H level
		Description addition	bp3 Description External interrupt 3 Enable Input Level setup 0:L level 1:H level	bp3 Description External interrupt 3 Enable Input Level setup (Enable at bp:3 LVLEN3="1") 0:L level 1:H level
		Description addition	bp1 Description External interrupt 2 Enable Input Level setup 0:L level 1:H level	bp1 Description External interrupt 2 Enable Input Level setup (Enable at bp:2 LVLEN2="1") 0:L level 1:H level
III-63	First Key	Description addition	... so that unknown value is not input.	... so that unknown value is not input. If unknown value is input to pin, through current flow.
III-64	Description	Error correction	(4) Set the IRQ2E flag of ...	(4) Set the IRQ2IE flag of ...
III-65	Second Key	Description addition	... so that unknown value is not input.	... so that unknown value is not input. If unknown value is input to pin, through current flow.
III-67	Third Note	Description change	Key	Note
III-68	3	Description addition	…Also, if the key input pin becomes low level, it is possible from the standby mode.	… Also, if the key input pin becomes low level, it is possible to return from the standby mode. When rising edge is set by the external interrupt 5 (ICR5IRQ), the key input default state is changed from "L" to "H".
	Setup Procedure	Error correction	(1) Set the key input to input P5DIR(0x03F35) bp3-0:P5DIR7-0=00000000	(1) Set the key input to input P5DIR(0x03F35) bp7-0:P5DIR7-0=00000000
III-70	Square	Description deletion	Noise remove Function Operation After sampling the input signal to ... , the previous level is sent. It means that only the signal ...	Noise remove Function Operation After sampling the input signal to ... , the previous level is sent.
III-72	Setup procedure	Description change	(1),(2),(3),(4),(5)	(1)→(2),(2)→(3),(3)→(4),(4)→(5),(5)→(6)
	Setup procedure	Description addition	-	(1) External interrupt setup IRQCNT (0x03F3D) bp0:P20EN =1
	Description	Description addition	-	(1) Set the P20EN flag of the external interrupt setting register (IRQCNT) to "1" to set P20 to external interrupt.
	Setup procedure	Error correction	(3) bp2-1	(3) bp7-5
	Setup procedure	Error correction	(4) bp0	(4) bp4
	3 from the bottom	Description change	Above (2) and (3) can be set at the same time.	Above (3) and (4) can be set at the same time.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IV-3	First Key	Description addition	-	The values of pull-up/pull-down resistors should be calculated in the following ways based on the electrical ...
IV-14 IV-28 IV-41 IV-54 IV-68 IV-82 IV-95 IV-110	2	Description addition	-	The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized "H" can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.
	bp7 to bp0	Description change	Port 7 Port 6 Port 5 Port 4 Port 3 Port 2 Port 1 Port 0	Port 70 to Port 77 Port 60 to Port 67 Port 50 to Port 57 Port 40 to Port 47 Port 30 to Port 36 Port 20 to Port 24 Port 10 to Port 16 Port 00 to Port 07
IV-16-23	Chapter	Description addition	-	Add block diagram of each port 4.3.3 Block Diagram
IV-31-37	Chapter	Description addition	-	Add block diagram of each port 4.4.3 Block Diagram
IV-43-48	Chapter	Description addition	-	Add block diagram of each port 4.5.3 Block Diagram
IV-49	3 from the bottom	Error correction	... When the SC4SBOS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", ...	... When the SC4SBTS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", ...
IV-50	1	Error correction	... When the SC2SBIS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", ...	... When the SC4SBIS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", ...
IV-56-62	Chapter	Description addition	-	Add block diagram of each port 4.6.3 Block Diagram
IV-70-77	Chapter	Description addition	-	Add block diagram of each port 4.7.3 Block Diagram
IV-85-90	Chapter	Description addition	-	Add block diagram of each port 4.8.3 Block Diagram
IV-97-104	Chapter	Description addition	-	Add block diagram of each port 4.9.3 Block Diagram
IV-112-119	Chapter	Description addition	-	Add block diagram of each port 4.10.3 Block Diagram
IV-127 IV-139 IV-150 IV-163	3 or 2	Description addition	-	The input level of P8 (P80 to P87) to PB (PB0 to PB7) recognized "H" can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.
	bp3 to bp0	Description change	Port B Port A Port 9 Port 8	Port B0 to Port B7 Port A0 to Port A7 Port 90 to Port 96 Port 80 to Port 87
IV-128-135	Chapter	Description addition	-	Add block diagram of each port 4.11.3 Block Diagram
IV-140-143	Chapter	Description addition	-	Add block diagram of each port 4.12.3 Block Diagram

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IV-146	Square	Error correction	-Port A Pull-up Resistor Control Register(PAPLUD:0x03F4A)	-Port A Pull-up Resistor Control Register(PAPLU:0x03F4A)
IV-151-158	Chapter	Description addition	-	Add block diagram of each port 4.13.3 Block Diagram
IV-164	Chapter	Description addition	-	Add block diagram of each port 4.14.3 Block Diagram
IV-166	Second Note	Description addition	-	When real time output realease (the write operation to P8CNT1, P8CNT2 and PACNT) and the event generation ...
IV-167	Figure 4.15.1	Error correction	PATCNT set value — Timer output — PATCNT s... Write operation to PAOUT register	PATCNT set value — Timer output — PATCN... Write operation to PACNT register
IV-169	Square	Error correction	- Port 8 Synchrounous Output (Timer 1,2 and 7) ... The port 8 output latched data is output from the port 7 at the timing of the TMnIRQ flag rising.	- Port 8 Synchrounous Output (Timer 1,2 and 7)... The port 8 output latched data is output from the port 8 at the timing of the TMnIRQ flag rising.
V-3	Table Clock source of Time 1	Error correction	Synchronous TM1O input	Synchronous TM1IO input
V-11	CK1MD	Error correction	bp3-0 0X11 : fs/4 1XX1 : fs/8	bp3-0 0X11 : fs/8 1XX1 : fs/4
V-12	CK3MD	Error correction	bp3-0 0X11 : fs/4 1XX1 : fs/8	bp3-0 0X11 : fs/8 1XX1 : fs/4
V-26	Table	Description change	fosc=10 MHz	fpll=fosc=10 MHz
V-28	First Key	Description addition	... = (count till the interrupt request -1)	... = (count till the interrupt request -1) However, the interrupt generation cycle when the compare register is set to "00" is the same as it is set to "01".
	Third Key	Error correction	If the interrupt is enabled, the timer interrupt request ...	If the timer interrupt request flag may have already been set before timer is started, the timer interrupt request ...
V-29	First Key	Description deletion	If "00" is specified for the Compare Register (TMnOC), an interrupt timing is the same as if you set it to "01".	-
	First Note	Description addition	-	If CPU operation mode is changed (from NORMAL to SLOW) when the high-frequency oscillation clock (fpll) or ...

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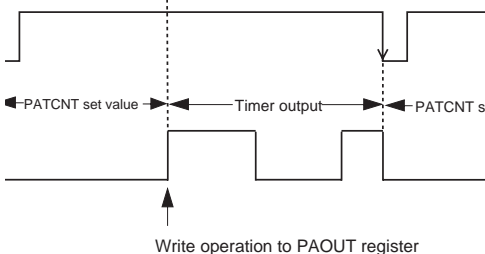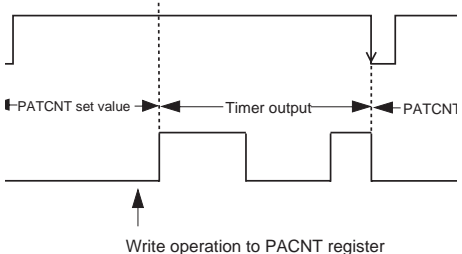| Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
V-33	First Key	Description change	<u>Note</u>	<u>Key</u>
	First Note	Description addition	-	<u>Input from TMnIO should be used to a waveform, which has 2 times and over cycles of system clock (fs). If less than the above waveforms are input, it may not be counted correctly.</u>
V-34	Setup procedure	Error correction	(3)Set the special function pin to input PADIR(0x03F3A) bp0 :PADIR0 =0	(3)Set the special function pin to input PADIR(0x03F3A) bp0 :PADIR0 =0 <u>TMINSEL1(0x03E44)</u> <u>bp1-0: TMINSEL11-10=00</u> <u>TMCKSEL1(0x03E42)</u> <u>bp0 :TM0IOSEL =0</u>
	Description	Error correction	(3) Set the PADIR0 flag of the port A direction control register (PADIR) to "0" <u>to set PA0 pin to input mode.…</u>	(3) Set the PADIR0 flag of the port A direction control register (PADIR) to "0", <u>TMINSEL11 to 10 flag of TMINSEL1 register to "00" and TM0IOSEL of TM0IOSEL1 register to "0" in order to set PA0 pin to input mode.</u>
	Setup procedure	Description deletion	(4) Select the count clock source <u>TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01</u>	-
	Description	Description deletion	(4) <u>Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.</u>	-
V-38	First Key	Description change	If any data is written to compare register when the binary counter is stopped, timer output is <u>reset to "L".</u>	If any data is written to compare register when the binary counter is stopped, timer output is "L".
V-40	3	Error correction	(A) is"H" while <u>counting</u> up from 0x01 ...	(A) <u>TMnIO output</u> is "H" while <u>the value of binary counter count</u> up from 0x01 ...
	5	Error correction	(B) is "L" after the match to the value ...	(B) <u>TMnIO output</u> is "L" after the <u>value of bunary counter</u> match to the value
V-42	5,6,8,9 Table 5.7.2	Error correction	<u>bits 4 and 5</u> of CK*MD Table:5.7.2 <u>bit5, bit4</u>	<u>bits 5 and 6</u> of CK*MD Table:5.7.2 <u>bit6, bit5</u>
V-43	First Note	Description addition	-	<u>Do not change the setting of Timer n prescaler selection register (CKnMD) during timer operation.</u>
V-44	Description	Description addition	(3) Set the TM0PWM flag of the TM0MD register to "1" and the TM0MOD flag to "0" to select the PWM operation.	(3) Set the TM0PWM flag of the TM0MD register to "1"<u>, the TM0MOD flag to "0" and TM0POP flag to "0"</u> to select the PWM operation.
V-47	Description	Error correction	(2) Set the P8SEV1 to 0 flag of the pin control register (P8SEV) to "11" to set the synchronous output event to <u>the timer 2 interrupt.</u>	(2) Set the P8SEV1 to 0 flag of the pin control register (P8SEV) to "11" to set the synchronous output event to <u>the timer 1 interrupt.</u>
V-50	2 from the bottom	Error correction	... TMnEN flag is <u>ON</u> ("1") and ...	... TMnEN flag is <u>operated</u> ("1") and ...
V-51	Setup procedure(4)	Error correction	bp<u>2-1</u> : TM0PSC1<u>-0</u> = <u>X0</u>	bp<u>3-1</u> : TM0PSC<u>2-0</u> = <u>0X0</u>

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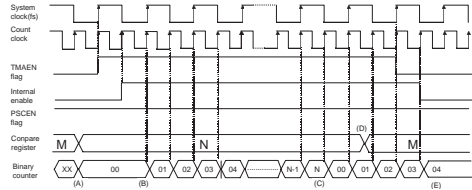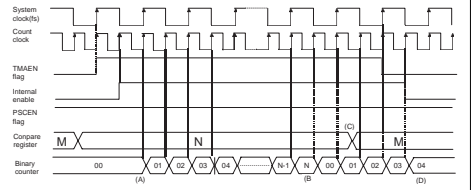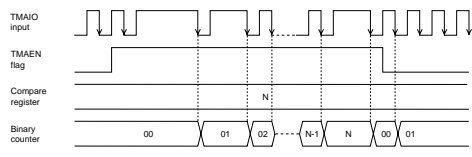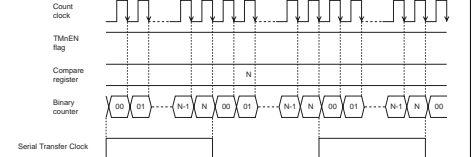| Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
V-52	5.11.1	Description change	5.11.1 Operation	5.11.1 <u>16-bit Cascade Connection</u> Operation
	Square	Description deletion	<u>8-bit Timer Cascade Connection</u> Operation	Operation
	Table	Description change	Table 5.11.1 Timer Functions at Cascade Connection	Table 5.11.1 Timer Functions at <u>16-bit</u> Cascade Connection
V-53	Third key	Description change	At cascade connection, when ...	At <u>16-bit</u> cascade connection, when ...
	Second Note	Description addition	-	<u>Stop the timer in order to read out the balue of timer connected in cascade</u>
V-54	Table	Description change	Table 5.11.2 Timer Functions in Cascade Connection	Table 5.11.2 Timer Functions in <u>24-bit</u> Cascade Connection
V-55	Second Key	Description change	At cascade connection, when ...	At <u>24-bit</u> cascade connection, when ...
	Third Note	Description addition	-	<u>Stop the timer in order to read out the balue of timer connected in cascade</u>
V-56	Table	Description change	Table 5.11.3 Timer Functions in Cascade Connection	Table 5.11.3 Timer Functions in <u>32-bit</u> Cascade Connection
V-57	Second Key	Description change	At cascade connection, when ...	At <u>32-bit</u> cascade connection, when ...
	Third Note	Description addition	-	<u>Stop the timer in order to read out the balue of timer connected in cascade</u>
V-58	Square	Description addition	- Cascade Connection Timer Setup Example (Timer 0 + Timer 2)	- <u>16-bit</u> Cascade Connection Timer Setup Example (Timer 0 + Timer 2)
	Description	Description addition	(1) Set the TM0EN flag ... , the TM1EN flag of the timer 1 mode register to "0" to stop ...	(1) Set the TM0EN flag ... , the TM1EN flag of the timer 1 mode register <u>(TM1MD)</u> to "0" to stop ...
	Setup Procedure(7)	Description change	<u>TMnOC</u> (0x03F52,0x03F53) = 0x09C3	<u>TM1OC,TM0OC</u> (0x03F53,0x03F52) = 0x09C3
VI-2	1	Description change	This timer is a 8-bit simple timer that can be used as a serial transfer clock, LCD <u>frequency or timer count</u>.	This timer is a 8-bit simple timer that can be used as a serial transfer clock, LCD <u>clock or 8 bit/16 bit timer count</u>.
	9	Description change	Table:6.1.1 shows <u>functions that can be used with each timer.</u>	Table:6.1.1 shows <u>clock sources of 8-bit simple timer.</u>
VI-3	Figure 6.1.1	Error correction		
VI-5	5	Description change	<u>If any data is written to compare register the counting is stopped and binary counter</u> is cleared to 0x00.	<u>The binary counter to stop the count operation</u> is cleared to 0x00.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VI-6	TMAMD1	Error correction	bp4 Flag :- At reset :- Access :- Description :-	bp4 Flag :Reserved At reset :0 Access :R/W Description :Always set to "0"
VI-7	TMAMD2	Error correction	bp7 : Access -	bp7 : Access R/W
		Error correction	bp6 Description Timer A count control	bp6 Description Prescaler operation control
VI-8	1	Description deletion	8-bit simple timer contains one timer as an auxiliary function of "Chapter 5 8-bit Timers ".	8-bit simple timer in this LSI contains one timer as only a basic function of "Chapter 5 8-bit Timers ".
	Note	Description addition	-	When fpll is selected the clock source, prescaler operation control frag (PSCEN flag of TMAMD2 register) is set necessary before set TMAEN flag.
VI-9	Figure 6.3.1	Description deletion		
	4	Description deletion	(A) If the value is written to the compare register during the TMAEN flag is stopped ("0"), the binary counter is cleared to 0x00.	-
	11	Error correction	(E) When the TMAEN flag stops operating ("0"), the Internal Enable will be turned off at the next Count Clock. As a result, the binary counter stops counting.	(D) When the TMAEN flag stops operating ("0"), the binary counter stops counting and cleared to 0x00.
	Third Note	Description deletion	When the compare register (TMAOC) is set to '00', clear the binary counter before starting the operation.	-
VI-10	Figure 6.4.1	Error correction		
	First Key	Description addition	-	The output signal of this timer can use as the clock source of 8-bit timer/16-bit timer as well as above-mentioned the serial transfer clock.
VI-11	Description	Description deletion	(3) ... that the baud rate comes to 300 bps. At that time, the timer A binary counter (TMABC) is initialized to 0x00.	(3) ... that the baud rate comes to 300 bps.
VII-2	1	Description addition	The 16-bit timer has compare register with double buffer.	The 16-bit timer has compare register with double buffer and single buffer. The buffer can be selected.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-3	Table 7.1.1	Error correction	T7OC2IRQ T8OC2IRQ T9OC2IRQ	TM7OC2IRQ TM8OC2IRQ TM9OC2IRQ
		Description addition	Clock source ... Synchronous TM7IO/16 input	Clock source ... Synchronous TM7IO/16 input Timer A output Timer A output/2 Timer A output/4 Timer A output/16
VII-4	Figure 7.1.1	Error correction		
VII-5	Figure 7.1.2	Error correction		
VII-6	Figure 7.1.3	Error correction		
VII-12	1	Description addition	Binary counter is a 16-bit up counter. If any data is written to a preset register when ...	Binary counter is a 16-bit up counter. If any data is written to a preset register 1 when ...
	TM7BCL	Error correction	At reset bp7-0: 0	At reset bp7-0: X
	TM7BCH	Error correction	At reset bp7-0: 0	At reset bp7-0: X
VII-16	1	Description addition	Binary counter is a 16-bit up counter. If any data is written to a preset register when...	Binary counter is a 16-bit up counter. If any data is written to a preset register 1 when ...
	TM8BCL	Error correction	At reset bp7-0: 0	At reset bp7-0: X
	TM8BCH	Error correction	At reset bp7-0: 0	At reset bp7-0: X

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-19	1	Description addition	Binary counter is a 16-bit up counter. If any data is written to a preset register when ...	Binary counter is a 16-bit up counter. If any data is written to a preset register <u>1</u> when ...
VII-22	Description	Description addition	bp6 Buffer selection	bp6 <u>TM7OC1,2</u> buffer selection
	Description	Error correction	bp5 0: <u>Rising</u> edge	bp5 0: <u>Falling</u> edge
VII-23	TM7MD4	Error correction	bp7 Flag　　　　:<u>Reserved</u> Description :<u>Always set to "0".</u>	bp7 Flag　　　　:<u>T7TRGACT</u> Description :<u>Trigger reception flag of IGBT active outputting</u> <u>0:Enable</u> <u>1:Disable</u>
VII-26	Description	Description addition	bp6 Buffer selection	bp6 <u>TM8OC1, 2</u> buffer selection
	Description	Error correction	bp4 1: <u>Rising</u> edge	bp4 1: <u>Both</u> edges
	Flag	Error correction	bp1 TM8PWM<u>0</u>	bp1 TM8PWM<u>O</u>
	First Note	Error correction	<u>When T8IGB** is not selected, set as T8IGBTEN=0</u> <u>T8IGBT1-0=00</u>	-
VII-31	TMCKSEL2	Error correction	bp2-0 1:<u>Simple timer</u>	bp2-0 1:<u>Timer A output</u>
VII-34	Third Note	Description addition	-	<u>Set the timer n mode register when the TMnEN flag of the TMnMD1 register is set to "0" to stop counting.</u>
	Fourth Note	Description addition	-	<u>When changing CPU operation mode (NORMAL mode to SLOW mode) at selecting the high oscillation clock ...</u>
VII-35	First Note	Description addition	-	<u>When a data is written to 16-bit timer preset register (TMnPR1, TMnPR2), it is recognized as a 8-bit unit data inside LSI even ...</u>
VII-37	First Key	Description addition	... till the interrupt generation-1)	... till the interrupt generation-1) <u>However, if "00" is specified for the compare register, an interrupt timing is the same as if you set it to "01".</u>
	First Note	Description change	Up to 3 system clock is needed <u>from Timer n interrupt request flag till the next interrupt request flag.</u> During ...	Up to 3 system clock is needed <u>till the next interrupt request flag generated.</u> During ...
	Third Key	Description change	<u>On the interrupt service routine, clear the timer interrupt request flag before the timer is started.</u>	<u>There is a possibility that the timer interrupt request flag has already been set before the timer is started, clear the timer interrupt request flag.</u>
	Second Note	Description change	<u>Key</u> <u>When the TMnEN flag of the TMnMD register is not changed with other bits, the binary counter may count up by switching operation.</u>	<u>Note</u> <u>The TMnEN flag of the TMnMD register is not changed with other bits. There a possibility of mulfunctioning.</u>
VII-38	3	Error correction	200 <u>ms</u>	200 <u>μs</u>
	Description	Error correction	(8) Set the <u>TM7IC</u> flag of the TM7ICR register to "1" to enable the interrupt.	(8) Set the <u>TM7IE</u> flag of the TM7ICR register to "1" to enable the interrupt.

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-40	First Key	Description change	If the binary counter is read out during operation, incorrect data at counting up ...	If the event input (TMnIO input) is selected by count clock source, don't read ...
	Third Note	Error correction	... To prevent this, select the system clock (fx) for the count clock source once, ...	... To prevent this, select the system clock (fs) for the count clock source once, ...
	Fourth Note	Description change	The binary counter should not be read out after the timer operation is stopped ...	When the event input (TMnIO) input is selected as the count clock source, all pins from TMnIOA to TMnIOC are input mode. Therefore the procedure ...
VII-41	First Note	Description addition	-	Input from TMnIO should be used to a waveform, which has 2 times and over cycles of system clock (fs). If less than the above waveforms are input, it may not be counted correctly.
VII-46	Second Key	Error correction	... the timer output is "L", when the TMnCL flag of the TMnMD2 register is set to "1".	... the timer output is "L", when the TMnCL flag of the TMnMD1 register is set to "1".
	Second Note	Description change	When the prescaler is operated by the timer pulse output,...	When operating timer pulse output with the divided clock source,...
VII-49	2	Description deletion	Select the TM8IO/TM8O output waveform..	Select the TM8IO output waveform..
VII-51	Figure 7.6.4	Error correction	400 Hz	152.6 Hz
VII-57	Description	Error correction	(8) ... 25000/4=6250 (0x1869) ...	(8) ... 25000/4-1=6249 (0x1869) ...
VII-61	First Key	Error correction	... To prevent this, use fx or synchronous TMnIO input as the count clock...	... To prevent this, use fs or synchronous TMnIO input as the count clock...
	First Note	Error correction	Capture trigger signals of the 16-bit timers 7 and 8 are generated by sampling the rising ...	Capture trigger signals of the 16-bit timers n are generated by sampling the rising ...
VII-63	First Key	Error correction	..., or set the TMnBCR flag of the TM7MD2 to "0".	..., or set the TMnBCR flag of the TMnMD2 to "0".
	First Note	Description addition	-	Capture trigger samples the external interrupt input signal by system clock ...
	Second Note	Description addition	-	When using th external interrupt signal as capture trigger, to make external ...
VII-64	Third Key	Description addition	-	If the capture operation is done during the event count operation, an incomplete ...
VII-67	Description	Error correction	(2) Set the IRQIE flag of ...	(2) Set the IRQ0IE flag of ...
VII-69	2	Error correction	TM7I0, TM8I0. Startup trigger can be ...	TM7IO, TM8IO. Startup trigger can be ...
	13	Error correction	.. Make sure to set the TM7IGBT0, 1 of ...	.. Make sure to set the T7IGBT0, 1 of ...
	Table 7.10.1	Description deletion	Timer 8	-

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-74	Setup Procedure	Description addition	-	(3) Set the timer output pin TM7MD2(0x03F79) bp4:TM7PWM =1 TM7MD1(0x03F78) bp5:TM7CL =0
	Description	Description addition	-	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to set the output from PA5 pin to PWM output. Set the TM7CL flag of the timer 7 mode register 1 (TM7MD1) to "0" to enable timer output.
VII-75	Setup Procedure	Description addition	-	(11) Enable of external interrupt 0 input IRQCNT (0x03F3D) bp0:P20EN =1
	Description	Description addition	-	(11) Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.
VII-77	12	Error correction	.. Make sure to set the TM7IGBT0, 1 of ...	.. Make sure to set the T7IGBT0, 1 of ...
	Table 7.11.1	Description deletion	Timer 8	-
VII-79	Figure 7.11.1	Error correction		
	Figure 7.11.2	Error correction		
VII-80	Figure 7.11.3	Error correction		
	First Note	Description change	For standard IGBT output, set the TM7BCR flag of the TM7MD2 ...	When used for standard IGBT output, set the TM7BCR flag of the TM7MD2 ...

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-81	Setup Procedure	Error correction	(3) ... TM7MD3(0x03F8E) bp2:<u>TM7IGBTEN</u> =1 ...	(3) ... TM7MD3(0x03F8E) bp2:<u>T7IGBTEN</u> =1 ...
	Setup Procedure	Description addition	(3) ... TM7MD2(0x03F79) bp4:<u>PM7PWM</u> =1	(3) ... TM7MD2(0x03F79) bp4:<u>TM7PWM</u> =1 <u>TM7MD1(0x03F78)</u> <u>bp5:TM7CL =0</u>
	Description	Description addition	(3) ...TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select IGBT output.	(3) ... the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select IGBT output.<u>Set TM7CL flag of the timer7 mode register 1 (TM7MD1) to "0" to enable of timer output.</u>
VII-82	Setup Procedure	Description addition	-	<u>(10) Enable of external interrupt 0 input IRQCNT (0x03F3D)</u> <u>bp0:P20EN =1</u>
	Description	Description addition	-	<u>(10) Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.</u>
	Last line	Description addition	-	<u>TM7BC is counting from 0x0000 by external interrupt 0 input signal. IGBT ...</u>
VII-83	15	Description change	To control the startup by the commands, <u>TM7EN</u> count operation ...	To control the startup by the commands, <u>timer7</u> count operation ...
	17	Error correction	.. Make sure to set the <u>TM7IGBT0</u>, 1 of ...	.. Make sure to set the <u>T7IGBT0</u>, 1 of ...
VII-84	Figure 7.12.1	Description addition		
VII-85	3	Error correction	(B)After the trigger is input and after 1 count clock <u>falling</u> edge of the next count clock ...	(B)After the trigger is input and after 1 count clock <u>rising</u> edge of the next count clock ...
VII-87	Title	Error correction	(<u>At continuous counting</u>:T7IGBTCNT=1) (Timer 7)	(<u>BC operation when IGBT trigger disable</u>:T7IGBTCNT=1) (Timer 7)
	3	Description addition	-	<u>Setting the T7IGBTCNT flag of the timer 7 mode register 4 (TM7MD4) to "1" can continuous operation of binary counter when IGBT trigger disable.</u>
	Figure 7.12.3	Error correction	<u>TM8IOM</u>(IGBT output) <u>TMDEADPR1</u> <u>TMDEADPR2</u>	<u>TM8IO</u>(IGBT output) <u>TMDPR1</u> <u>TMDPR2</u>
		Error correction	Firgure 7.12.3 Count Timing of Dead Time High Precision IGBT Output(<u>At continuous counting</u>:T7IGBTCNT=1) (Timer 7)	Figure 7.12.3 Count Timing of Dead Time High Precision IGBT Output(<u>BC operation when IGBT trigger disable</u>:T7IGBTCNT=1) (Timer 7)

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-88	Figure 7.12.4	Description change	dead <u>count binary</u> counter 1,2 dead <u>count</u> preset register 1,2 dead <u>count</u> compare register 1,2	dead <u>time</u> counter 1,2 dead <u>time</u> preset register 1,2 dead <u>time</u> compare register 1,2
	6	Description change	(B) The value of the dead <u>count binary</u> counter 1 and the dead <u>count</u> compare register 1 ...	(B) The value of the dead <u>time</u> counter 1 and the dead <u>time</u> compare register 1 ...
	7	Description change	(C)... Also, the dead <u>count binary</u> counter 2 begins count operation	(C) ... Also, the dead <u>time</u> counter 2 begins count operation
	9	Description change	(D) The value of the dead <u>count binary</u> counter 2 and the dead <u>count</u> compare register 2 ...	(D) The value of the dead <u>time</u> counter 2 and the dead <u>time</u> compare register 2 ...
	11	Error correction	(E) ... because <u>IGBT output</u> is valid.	(E) ... because <u>T7TRGACT flag</u> is valid.
	14	Description change	(F) ...and the dead <u>count</u> preset register 1 and 2.	(F) ...and the dead <u>time</u> preset register 1 and 2.
	15	Description change	(G) ...However, the values same as the dead <u>count</u> preset register 1 and 2 are loaded to the dead <u>count</u> compare register 1 and 2 at the next count clock, as usual.	(G) ...However, the values same as the dead <u>time</u> preset register 1 and 2 are loaded to the dead <u>time</u> compare register 1 and 2 at the next count clock, as usual.
VII-89	Figure 7.12.5	Description change	IGBT waveform	IGBT <u>basic</u> waveform
	Setup Procedure	Error correction	(3)... bp1-0:<u>TM7IGBT1</u>-0 =01	(3)... bp1-0:<u>T7IGBT1</u>-0 =01
	Description	Error correction	(4)Set the T7IGBTTR flag of the TM7MD3 register to "1" to <u>select the rising edge as the interrupt generation valid edge.</u>	(4)Set the T7IGBTTR flag of the TM7MD3 register to "1" to <u>set IGBT trigger level to "H".</u>
	Description	Error correction	(5)Set the T7IGBTDT flag of the timer 7 mode register 3 (TM7MD3) to "0" to select the falling standard as the dead time <u>edge</u>.	(5)Set the T7IGBTDT flag of the timer 7 mode register 3 (TM7MD3) to "0" to select the falling standard as the dead time <u>insert timing</u>.
VII-90	Setup Procedure	Description addition	-	<u>(6)Enable of external interrupt 0 input IRQCNT (0x03F3D)</u> <u>bp0:P20EN =1</u>
	Description	Description addition	-	<u>(6)Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.</u>
	Setup Procedure	Error correction	(8) ... bp1:<u>IRQ1IE</u> =1	(8) ... bp1:<u>IRQ0IE</u> =1
	Setup Procedure	Description Deletion	(10) ... TM7PR1(0x03F75, 0x03F74) =0x9C3F <u>bp2:T7ICEN =1</u>	(10) ... TM7PR1(0x03F75, 0x03F74) =0x9C3F
	Description (12)	Error correction	<u>TM7DEADPR1</u> <u>TM7DEADPR2</u>	<u>TM7DPR1</u> <u>TM7DPR2</u>

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-90	Setup Procedure	Description addition	(13) ... TM8MD3 (0x03F8F) bp2:TM8SEL =1	(13) ... TM8MD<u>4</u> (0x03F<u>6F</u>) bp2:TM8SEL =1 <u>TM7MD1 (0x03F78)</u> <u>bp5:TM7CL =0</u>
	Description	Description addition	(13) ...Set TM8SEL_A flag of the timer 8 mode register 4 (TM8MD4) to "1" to select the timer 7 IGBT output.	(13) ...Set TM8SEL_A flag of the timer 8 mode register 4 (TM8MD4) to "1" to select the timer 7 IGBT output. <u>Set TM7CL flag of the timer 7 mode register 1 (TM7MD1) to "0" to enable the timer output.</u>
VII-91	Description	Error correction	(15) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7. After "H" is input to <u>P54</u> pin, IGBT is output from <u>P14</u>, <u>P15</u>.	(15) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7. After "H" is input to <u>P20</u> pin, IGBT is output from <u>PA5</u>, <u>PA6</u>.
VII-92	Table 7.13.1	Description change	Interrupt source <u>TM8IRQ1, TM8IRQ2</u>	Interrupt source <u>TM8IRQ, TM8OC2IRQ</u>
		Description addition	Clock source -	Clock source <u>TimerA output</u> <u>TimerA output/2</u> <u>TimerA output/4</u> <u>TimerA output/16</u>
VII-93	First Key	Description change	<u>*</u> At cascade connection, timer 8 interrupt factor is only counter-clear.	At cascade connection, timer 8 interrupt factor is only counter-clear.
	First Note	Error correction	<u>...</u> <u>Timer 7 interrupt should be disabled as the interrupt request of timer 7 is generated.</u>	<u>...</u> <u>The interrupt request of timer 7 is not generated. But timer 7 interrupt should be disabled.</u>
	Second Note	Error correction	... the correct data <u>may not be</u> loaded.	... the correct data <u>is not</u> loaded. <u>To prevent this, it puts into the count stop condition and rewrite the preset register once.</u>
	Second Key	Description addition	-	<u>Stop the timer in order to read out the correct value of the timer in cascade connection.</u>

VII-94	Setup Procedure	Error correction	(3) TM7MD2 (0x03F79)
			  bp2 : T7ICEN =0
			  <u>TM7MD3 (0x03F6C)</u>
			  <u>bp1-0 : T7OUT1-0 =00</u>
				(3) TM7MD2 (0x03F79)
				  bp2 : T7ICEN =0
				  <u>bp4 : TM7PWM =0</u>

	Description	Error correction	(3) Set the T7ICEN flag <u>of the TM7MD2, 3 register</u> to "0" to select the normal timer operation.	(3) Set the T7ICEN flag <u>and TM7PWM flag of the TM7MD2 register</u> to "0" to select the normal timer operation.
VII-95	Description	Error correction	(9) Set the interrupt level by the <u>TM8LS1</u> to 0 flag ...	(9) Set the interrupt level by the <u>TM8LV1</u> to 0 flag ...
VII-96	Setup Procedure	Error correction	(3) ... <u>TM8MD1(0x03F88)</u> bp<u>6</u>:TM8CAS=	(3) ... <u>TM8MD3(0x03F8F)</u> bp0:TM8CAS=
	Description	Error correction	(3) Set the TM8CAS flag of the <u>TM8MD1</u> register ...	(3) Set the TM8CAS flag of the <u>TM8MD3</u> register ...
VIII-4	3	Description change	Both timers are operated by the enable signal of the <u>TM6BEN</u>.	Both timers are operated by the enable signal of the <u>timer 6 enable register (TM6BEN)</u>.

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VIII-6	TM6BEN	Error correction	bp2 Flag : - At reset : - Access : -	bp2 Flag : Reserved At reset : 0 Access : R/W
VIII-11	First Key	Description addition	... = (count till the interrupt request - 1)	... = (count till the interrupt request - 1) However, the interrupt generation cycle when the compare register is set to "00" is hte same as it is set to "01".
	First Note	Description addition	... when the binary counter is read on the operation, uncertain ...	... when the binary counter is read on the operation while CPU is operationg in the NORMAL mode, uncertain ...
	Second Note	Description addition	If fx is used as the clock source, the binary ...	If fx is used as the clock source while CPU is operationg in the NORMAL mode, the binary ...
	Fourth Note	Description addition	When the fx is selected for the count clock source and the value of the compare register is rewritten, the operation ...	When the fx is selected for the count clock source and the value of the compare register is rewritten while CPU is operationg in the NORMAL mode, the operation ...
VIII-13	Setup Procedure	Description addition	-	(1) Stop the counter TM6BEN(0x03F6C) bp0 :TM6EN =0
	Description	Description addition	-	(1) Set the TM6EN flag of the TM6BEN register to "0" to stop the timer 6 counting.
VIII-15	Figure 8.4.1	Error correction		
VIII-16	Setup Procedure	Description addition	-	(1) Stop the counter TM6BEN(0x03F6C) bp1 :TBEN =0
	Description	Description addition	-	(1) Set the TBEN flag of the TM6BEN register to "0" to stop the time base timer counting.
IX-5	bp7	Description change	0:TM0IOC 1:RMOUTC	0:Timer 0 output (TM0IOC) 1:Remote control carrier output (RMOUTC)
	bp6	Description change	0:TM0IOB 1:RMOUTB	0:Timer 0 output (TM0IOB) 1:Remote control carrier output (RMOUTB)
	bp4	Description change	0:TM0IOA 1:RMOUTA	0:Timer 0 output (TM0IOA) 1:Remote control carrier output (RMOUTA)
	bp2-1	Error correction	1- : Timer output	1- : 1/1 duty
	bp0	Error correction	Remote control carrier base timer selection	Remote control carrier output base timer selection

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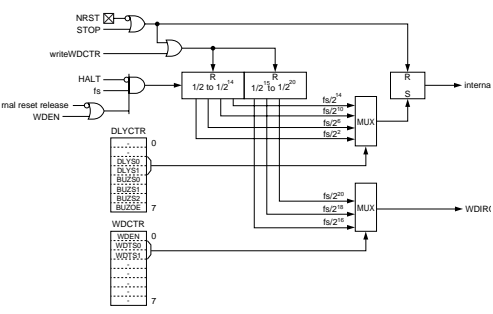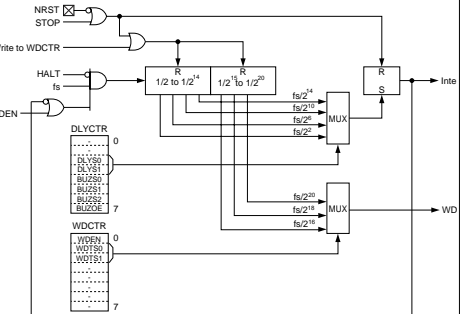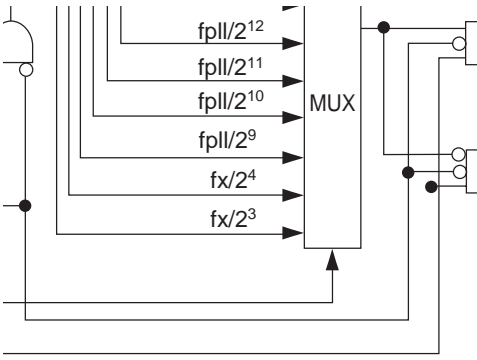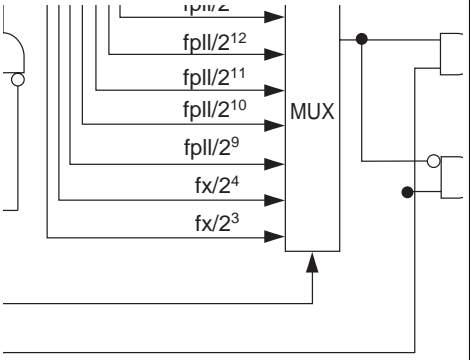| Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IX-6	First Note	Description addition	-	When set RMOEN flag to "1", don't change the flags oter than RMOEN flag.
	Key	Description addition	-	Do not change RMDTY 1,0 flag, RMBTMS flag and TMORM flag with RMOEN flag ...
	Second Note	Description addition	-	The cycle of the remote control carrier output base timer is set to the system clock ...
	Third Note	Description addition	-	Always set "0" to the bp denoted by *.
IX-7	4	Error correction	Duty ratio is selectable from 1/2, 1/3, Timer output. Remote ...	Duty ratio is selectable from 1/1, 1/2, 1/3. Remote ...
	Figure 9.3.1	Error correction		
	Figure 9.3.2	Error correction		
IX-8	First Key	Description deletion	When RMOEN flag is changed, the base cycle and the duty selection timer ...	-
	First Note	Description deletion	Set the timer output over 1 cycle of the system clock. The remote control carrier output ...	-
	Square	Description addition	Remote Control carrier Output Functions Setup	Remote Control carrier Output Functions Setup (Timer0, Timer3)
	2	Description addition	... RMOUT pin with the timer 0 are shown below ...	... RMOUT pin with the timer 0 used for the remote control carrier output base timer are shown below ...
	Figure 9.3.3	Error correction		
	Description	Description addition	(6) Set the TM0PWM flag of the TM0MD register ...	(6) Set the TM0PWM and TM0MOD flags of the TM0MD register ...

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IX-9	Setup Procedure	Error correction	(10) <u>Start the timer operation ...</u> (11) <u>Enable the remote control ...</u>	(10) <u>Enable the remote control ...</u> (11) <u>Start the timer operation ...</u>
	Description	Error correction	(10) <u>Set the TM0EN flag of the TM0MD ...</u> (11) <u>Set the RMOEN flag of the RMCTR ...</u>	(10) <u>Set the RMOEN flag of the RMCTR ...</u> (11) <u>Set the TM0EN flag of the TM0MD ...</u>
	First Note	Description addition	-	<u>When enabled the remote control carrier output during timer operation, the duty of remote control carrier ouput ...</u>
	Second Note	Description addition	-	<u>When stop the remote control carrier output, execute the remote control carrier output stop setting (RMOEN=0). And after ...</u>
X-2	Table 10.1.1	Description change	2^{16} of system clock 2^{18} of system clock 2^{20} of system clock	2^{16} of system clock <u>cycle</u> 2^{18} of system clock <u>cycle</u> 2^{20} of system clock <u>cycle</u>
X-3	Figure 10.1.1	Error correction		
X-5	WDCTR	Description change	bp5-3 <u>Set always to "0"</u>	Description <u>Always set to "0" *</u>
	WDCTR	Error correction	bp2-1 Watchdog runaway detect cycles <u>setup</u>	bp2-1 Watchdog runaway detect cycles <u>selection</u>
	First Note	Description addition	-	<u>Once WDEN flag is set to "1", WDEN flag can't be cleared to "0". But when ...</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
X-6	DLYCTR	Error correction	bp3-2 00 : <u>fs/2^{14}</u> 01 : <u>fs/2^{10}</u> 10 : <u>fs/2^{6}</u> * 1 11 : <u>fs/2^{2}</u> * 1	bp3-2 00 : <u>2^{14} of system clock cycle</u> 01 : <u>2^{10} of system clock cycle</u> 10 : <u>2^{6} of system clock cycle</u> 11 : <u>2^{2} of system clock cycle</u>
	2	Error correction	<u>*1:Do not use at high-speed operation (NORMAL mode). Use at slow-speed operation (SLOW mode).</u>	-
	First Note	Description addition	-	<u>We recommend selecting the oscillation stabilization time of high-speed and slow-speed oscillation by set of DLYS1-0 ...</u>
	First Key	Description addition	-	<u>About buzzer function refer to [Chapter 11 Buzzer].</u>

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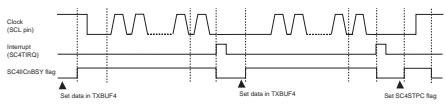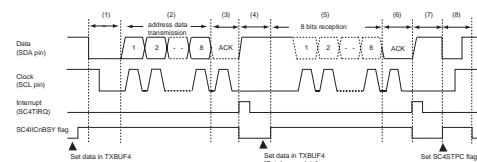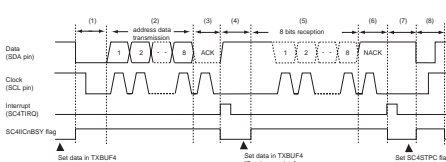
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
X-7	5	Description addition	As a result of the generation twice, consecutively, of the watchdog interrupt , ...	As a result of the generation twice, consecutively, of the watchdog interrupt (WDIRQ), ...
	First Note	Description addition	However, the watchdog timer stops during the HALT mode.	However, the watchdog timer stops during the Stop mode and the HALT mode.
	13	Error correction	... the watchdog timer detects errors when, 1. The watchdog timer overflows. When the watchdog timer detects ...	... the watchdog timer detects errors when, The watchdog timer overflows. When the watchdog timer detects ...
X-8	2	Error correction	The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR). The watchdog timer can be cleared regardless of the writing data ...	The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR) regardless of the writing data ...
	9	Error correction	The system clock is decided by the CPU mode control register (CPUM).	The system clock is decided by setting of the CPU mode control register (CPUM).
	Table 10.3.1	Description change	1. In NORMAL, IDLE, SLOW mode, the... ... 7. The counting of ... is released.	Table 10.3.1
	First Note	Description change	Generally, in the system use STOP mode is used or not in the execution of...	Note In the system use STOP mode is used or not in the execution of...
X-9	1, Description	Error correction	system clock	system clock cycle
	First Note	Error correction	The operation, just before the watchdog interrupt may be executed wrongly. Therefore, if the watchdog interrupt is generated, initialize the system.	The operation, just before the watchdog interrupt may be executed wrongly. In that case, proper operation is not guaranteed.
XI-3	Figure 11.1.1	Error correction		
XI-6	First Note	Description addition	-	The BUZ0E flag and BUZS2 to 0 flags should not be set at the same time.
	First Key	Description addition	-	DLYS 1 to 0 flag is setting flag of watchdog timer function. Refer to [Chapter 10 Watchdog Timer] for watchdog timer function.
XI-7	First Key	Error correction	At the instant that the BUZOE flag is set to "0", the output of the buzzer becomes "Low".	At the instant that the BUZOE flag is set to "0", the output of the buzzer (BUZZER and NBUZZER) becomes "Low".

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XI-8	First Note	Error correction	... the buzzer output is switched <u>enable</u> from <u>disable</u>, the buzzer dividing counter is not cleared unless more than 1 clock of the low oscillation clock is secured.	... the buzzer output is switched <u>disable</u> from <u>enable</u>, the buzzer dividing counter is not cleared unless more than 1 clock of the low oscillation clock is secured. <u>When enable buzzer output again, enable buzzer output after waiting one clock of low-speed oscillation clock.</u>
XII-4	Table 12.1.3	Description deletion	<u>Communication style</u> to <u>Maximum transfer rate</u>	-
XII-6	Table 12.1.5	Error correction	Communication format Standard mode (100 <u>Kbit/s</u>) High-speed mode (400 <u>Kbit/s</u>)	Communication format Standard mode (100 <u>bit/s</u>) High-speed mode (400 <u>bit/s</u>)
XII-7	Figure: 12.1.1	Error correction		
XII-8	Figure: 12.1.2	Error correction		
XII-9	Figure: 12.1.3	Error correction		

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-10	Figure: 12.1.4	Error correction		
XII-13,14, 15,16	PERIICR	Error correction	0x03FFF	0x03FFE
XII-16	First Note	Description addition	-	If changing the setting value of mode registers, execute rewriting after setting the serial forced reset...
	Second Note	Description addition	-	If changing the setting value of mode register (except for SC4STE flag, SC4STPC flag, IIC4REX flag and SC4ACK0 flag)...
XII-25	SCnMD1	Error correction	bp6 0 : Port 1 : Transfer clock I/O	bp6 0 : Port 1 : Serial clock I/O
		Error correction	bp5 Serial input control selection 0 : "1" input 1 : Serial input	bp5 Serial data input control selection 0 : "1" input 1 : Serial data input
XII-26	First Note	Description addition	-	If selecting the external clock (clock slave), set the internal clock that has the same or lower clock cycle to the external clock.
	First Key	Description addition	-	When set both bp5 of SCnSBIS flag and bp4 of SCnSBOS flag to "0", the serial forced reset is set and serial ...
	Second Note	Description addition	-	If setting the communication state of this serial interface to "UART", set the mode register (SCnMD1) to the serial ...
	First Note	Description addition	-	If changing the setting value of mode registers, execute rewriting after setting the serial forced reset...
XII-28	SCnMD3	Error correction	bp7-6 11 : Reserved	bp7-6 11 : Prohibited
	First Note	Description addition	-	If selecting the external clock (clock slave), set the internal clock that has the same or lower clock cycle to the external clock.
XII-32	First Note	Description addition	-	If changing the setting value of mode register (except for SC4STE flag, SC4STPC flag, IIC4REX flag and SC4ACK0 flag)...

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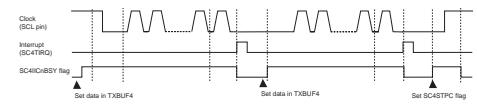| Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-33	SC4MD2	Error correction	bp7-6 ... 10 : Fix at "0" (Low) output 01 : Final data hold 11 : Reserved	bp7-6 ... 01 : Final data hold 10 : Fix at "0" (Low) output 11 : Prohibited
XII-34	SC4MD3	Description change	bp7-6 Flag, Description bp7 SC4SMB, SM-Bus support selection ... bp6 Reserved, Always set "0"	bp7-6 Flag, Description bp7-6 Reserved, Always set to "0" *
	SC4MD3	Error correction	bp1 Description ACK bit enable 0: Enable 1: Disable	bp1 Description ACK bit enable 0: Disable 1: Enable
	Second Note	Description change	Set the data to the serial interface 4 mode register 3 by Mov instruction, not by BSET/ BCLR control. If data is set by ...	Set the setting data to the serial interface 4 mode register 3 by Mov instruction once, not by BSET/BCLR control. After read ...
	Third Note	Description change	-	Always set "0" to the bp denoted by asterisk.
XII-35	1	Error correction	Serial interface 4 has 10 bits of the address set register.	Serial interface 4 has 7 bits of the address set register.
	Square	Description deletion	- Reserved Register (Reserved: 0x03FB5)	-
	First Note	Description addition	-	Do not word access to SC4AD0 register
XII-37	First Note	Description addition	-	SC4ABT_LST can not write "1"; can write "0" only.
XII-41	SC5STR	Error correction	bp0 At reset 0 Access R	bp0 At reset - Access -
XII-42	First Second Note	Description change	-	First and second Note moved from XII-43
XII-43	Square	Error correction	Transmission Data Buffer ... Whether during data loading period or not is determined by monitoring the transmission buffer empty flag SCnTEMP of SCnsSTR...	Transmission Data Buffer ... Whether during data loading period or not is determined by monitoring the transmission buffer empty flag SCnTEMP of SCnSTR...
XII-45	2 from the bottom	Error correction	In master communication, communication blanks, from SCn(T)IRQ generation ...	Communication blanks, from SCn(T)IRQ generation ...
XII-49	10	Error correction	At emergency reset, the status register (the SCnBRKF flag of the SCnMD2 register, all flags of the SCnSTR register) is initialized to the reset value,	At emergency reset, the status register (the SCnBRKF flag of the SCnMD2 register, all flags of the SC0STR, SC1STR and SC2STR registers,...
	Table 12.3.5	Error correction	Reserved	Prohibited

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-55	5	Error correction	When transmission and reception are executed with the start condition "enable", "the start condition enable" should be ...	When transmission and reception are executed with the start condition "enable", "the start condition enable" should be ....
	First Note	Description change	When executing transmission and reception at the same time, select "start condition disabled" to prevent malfunction.	When operating transmission and reception at the same time, select "start condition disable"; otherwise, it may cause improper operations.
XII-56	4, 8 Figure 12.3.16	Error correction	NORMAL mode	CPU operation mode
XII-57	Table	Error correction	0SL0 : 1, 0	OSL0 : 0→1, 1→0
XII-58	Table	Error correction	0SL1 : 1, 0	OSL1 : 0→1, 1→0
XII-59	Table	Error correction	0SL2 : 1, 0	OSL2 : 0→1, 1→0
XII-60	Table	Error correction	0SL3 : 1, 0	OSL3 : 0→1, 1→0
XII-61	Table	Error correction	0SL4 : 1, 0	OSL4 : 0→1, 1→0
XII-62	Description	Error correction	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler operation".	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler count enable".
XII-63	Setup Procedure	Error correction	(8) Set the interrupt level SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10	(8) Set the interrupt level PSW bp6 :MIE =0 SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10
	Description	Error correction	(8) Set the interrupt ...	(8) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt ...
	Setup Procedure	Error correction	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1 PSW bp6 :MIE =1
	Description	Error correction	(9) ... prior to enabling the interrupt.	(9) ... prior to enabling the interrupt. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.
	1	Error correction	*Each setup in (1) to (3), (6) to (7) and (8) to (9) can be set at the same time.	*Each setup in (1) to (3) and (6) to (7) can be set at the same time.
XII-64	First Key	Error correction	... SC0SBIS of the SC0MD1 register must be set to "1" to select "serial data input"....	... SCnSBIS of the SCnMD1 register must be set to "1" to select "serial data input"....
	Second Note	Description change	Key The transfer rate must be under 5.0 MHz ...	Note The transfer rate must be under 5.0 MHz ...

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-65	Description	Error correction	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler operation".	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler count enable".
	Setup Procedure	Error correction	(5) Control the pin direction [set the pin corresponding to each serial] P0DIR (0x03F30) bp2-1 :P0DIR2-1 =11	(5) Control the pin direction [set the pin corresponding to each serial] P0DIR (0x03F30) bp2 :P0DIR2 =0 bp0 :P0DIR0 =0
	Description	Error correction	(5) Set the P0DIR2 -1 flags of the port 0 pin direction control register (P0DIR) to "11" to set p01 and p02 to output mode and p00 to input mode.	(5) Set the P0DIR2 flag of the port 0 pin direction control register (P0DIR) to "0" and set the P0DIR0 flag to "0" to set P00 and P02 to input mode.
XII-66	Description	Error correction	(7) ... for serial 0, 1 and 2. Set the SC1SBOS of the SC1MD1 register to "0" and the SC1SBIS and SC1SBTS flags to "1" to set ...	(7) ... for serial 0, 1 and 2. Set the SC1SBIS and SC1SBTS flags of the SC1MD1 register to "1" to set the SBI1 pin to the ...
	Setup Procedure	Error correction	(8) Set the interrupt level SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10	(8) Set the interrupt level PSW bp6 :MIE =0 SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10
	Description	Error correction	(8) Set the interrupt ...	(8) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt ...
	Setup Procedure	Error correction	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1 PSW bp6 :MIE =1
	Description	Error correction	(9) ... prior to enabling the interrupt.	(9) ... prior to enabling the interrupt. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.
XII-67	1	Error correction	*Each setup (1) to (3) and (6) to (8) can be set at the same time.	*Each setup (1) to (3) and (6) to (7) can be set at the same time.
	First Note	Description deletion	Set the SCnSBIS of the SCnMD1 register to "0" and select a port in order to operate ...	-
	Second Note	Description change	Key The transfer rate must be under 5.0 MHz ...	Note The transfer rate must be under 5.0 MHz ...
	Third Note	Description addition	-	Insert three NOP instructions right after the instruction of the transition to HALT, STOP mode.
XII-68	First Note	Description addition	-	If setting the communication state of this serial interface to "UART", set the mode ...
XII-71	8	Description change	Set the next data to TXBUFn before the transmission complete interrupt SCnTIRQ is generated since the previous data setup	Set the next data to TXBUFn before the transmission complete interrupt SCnTIRQ is generated since data is setup to tranmission shift register
XII-73	Figure 12.4.4	Description addition	Figure:12.4.4 Setup Value of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.4 Setup Value of UART Serial Interface Transfer Speed (decimal) when setting devide-by-8 clock source
XII-74	Figure 12.4.5	Description addition	Figure:12.4.5 Setup Value of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.5 Setup Value of UART Serial Interface Transfer Speed (decimal) when setting devide-by-8 clock source

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-75	Figure 12.4.6	Description addition	Figure:12.4.6 Setup Valuse of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.6 Setup Valuse of UART Serial Interface Transfer Speed (decimal) <u>when setting devide-by-16 clock source</u>
XII-76	Figure 12.4.7	Description addition	Figure:12.4.7 Setup Valuse of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.7 Setup Valuse of UART Serial Interface Transfer Speed (decimal) <u>when setting devide-by-16 clock source</u>
XII-80	Table	Error correction	<u>0SL</u>0	<u>OSL</u>0
XII-81	Table	Error correction	<u>0SL</u>1	<u>OSL</u>1
XII-82	Table	Error correction	<u>0SL</u>2	<u>OSL</u>2
XII-83	Table	Error correction	<u>0SL</u>3	<u>OSL</u>3
XII-84,85		Error correction	<u>(1), (2), (3), (4), (5), (6), (7)</u>	<u>(1)→(7), (2)→(1), (3)→(2), (4)→(3), (5)→(4), (6)→(5), (7)→(6)</u>
XII-85	Setup Procedure	Error correction	(8) Enable the interrupt IRQEPEN(0x03F4E) bp1 :IRQEPEN1 =1 PERIICR(0x03FFE) bp1 :PERIIE =1 SC1TICR (<u>0x03FF5</u>) bp1 :SC1TIE =1	(8) Enable the interrupt <u>PSW</u> <u>bp6 :MIE =0</u> IRQEPEN(0x03F4E) bp1 :IRQEPEN1 =1 PERIICR(0x03FFE) bp1 :PERIIE =1 SC1TICR (<u>0x03FF8</u>) bp1 :SC1TIE =1 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Error correction	(8) Set the IRQEPEN1 flag of ... clear the request flag.	(8) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt.</u> Set the IRQEPEN1 flag of ... clear the request flag. <u>Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.</u>
XII-86	Second Note	Description addition	-	<u>When communication format of this serial interface set to "UART", set the Serial ...</u>
XII-87	First Note	Description change	<u>Key</u> Make sure to set the SC4SBIS flag ...	<u>Note</u> Make sure to set the SC4SBIS flag ...
	Second Note	Description addition	-	<u>Nch open-drain should be used for pin for-mat because the bus is switched ...</u>
XII-92	5	Description change	The stop condition should be requested only when this IIC occupies the bus as the master.	The stop condition should be requested only when this IIC occupies the bus as the master <u>and communication is completed</u>.
	First Note	Error correction	-	<u>Do not write to transmission buffer (TXBUF4) until bus busy flag BUSBSY (SCSTR1:bp3) is set to "0" after....</u>
XII-93	5	Description change	When it is detected that the data line (SDA4 pin) changes while the clock line (SCL4 pin) is "H" <u>...</u>	When it is detected that the data line (SDA4 pin) changes while the clock line (SCL4 pin) is "H" <u>after start condition is detected,....</u>

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-94	7	Error correction	... transmission starts with the clock transmitted from the master. In slave reception, ...	... transmission starts with the clock transmitted from the master. It is not necessary to set data to TXBUF4 register because bus line is automatically opened when NACK is received. In slave reception, ...
	12	Error correction	... the address compare flag SC4ADD_ACC of SC4STR1 is set to "1" and ACK is automatically transmitted.	... the address compare flag SC4ADD_ACC flag of SC4STR1 register is set to "1" and ACK is automatically transmitted.
	8 from the bottom	Description change	... and the ACK bit is stored in the SC4ACK0 of the SC4MD3 register....	... and the ACK bit is stored in the SC4ACK0 flag of the SC4MD3 register ...
	3 from the bottom	Description change	... At slave operation, the transmission is finished by automatically releasing the data line (SDA4).	... At slave operation, it is not necessary to set data to TXBUF4 register because the transmission is finished by automatically releasing the data line (SDA4).
XII-95	4	Error correction	... ACK bit level for output can be set with SC3ACK0 the SC3MD3 register.	... ACK bit level for output can be set with SC4ACK0 flag the SC4MD3 register.
	7	Error correction	During master communication, when competing with other master, data is compared; If the communication is ...	During master transmission, data bus(SDA) compares output data from this circuit with every 1-bit to detect the competition ...
	2 from the bottom	Description addition	... timing of flag set/clear.	... timing of flag set/clear. The time is required between the data is set to TXBUF4 register and the SC4IICBSY flag is set (the communication is started) at most the internal transfer clock 1 cycle.
XII-99	Figure 12.5.11	Error correction		
	3	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the data is set to TXBUF4.
	9	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.
	15	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the SC4STPC flag is set.
XII-100	Figure 12.5.12	Error correction		
	8	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.
	11	Error correction	(6) ACK bit output	(6) NACK bit output
	14	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the SC4STPC flag is set.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-101	7, 13	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.
XII-102	7	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.
XII-103, 104	7, 13	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.
XII-105	Table	Error correction	Pin setup (flag setup) SC4SEL register ... SC4SEL	Pin setup (flag setup) SC4SEL register ... OSL4
XII-106	Table 12.5.6	Error correction	Pin : A stream (port 6)	Pin : A system (port 6)
	Table 12.5.6	Error correction	Master/Slave : Master	Master/Slave : Master (Multimaster)
	Description	Error correction	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select prescaler operation.	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select "prescaler count enable".
	Description	Error correction	(3) Set the OSL4 flag of SC4SEL register to "0" to select A stream (port 6) for the I/O pin.	(3) Set the OSL4 flag of SC4SEL register to "0" to select A system (port 6) for the I/O pin.
XII-107	Setup Procedure, Description	Description change	(6), (7), (8), (9)	(6)
XII-108	Setup Procedure	Error correction	(10) Set the interrupt level SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10	(10) Set the interrupt level PSW bp6 :MIE =0 SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10
	Description	Error correction	(10) Set the interrupt ...	(10) Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt ...
	Setup Procedure	Error correction	(11) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0	(11) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0 PSW bp6 :MIE =1
	Description	Description change	(11) ... enabling interrupts. [Chapter ...	(11) ... enabling interrupts. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt. [Chapter...
XII-109	2	Error correction	*(1) and (2) can be set at once. *(6) to (10) can be set at once. * Each setup in (11) and (12) can be set at once. *(13) to (14) can be set at once.	*(1) and (2) can be set at once. *Each setup in (8) and (9) can be set at once. *(10) to (11) can be set at once.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-110	Table 12.5.7	Error correction	Pin : A <u>stream</u> (port 6)	Pin : A <u>system</u> (port 6)
	Table 12.5.7	Error correction	Master/Slave : Master	Master/Slave : Master <u>(Multimaster)</u>
	Description	Error correction	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select <u>"prescaler operation"</u>.	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select <u>"prescaler count enable"</u>.
	Description	Error correction	(3) Set the OSL4 flag of SC4SEL register to "0" to select A <u>stream</u> (port 6) for the I/O pin.	(3) Set the OSL4 flag of SC4SEL register to "0" to select A <u>system</u> (port 6) for the I/O pin.
XII-111	Setup Procedure, Destcription	Description change	<u>(6), (7), (8)</u>	<u>(6)</u>
	Description	Error correction	(6) Set the SC4ACKS flag of the serial 4 mode register 3 (SC4MD3) to "1" to select "ACK bit enabled". ACK bit is received at transmission and the level setting of ACK bit with the <u>SC4ACKS flag is not needed</u>.	(6) Set the SC4ACKS flag of the serial 4 mode register 3 (SC4MD3) to "1" to select "ACK bit enabled". ACK bit is received at transmission and the level setting of ACK bit with the <u>SC4ACKO flag is not required</u>...
	Setup Procedure	Error correction	(11) Set the interrupt level SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10	(11) Set the interrupt level <u>PSW</u> <u>bp6 :MIE =0</u> SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10
	Description	Error correction	(11) Set the interrupt level by the <u>SL4LV</u>1-0 flags ...	(11) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt.</u> Set the interrupt level by the <u>SC4LV</u>1-0 flags ...
XII-112	Setup Procedure	Error correction	(12) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0	(12) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Error correction	(12) ... Control Register Setup]	(12) ... Control Register Setup] <u>Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.</u> [Chapter ....
	Description	Error correction	(14) Communication complete interrupt (<u>SC4TIRQ</u>) is generated ...	(14) Communication complete interrupt (<u>SC4IRQ</u>) is generated ...
	1	Description addition	-	<u>*(1) and (2) can be set at once.</u> *Each setting in (9) to (10) can be set at once. *(10) to (11) can be set at once.
	First Note	Description addition	-	<u>Set each flag in accordance with the order of the setup procedure. Activate the ...</u>
XII-116	Table 12.6.2	Error correction	Item Clock pin (<u>SCI</u>)	Item Clock pin (<u>SCL</u>)
	Description	Error correction	(3) Set the <u>SC5SL</u> flag of the <u>OSL5</u> register ...	(3) Set the <u>OSL5</u> flag of the <u>SC5SEL</u> register ...

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XIII-3	First Note	Description addition	-	This function can't be used ni STOP/HALT mode.
	Second Note	Description addition	-	Don't execute mode switching as follows; ...
	First Key	Description addition	-	To realize a low power consumption, ladder resistance is turned OFF before STOP/HALT mode switching.
	Third Note	Description addition	-	The reference voltage input V_{ref+} pin uses value of $2.0\ V \leq V_{ref+} \leq V_{DD5}$. When ...
XIII-6	ANCTR0	Error correction	bp2, 5-4 1XX:fs/16 *as $T_{AD} \geq 800$ ns	bp2, 5-4 1XX:fs/16 111:Prohibited *as 800 ns $\leq T_{AD} \leq 15.26\ \mu s$
XIII-8	ANCTR2	Error correction	bp6-5 11: Continuous conversion or Set ANST flag to "1"	bp6-5 11: A/D conversion interrupt or Set ANST flag to "1"
XIII-11	Fifth Note	Description addition	-	If the flags of ANCTR0, ANCTR1 are changed during A/D conversion, we can't guarantee the operation and the result ...
XIII-12	4	Error correction	Set the A/D conversion cycle (T_{AD}) more than 800 ns.	Set the A/D conversion cycle (T_{AD}) more than 800 ns or less than 15.26 μs.
	Table: 13.3.1	Error correction	244.14 μs 488.28 μs 976.56 μs 15.26 μs 1953.12 μs	244.14 μs (no usable) 488.28 μs (no usable) 976.56 μs (no usable) 15.26 μs 1953.12 μs (no usable)
	Square	Description change	A/D Conversion Sampling Time (T_S) Setup	A/D Conversion Sample Hold Time (T_S) Setup
XIII-13	Key	Error correction	... ,the valid edge should be assigned at REDG flag of the continuous conversion control register (ANCTR2) and ...	... ,the valid edge should be assigned at REDG flag of the external interrupt control register (IRQ2ICR) and ...
XV-3	Second Note	Error correction	Set bp0 of the low-speed oscillation switching register (XSEL) to "1" before the transition to the slow oscillation mode.	Set bp5 of the low-speed oscillation selection register (XSEL) to "1" before the transition to the slow oscillation mode.
XV-4	4	Error correction	Switching of normal port, common pin and VLC pin is controlled with the LCD output control register 0 (LCCTR0).	Switching of normal port, common pin and V_{LC1} pin to V_{LC3} pin are controlled with the LCD output control register 0 (LCCTR0).
	7	Error correction	Segment pin, common pin and VLC pin are switchable to I/O port in 1-bit unit.	Segment pin, common pin and V_{LC1} pin to V_{LC3} pin are switchable to I/O port in 1-bit unit.
XV-5	Figure 15.1.1	Error correction		

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XV-7	Table 15.2.2	Error correction	Table 15.2.2: <u>LCD Control Registers List</u>	Table 15.2.2: <u>LCD Mode Control Register 1</u>
	LCDMD1	Error correction	Flag bp5 <u>DUTY1</u> bp4 <u>DUTY0</u>	Flag bp5 <u>LCDTY1</u> bp4 <u>LCDTY0</u>
	LCDMD1	Error correction	bp6 description <u>Set always "0".</u>	bp6 description <u>Always set to "0" *.</u>
XV-8	Second Note	Description addition	-	<u>When the LCDEN flag of LCDMD1 register being set, do not change other flags of LCDMDn register to prevent malfunction.</u>
	Third Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-9	Table 15.2.3	Error correction	Table 15.2.3: <u>LCD Control Registers List</u>	Table 15.2.3: <u>LCD Mode Control Register 2</u>
	LCDMD2	Description change	bp7-4/1-0 Description <u>Set always "0".</u>	bp7-4/1-0 Description <u>Always set to "0" *.</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-10	Table 15.2.4	Error correction	Table 15.2.4: <u>LCD Control Registers List</u>	Table 15.2.4: <u>LCD Mode Control Register 3</u>
	LCDMD3	Description change	bp7-4 Description <u>Set always "0".</u>	bp7-4 Description <u>Always set to "0" *.</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-11	1	Error correction	... that switches Port I/O (P92 to 94) and <u>nd</u> VLC pins (<u>VLC1</u> to <u>VLC3</u>). The value of the LCCTR0 register is set <u>I/O</u> port at reset.	... that <u>switches Port I/O (P84 to P87) and VLC pins (COM0 to COM3) and</u> switches Port I/O (P92 to 94) and VLC pins (<u>V$_{LC1}$</u> to <u>V$_{LC3}$</u>). The value of the LCCTR0 register is set port at reset.
	Table 15.2.5	Error correction	Table 15.2.5: <u>LCD Control Registers List</u>	Table 15.2.5: <u>LCD Output Control Register 0</u>
	LCCTR0	Description change	bp3 Description Always set to "0".	bp3 Description Always set to "0" <u>*.</u>
XV-12	Key	Description change	<u>If internal voltage booster circuit is used, ...</u>	<u>P94(V$_{LC1}$), P93(V$_{LC2}$) and P92(V$_{LC3}$) can be used as a port...</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-13-19	2	Error correction	... At reset, these ports are set to the <u>input</u> port.	... At reset, these ports are set to the port.
XV-13	Table 15.2.6	Error correction	Table 15.2.6: <u>LCD Control Registers List</u>	Table 15.2.6: <u>LCD Output Control Register 1</u>
XV-14	Table 15.2.7	Error correction	Table 15.2.7: <u>LCD Control Registers List</u>	Table 15.2.7: <u>LCD Output Control Register 2</u>
XV-15	Table 15.2.8	Error correction	Table 15.2.8: <u>LCD Control Registers List</u>	Table 15.2.8: <u>LCD Output Control Register 3</u>
XV-16	Table 15.2.9	Error correction	Table 15.2.9: <u>LCD Control Registers List</u>	Table 15.2.9: <u>LCD Output Control Register 4</u>
XV-17	Table 15.2.10	Error correction	Table 15.2.10: <u>LCD Control Registers List</u>	Table 15.2.10: <u>LCD Output Control Register 5</u>

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XV-18	Table 15.2.11	Error correction	Table 15.2.11: <u>LCD Control Registers List</u>	Table 15.2.11: <u>LCD Output Control Register 6</u>
XV-19	Table 15.2.12	Error correction	Table 15.2.12: <u>LCD Control Registers List</u>	Table 15.2.12: <u>LCD Output Control Register 7</u>
XV-22	5	Error correction	... voltage $\underline{V_{DD}}$ for LCD panel drive can be used at higher voltage than the V_{DD5} power supply (usable at $V_{LCD} \leq \underline{V_{DD}} \leq 5.5$ V).	... voltage $\underline{V_{LCD}}$ for LCD panel drive can be used at higher voltage than the V_{DD5} power supply (usable at $V_{LCD} \leq \underline{V_{DD5}} \leq 5.5$ V).
XV-25	Figure 15.3.2	Error correction	LCD Power Supply Connection	LCD Power Supply Connection (<u>In external Voltage divider</u>)
	Key	Description change	... In Figure:15.3.3, a bypass capacitor C (<u>0.01 μF to</u> 0.1 μF) is used to lower the impedance of power supply.	... In Figure:15.3.3, a bypass capacitor C (<u>about</u> 0.1 μF) is used to lower the impedance of power supply.
XV-26	Table 15.3.3	Description addition	Table: 15.3.3	Table: 15.3.3 <u>LCD voltage when using the internal voltage dividing resistor</u>
	First Key	Description addition	-	<u>P94(V_{LC1}), P93(V_{LC2}) and P92(V_{LC3}) can be used as a port...</u>
XV-28	5	Desctiption change	Refer to XV-22. Figure:<u>15.3.5</u> for the LCD power supply connection. Refer to <u>Chapter 15.4 LCD display</u> for connection of LCD panel.	Refer to XV-22. Figure:<u>15.3.2</u> for the LCD power supply connection. Refer to [<u>Chapter 15 15.4 Display</u>] for connection of LCD panel.
	Description	Error correction	(3) Set COMSL3 to 0 flags of the LCD mode control register <u>1</u> (LCCTR<u>1</u>) ...	(3) Set COMSL3 to 0 flags of the LCD mode control register <u>0</u> (LCCTR<u>0</u>) ...
	Setup Procedure	Error correction	(5) ... bp5-4 : <u>DUTY1</u>-0 = 00	(5) ... bp5-4 : <u>LCDTY1</u>-0 = 00
XV-31	4	Error correction	[Chapter <u>16</u>. 15.4.1 <u>LCD Display (static)</u>]	[Chapter <u>15</u>. 15.4.1 <u>static</u>]
	Description	Error correction	(5) ... [Chapter 15.4.<u>2. Setup example (static)</u>]	(5) ... [Chapter 15.4.<u>1. static</u>]
XV-35	4	Error correction	[Chapter <u>15.4.1 LCD Display (static)</u>]	[Chapter <u>15. 15.4.3 1/2 Duty</u>]
	Setup Procedure	Error correction	(2) ... bp5-4 :<u>DUTY1</u>-0= 10	(2) ... bp5-4 :<u>LCDTY1</u>-0= 10
	Description	Error correction	(2) Set the <u>DUTY1 to DUTY0</u> flags of ...	(2) Set the <u>LCDTY1 to LCDTY0</u> flags of ...
XV-39	4	Error correction	[Chapter <u>15.4.1 LCD Display (static)</u>]	[Chapter <u>15. 15.4.5 1/3 Duty</u>]
	Setup Procedure	Error correction	(2) ... bp5-4 :<u>LCDDDTY1</u>-0= 10	(2) ... bp5-4 :<u>LCDTY1</u>-0= 10
XV-43	Setup Procedure	Error correction	(2) ... bp5-4 :<u>DUTY1</u>-0= 10	(2) ... bp5-4 :<u>LCDTY1</u>-0= 10
	Description	Error correction	(2) Set the <u>DUTY1 to DUTY0</u> flags of ...	(2) Set the <u>LCDTY1 to LCDTY0</u> flags of ...
	Description	Description addition	(5) Display "23" ... the segment output latch SEG0 to SEG7.	(5) Display "23" ... the segment output latch SEG0 to SEG7. <u>[Chapter 15 15.4.7 1/4 duty]</u>

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XVI-2	First Key	Error correction	... type of interrupt ATCn, a regular interrupt is generated after the automatic transfer ends.	... type of interrupt ATCn, <u>hardware handling of</u> a regular interrupt is generated after the automatic transfer ends.
	First Note	Description addition	-	<u>The order of an interrupt acceptace may be changed by software when setting each ...</u>
	Third Key	Description addition	-	<u>ATC1 can't be used in standby mode (HALT mode and STOP mode). ATC1 starts ...</u>
XVI-3	Table 16.1.1	Description addition	... Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt * Software startup	... Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt <u>*1</u> Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt <u>*1</u> Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt <u>*1</u> Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt <u>*1</u> Software startup
XVI-4	First Note	Description addition	-	<u>Change the ATCn activation factor and the transfer mode while ATCn transfer is ...</u>
XVI-7	ATnCNT0	Error correction	bp7 Flag <u>FM0DE</u>	bp7 Flag <u>FMODE</u>
	ATnCNT0	Description change	bp1 Description <u>Set always "0".</u>	bp1 Description <u>Always set to "0" *.</u>
	First Note	Description addition	-	<u>ATnACT flag of the ATCn control register0 (ATnCNT0) is cleared by hardware ...</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XVI-8	AT0CNT1	Description change	bp5 Description <u>Set always "0".</u>	bp5 Description <u>Always set to "0" *.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
	Third Note	Description addition	-	<u>Bp5 of the ATCn control register1 (ATnCNT1) may be set by hardware ...</u>
XVI-9	AT1CNT1	Description change	bp5 Description <u>Set always "0".</u>	bp5 Description <u>Always set to "0" *.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XVI-14	Second Key	Description addition	-	<u>When the software activation is selected as an activation factor of ATCn, maximum ...</u>
XVI-15	First Key	Description addition	... I/O space (special registers) 3 cycles	... I/O space (special registers) 3 cycles <u>LOAD cycle and STORE cycle are set as follows. An access timing corresponding to each memory space + 1 cycle</u>
XVI-16	First Note	Description addition	-	<u>Set the memory address while ATCn transfer is disabled (ATnEN flag of the ...</u>
XVI-17	First Note	Description addition	-	<u>Set the number of data transfer while ATCn transfer is disabled (ATnEN flag of the ...</u>

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XVI-18	12	Error correction	... ATCn is activated everytime when timer 0 overflows and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 overflow) is ...	... ATCn is activated everytime when interrupt request of timer 0 interrupt generates and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 interrupt request generation) is ...
	Second Note	Description addition	-	Set the data transfer mode while ATCn transfer is disabled (ATnEN flag of the ...
XVI-35	12	Error correction	... is set, the ATCn data transfer shuts down immediately. During this ...	... is set, the ATCn data automatic transfer shuts down immediately after one byte transfer completed. During this ...
XVI-36	12	Error correction	... is set, the ATCn data transfer shuts down immediately. During this ...	... is set, the ATCn data automatic transfer shuts down immediately after one byte transfer completed. During this ...
XVI-37	Setup Procedure	Error correction	-	(1) Disable the data automatic transfer ATnCNT0 (AT0CNT0:0x03EC0,AT1CNT0:0x03ED0) bp0 :ATnEH = 0
	Description	Error correction	-	(1) Set the ATnEN flag of ATnCNT0 register to "0" to disable ATCn data automatic transfer.
XVI-38	First Note	Description addition	-	Set the ATCn data automatic transfer while ATCn transfer is disabled (ATnEN flag of ...
XVII-5	First Note	Error correction	... The external wait count $\geq$ WTHLD, RDHLD.	... The external wait count $\geq$ WTHLD, RDHLD.
	Third Note	Description addition	To use AC timing variable function, set the EXW1-0 ... to "01" (1 wait) or "10" (2 wait).	To use AC timing variable function, set the EXW1-0 ... to "01" (1 wait) or "10" (2 wait). If set to "11" (3 wait), the operation is not guaranteed.
XVII-6	6	Error correction	... , "hold" means the expanded cycle of the hold time.	... , "WTHLD0" and "WTHLD1" means the expanded cycle of the hold time.
	First Note	Description addition	-	In order to prevent through current, ..., pull-down resistor or level hold circuit etc., (Please take special caution in the standby mode.)
	Second Note	Description addition	-	This function is for refererence and does not guarantee AC timing. Please contact us if you consider using this function.
XVII-7	Setup Procedure	Description addition	(2) Set the ACTMD register bp5-4 : WTHLD1-0 = 01	(2) Set the ACTMD register ACTMD (0x03F06) bp5-4 : WTHLD1-0 = 01
XVIII-2	Figure 18.1.1	Description change	-	Figure is changed
	First Note	Description Deletion	... (For instance, in the case of MN101EF29G, when block 1 and 2 are programmed separately, 2 programming count is added.) ...	... (For instance, when block 1 and 2 are programmed separately, 2 programming count is added.) ...
XVIII-3	Table 18.1.1	Description addition	Programming area MAIN DATA	Programming area MAIN DATA BOOT
		Description change	Matsushita Electric Industrial Co., Ltd	Panasonic Corporation
		Description deletion	-	Website column deleted.

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Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XVIII-5	4 from the bottom	Description change	Matsushita Electric Industrial Co., Ltd	Panasonic Corporation
XVIII-6	Figure 18.3.1	Description change		
	7	Description addition	Pins : :	Pins : OSC1 (16 pin) : Clock input pin OSC1 (17 pin) : Clock input pin :
	First Note	Description addition		Please note that though the lower limit of microcontroller operation power voltage is 2.2V, in programming it is 2.7V
XVIII-8	-	Specification addtion	-	18.4 Microcontroller Rewriting Mode
XVIII-28	-	Specification addtion	-	18.5 Connecting the PX-FW2
XVIII-30	-	Specification addtion	-	18.6 Component Value Calculations
XVIII-34	-	Specification addtion	-	18.7 Flash Memory Programming Procedure
XVIII-35	-	Specification addtion	-	18.8 Boot Area Programming Procedure
XVIII-36	-	Specification addtion	-	18.9 ROM Programming Service
XVIII-39	-	Specification addtion	-	18.10 Special Function Resisters LIst

Remark : Definition in the above table is classified according to the content of changes as follows.
Error correction, Description change, Description addition, Description deletion : For the description of LSI manual.
Specification change, Specification addition, Specification deletion : For microcontroller's specification.

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The following shows the changes in the publication of "MN101E29G/F29G LSI User's Manual" (From the 1st Edition 2nd Printing dated in May, 2006 to the 1st Edition 4th Printing dated in January, 2008.)

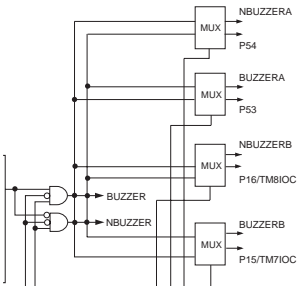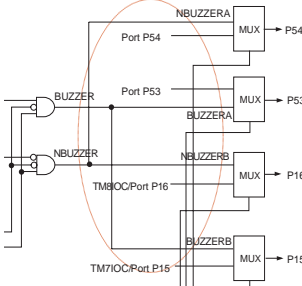| Page	Line	Definition	Former Edition (1.2)	New Edition (1.4)
II-17,18	Note	Description Addtion		It is not guaranteed to ensure proper operation in accessing to unimple-mented spaces, such as internal ROM/RAM spaces without memory (ROM/RAM) and special register spaces with-out special register.

Remark : Definition in the above table is classified according to the content of changes as follows.
Error correction, Description change, Description addition, Description deletion : For the description of LSI manual.
Specification change, Specification addition, Specification deletion : For microcontroller's specification.

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The following shows the changes in the publication of "MN101E29G/F29G LSI User's Manual" (From the 1st Edition dated in March, 2005 to the 1st Edition 2nd Printing dated in May, 2006.)

Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
I-30	*2	Change	between power supply pin and the ground for latch-up prevention	between V_{DD5} power supply pin and the ground for latch-up prevention
	*3	Add	-	T8OC2IRQ-Timer 8 interrupt (16-bit timer)
I-39	Table	Change	40. MAX: ±400	40. MAX: ±500
II-23	Figure 2.2.5	Change	0x03EF9: P8OMD2	0x03EF9: Reserved
II-27	RCCTR0	Change	Flag bp7: - At reset bp7: - Access bp7: -	Flag bp7: Reserved At reset bp7: 0 Access bp7: RW
II-39	Figure 2.4.4	Change	0x8FFFF	0xEFFFF
IV-10	P0OMD	Change	Flag bp4: - At reset bp4: - Access bp4: -	Flag bp4: P0OMD4 At reset bp4: 0 Access bp4: RW
			bp4: -	bp4: P03 special function setting 0: TM0IOB/RMOUTB 1: TM2IOB
			bp3: I/O port, TM2IOB/RMOUTB selection 1: TM2IOB/RMOUTB	bp3: I/O port, TM0IOB/TM2IOB/RMOUTB selection 1: TM0IOB/TM2IOB/RMOUTB
			bp2 1: SYSCLK	bp2 1: TM9IOB
			bp1 1: NBUZZER	bp2 1: TM8IOB
			bp1 1: BUZZER	bp2 1: TM7IOB
IV-20	6 to 7 from the bottom	Change	To read out the data of AC zero-cross, set the bp7, 4 of the noise filter control register (NFnCTR) to "1",	To use the detection function of AC zero-cross, set the bp7, 3 of the AC zero-cross detection interrupt control register (ACZCTR) to "1",
IV-31	Last paragraph	Add	-	P47 is also used as the serial 5 clock input pin. When the SEL12C flag ...
IV-34	P4ODC	Change	-	P4ODC register Table is changed

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Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
IV-40	P5ODC	Change	Flag bp1: P5ODC bp0: - At reset bp1: 0 bp0: - Access bp1: R/W bp0: -	Flag bp1: - bp0: P5ODC0 At reset bp1: - bp0: 0 Access bp1: - bp0: R/W
			bp0: -	bp0: Nch open-drain output selection 0: Push-pull output 1: Nch open-drain output
IV-42	BUZSEL	Change	Flag bp4: P5OMD14 bp3: P5OMD13 bp2: P5OMD12 bp1: P5OMD11	Flag bp4: BUZSEL4 bp3: BUZSEL3 bp2: BUZSEL2 bp1: BUZSEL1
IV-66	P9OMD	Change	Flag bp4: SYSCLK	Flag bp4: Reserved
			bp4: I/O port, SYSCLK selection 0: Output 1: Not output	bp4: Always set to "0".
IV-82	Table 4.15.1	Add	-	PACNT, Add Port 8
IV-83	-	Add	-	Add Port 8 description
V-51	The last paragraph	Change	TM0BC starts to count up from 0x00 with negative edge of the external interrupt 0 (IRQ0) input as a trigger. Timer 0 continues to...	At sampling the negative edge of the external interrupt 0 (IRQ0) input with the count clock, the internal enable is set. And after the setting, the next count clock makes
VI-9	The first key mark	Change	the interrupt request flag is set and the binary counter is cleared, at the next count clock. So set the compare register as: Compare register setting = (count till the interrupt request -1)	the value of the internal count clock is inverted at the next count clock. So set the compare register as: Compare register setting = (count till the compare match -1)
VII-56	Figure 7.7.4	Change	152.6 Hz	400 Hz
IX-9	Step (9)	Change	To get 1/2 dividing of 36.7 kHz (73.4 kHz)	To get 2-times frequency of 36.7 kHz (73.4 kHz).....
XI-3	Figure 11.1.1	Change		

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Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
XII-7 to 12	Figure 12.1.1 to 12.1.2	Change		
XII-82	6	Change	-	Add IRQEXPEN
XV-13	1	Change	.....port I/O (P60 to P63, <u>P54 to P57</u>)	.....port I/O (P60 to P63, <u>P50 to P53</u>) .....
	LCCTR3	Change	bp7: SEG23/Port<u>54</u> selection 0: Port<u>54</u>	bp7: SEG23/Port<u>53</u> selection 0: Port<u>53</u>
			bp6: SEG22/Port<u>55</u> selection 0: Port<u>55</u>	bp6: SEG22/Port<u>52</u> selection 0: Port<u>52</u>
			bp5: SEG21/Port<u>56</u> selection 0: Port<u>56</u>	bp5: SEG21/Port<u>51</u> selection 0: Port<u>51</u>
			bp4: SEG20/Port<u>57</u> selection 0: Port<u>57</u>	bp4: SEG20/Port<u>50</u> selection 0: Port<u>50</u>
XV-14	1	Change	.....port I/O (<u>P50 to P53</u>, P44 to P47)	.....port I/O (<u>P54 to P57</u>, P44 to P47) .....
	LCCTR4	Change	bp3: SEG27/Port<u>50</u> selection 0: Port<u>50</u>	bp3: SEG27/Port<u>57</u> selection 0: Port<u>57</u>
			bp2: SEG26/Port<u>50</u> selection 0: Port<u>50</u>	bp2: SEG26/Port<u>56</u> selection 0: Port<u>56</u>
			bp1: SEG25/Port<u>51</u> selection 0: Port<u>51</u>	bp1: SEG25/Port<u>55</u> selection 0: Port<u>55</u>
			bp0: SEG24/Port<u>52</u> selection 0: Port<u>52</u>	bp0: SEG24/Port<u>54</u> selection 0: Port<u>54</u>
XVI-8	-	Change	ATCn control register(AT0CNT1:0x03EC1, AT1CNT1:0x03ED1)	Changed to ATC0 control register1 (AT0CNT1:0x03EC1), ATC1 control register1(AT1CNT1:0x03ED1)
XVIII-2	10	Add	-	-Data area description is added
	Figure 18.1.1	Add		
XVIII-3	Table 18.1.1	Add	-	Data area field is added
			-	OBJECT Co., Ltd. field is added

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Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
XVIII-5	The last line	Add	-	OBJECT Co., Ltd. description is added
XVIII-7	Table	Add	Frequency -	Frequency <u>2.0 to 20 MHz</u>
XVIII-7	Note	Add	-	Do not set the relation between micro-controller clock pin frequency and communication clock frequency to 1/20 or less.

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Inquiries

If you have questions regarding technical information on this manual, please visit the following URL.

Panasonic Corporation

URL: http://www.semicon.panasonic.co.jp/en