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MICROCOMPUTER MN101E

MN101E29G/F29G
LSI User's Manual Vol.1

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About This Manual

■Objective

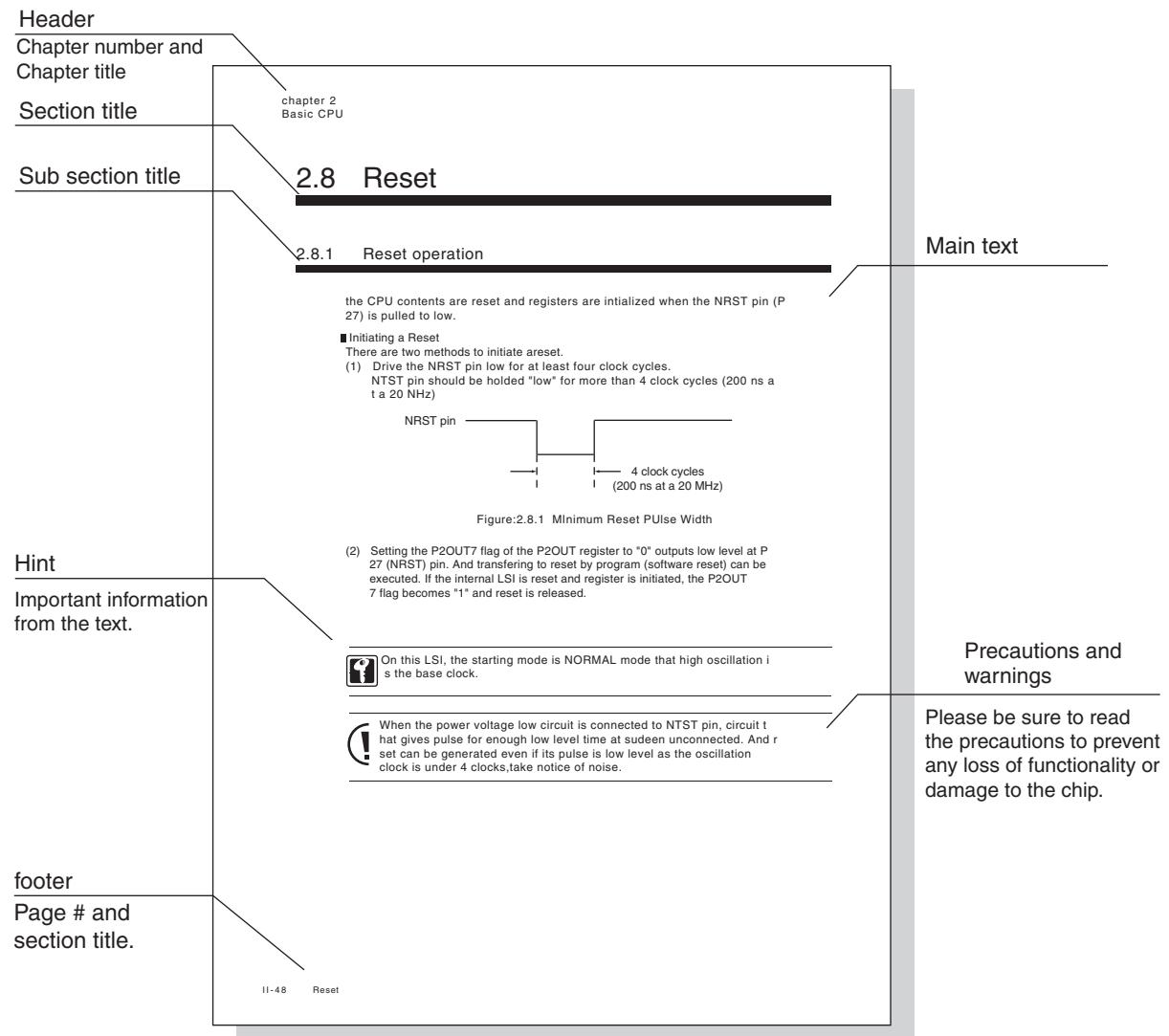
The primary objective of this LSI manual is to describe the features of this product including an overview, CPU basic functions, interrupt, port, timer, serial interface, and other peripheral hardware functions.

Each section consists of brief functional information, block diagrams and the details of control registers including operation methods and setting examples.

■Structure of This Manual

Each section of this manual consists of a title, summary, main text, hint, precautions and warnings, and references.

The layout and definition of each section are shown below.



This page serves as an example to the explanations above. It may be different on an actual page.

■Finding Desired Information

This manual provides three methods for finding the desired information quickly and easily.

1. Refer to the index at the front of the manual to locate the beginning of each section.
2. Refer to the table of contents at the front of the manual to locate the desired titles.
3. The chapter number and chapter title are located at the top corner of each page, and the section titles are located at the bottom corner of each page.

■Related Manuals

Note that the following related documents are available.

- "MN101E Series Instruction Manual"
<Describes the instruction set.>
- "MN101C/MN101E Series Cross-assembler User's Manual"
<Describes the assembler syntax and notation.>
- "MN101C/MN101E Series C Compiler User's Manual Usage Guide"
<Describes the installation, commands and options of the C Compiler.>
- "MN101C/MN101E Series C Compiler User's Manual Language Description"
<Describes the syntax of the C Compiler.>
- "MN101C/MN101E Series C Compiler User's Manual Library Reference"
<Describes the standard library of the C Compiler.>
- "MN101C/MN101E Series Installation Manual"
<Describes the steps to install the Integrated Development Environment (DebugFactory Builder), C compiler and the real-time OS. It also describes the procedure to setup the in-circuit emulator (PX-ICE101C/E).>
- "MN101C/MN101E/MN103L Series Software Development Environment Installation Manual"
<Describes the steps to install the Integrated Development Environment (DebugFactory Builder), C compiler and the real-time OS. It also describes the procedure to setup the in-circuit emulator (PX-ICE101C/E-Advance, PX-ICE101C/E-Lite).>

■Contact Information

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Chapter 1 Overview

1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. The MN101E29 series have an internal 128 KB(maximum) of ROM and 6 KB(maximum) of RAM. Peripheral functions include 6 external interrupts, 28 internal interrupts including NMI, 10 timer counters, 6 sets of serial interfaces, A/D converter, D/A converter, LCD driver, watchdog timer, 2 sets of automatic data transfer, synchronous output function and buzzer output. The configuration of this microcomputer is well suited for application as a system controller in camera, timer selector for VCR, CD player, or minicomponent.

With three oscillation system (high frequency : max. 10 MHz / low frequency : 32.768 kHz and PLL : frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high frequency input (high speed mode), PLL input (PLL mode), or to low frequency input (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software. High speed mode has the normal mode which is based on 2-cycle clock ($f_{PLL}/2$) and the double speed mode which is based on the not-devided clock with f_{PLL} .

A machine cycle (min. instructions execution) in the normal mode is 200 ns when f_{OSC} is 10 MHz (at the time that PLL is not used). A machine cycle in the double speed mode is 100 ns when f_{OSC} is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).The package is 100-pin QFP, LQFP.

1.1.2 Product Summary

This manual describes the following models of the MN101E29 series. These products have identical functions.

Please note that mainly dealed here is MN101E29G.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101E29G	128 KB	6 KB	Mask ROM version
MN101EF29G	128 KB + 4 KB	6 KB	Flash EEPROM version

1.2 Hardware Functions

■ Feature

ROM Capacity: 128 Kbyte

RAM Capacity: 6 Kbyte

Package: 100pin QFP (18 mm square, 0.65 mm pitch)

100pin LQFP (14 mm square, 0.5 mm pitch)

Machine Cycle: High speed mode

0.10 µs/ 10 MHz (2.2 V to 5.5 V)

PLL mode

0.05 µs/ 20 MHz (2.2 V to 5.5 V)

Low speed mode

62.5 µs/32 kHz (2.2 V to 5.5 V)

Clock Gear: Operation speed of system clock is variable by changing the frequency.

Multiplied Clock: High-speed frequency clock (fosc) can be multiplied by 2, 3, 4, 5, 6, 8 and 10.

Memory bank : Data memory space is expanded by the bank system.

Bank for the source address/Bank for the destination address.

ROM correction: Correcting address designation : up to 7 addresses possible

Operation Modes:

NORMAL mode (High speed mode)

PLL mode

SLOW mode (Low speed mode)

HALT mode

STOP mode

(The operation clock can be switched in each mode.)

Operating Voltage: 2.2 V to 5.5 V

Operating Temperature: -40°C to +85°C

Interrupt: 34 levels

<Watchdog timer>

NMI-Watchdog timer overflow

<Timer interrupts>

TM0IRQ-Timer 0 interrupt (8-bit timer)

TM1IRQ-Timer 1 interrupt (8-bit timer)

TM2IRQ-Timer 2 interrupt (8-bit timer)

TM3IRQ-Timer 3 interrupt (8-bit timer)

TM4IRQ-Timer 4 interrupt (8-bit timer)

TM6IRQ-Timer 6 interrupt (8-bit timer)

TBIRQ-Clock timer interrupt

TM7IRQ-Timer 7 interrupt (16-bit timer)

T7OC2IRQ- Timer 7 interrupt (16-bit timer)

TM8IRQ-Timer 8 interrupt (16-bit timer)

T8OC2IRQ- Timer 8 interrupt (16-bit timer)

TM9IRQ-Timer 9 interrupt (16-bit timer)

T9OC2IRQ- Timer 9 interrupt (16-bit timer)

<Serial interrupts>

SC0TIRQ-Serial interface 0 interrupt (UART transmission, synchronous)

SC0RIRQ-Serial interface 0 interrupt (UART reception)

(Peripheral function group interrupt)

SC1TIRQ-Serial interface 1 interrupt (UART transmission, synchronous)

SC1RIRQ-Serial interface 1 interrupt (UART reception)

(Peripheral function group interrupt)

SC2TIRQ-Serial interface 2 interrupt (UART transmission, synchronous)

SC2RIRQ-Serial interface 2 interrupt (UART reception)

SC3TIRQ-Serial interface 3 interrupt (UART transmission, synchronous)

SC3RIRQ-Serial interface 3 interrupt (UART reception)

(Peripheral function group interrupt)

SC4TIRQ- Serial interface 4 interrupt (Synchronous)

SC4SIRQ- Serial interface 4 interrupt (Multi master I2C, Stop condition)

(Peripheral function group interrupt)

SC5TIRQ- Serial interface 5 interrupt (Slave I2C)

(Peripheral function group interrupt)

<A/D conversion end>

ADIRQ-AD conversion end

<Automatic Transfer Controller interrupts>

ATC0IRQ, ATC1IRQ (Peripheral function group interrupt)

<External interrupts> Edge selectable

IRQ0:External interrupt (AC zero-cross detector, With/Without noise filter)

IRQ1:External interrupt (AC zero-cross detector, With/Without noise filter)

IRQ2:External interrupt (Both edges interrupt)

IRQ3:External interrupt (Both edges interrupt)

IRQ4:External interrupt (Both edges interrupt)

IRQ5:External interrupt (Key scan interrupt only)

Timer Counter: 11 timers All timer counters generate interrupt (10 can be operated independently)

8-bit timer for general use : 5 sets

8-bit free-running timer : 1 set

Time base timer : 1 set

16-bit timer for general use : 3 sets

Simple 8-bit timer : 1 set

Timer 0 (8-bit timer for general use)

-Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM0IOB), event count, remote control carrier output, simple pulse with measurement

-Clock source

fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock,

TimerA output

-Real timer output control

Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 1 (8-bit timer for general use)

- Square wave output(timer pulse output), event count, 16-bit cascade connected (timer0, 1)
- timer synchronous output event

- Clock source
- fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock,
- TimerA output

Timer 2 (8-bit timer for general use)

- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM2IOB), event count,
- simple pulse with measurement, 24-bit cascade connected (timer0, 1)
- timer synchronous output event

- Clock source
- fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock,
- TimerA output

- Real timer output control
- Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0)
- with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 3 (8-bit timer for general use)

- Square wave output(timer pulse output), event count, remote control carrier output,
- 16bit cascade connected (timer2), 32-bit cascade connected (timer0, 1, 2)

- Clock source
- fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock,
- TimerA output

Timer 4 (8-bit timer for general use)

- Square wave output (timer pulse output), added pulse(2-bit) system PWM output,
- event count, serial transfer clock, simple pulse measurement

- Clock source
- fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock,
- TimerA output

Timer 6 (8-bit free-running timer, Time base timer)

-8-bit free-running timer

-Clock source

fpll, fpll/2¹², fpll/2¹³, fs, fx, fx/2¹², fx/2¹³

Time base timer

-Interrupt generation cycle

fpll/2⁷, fpll/2⁸, fpll/2⁹, fpll/2¹⁰, fpll/2¹³, fpll/2¹⁵,

fx/2⁷, fx/2⁸, fx/2⁹, fx/2¹⁰, fx/2¹³, fx/2¹⁵

Timer 7 (16-bit timer for general use)

-Clock source

fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16

1/1, 1/2, 1/4, 1/16 of the external clock

TimerA output

-Hardware organization

Compare register with double buffer : 2 sets

Input capture register : 1 set

Timer interrupt : 2 vectors

-Timer functions

Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable), IGBT output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB

Timer synchronous output, event count, Input capture function (Both edges can be operated)

-Real timer output control

Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0)

with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 8 (16-bit timer for general use)

-Clock source

fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16

1/1, 1/2, 1/4, 1/16 of the external clock

TimerA output

-Hardware organization

Compare register with double buffer : 2 sets

Input capture register : 1 set

Timer interrupt : 2 vectors

-Timer functions

Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture (Both edge available), 32-bit cascade connected (Timer7, 8), 32-bit PWM output, Input capture is available at 32-bit cascade

Timer 9 (16-bit timer for general use)

-Clock source

fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16, 1/1, 1/2, 1/4, 1/16 of the external clock
TimerA output

-Hardware organization

Compare register with double buffer : 2 sets
Input capture register : 1 sets
Timer interrupt : 2 vectors

-Timer functions

Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM9IOB, event count, pulse width measurement, input capture (Both edge available)

-Real timer output control

Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0)
with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

TimerA output (Simple timer counter A)

Clock output for peripheral function

Watchdog timer

Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$

On detection of errors, hard reset is done inside LSI.

Synchronous output function

Timer synchronous output, interrupt synchronous output

Port 8 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 2, or 7, or of the external interrupt 2 (IRQ2).

Buzzer Output/Reverse Buzzer Output:

Output frequency can be selected from $f_{PLL}/2^9, f_{PLL}/2^{10}, f_{PLL}/2^{11}, f_{PLL}/2^{12}, f_{PLL}/2^{13}, f_{PLL}/2^{14}, f_x/2^3, f_x/2^4$.

Remote Control Carrier Output:

A remote control carrier output with duty cycle of 1/2 or 1/3 of timer 0 or timer 3 output are available.

A/D Converter: 10-bit x 16 channels

D/A Converter: 8-bit x 4 channels

Data automatic transfer : 2 systems

ATC0

Data is transferred automatically in all memory space

- External request/internal event request/software request
- Maximum transfer cycles are 255
- Support continuous serial transmission / reception.
- Burst transfer function (Urgent stop of interrupts is contained.)

ATC1

Data is transferred automatically in all memory space

- External request/internal event request/software request
- Maximum transfer cycles are 255
- Support continuous serial transmission / reception.
- Burst transfer function (Urgent stop of interrupts is contained.)

Serial Interface: 6 channels

Serial 0 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
 - $f_{PLL}/2, f_{PLL}/4, f_{PLL}/16, f_{PLL}/64, f_s/2, f_s/4,$
 - Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
- fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4,
- Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
- fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4,
- Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 3 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
- fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4,
- Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 4 (multi master IIC / Synchronous serial interface)

Synchronous serial interface

-Transfer clock source

fpll/2, fpll/4, fpll/8, fpll/32, fs/2, fs/4,

Timer0,1,2,3,4 and A output, external clock

-MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.

-Sequence transmission, reception or both are available.

Multi master IIC

-7-bit of slave address can be set.

-General call communication mode handling

Serial5

-IIC slave interface

-IIC high-speed transfer mode (communication speed: 400 kbps)

-7-bit or 10-bit of slave address can be set.

-General call communication mode handling

LED Driver: 8 pins (Push-pull structure)

Automatic Reset

LCD Driver: LCD driver pins

Segment output max. 55 pins (SEG0 to 54)

SEG0 to 54 can be switched to I/O ports by 1 pin

[Note:At reset, SEG0 to 54 are input ports.]

Common output pins:4 pins

COM0 to 3 can be switched to I/O ports by 1 pin

Display mode selection

Static

1/2 duty, 1/2 bias

1/3 duty, 1/3 bias

1/4 duty, 1/3 bias

LCD driver clock

When the source clock is the main clock (fpll)

$1/2^{18}, 1/2^{17}, 1/2^{16}, 1/2^{15}, 1/2^{14}, 1/2^{13}, 1/2^{12}, 1/2^{11}$

When the source clock is the sub clock (fx)

$1/2^9, 1/2^8, 1/2^7, 1/2^6$

When the source clock is the main clock

Timer0,1,2,3,4 and A output

LCD power supply

Use at $V_{DD5} \geq V_{LC1}$

External supply voltage is input from V_{LC1} , V_{LC2} , V_{LC3} pins or voltage applied to V_{LC1} is divided by internal resistance and supplied to V_{LC2} and V_{LC3} pins.

Port:

I/O ports : 90 pins

LED (large current) driver pins : 8 pins

LCD driver for segment : 55 pins

LCD driver for common : 4 pins

serial interface pin : 34 pins

Timer I/O : 28 pins

Buzzer output : 4 pins

A/D input : 16 pins

External interrupt pin : 5 pins

LCD power : 3 pins

XI/XO : 2 pins

D/A output : 4 pins

Special pins : 10 pins

Operation mode input pins : 3 pins

Analog reference voltage input pin : 1 pin

Reset input pin : 1 pin

Oscillation pins : 2 pins

Power pins : 3 pins

1.3 Pin Description

1.3.1 Pin configuration

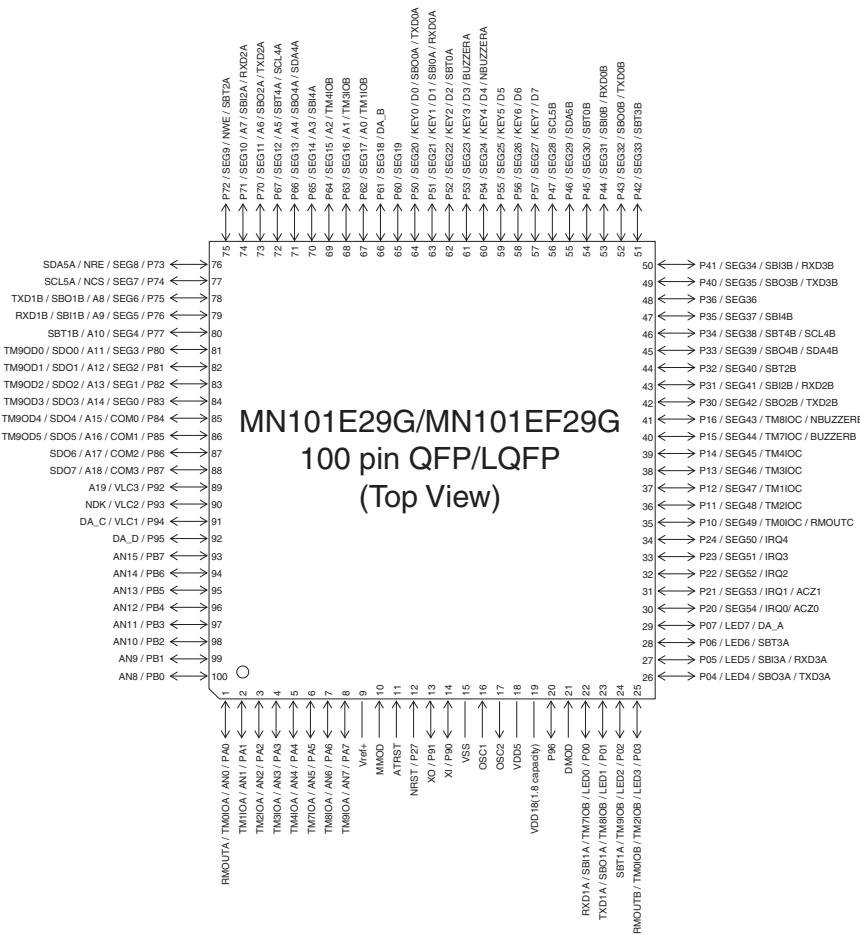


Figure:1.3.1 Pin Configuration (100QFP: TOP VIEW)

Mode	Object micro-controller	Activation area	Pin setting						Register setting
			NRST	ATRST	DMOD	P01	P02	MMOD	
Single chip mode	FLASH-ROM MASK-ROM	MAIN	(1)	L or H	H	Normal pin			L 0
Memory extend mode	FLASH-ROM MASK-ROM	MAIN	(1)	L or H	H	Normal pin			L 1
Microcontroller rewriting mode (3)(4)	FLASH-ROM	BOOT	(1)	L	H	Normal pin			H 0
D-wire communication mode(3)	FLASH-ROM	-	(2)	L	(2)	Pull up(2)	Pull up(2)	L	0

(1)The mode becomes fixed from the pin state in releasing NRST(L to H).

(2)This is controlled by a dedicated on-board programmer

(3)This mode becomes the rewriting mode only for Flash microcontroller. Therefore does not exist in the Mask version (MN101E29G)

(4)The microcontroller rewriting mode can not be available in security-set MN101EF29G * Refer to Chapter 18 for details.

1.3.2 Pin Specification

Table:1.3.1 Pin Specification

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P00	RXD1A	SBI1A	in/out	P0DIR0	P0PLU0	RXD1A: UART1 reception data input	SBI1A: Serial1 reception data output
P01	TM7IOB	LED0				TM7IOB: Timer 7 input / output	LED0: LED driver pin 0
	TXD1A	SBO1A	in/out	P0DIR1	P0PLUD1	TXD1A: UART1 transmission data output	SBO1A: Serial1 transmission data output
P02	TM8IOB	LED1				TM8IOB: Timer 8 input / output	LED1: LED driving pin 1
	SBT1A	TM9IOB	in/out	P0DIR2	P0PLUD2	SBT1A: Serial 1 clock input / output	TM9IOB: Timer 9 input / output
P03	LED2					LED2: LED driving pin 2	
P04	RMOUTB	TM0IOB	in/out	P0DIR3	P0PLUD3	RMOUTB: Remote control carrier output	TM0IOB: Timer 0 input / output
	TM2IOB	LED3				TM2IOB: Timer 2 input / output	LED3: LED driving pin 3
P05	LED4	SBO3A	in/out	P0DIR4	P0PLUD4	LED4: LED driving pin 4	SBO3A: Serial3 transmission data output
	TXD3A					TXD3A: UART3 transmission data output	
P06	LED5	SBI3A	in/out	P0DIR5	P0PLUD5	LED5: LED driving pin 5	SBI3A: Serial3 reception data output
	RXD3A					RXD3A: UART3 reception data input	
P07	LED6	SBT3A	in/out	P0DIR6	P0PLUD6	LED6: LED driving pin 6	SBT3A: Serial3 clock input / output
	LED7	DA_A	in/out	P0DIR7	P0PLUD7	LED7: LED driving pin 7	DA_A: Analog0 output
P10	SEG49	TM0IOC	in/out	P1DIR0	P1PLUD0	SEG49: Segment49 output	TM0IOC: Timer0 input / output
	RMOUTC					RMOUTC: Remote control carrier output	
P11	SEG48	TM2IOC	in/out	P1DIR1	P1PLUD1	SEG48: Segment48 output	TM2IOC: Timer2 input / output
P12	SEG47	TM1IOC	in/out	P1DIR2	P1PLUD2	SEG47: Segment47 output	TM1IOC: Timer1 input / output
P13	SEG46	TM3IOC	in/out	P1DIR3	P1PLUD3	SEG46: Segment46 output	TM3IOC: Timer3 input / output
P14	SEG45	TM4IOC	in/out	P1DIR4	P1PLUD4	SEG45: Segment45 output	TM4IOC: Timer4 input / output
P15	SEG44	TM7IOC	in/out	P1DIR5	P1PLUD5	SEG44: Segment44 output	TM7IOC: Timer7 input / output
P16	BUZZERB					BUZZERB: Buzzer output	
	SEG43	TM8IOC	in/out	P1DIR6	P1PLUD6	SEG43: Segment43 output	TM8IOC: Timer8 input / output
	NBUZZERB					NBUZZERB: Buzzer inversion output	
P20	SEG54	IRQ0	in/out	P2DIR0	P2PLUD0	SEG54: Segment54 output	IRQ0: External interrupt0
	ACZ0					ACZ0: Zero-cross detection input	
P21	SEG53	IRQ1	in/out	P2DIR1	P2PLUD1	SEG53: Segment53 output	IRQ1: External interrupt1
	ACZ1					ACZ1: Zero-cross detection input	
P22	SEG52	IRQ2	in/out	P2DIR2	P2PLUD2	SEG52: Segment52 output	IRQ2: External interrupt2
P23	SEG51	IRQ3	in/out	P2DIR3	P2PLUD3	SEG51: Segment51 output	IRQ3: External interrupt3
P24	SEG50	IRQ4	in/out	P2DIR4	P2PLUD4	SEG50: Segment50 output	IRQ4: External interrupt4
P27	NRST		in	-	-	NRST: Reset	

Pins	Special Functions	I/O	Direction Control	Pin Control	Functions Description	
P30	SEG42	SBO2B	in/out	P3DIR0	P3PLUD0	SEG42: Segment42 output SBO2B: Serial2 transmission data output
	TXD2B					TXD2B: UART2 transmission data output
P31	SEG41	SBI2B	in/out	P3DIR1	P3PLUD1	SEG41: Segment41 output SBI2B: Serial2 reception data output
	RXD2B					RXD2B: UART2 reception data input
P32	SEG40	SBT2B	in/out	P3DIR2	P3PLUD2	SEG40: Segment40 output SBT2B: Serial2 clock input / output
P33	SEG39	SBO4B	in/out	P3DIR3	P3PLUD3	SEG39: Segment39 output SBO4B: Serial4 transmission data output
	SDA4B					SDA4B: IIC4 data input / output
P34	SEG38	SBT4B	in/out	P3DIR4	P3PLUD4	SEG38: Segment38 output SBT4B: Serial4 clock input / output
	SCL4B					SCL4B: IIC4 clock input / output
P35	SEG37	SBI4B	in/out	P3DIR5	P3PLUD5	SEG37: Segment37 output SBI4B: Serial4 reception data output
P36	SEG36		in/out	P3DIR6	P3PLUD6	SEG36: Segment36 output
P40	SEG35	SBO3B	in/out	P4DIR0	P4PLUD0	SEG35: Segment35 output SBO3B: Serial3 transmission data output
	TXD3B					TXD3B: UART3 transmission data output
P41	SEG34	SBI3B	in/out	P4DIR1	P4PLUD1	SEG34: Segment34 output SBI3B: Serial3 reception data output
	RXD3B					RXD3B: UART3 reception data input
P42	SEG33	SBT3B	in/out	P4DIR2	P4PLUD2	SEG33: Segment33 output SBT3B: Serial3 clock input / output
P43	SEG32	SBO0B	in/out	P4DIR3	P4PLUD3	SEG32: Segment32 output SBO0B: Serial0 transmission data output
	TXD0B					TXD0B: UART0 transmission data output
P44	SEG31	SBI0B	in/out	P4DIR4	P4PLUD4	SEG31: Segment31 output SBI0B: Serial0 reception data output
	RXD0B					RXD0B: UART0 reception data input
P45	SEG30	SBT0B	in/out	P4DIR5	P4PLUD5	SEG30: Segment30 output SBT0B: Serial0 clock input / output
P46	SEG29	SDA5B	in/out	P4DIR6	P4PLUD6	SEG29: Segment29 output SDA5B: IIC5 data input / output
P47	SEG28	SCL5B	in/out	P4DIR7	P4PLUD7	SEG28: Segment28 output SCL5B: IIC5 clock input / output
P50	SEG20	KEY0	in/out	P5DIR0	P5PLUD0	SEG20: Segment20 output KEY0: KEY interrupt input0
	D0	SBO0A				D0: Data input / output(bp0) SBO0A: Serial0 transmission data output
P51	TXD0A					TXD0A: UART0 reception data input
SEG21	KEY1	KEY1	in/out	P5DIR1	P5PLUD1	SEG21: Segment21 output KEY1: KEY interrupt input1
D1	SBI0A					D1: data input / output(bp1) SBI0A: Serial0 reception data output
	RXD0A					RXD0A: UART0 transmission data output
P52	SEG22	KEY2	in/out	P5DIR2	P5PLUD2	SEG22: Segment22 output KEY2: KEY interrupt input2
D2	SBT0A					D2: Data input / output(bp2) SBT0A: Serial0 clock input / output
P53	SEG23	KEY3	in/out	P5DIR3	P5PLUD3	SEG23: Segment23 output KEY3: KEY interrupt input3
D3	BUZZERA					D3: Data input / output(bp3) BUZZERA: Buzzer output
P54	SEG24	KEY4	in/out	P5DIR4	P5PLUD4	SEG24: Segment24 output KEY4: KEY interrupt input4
D4	NBUZZERA					D4: data input / output(bp4) NBUZZERA: Buzzer inversion output
P55	SEG25	KEY5	in/out	P5DIR5	P5PLUD5	SEG25: Segment25 output KEY5: KEY interrupt input5
D5						D5: Data input / output(bp5)
P56	SEG26	KEY6	in/out	P5DIR6	P5PLUD6	SEG26: Segment26 output KEY6: KEY interrupt input6
D6						D6: data input / output(bp6)
P57	SEG27	KEY7	in/out	P5DIR7	P5PLUD7	SEG27: Segment27 output KEY7: KEY interrupt input7
D7						D7: Data input / output(bp7)

Pins	Special Functions	I/O	Direction Control	Pin Control	Functions Description	
P60	SEG19	in/out	P6DIR0	P6PLUD0	SEG19: Segment19 output	
P61	SEG18	DA_B	in/out	P6DIR1	P6PLUD1	SEG18: Segment18 output
P62	SEG17	A0	in/out	P6DIR2	P6PLUD2	SEG17: Segment17 output
	TM1IOB				TM1IOB: Timer1 input / output	
P63	SEG16	A1	in/out	P6DIR3	P6PLUD3	SEG16: Segment16 output
	TM3IOB				TM3IOB: Timer3 input / output	
P64	SEG15	A2	in/out	P6DIR4	P6PLUD4	SEG15: Segment15 output
	TM4IOB				TM4IOB: Timer4 input / output	
P65	SEG14	A3	in/out	P6DIR5	P6PLUD5	SEG14: Segment14 output
	SBI4A				SBI4A: Serial4 reception data output	
P66	SEG13	A4	in/out	P6DIR6	P6PLUD6	SEG13: Segment13 output
	SBO4A	SDA4A			SBO4A: Serial4 transmission data output	
P67	SEG12	A5	in/out	P6DIR7	P6PLUD7	SEG12: Segment12 output
	SBT4A	SCL4A			SBT4A: Serial4 clockinput / output	
					SCL4A: IIC4 clock input / output	
P70	SEG11	A6	in/out	P7DIR0	P7PLUD0	SEG11: Segment11 output
	SBO2A	TXD2A			SBO2A: Serial2 transmission data output	
P71	SEG10	A7	in/out	P7DIR1	P7PLUD1	TXD2A: UART2 transmission data output
	SBI2A	RXD2A			SEG10: Segment10 output	
					SBI2A: Serial2 reception data output	
P72	SEG9	NWE	in/out	P7DIR2	P7PLUD2	A7: Address output(bp7)
	SBT2A				RXD2A: UART2 reception data input	
P73	SDA5A	NRE	in/out	P7DIR3	P7PLUD3	NWE: Write enable signal
	SEG8				SDA5A: IIC5 data input / output	
P74	SCL5A	NCS	in/out	P7DIR4	P7PLUD4	SEG8: Segment8 output
	SEG7				SCL5A: IIC5 clock input / output	
P75	TXD1B	SBO1B	in/out	P7DIR5	P7PLUD5	NRE: Read enable signal
	A8	SEG6			SEG7: Segment7 output	
P76	RXD1B	SBI1B	in/out	P7DIR6	P7PLUD6	TXD1B: UART1 transmission data output
	A9	SEG5			RXD1B: UART1 reception data input	
P77	SBT1B	A10	in/out	P7DIR7	P7PLUD7	A8: Address output(bp8)
	SEG4				SBT1B: Serial1 clock input / output	
					SEG6: Segment6 output	
					SBO1B: Serial1 transmission data output	
					SBI1B: Serial1 reception data output	
					SEG5: Segment5output	
					A9: Address output(bp9)	
					SEG4: Segment4 output	
					A10: Address output(bp10)	
P80	TM9OD0	SDO0	in/out	P8DIR0	P8PLU0	SDO0: Timer synchronous output0
	A11	SEG3			A11: Address output(bp11)	SEG3: Segment3 output
P81	TM9OD1	SDO1	in/out	P8DIR1	P8PLU1	SDO1: Timer synchronous output1
	A12	SEG2			A12: Address output(bp12)	SEG2: Segment2 output
P82	TM9OD2	SDO2	in/out	P8DIR2	P8PLU2	SDO2: Timer synchronous output2
	A13	SEG1			A13: Address output(bp13)	SEG1: Segment1 output
P83	TM9OD3	SDO3	in/out	P8DIR3	P8PLU3	SDO3: Timer synchronous output3
	A14	SEG0			A14: Address output(bp14)	SEG0: Segment0 output
P84	TM9OD4	SDO4	in/out	P8DIR4	P8PLU4	SDO4: Timer synchronous output4
	A15	COM0			A15: Address output(bp15)	COM0: LCD common output
P85	TM9OD5	SDO5	in/out	P8DIR5	P8PLU5	SDO5: Timer synchronous output5
	A16	COM1			A16: Address output(bp16)	COM1:LCD common output
P86	SDO6	A17	in/out	P8DIR6	P8PLU6	A17: Address output(bp17)
	COM2				SDO6: Timer synchronous output6	COM2:LCD common output
P87	SDO7	A18	in/out	P8DIR7	P8PLU7	SDO7: Timer synchronous output7
	COM3				COM3:LCD common output	A18: Address output(bp18)

Pins	Special Functions	I/O	Direction Control	Pin Control	Functions Description	
P90	XI	in	P9DIR0	P9PLU0	XI: Clock input pin	
P91	XO	out	P9DIR1	P9PLU1	XO: Clock output pin	
P92	A19	V _{LC3}	in/out	P9DIR2	P9PLU2	A19: Address output(bp19)
P93	NDK	V _{LC2}	in/out	P9DIR3	P9PLU3	NDK: Data acknowledge signal
P94	V _{LC1}	DA_C	in/out	P9DIR4	P9PLU4	V _{LC1} :LCD power supply
P95	DA_D		in/out	P9DIR5	P9PLU5	DA_C: AnalogC output
P96			in/out	P9DIR6	P9PLU6	DA_D: AnalogD output
PA0	RMOUTA AN0	TM0IOA	in/out	PADIR0	PAPLU0	RMOUTA:Remote control career output AN0: Analog0 input
PA1	TM1IOA	AN1	in/out	PADIR1	PAPLU1	TM1IOA: Timer1 input / output
PA2	TM2IOA	AN2	in/out	PADIR2	PAPLU2	TM2IOA: Timer2 input / output
PA3	TM3IOA	AN3	in/out	PADIR3	PAPLU3	TM3IOA: Timer3 input / output
PA4	TM4IOA	AN4	in/out	PADIR4	PAPLU4	TM4IOA: Timer4 input / output
PA5	TM7IOA	AN5	in/out	PADIR5	PAPLU5	TM7IOA: Timer7 input / output
PA6	TM8IOA	AN6	in/out	PADIR6	PAPLU6	TM8IOA: Timer8 input / output
PA7	TM9IOA	AN7	in/out	PADIR7	PAPLU7	TM9IOA: Timer9 input / output
PB0	AN8		in/out	PBDIR0	PBPLU0	AN8: Analog8 input
PB1	AN9		in/out	PBDIR1	PBPLU1	AN9: Analog9 input
PB2	AN10		in/out	PBDIR2	PBPLU2	AN10: Analog10 input
PB3	AN11		in/out	PBDIR3	PBPLU3	AN11: Analog11 input
PB4	AN12		in/out	PBDIR4	PBPLU4	AN12: Analog12 input
PB5	AN13		in/out	PBDIR5	PBPLU5	AN13: Analog13 input
PB6	AN14		in/out	PBDIR6	PBPLU6	AN14: Analog14 input
PB7	AN15		in/out	PBDIR7	PBPLU7	AN15: Analog15 input

1.3.3 Pin Functions

Table:1.3.2 Pin Functions

Name	NO	I/O	Other Function	Function	Description
V _{SS} V _{DD5}	15 18	-		Power connect pins	Apply 2.2 V to 5.5 V to V _{DD5} and 0 V to V _{SS} . Connect approximate 10-times capacity to connect to V _{DD18} pin for stabilization of internal power supply.
V _{DD18} (Capacity 1.8V)	19			Capacity connect pins	For internal power circuit output stability, connect at least one bypass capacitor of 1 uF or larger between V _{DD18} and V _{SS} .
OSC1 OSC2	16 17	Input Output		Clock input pins Clock output pins	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	14 13	Input Output	P90, P91	Clock input pins Clock output pins	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. the chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to V _{SS} and leave XO open.
NRST	12	Input	P27	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. 50 kΩ). Setting this pin low initializes the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and V _{SS} , it is recommended that a discharge diode be placed between NRST and V _{DD} .
ATRST	11	input		Auto reset setting pin	Input "H" to enable auto reset function and "L" to disable this function
P00 P01 P02 P03 P04 P05 P06 P07	22 23 24 25 26 27 28 29	I/O	RXD1A,SBI1A,TM7IOB,LED0 TXD1A,SBO1A,TM8IOB,LED 1 SBT1A,TM9IOB,LED2 RMOUTB,TM0IOB, TM2IOB,LED3 LED4,SBO3A,TXD3A LED5,SBI3A,RXD3A LED6,SBT3A LED7,DA_A	I/O port0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) Direct LED drive available at output. At reset, the input mode is selected and pull-up resistors are disabled (high impedance) .
P10 P11 P12 P13 P14 P15 P16	35 36 37 38 39 40 41	I/O	SEG49,TM0IOC,RMOUTC SEG48,TM2IOC SEG47,TM1IOC SEG46,TM3IOC SEG45,TM4IOC SEG44,TM7IOC,BUZZERB SEG43,TM8IOC,NBUZZERB	I/O port1	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P1PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance) .

Name	NO	I/O	Other Function	Function	Description
P20	30	I/O	SEG54,IRQ0,ACZ0	I/O port2	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P2PLUD register.
P21	31		SEG53,IRQ1,ACZ1		
P22	32		SEG52,IRQ2		
P23	33		SEG51,IRQ3		
P24	34		SEG50,IRQ4		A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P27	12	input	NRST	I/O port2	Port P27 has an N-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.
P30	42	I/O	SEG42,SBO2B,TXD2B	I/O port3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P3PLUD register.
P31	43		SEG41,SBI2B,RXD2B		
P32	44		SEG40,SBT2B		
P33	45		SEG39,SBO4B,SDA4B		
P34	46		SEG38,SBT4B,SCL4B		
P35	47		SEG37,SBI4B		
P36	48		SEG36		A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P40	49	I/O	SEG35,SBO3B,TXD3B	I/O port4	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register.
P41	50		SEG34,SBI3B,RXD3B		
P42	51		SEG33,SBT3B		
P43	52		SEG32,SBO0B,TXD0B		
P44	53		SEG31,SBI0B,RXD0B		
P45	54		SEG30,SBT0B		
P46	55		SEG29,SDA5B		
P47	56		SEG28,SCL5B		A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P50	64	I/O	SEG20,KEY0,D0,SBO0A, TXD0A	I/O port5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register.
P51	63		SEG21,KEY1,D1,SBI0A, RXD0A		
P52	62		SEG22,KEY2,D2,SBT0A		
P53	61		SEG23,KEY3,D3,BUZZERA		
P54	60		SEG24,KEY4,D4,NBUZZERA		
P55	59		SEG25,KEY5,D5		
P56	58		SEG26,KEY6,D6		
P57	57		SEG27,KEY7,D7		A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P60	65	I/O	SEG19	I/O port6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P6PLUD register.
P61	66		SEG18,DA_B		
P62	67		SEG17,A0,TM1IOB		
P63	68		SEG16,A1,TM3IOB		
P64	69		SEG15,A2,TM4IOB		
P65	70		SEG14,A3,SBI4A		
P66	71		SEG13,A4,SBO4A,SDA4A		
P67	72		SEG12,A5,SBT4A,SCL4A		A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P70	73	I/O	SEG11,A6,SBO2A,TXD2A	I/O port7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register.
P71	74		SEG10,A7,SBI2A,RXD2A		
P72	75		SEG9,NWE,SBT2A		
P73	76		SEG8,SDA5A,NRE		
P74	77		SEG7,SCL5A,NCS		
P75	78		SEG6,TXD1B,SBO1B,A8		
P76	79		SEG5,RXD1B,SBI1B,A9		
P77	80		SEG4,SBT1B,A10		A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)

Name	NO	I/O	Other Function	Function	Description
P80	81	I/O	TM9OD0,SDO0,A11,SEG3	I/O port8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P81	82		TM9OD1,SDO1,A12,SEG2		
P82	83		TM9OD2,SDO2,A13,SEG1		
P83	84		TM9OD3,SDO3,A14,SEG0		
P84	85		TM9OD4,SDO4,A15,COM0		
P85	86		TM9OD5,SDO5,A16,COM1		
P86	87		SDO6,A17,COM2		
P87	88		SDO7,A18,COM3		
P90	14	I/O	XI	I/O port9	7-bit CMOS tri-state I/O port.
P91	13		XO		Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register.
P92	89		A19,V _{LC3}		
P93	90		NDK,V _{LC2}		
P94	91		DA_C,V _{LC1}		
P95	92		DA_D		
P96	20				
PA0	1	I/O	RMOUTA,TM0IOA,AN0	I/O portA	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
PA1	2		TM1IOA,AN1		
PA2	3		TM2IOA,AN2		
PA3	4		TM3IOA,AN3		
PA4	5		TM4IOA,AN4		
PA5	6		TM7IOA,AN5		
PA6	7		TM8IOA,AN6		
PA7	8		TM9IOA,AN7		
PB0	100	I/O	AN8	I/O portB	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up resistor for each bit can be selected individually by the PBPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
PB1	99		AN9		
PB2	98		AN10		
PB3	97		AN11		
PB4	96		AN12		
PB5	95		AN13		
PB6	94		AN14		
PB7	93		AN15		
SBO0A	64	I/O	P50,SEG20,KEY0,D0	Serial interface transmission data output pins	Transmission data output pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBO0B	52		P43,SEG32,TXD0B		
SBO1A	23		TXD1A,TM8IOB,LED1,P01		
SBO1B	78		TXD1B,A8,SEG6,P75		
SBO2A	73		P70,SEG11,A6,TXD2A		
SBO2B	42		P30,SEG42,TXD2B		
SBO3A	26		P04,LED4,TXD3A		
SBO3B	49		P40,SEG35,TXD3B		
SBO4A	71		P66,SEG13,A4,SDA4A		
SBO4B	45		P33,SEG39,SDA4B		
SBI0A	63	input	P51,SEG21,KEY1,D1	Serial interface reception data input pins	Reception data output pins for serial interface 0 to 4. A pull-up resistor can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0B	53		P44,SEG31,RXD0B		
SBI1A	22		RXD1A,TM7IOB,LED0,P00		
SBI1B	79		RXD1B,A9,SEG5,P76		
SBI2A	74		P71,SEG10,A7,RXD2A		
SBI2B	43		P31,SEG41,RXD2B		
SBI3A	27		P05,LED5,RXD3A		
SBI3B	50		P41,SEG34,RXD3B		
SBI4A	70		P65,SEG14,A3		
SBI4B	47		P35,SEG37		

Name	NO	I/O	Other Function	Function	Description
SBT0A	62	I/O	P52,SEG22,KEY2,D2	Serial interface clock I/O pins	Clock I/O pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the clock I/O with the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and clock I/O by serial mode register 1 (SC0MD1 to SC4MD1) according to the communication.
SBT0B	54		P45,SEG30		These can be used as normal I/O pins when the serial interface is not used.
SBT1A	24		TM9IOB,LED2,P02		
SBT1B	80		A10,SEG4,P77		
SBT2A	75		P72,SEG9,NWE		
SBT2B	44		P32,SEG40		
SBT3A	28		P06,LED6		
SBT3B	51		P42,SEG33		
SBT4A	72		P67,SEG12,A5,SCL4A		
SBT4B	46		P34,SEG38,SCL4B		
TXD0A	64	output	P50,SEG20,KEY0,D0,SBO0A	UART transmission data output pins	In the serial interface0 to 3 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR and P7DIR registers and serial data output by serial mode register 1 (SC0MD1 to SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
TXD0B	52		P43,SEG32,SBO0B		
TXD1A	23		SBO1A,TM8IOB,LED1,P01		
TXD1B	78		SBO1B,A8,SEG6,P75		
TXD2A	73		P70,SEG11,A6,SBO2A		
TXD2B	42		P30,SEG42,SBO2B		
TXD3A	26		P04,LED4,SBO3A		
TXD3B	49		P40,SEG35,SBO3B		
RXD0A	63	input	P51,SEG21,KEY1,D1,SBI0A	UART reception data input pins	In the serial interface0 to 3 in UART mode, this pin is configured as the reception data output pin. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR and P7DIR registers and serial data input by serial mode register 1 (SC0MD1 to SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0B	53		P44,SEG30,SBI0B		
RXD1A	22		SBI1A,TM7IOB,LED0,P00		
RXD1B	79		SBI1B,A9,SEG5,P76		
RXD2A	74		P71,SEG10,A7,SBI2A		
RXD2B	43		P31,SEG41,SBI2B		
RXD3A	27		P05,LED5,SBI3A		
RXD3B	50		P41,SEG34,SBI3B		
SDA4A	71	I/O	P66,SEG13,A4,SBO4A	IIC data I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the data input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and serial data I/O by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4B	45		P33,SEG39,SBO4B		
SDA5A	76		NRE,SEG8,P73		
SDA5B	55		P46,SEG29		
SCL4A	72	I/O	P67,SEG12,A5,SBT4A		In the serial interface4, 5 in IIC mode, this pin is configured as the clock input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and clock I/O by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used
SCL4B	46		P34,SEG38,SBT4B		
SCL5A	77		NCS,SEG7,P74		
SCL5B	56		P47,SEG28		

Name	NO	I/O	Other Function	Function	Description
TM0IOA	1	I/O	RMOUTA,AN0,PA0	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 4.
TM0IOB	25		RMOUTB,TM2IOB,LED3,P03		To use this pin as event clock input, configure this as input by P0DIR register, P1DIR register, P6DIR register and PADIR register. In the input mode, pull-up resistors can be selected by the P0PLUD register, P1PLUD register, P6PLUD register and PAPLU register.
TM0IOC	35		P10,SEG49,RMOUTC		For timer output, PWM signal output, select the special function pin by port 0 output mode register, port 1 output mode register, port 6 output mode register and port A output mode register ((P0OMD, P1OMD, P6OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register.
TM1IOA	2		AN1,PA1		These can be used as normal I/O pins when are not used as timer I/O pins.
TM1IOB	67		P62,SEG17,A0		
TM1IOC	37		P12,SEG47		
TM2IOA	3		AN2,PA2		
TM2IOB	25		RMOUTB,TM0IOB,LED3,P03		
TM2IOC	36		P11,SEG48		
TM3IOA	4		AN3,PA3		
TM3IOB	68		P63,SEG16,A1		
TM3IOC	38		P13,SEG46		
TM4IOA	5		AN4,PA4		
TM4IOB	69		P64,SEG15,A2		
TM4IOC	39		P14,SEG45		
RMOUTA	1	I/O	TM0IOA,AN0,PA0	Remote control transmission signal output pins	Output pin for remote control transmission with a carrier signal.
RMOUTB	25		TM0IOB,TM2IOB,LED3,P03		For remote control carrier output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode by the P0DIR register, P1DIR register, P6DIR register and PADIR register.
RMOUTC	35		P10,SEG49,TM0IOC		At the same time, select buzzer output at oscillation stabilization waiting control register.
					These can be used as normal I/O pins when the buzzer output is not used.
BUZZERA	61	I/O	P53,SEG23,KEY3,D3	Buzzer output	Piezoelectric buzzer driving pin. Buzzer output is available to port1, port5.
BUZZERB	40		P15,SEG44,TM7IOC		The driving frequency can be selected with the DLYCTR register.
NBUZZERA	60		P54,SEG24,KEY4,D4		To select buzzer output for port1, port5, select the special function pin by the port 1 output mode register and port 5 output mode register (P1OMD and P5OMD), and set to the output mode by the P1DIR register and P5DIR register.
NBUZZERB	41		P16,SEG43,TM8IOC		At the same time, select buzzer output by the oscillation stabilization wait control register (DLYCTR).
					These can be used as normal I/O pins when the serial interface is not used.
TM7IOA	6	I/O	AN5,PA5	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 8.
TM7IOB	22		RXD1A,SBI1A,LED0,P00		To use this pin as event clock input, configure this as input with the PADIR register. In the input mode, pull-up resistors can be selected by P0PLU register, P1PLU register and PAPLU register.
TM7IOC	40		P15,SEG44,BUZZERB		For timer output, PWM signal output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register.
TM8IOA	7		AN6,PA6		These can be used as normal I/O pins when are not used as timer I/O pins.
TM8IOB	23		TXD1A,SBO1A,LED1,P01		
TM8IOC	41		P16,SEG43,NBUZZERB		
TM9IOA	8		AN7,PA7		
TM9IOB	24		SBT1A,LED2,P02		
TM9OD0	81	output	SDO0,A11,SEG3,P80	Timer output pins	timer output and PWM signal output pin for 16-bit timer.
TM9OD1	82		SDO1,A12,SEG2,P81		To select timer output and PWM signal output, select the special function pin by the P8DIR register, and set to the output mode at the P8OMD1 register.
TM9OD2	83		SDO2,A13,SEG1,P82		These can be used as normal I/O pins when are not used as timer I/O pins.
TM9OD3	84		SDO3,A14,SEG0,P83		
TM9OD4	85		SDO4,A15,COM0,P84		
TM9OD5	86		SDO5,A16,COM1,P85		

Name	NO	I/O	Other Function	Function	Description
SDO0	81	output	TM9OD0,A11,SEG3,P80	Synchronous output pins	8-bit synchronous output pins.
SDO1	82		TM9OD1,A12,SEG2,P81		Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). Set to the output mode by the P8DIR register. These pins can be used as a normal I/O pins when not used for synchronous output.
SDO2	83		TM9OD2,A13,SEG1,P82		
SDO3	84		TM9OD3,A14,SEG0,P83		
SDO4	85		TM9OD4,A15,COM0,P84		
SDO5	86		TM9OD5,A16,COM1,P85		
SDO6	87		A17,COM2,P86		
SDO7	88		A18,COM3,P87		
V _{REF+}	9	-		+ power supply for A/D converter	Reference power supply pins for the A/D converter. The values of $2.0 \text{ V} \leq V_{\text{REF+}} \leq V_{\text{DD5}}$ is used.
AN0	1	input	RMOUTA,TM0IOA,PA0	Analog input pins	Analog input pins for an 16-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
AN1	2		TM1IOA,PA1		
AN2	3		TM2IOA,PA2		
AN3	4		TM3IOA,PA3		
AN4	5		TM4IOA,PA4		
AN5	6		TM7IOA,PA5		
AN6	7		TM8IOA,PA6		
AN7	8		TM9IOA,PA7		
AN8	100		PB0		
AN9	99		PB1		
AN10	98		PB2		
AN11	97		PB3		
AN12	96		PB4		
AN13	95		PB5		
AN14	94		PB6		
AN15	93		PB7		
DA_A	29	output	P07,LED7	Analog output pins	Analog input pins for an 4-channel, 8-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
DA_B	66		P61,SEG18		
DA_C	91		V _{LC1} ,P94		
DA_D	92		P95		
IRQ0	30	input	P20,SEG54,ACZ0	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected with the IRQnICR register.
IRQ1	31		P21,SEG53,ACZ1		IRQ1 has AC zero-cross detection function. IRQ1 can be set at both edges at pin voltage level.
IRQ2	32		P22,SEG52		
IRQ3	33		P23,SEG51		When not used for interrupts, these can be used as normal input pins.
IRQ4	34		P24,SEG50		
ACZ1	31	input	P21,SEG53,IRQ1	AC zero-cross detection input pins	AC zero-cross detection input pin. AC zero-cross detection output "H" when input level is mid-level and "L" otherwise.
ACZ0	30		P20,SEG54,IRQ0		ACZ input signal is connected to P20 input and IRQ0 interrupt circuit or P21 input and IRQ1 interrupt circuit. When not used for AC zero-cross detection, these can be used as normal input pins.

Name	NO	I/O	Other Function	Function	Description
KEY0	64	input	P50,SEG20,D0,SBO0A, TXD0A	Key interrupt input pins	Input pins for interrupt based on OR result of pin inputs. These can be set to key input pins by 1-bit with the key interrupt control register (KEYT3_1IMD, KEYT3_2IMD) and by 2-bit with the key interrupt control register (KEYT3_1IMD).
KEY1	63		P51,SEG21,D1,SBI0A, RXD0A		When not used for KEY input, these pins can be used as normal I/O pins.
KEY2	62		P52,SEG22,D2,SBT0A		
KEY3	61		P53,SEG23,D3,BUZZERA		
KEY4	60		P54,SEG24,D4,NBUZZERA		
KEY5	59		P55,SEG25,D5		
KEY6	58		P56,SEG26,D6		
KEY7	57		P57,SEG27,D7		
LED0	22	I/O	RXD1A,SBI1A,TM7IOB,P00	LED drive pins	Large current output pins.
LED1	23		TXD1A,SBO1A,TM8IOB,P01		When not used for LED output, these pins can be used as normal I/O pins.
LED2	24		SBT1A,TM9IOB,P02		
LED3	25		RMOUTB,TM0IOB,TM2IOB, P03		
LED4	26		P04,SBO3A,TXD3A		
LED5	27		P05,SBI3A,RXD3A		
LED6	28		P06,SBT3A		
LED7	29		P07,DA_A		

Name	NO	I/O	Other Function	Function	Description
NWE	75	output	P72,SEG9,SBT2A	Write enable pins [Active low]	Memory control signal used when the memory area is expanded to the external of this LSI.
NRE	76		SDA5A,SEG8,P73	Read enable pins [Active low]	NWE is the strobe signal output for the write operation of the external memory and NRE is the strobe signal output for the read operation of the external memory
NCS	77		SCL5A,SEG7,P74	Chip select pins [Active low]	NCS is the chip selection signal outputs the external memory at the access.
NDK	90	input	V _{LC2} ,P93	Data acknowledge pins [Active low]	NDK is the acknowledge signal that indicates close of access to the external memory.
A0	67	output	P62,SEG17,TM1IOB	Address pin	A0-A19 is the address signal to the external memory.
A1	68		P63,SEG16,TM3IOB		D0-D7 is the data I/O signal to the external memory.
A2	69		P64,SEG15,TM4IOB		
A3	70		P65,SEG14,SBI4A		
A4	71		P66,SEG13,SBO4A,SDA4A		
A5	72		P67,SEG12,SBT4A,SCL4A		
A6	73		P70,SEG11,SBO2A,TXD2A		
A7	74		P71,SEG10,SBI2A,RXD2A		
A8	78		TXD1B,SBO1B,SEG6,P75		
A9	79		RXD1B,SBI1B,SEG5,P76		
A10	80		SBT1B,SEG4,P77		
A11	81		TM9OD0,SDO0,SEG3,P80		
A12	82		TM9OD1,SDO1,SEG2,P81		
A13	83		TM9OD2,SDO2,SEG1,P82		
A14	84		TM9OD3,SDO3,SEG0,P83		
A15	85		TM9OD4,SDO4,COM0,P84		
A16	86		TM9OD5,SDO5,COM1,P85		
A17	87		SDO6,COM2,P86		
A18	88		SDO7,COM3,P87		
A19	89		V _{LC3} ,P92		
D0	64	I/O	P50,SEG20,KEY0,SBO0A, TXD0A	Data pin	
D1	63		P51,SEG21,KEY1,SBI0A, RXD0A		
D2	62		P52,SEG22,KEY2,SBT0A		
D3	61		P53,SEG23,KEY3,BUZZERA		
D4	60		P54,SEG24,KEY4,NBUZZER A		
D5	59		P55,SEG25,KEY5		
D6	58		P56,SEG26,KEY6		
D7	57		P57,SEG27,KEY7		
COM0	85	Output	TM9OD4,SDO4,A15,P84	LCD common output pins	These pins output common signal of required timing for LCD display.
COM1	86		TM9OD5,SDO5,A16,P85		Connect to the common pins of LCD display panel.
COM2	87		SDO6,A17,P86		When the LCD functions are not used, these pins can be used as normal I/O port by the setting the LCD output control register LCCTR0.
COM3	88		SDO7,A18,P87		
V _{LC1}	91	-	SYCLK,DA_C,P94	LCD power supply pins	Supply for LCD power. Apply $5.5V \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} \geq 0$ V.
V _{LC2}	90		NDK,P93		When the internal voltage divider resistor is used, $V_{LC1}=V_{DD5}$ pin is selected as the reference voltage input pin.
V _{LC3}	89		A19,P92		When LCD is not used, V_{LC1} to V_{LC3} can be used as normal I/O pins with the setting of LCD output control register0 (LCCTR0).

Name	NO	I/O	Other Function	Function	Description
SEG0	84	output	TM9OD3,SDO3,A14,P83	LCD segment output pinas	These pins output segment signal of required timing for LCD display.
SEG1	83		TM9OD2,SDO2,A13,P82		Connect to the segment pins of the LCD display panel. When LCD display is turned off, V _{ss} level is output. These pins can be used as normal I/O pins with the setting of LCD output control register LCCTR1 to 7.
SEG2	82		TM9OD1,SDO1,A12,P81		SEG can exchange segment pins and normal port by each bit.
SEG3	81		TM9OD0,SDO0,A11,P80		
SEG4	80		SBT1B,A10,P77		
SEG5	79		RXD1B,SBI1B,A9,P76		
SEG6	78		TXD1B,SBO1B,A8,P75		
SEG7	77		SCL5A,NCS,P74		
SEG8	76		SDA5A,NRE,P73		
SEG9	75		P72,NWE,SBT2A		
SEG10	74		P71,A7,SBI2A,RXD2A		
SEG11	73		P70,A6,SBO2A,TXD2A		
SEG12	72		P67,A5,SBT4A,SCL4A		
SEG13	71		P66,A4,SBO4A,SDA4A		
SEG14	70		P65,A3,SBI4A		
SEG15	69		P64,A2,TM4IOB		
SEG16	68		P63,A1,TM3IOB		
SEG17	67		P62,A0,TM1IOB		
SEG18	66		P61,DA_B		
SEG19	65		P60		
SEG20	64		P50,KEY0,D0,SBO0A,TXD0A		
SEG21	63		P51,KEY1,D1,SBI0A,RXD0A		
SEG22	62		P52,KEY2,D2,SBT0A		
SEG23	61		P53,KEY3,D3,BUZZERA		
SEG24	60		P54,KEY4,D4,NBUZZERA		
SEG25	59		P55,KEY5,D5		
SEG26	58		P56,KEY6,D6		
SEG27	57		P57,KEY7,D7		
SEG28	56		P47,SCL5B		

Name	NO	I/O	Other Function	Function	Description
SEG29	55		P46,SDA5B		
SEG30	54		P45,SBT0B		
SEG31	53		P44,SBI0B,RXD0B		
SEG32	52		P43,SBO0B,TXD0B		
SEG33	51		P42,SBT3B		
SEG34	50		P41,SBI3B,RXD3B		
SEG35	49		P40,SBO3B,TXD3B		
SEG36	48		P36		
SEG37	47		P35,SBI4B		
SEG38	46		P34,SBT4B,SCL4B		
SEG39	45		P33,SBO4B,SDA4B		
SEG40	44		P32,SBT2B		
SEG41	43		P31,SBI2B,RXD2B		
SEG42	42		P30,SBO2B,TXD2B		
SEG43	41		P16,TM8IOC,NBUZZERB		
SEG44	40		P15,TM7IOC,BUZZERB		
SEG45	39		P14,TM4IOC		
SEG46	38		P13,TM3IOC		
SEG47	37		P12,TM1IOC		
SEG48	36		P11,TM2IOC		
SEG49	35		P10,TM0IOC,RMOUTC		
SEG50	34		P24,IRQ4		
SEG51	33		P23,IRQ3		
SEG52	32		P22,IRQ2		
SEG53	31		P21,IRQ1,ACZ1		
SEG54	30		P20,IRQ0,ACZ0		
MMOD	10	input		Memory mode switch input pins	Set always to V _{SS} .
DMOD	21	input		Mode switch input pins	Set always to V _{DD5} .

1.4 Block Diagram

1.4.1 Block Diagram

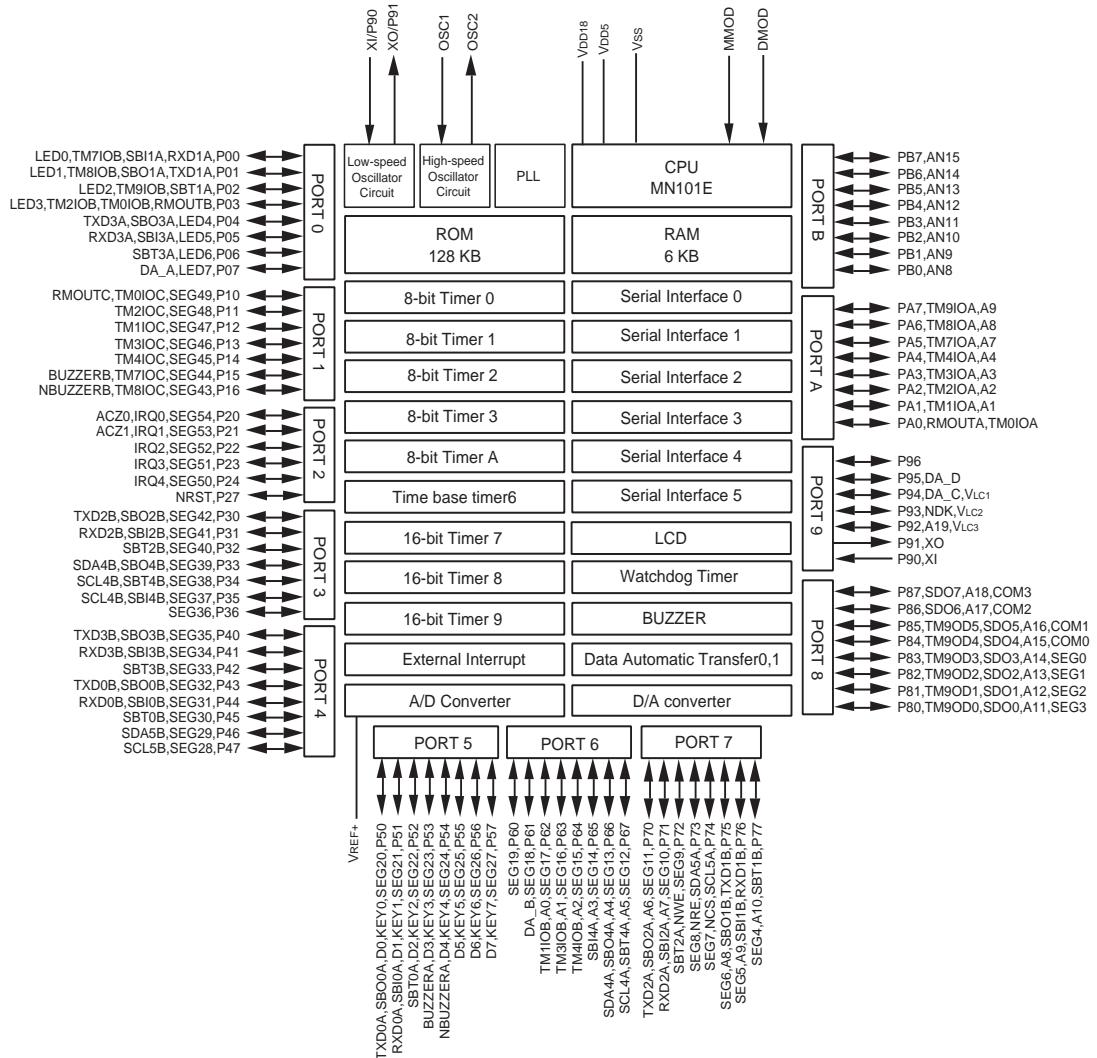


Figure:1.4.1 Block Diagram

* Depending on the models. See [1.1.2 Product Summary]

1.5 Electrical Characteristics

This LSI manual describes the standard specification.

Machine cycle (system clock f_s) is described based on the standard mode:double high oscillation $f_{osc}=f_s$ (Normal mode), $f_{osc}=f_s$ (Double speed mode), $f_s \leq 20$ MHz (Multiplied by 2 to 10 mode) at NORMAL mode, or on the clock frequency:Double low oscillation at SLOW mode. Please ask our sales offices for the product specifications.

Model	MN101E29		
Contents	Structure	CMOS integrated circuit	
	Application	General purpose	
	Function	CMOS, 8-bit, single chip micro controller	

1.5.1 Absolute Maximum Ratings

	V _{SS} =0 V			
	Parameter	Symbol	Rating	Unit
1	Power supply voltage	V _{DD5}	-0.3 to + 7.0	V
2	Capacity connect pin voltage	V _{DD18}	-0.3 to + 2.5	
3	Input clamp current(ACZ)	I _c	-500 to + 500	μA
4	Input pin voltage	V _I	-0.3 to V _{DD5} + 0.3 (up to 7)	V
5	output pin voltage	V _O	-0.3 to V _{DD5} + 0.3 (up to 7)	
6	I/O pin voltage	V _{IO1}	-0.3 to V _{DD5} + 0.3 (up to 7)	
7	Pointed output current	P ₀	I _{OL1} (peak)	30
8		Any other than P ₀	I _{OL2} (peak)	20
9		All pins	I _{OH} (peak)	-10
10	Average output current *1	P ₀	I _{OL1} (avg)	20
11		Any other than P ₀	I _{OL2} (avg)	15
12		All pins	I _{OH} (avg)	-5
13	Power dissipation	P _T	400	mW
14	Operating ambient temperature	T _{opr}	-40 to +85	°C
15	Storage temperature	T _{stg}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1μF or larger between V_{DD5} power supply pin and the ground for latch-up prevention.

*3 Connect approximate 1μF capacitor between V_{DD18} power supply pin and the ground, and apprroximate 10-times capacitor connect to V_{DD18} between V_{DD5} power supply pin and the ground for the internal power supply stabilization.

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

1.5.2 Operating Conditions

V_{SS}=0V
Ta=-40°C to +85°C

Parameter		Symbol	Conditions	Rating			Unit
MIN	TYP			MAX			
Power supply voltage *4							
1	Power supply voltage	In not using PLL	V _{DD1}	f _{osc} ≤10 MHz [Double speed mode f _s =f _{osc}]	2.2		5.5
2		In using PLL	V _{DD2}	4.0 MHz≤f _{osc} ≤10 MHz [Multiplied by 2 to 10 f _s ≤20 MHz]	2.2		5.5
3			V _{DD3}	f _x =32.768 kHz [Normal mode f _s =f _x /2]	2.2		5.5
4		Voltage to maintain RAM data	V _{DD4}	[During STOP mode]	1.8		5.5
Operating speed *5							
5	Minimum instruction execution time	In not using PLL	t _{c1}	V _{DD5} =2.2V to 5.5V	0.10		
6		In using PLL	t _{c2}	V _{DD5} =2.2V to 5.5V	0.05		
7			t _{c3}	V _{DD5} =2.2V to 5.5V	61		

*4 f_{osc} : Input clock frequency to OSC1 pin.
f_x : Input clock frequency to XI pin

*5 t_{c1} : In the case of OSC1 as CPU clock.
t_{c2} : In the case of multiplied OSC1 by PLL as CPU clock.
t_{c3} : In the case of XI as CPU clock.

Note Use LCD power supply voltage with V_{LC1}≤V_{DD5}.

V_{SS}=0V
Ta=-40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Crystal oscillator 1 Fig.1-5-1 [NORMAL mode]						
8	Crystal frequency	f _{xtal1}	V _{DD5} =within the range of operation (Refer to specified value of power supply1 to 3)	2.0		10 MHz
9	External capacitors	C ₁₁			22	pF
10		C ₁₂			22	
11	Internal feedback resistor	R _{f10}	V _{DD5} =5.0 V		950	kΩ
Crystal oscillator 2 Fig.1-5-2 [SLOW mode]						
12	Crystal frequency	f _{xtal2}	V _{DD5} =2.2 V to 5.5 V		32.768	kHz
13	External capacitors	C ₂₁			7	pF
14		C ₂₂			7	
15	Internal feedback resistor	R _{f20}	V _{DD5} =5.0 V		6	MΩ

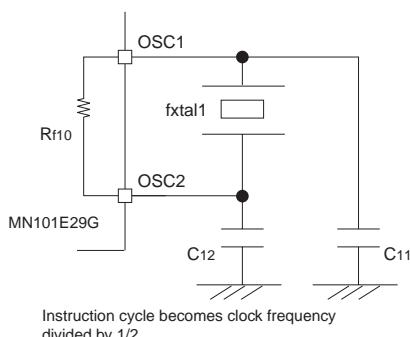


Figure:1.5.1 Crystal oscillator 1

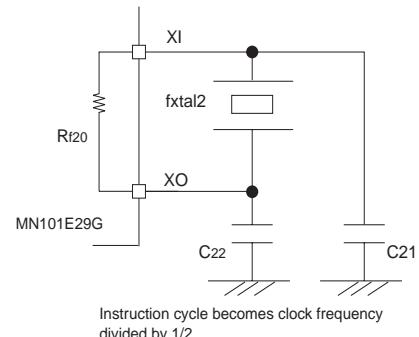


Figure:1.5.2 Crystal oscillator 2

Note Connect external capacitors that suits the used pin. When crystal oscillator or ceramic oscillator is used, the frequency is changed depending on the condenser rate. Therefore, consult the manufacturer of the pin for the appropriate external capacitor.

$V_{DD5}=2.2\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a=-40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
External clock input 1 OSC1(OSC2 is unconnected)						
16	Clock frequency	fosc1	1.0		10	MHz
17	High level pulse width *6	twh1	Fig. 1-5-3	45		
18	Low level pulse width *6	twl1		45		
19	Rising time *7	twr1	Fig. 1-5-3	0		5.0
20	Falling time *7	twf1		0		5.0
External clock input 2 XI(XO is unconnected)						
21	Clock frequency	fosc2		32.768		kHz
22	High level pulse width *6	twh2	Fig. 1-5-4	4.5		
23	Low level pulse width *6	twl2		4.5		μs
24	Rising time *7	twr2	Fig. 1-5-4	0		20
25	Falling time *7	twf2		0		20

*6 The clock duty rate in the standard mode should be 45% to 55%

*7 Rising time and falling time are different by oscillation frequency.
The max value is not a specified value but a rough value.
Consult the manufacturer of the pin for the appropriate after full matching evaluation.

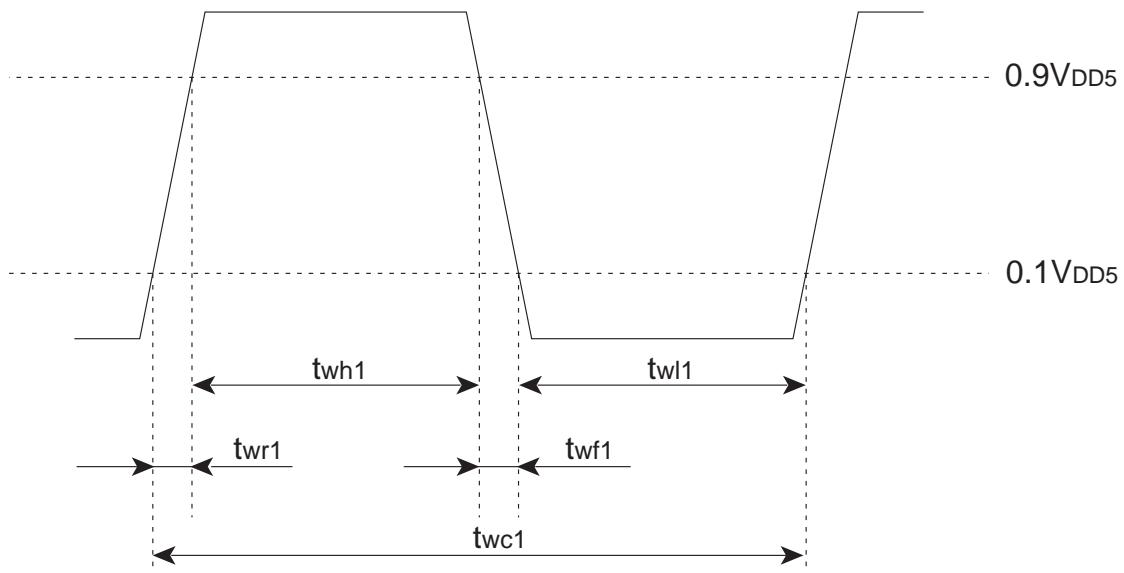


Figure:1.5.3 OSC1 Timing Chart

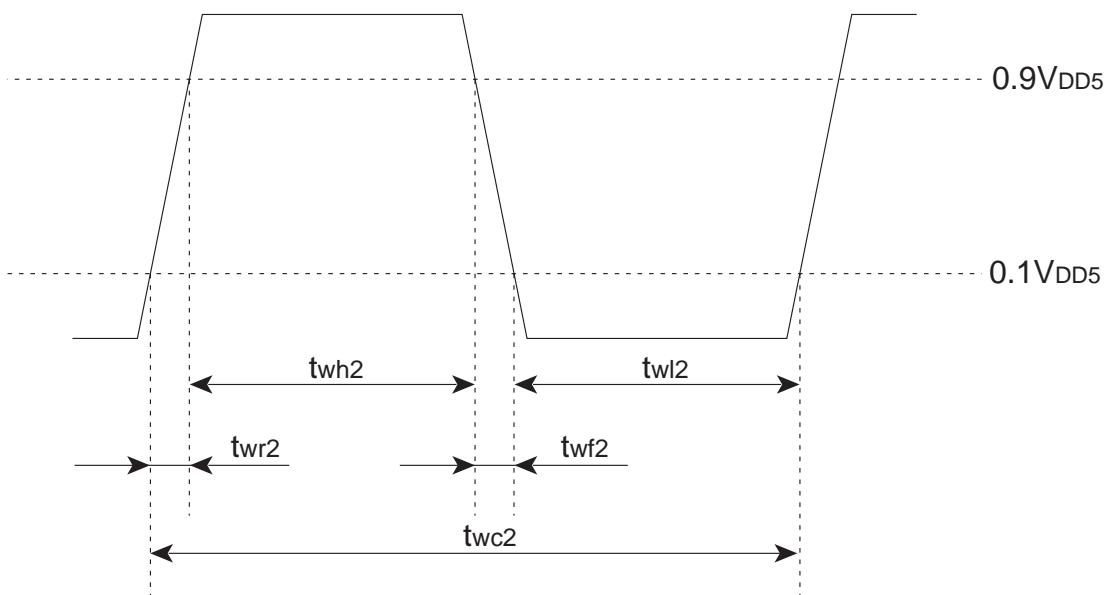


Figure:1.5.4 XI Timing Chart

1.5.3 DC Characteristics

$V_{SS}=0\text{ V}$
 $T_a=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Power supply current *8 (NORMAL mode : $fs=f_{osc}$ SLOW mode : $fs=fx/2$) Upper:M-ROM, Lower:Flash						
1 2 3 4 5 6	I_{DD1} I_{DD2} I_{DD3} I_{DD4} I_{DD5} I_{DD6}	$f_{osc}=10\text{ MHz}$ [Double-speed mode: $fs=f_{osc}$] $V_{DD5}=5\text{ V}$ (In not using PLL) $f_{osc}=8\text{ MHz}$ [Double-speed mode: $fs=f_{osc}$] $V_{DD5}=5\text{ V}$ (In not using PLL) $f_{osc}=4\text{ MHz}$ [Double-speed mode: $fs=f_{osc}$] $V_{DD5}=5\text{ V}$ (In not using PLL) $f_{osc}=4\text{ MHz}$ [Multiplied by 10: $fs=20\text{ MHz}$] $V_{DD5}=5\text{ V}$ (In using PLL) $fx=32.768\text{ MHz}$ [Normal mode: $fs=fx/2$] $T_a=25^{\circ}\text{C}$ $fx=32.768\text{ MHz}$ [Normal mode: $fs=fx/2$] $T_a=85^{\circ}\text{C}$	1.8	4.9		mA
			5.2	11		
			1.4	4.2		
			4.7	9		
			0.9	2.6		
			3	6		
7 8	I_{DD7} I_{DD8}	$fx=32.768\text{ MHz}$ $V_{DD5}=3\text{ V}$ $T_a=25^{\circ}\text{C}$ $fx=32.768\text{ kHz}$ $V_{DD5}=3\text{ V}$ $T_a=85^{\circ}\text{C}$	5.1	14		μA
			60	98		
9 10	I_{DD9}	$V_{DD5}=5\text{ V}$ $T_a=25^{\circ}\text{C}$		49		
					200	
	I_{DD10}	$V_{DD5}=5\text{ V}$ $T_a=85^{\circ}\text{C}$	3.5	11.0		
			4	16		
					50.4	
					78	
			1	5		
			1	7		
					40	
					60	

*8 Measured under conditions without load. (pull-up / pull-down resistors are unconnected.)

- The supply current during operation, I_{DD1} , I_{DD2} , I_{DD3} , I_{DD4} are measured under the following conditions:
After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 10 MHz square wave of V_{DD5} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD5} , I_{DD6} is measured under the following conditions:
After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 32.768 kHz square wave of V_{DD5} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT1 mode, I_{DD7} , I_{DD8} is measured under the following conditions:
After all I/O pins are set to input mode and the oscillation is set to <HALT1 mode>, the input pins are at V_{DD5} level, and an 32.768 kHz square wave of V_{DD5} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD9} , I_{DD10} is measured under the following conditions:
After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and the OSC1 and XI pins are unconnected.

$V_{DD5}=2.2\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a=-40^\circ\text{C to }+85^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Input pin 1 MMOD, DMOD, ATRST						
11	Input high voltage	V_{IH1}		$0.8V_{DD5}$		V_{DD5}
12	Input low voltage	V_{IL1}		0		$0.2V_{DD5}$
13	Input leakage current	I_{LK1}	$V_{IN}=0\text{ V to }V_{DD5}$			± 2 μA
I/O pin 2 P27 (NRST)						
14	Input high voltage	V_{IH2}		$0.8V_{DD5}$		V_{DD5}
15	Input low voltage	V_{IL2}		0		$0.15V_{DD5}$
16	Pull-up resistor	R_{RH1}	$V_{DD5}=5.0\text{V}$ $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100
Input pin 3 P10 to P16, P20 to P24, P30 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77						
17	Input high voltage	V_{IH3}		$0.8V_{DD5}$		V_{DD5}
18	Input low voltage	V_{IL3}		0		$0.2V_{DD5}$
19	Input leak current	I_{LK2}	$V_{IN}=0\text{ V to }V_{DD5}$			± 2 μA
20	Pull-up resistor	R_{RH2}	$V_{DD5}=5.0\text{V}$ $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100
21	Pull-down resistor	R_{RL1}	$V_{DD5}=5.0\text{V}$ $V_{IN}=V_{DD5}$ Pull-down resistor ON	10	50	100
22	Output high voltage	V_{OH1}	$V_{DD5}=5.0\text{V}$ $I_{OH}=0.5\text{ mA}$	4.5		
23	Output low voltage	V_{OL1}	$V_{DD5}=5.0\text{V}$ $I_{OL}=1.0\text{ mA}$			0.5

$V_{DD5}=2.2\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a=-40^\circ\text{C to }+85^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
I/O pin 4 P80 to P87, P90 to P96, PA0 to PA7, PB0 to PB7						
24	Input high voltage	V_{IH4}		$0.8V_{DD5}$		V_{DD5}
25	Input low voltage	V_{IL4}		0		$0.2V_{DD5}$
26	Input leak current	I_{LK3}	$V_{IN}=0\text{ V to }V_{DD5}$			± 2 μA
27	Pull-up resistor	R_{RH3}	$V_{DD5}=5.0\text{ V}$ $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100
28	Output high voltage	V_{OH2}	$V_{DD5}=5.0\text{ V}$ $I_{OH}=0.5\text{ mA}$	4.5		
29	Output low voltage	V_{OL2}	$V_{DD5}=5.0\text{ V}$ $I_{OL}=1.0\text{ mA}$			0.5
I/O pin 5 P00 to P07						
30	Input high voltage	V_{IH5}		$0.8V_{DD5}$		V_{DD5}
31	Input low voltage	V_{IL5}		0		$0.2V_{DD5}$
32	Input leak current	I_{LK4}	$V_{IN}=0\text{ V to }V_{DD5}$			± 2 μA
33	Pull-up resistor	R_{RH4}	$V_{DD5}=5.0\text{ V}$ $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100
34	Pull-down resistor	R_{RH2}	$V_{DD5}=5.0\text{ V}$ $V_{IN}=V_{DD5}$ Pull-down resistor ON	10	50	100
35	Output high voltage	V_{OH3}	$V_{DD5}=5.0\text{ V}$ $I_{OH}=0.5\text{ mA}$	4.5		
36	Output low voltage1	V_{OL3}	$V_{DD5}=5.0\text{ V}$ $I_{OL}=1.0\text{ mA}$ LED output OFF			0.5
37	Output low voltage2	V_{OL4}	$V_{DD5}=5.0\text{ V}$ $I_{OL}=1.0\text{ mA}$ LED output ON			1.0

$V_{DD5}=2.2\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a=-40^\circ\text{C to }+85^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
I/O pin 6 P20 (during used as ACZ) P21 (during used as ACZ) are stipulated 5.0 V						
38	Input high voltage1	V_{DHH}	Figure:1.5.5	4.5		
39	Input high voltage2	V_{DHL}		1.5		
40	Input low voltage1	V_{DLH}				3.5
41	Input low voltage2	V_{DLL}				0.5
42	Input clamp current	I_{C3}	$V_{IN}>0\text{ V to }V_{DD5}$			$\pm 500\text{ }\mu\text{A}$
Display output pin 1 COM0 to COM3 (At V_{LC1} , V_{SS} Voltage output) *9						
43	Output high voltage (In V_{LC1} voltage output)	V_{OCOMH}	$V_{DD5}=V_{LC1}=5.0\text{ V}$ $I_{COM} = -10\text{ }\mu\text{A}$	4.4		
44	Output low voltage (In V_{SS} voltage output)	V_{OCOML}	$V_{DD5}=V_{LC1}=5.0\text{ V}$ $I_{COM}=10\text{ }\mu\text{A}$			0.6
Display output pin 2 SEG0 to SEG40 (At V_{LC1} , V_{SS} Voltage output) *10						
45	Output high voltage (In V_{LC1} voltage output)	V_{OSEGH}	$V_{DD5}=V_{LC1}=5.0\text{ V}$ $I_{SEG} = -2\text{ }\mu\text{A}$	4.4		
46	Output low voltage (In V_{SS} voltage output)	V_{OSEGL}	$V_{DD5}=V_{LC1}=5.0\text{ V}$ $I_{SEG}=2\text{ }\mu\text{A}$			0.6
Display power pin 1 V_{LC1} , V_{LC2} , V_{LC3}						
47	Internal dividing resistor	R_{VL1}	$T_a=+25^\circ\text{C}$ (Impedance Between V_{LC1} , V_{SS})	142.5	300	570
48		R_{VL2}		15	30	60
			*11			$\text{k}\Omega$

*9 However, COM0 to COM3 are also used as P84 to P87.

*10 However, SEG0 to SEG54 are also used as P10 to P16, P20 to P24, P30 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77 and P80 to 83.

*11 The summation of 3 resistors among V_{LC1} and V_{LC2} , V_{LC2} and V_{LC3} , V_{LC3} and V_{SS} .

1.5.4 A/C Characteristics

$V_{DD5}=5.0\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
ACZ1 pin						
1	Rising time	t_{rs}	30			μs
2	Falling time	t_{fs}	30			

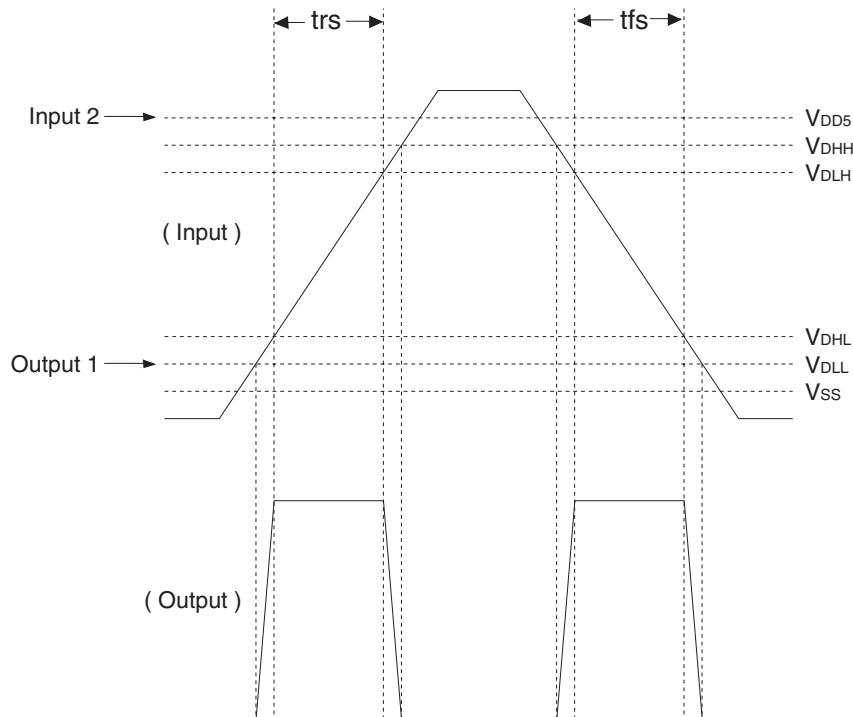


Figure:1.5.5 Operation of AC Zero-Cross Detection Circuit

1.5.5 A/D Converter Characteristics

$V_{DD} = 5.0 \text{ V}$ $V_{SS} = 0 \text{ V}$
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	None-linearity error 1		$V_{DD5} = 5.0 \text{ V}$, $V_{SS} = 0 \text{ V}$, $V_{ref+} = 5.0 \text{ V}$ $T_{AD} = 800 \text{ ns}^{*12}$			± 3	LSB
3	Differential non-linearity error					± 3	
4	Zero transition voltage		$V_{DD5} = 5.0 \text{ V}$, $V_{SS} = 0 \text{ V}$, $V_{ref+} = 5.0 \text{ V}$ $T_{AD} = 800 \text{ ns}^{*12}$	-30	10	30	mV
5	Full-scale transition voltage			4970	4990	5030	
6	A/D conversion time		$T_{AD} = 800 \text{ ns}^{*12}$	12		28	μs
7			$f_x = 32.768 \text{ kHz}$ $f_s = 8.192 \text{ kHz}$ $T_{AD} = 15.2 \mu\text{s}^{*12}$	610.37		854.53	
8	Sampling time		$T_{AD} = 800 \text{ ns}^{*12}$	1.6		14.4	
9			$f_x = 32.768 \text{ kHz}$ $T_{AD} = 15.2 \mu\text{s}^{*12}$	30.52		274.68	
10	Reference Voltage	V_{ref+}		2.0		V_{DD5}	V
11	Analog input voltage			V_{SS}		V_{ref+}	
12	Analog input leakage current		When channel is OFF $V_{ADIN} = 0 \text{ V}$ to 5.0 V			± 2	μA
13	Reference voltage pin Leakage current		In Ladder resistance OFF $V_{ref-} \leq V_{ref+} \leq V_{DD5}$			± 5	
14	Ladder resistance	R_{LADD}	$V_{DD5} = 5.0 \text{ V}$	15	40	80	k Ω

*12 T_{AD} is A/D conversion clock cycle.

The values of 2 to 5 are guaranteed on the condition that $V_{DD5}=V_{ref+}=5 \text{ V}$, $V_{SS}=0 \text{ V}$.



The reference voltage input V_{ref+} pin uses value of $2.0 \text{ V} \leq V_{ref+} \leq V_{DD5}$. When input voltage is $V_{ref+} < 2.0 \text{ V}$, there is a possibility that the microcontroller malfunctions.

1.5.6 D/A Converter Characteristics

T_a=25 °C V_{DD5} = 5.0 V V_{ss} = 0 V

Parameter	Symbol	Condition	Rationg			Unit
			MIN	TYP	MAX	
1 Resolution			-	-	8	Bits
2 Reference voltage low level	D _{AVSS}		V _{ss}	-		V
3 Reference voltage high level	D _{AVDD}			-	V _{DD5}	
4 Zero scale output voltage	V _{ZS}	D _{AVSS} =0 V D _{AVSS} =5 V D7 to D0=ALL"0"	-0.05	0	0.05	
5 Full scale output voltage	V _{FS}	D _{AVSS} =0 V D _{AVSS} =5 V D7 to D0=ALL"1"	4.93	4.98	5.03	
6 Analog output resistance (Minimum reference resistance)	R _{OAT}		5	10	15	kW
7 Non-linearity error	N _{LE}	D _{AVSS} =0 V D _{AVSS} =5 V	-	± 2.0	± 3.0	LSB
8 Differential non-linearity error	D _{NLE}	D _{AVSS} =0 V D _{AVSS} =5 V	-	± 2.0	± 3.0	
9 Setting time	T _{SET}	External capacitor CL=15 pF All bits are set to ON or OFF	-	1.5	3.0	μs

Ratings of items 7 and 8 are guaranteed at V_{DD5}=D_{AVDD}=5.0 V, V_{ss}=D_{AVSS}=0 V

1.5.7 Auto Reset Characteristics

$V_{DD5} = V_{RST}$ to 5.5 V $V_{SS} = 0$ V
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Power supply voltage						
1	Operation voltage	V_{DD7}	When using auto reset	V_{RST}	-	5.5 V
Auto reset circuit						
2	Reset detection voltage	V_{RST}	$\Delta t / \Delta V$	3.7	-	4.5 V
3	Rate of change power supply voltage	$\Delta t / \Delta V$		250	-	- $\mu\text{s/V}$
Power supply current						
4	Auto reset circuit consumption	I_{DD7}	$V_{DD5} = 5$ V	-	200	330 μA

1.5.8 Flash EEPROM Programming Condition

$V_{DD5} = 2.7$ V to 5.5 V $V_{SS} = 0$ V
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
1	Permitted times of programming	E_{max}	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-	-	1000 times

1.6 Package Dimension

Package code: QFP100-P-1818B

Units: mm

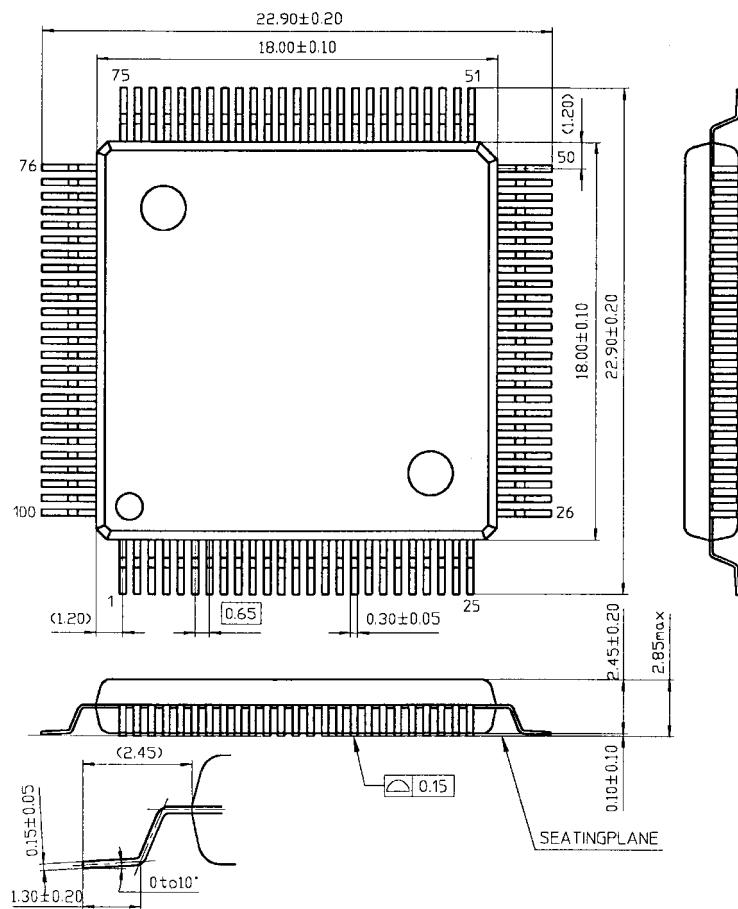


Figure:1.6.1 Package Dimension

Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating



The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Package code: LQFP100-P-1414

Units: mm

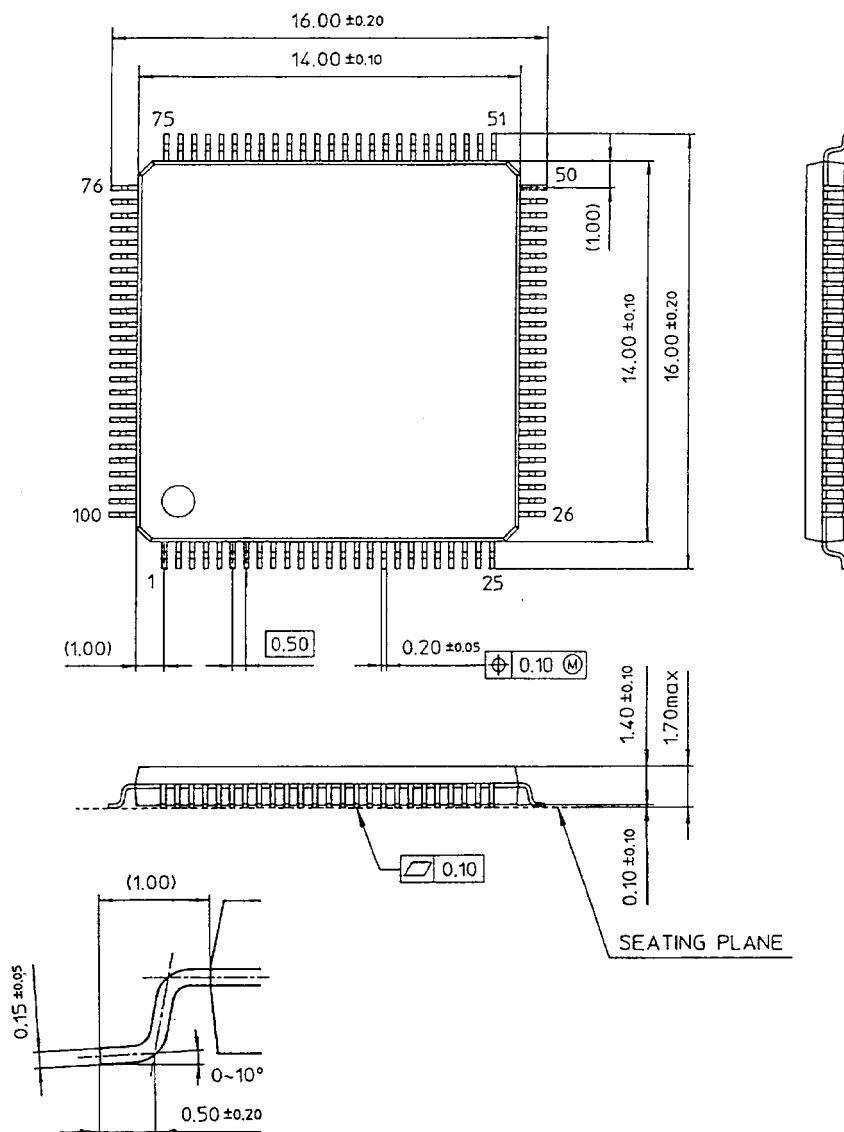


Figure:1.6.2 Package Dimension



The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

1.7 Cautions for Circuit Setup

1.7.1 General Usage

■ Connection of V_{DD5} pin and V_{SS} pin

All of the V_{DD5} and V_{SS} pins should be connected directly to the power source and ground in the external. Put them on printed circuit board after the location of LSI (package) pin is confirmed. Connection error may lead a fusion and breakdown of a micro controller.

■ V_{ref+} pin connection

When using V_{ref+} pin and V_{DD5} pin in the same potential, separate V_{ref+} pin from the root of the respective power supply.

■ Cautions for Operation

1. If you install the product close to high-field emissions (under the cathode ray tube, etc.), shield the package surface to ensure normal performance.
2. Operation temperature should be well considered. Each product has different condition. For example, if the operation temperature is over the condition, improper operation could be occurred.
3. Operation voltage should be also well considered. Each product has different operating range.
 - If the operation voltage is over the operating range, duration of the product could be shortened.
 - If the operation voltage is below the operating range, improper operation could be occurred.

1.7.2 Oscillator

This LSI's oscillation clock can be used with a ceramic and crystal oscillator.

■ Recommended oscillators

Figure:1.7.1 show basic configuration connected with a ceramic oscillator, and Table:1.7.1 shows recommended oscillators and the circuit constants.

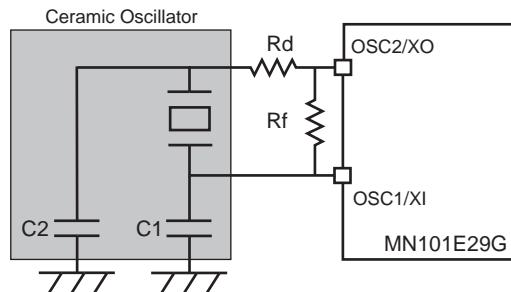


Figure:1.7.1 Basic configuration of oscillator connection

Table:1.7.1 Recommended oscillators and the circuit constants

Manufacturer	Frequency [Hz]	Oscillator Product Number	Recommended circuit constant		
			C1=C2[pF]	Feedback resistor value Rf[Ω]	Dumping resistor value Rd[Ω]
Murata Manufacturing Company, Ltd.	2M	CSTCC2M00G56Z-R0	(47)	open *	0
	4M	CSTCR4M00G55Z-R0	(39)	open *	0
		CSTLS4M00G56Z-B0	(47)	open *	0
	8M	CSTCE8M00G52Z-R0	(10)	open *	0
		CSTLS8M00G53Z-B0	(15)	open *	0
	10M	CSTCE10M00G52Z-R0	(10)	open *	0
		CSTLS10M00G53Z-B0	(15)	open *	0
EPSON TOYOCOM CORPORATION	32.768k	MC-306	4	open	0

* Insert 1 MΩ resistor in less than power supply : 2.4V for MN101E29G

() denotes internal capacity.

The above recommended value is the result of oscillator evaluation only on this LSI. After an evaluation on a set board, insert dumping resistor if needed.

Crystal oscillator is not evaluated. So consult the oscillator manufacturer for the appropriate circuit constants.



Oscillation between E29 series and E30 series which is added audio function to E29 is different. Before using, please conduct full matching evaluation.

Table:1.7.2 Recommended oscillators and the circuit constants¹

Products	Manufacturer	Frequency [Hz]	Oscillator Product Number	Recommended circuit constant			
				C1[pF] *1	C2[pF] *1	Feedback resistor value Rf[Ω]	Dumpin resistor value Rd[Ω]
MN101EF30R	Murata Manufacturing Company, Ltd	2M	CSTCC2M00G56Z-R0	(47)	(47)	open	None
		4M	CSTCR4M00G55Z-R0	(39)	(39)	open	None
		8M	CSTCE8M00G56Z-R0	(10)	(10)	open	None
		10M	CSTCE10M0G52Z-R0	(10)	(10)	open	None
		16M	CSTCE16M0V51Z-R0	(5)	(5)	open	None
		20M	CSTCE20M0V51Z-R0	(5)	(5)	open	None
	EPSON TOYOCOM CORPORATION	32.768k	MC-306	4	4	open	None
MN101E30N	Murata Manufacturing Company, Ltd	2M	CSTCC2M00G56Z-R0	(47)	(47)	open *2	None
		4M	CSTCR4M00G55Z-R0	(39)	(39)	open *2	None
		8M	CSTCE8M00G56Z-R0	(10)	(10)	open *2	None
		10M	CSTCE10M0G52Z-R0	(10)	(10)	open *2	None
		16M	CSTCE16M0V51Z-R0	(5)	(5)	open *2	None
		20M	CSTCE20M0V51Z-R0	(5)	(5)	open *2	None
	EPSON TOYOCOM CORPORATION	32.768k	MC-306	4	4	open	None

*1 Capacity denoted in () of lord capacity C1, C2 is included in oscillator.

*2 Insert 1 MΩ resistor in less than power supply : 2.4V.



Circuit constant of each ceramic or crystal oscillator, which is connected to OSC1/OSC2 or XI/XO, differs depending on stray capacitance of the oscillator or on the mounting circuit. So consult the oscillator manufacturer for the appropriate circuit constant.



When switching the products (Mask ROM version and Flash EEPROM version), matching evaluation with each product and oscillator is necessary. Mask ROM version and Flash EEPROM version may differ in their oscillation characteristics.

1.7.3 Unused pins

- Unused Pins (only for output)

Unconnect the unused output pins.

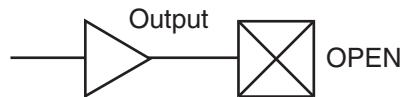


Figure:1.7.2 Unused Pins (only for output)

- Unused Pins (only for input)

Insert some $10\text{ k}\Omega$ resistor to unused pins (only for input) for pull-up or pull-down.

If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and becomes noise sources to power supply.

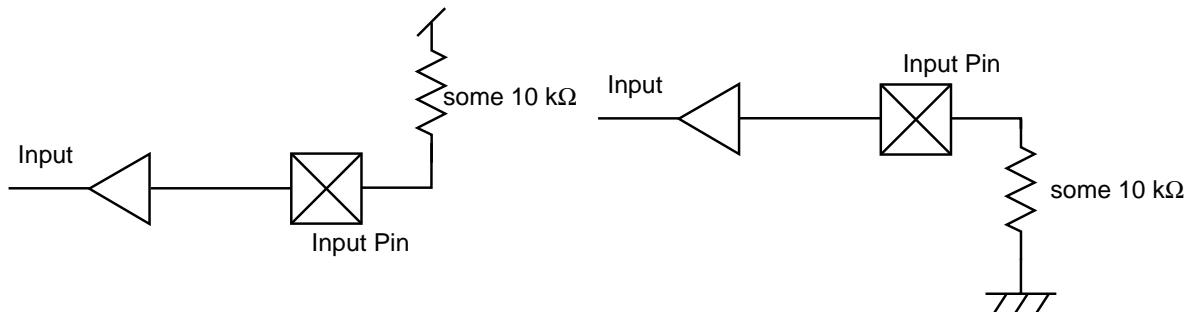


Figure:1.7.3 Unused Pins (only for input)

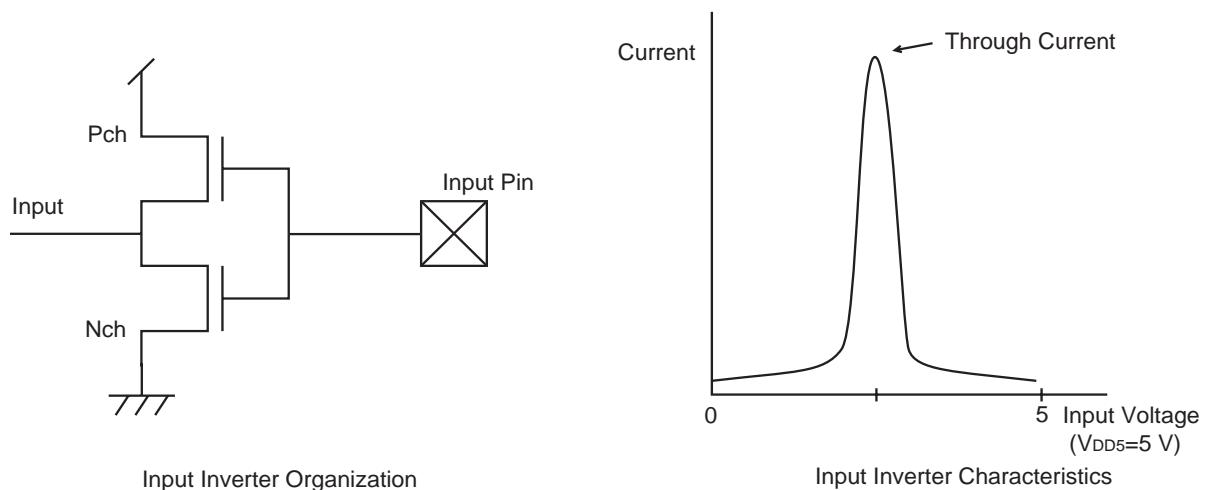


Figure:1.7.4 Input Inverter Organization and Characteristics

■ Unused Pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor: output off) at reset, to stabilize input, set some $10\text{ k}\Omega$ resistor to be pull-up or pull-down. If the output is on at reset, set them open. Pins used as both LCD and port pins should be set to open to be used as LCD output pins.

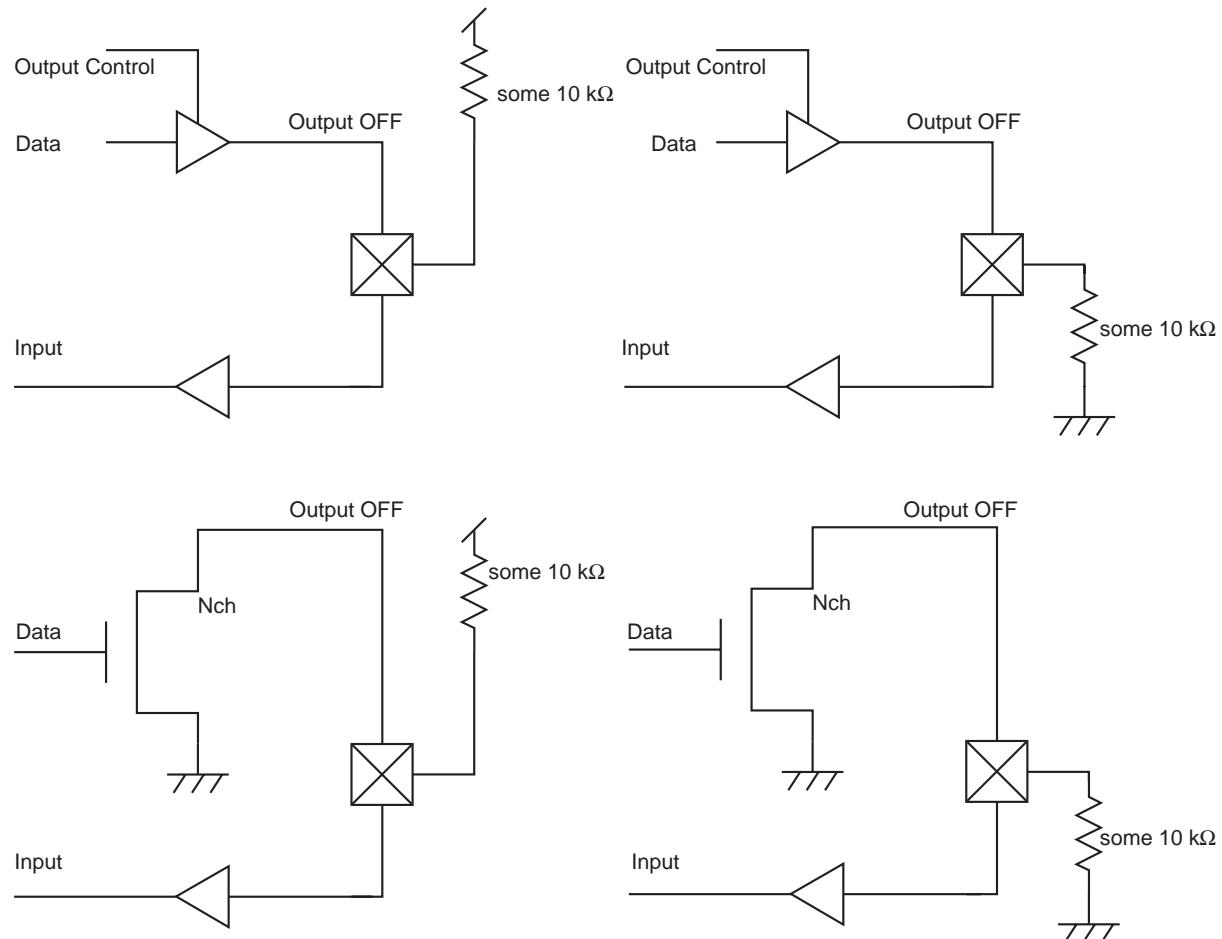


Figure 1.7.5 Unused I/O Pins (high impedance output at reset)

1.7.4 Power Supply

■ The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed the destruction of microcontroller by a large current flow could be occurred.

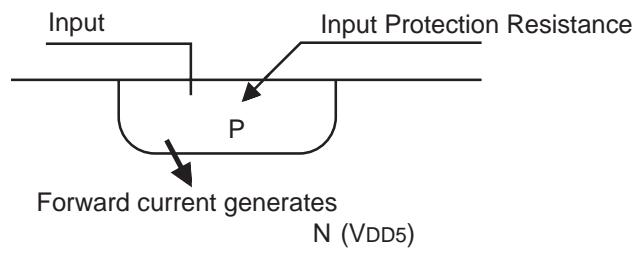


Figure:1.7.6 V_{DD5} and Input Pin Voltage

■ The Relation between V_{DD5} and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time before rising, in order to be recognized as a reset signal.

[Refer to Chapter 2. 2.8.1 Reset Operation]

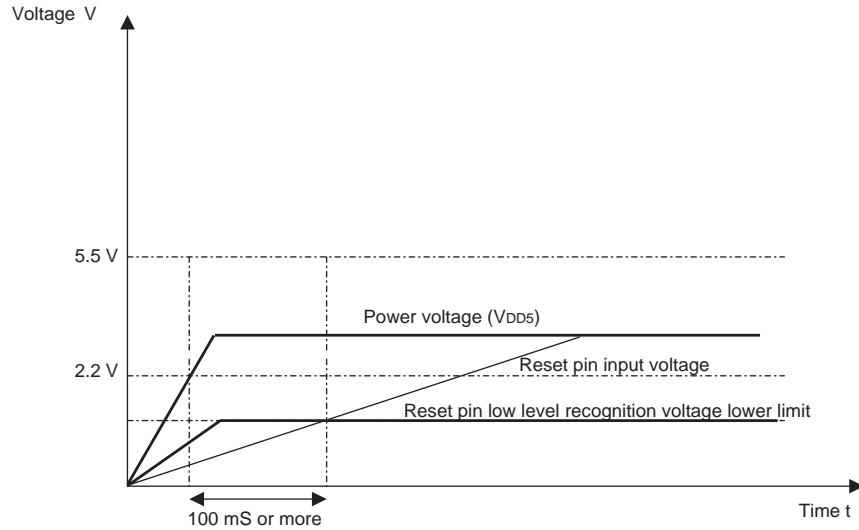


Figure 1.7.7 Power Supply and Reset Input Voltage

[In using auto reset]

■ Microcontroller Power On in using Auto Reset ($V_{DD5}=5V$)

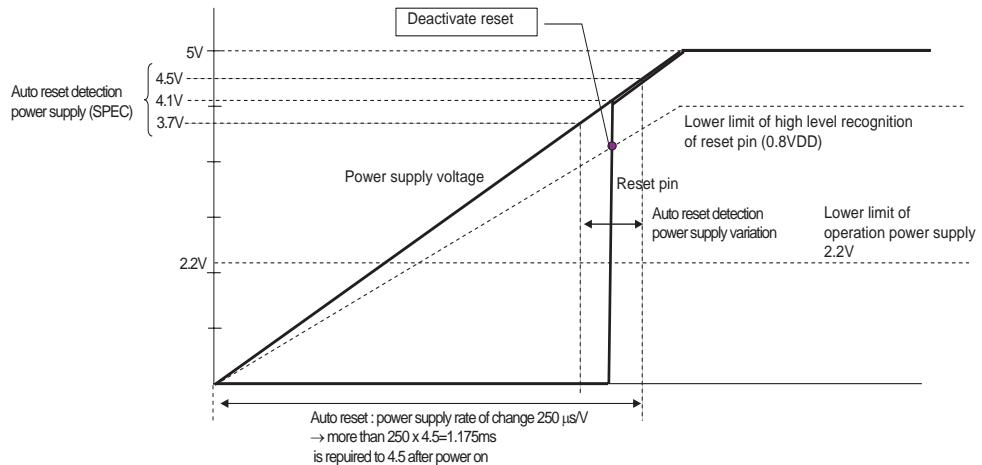


Figure 1.7.8 Microcontroller Power On in using Auto Reset

1.7.5 Power Supply Circuit

■ Cautions for Setting Circuit with V_{DD5}

The MOS logic such a microcomputer is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver.

Figure:1.7.9 shows an example for a circuit with V_{DD5} (Emitter follower type).

■ An Example for a Circuit with V_{DD5} (Emitter follower type)

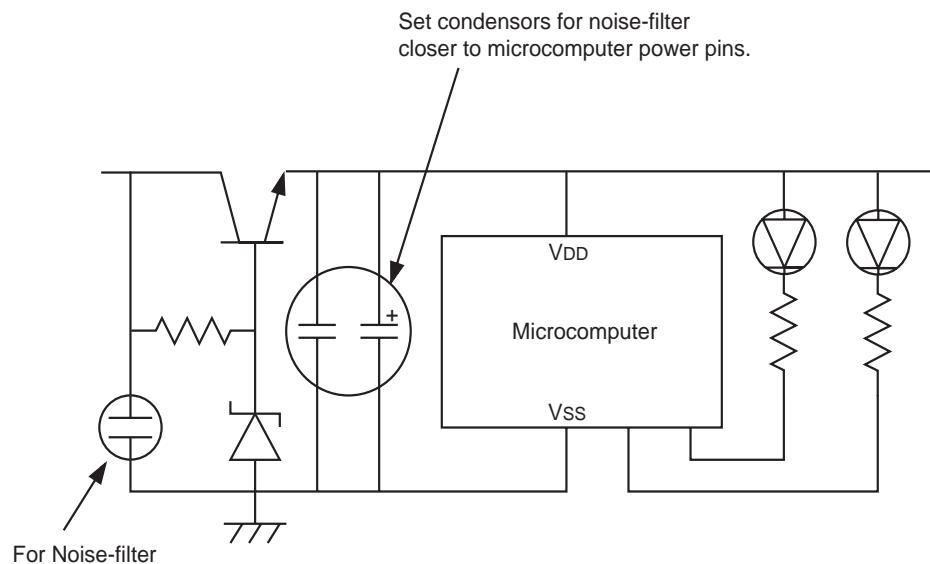


Figure:1.7.9 An Example for a Circuit of V_{DD5} Supply (Emitter follower type)

2

Chapter 2 CPU Basics

2.1 Overview

The MN101E CPU has a flexible and optimized hardware configuration. It is CPU which realizes coexistence of economical efficiency and high-speed operation with a simple and efficient instruction set. Specific features are as follows:

- Minimized code sizes with instruction lengths based on 4-bit increments:

The series keeps code sizes down by adopting a basic instruction length of one byte and variable instruction-lengths based on 4-bit increments.

- Minimum execution instruction time is one system clock cycle. (50 ns)
- Minimized register set that simplifies the architecture and supports C language :

The instruction set has been determined, depending on the size and capacity of hardware, after on analysis of embedded application programming code and creation code by C language compiler. Therefore, the set is simple instruction using the minimal register set required for C language compiler.

Table:2.1.1 Basic Specifications

Structure	Structure	
	Six registers	Data : 8-bit × 4 Address : 16-bit × 2
	Others	PC:21-bit PSW:8-bit SP:16-bit
Instructions	Number of instructions	39
	Addressing modes	9
	Instruction length	Basic portion : 1 byte (min.) Extended portion : 0.5-byte × n (0≤n≤9)
Basic performance	Internal operating frequency (max)	20 MHz *1
	Instruction execution	Min. 1 cycle
	Inter-register operation	Min. 2 cycle
	Load / store	Min. 2 cycle
	Conditional branch	2 to 3 cycles
Pipeline	3-stage (instruction fetch, decode, execution)	
Address space	1 MB (Data area : 64 KB (MAX))	
	Instruction/data space	
External bus	Address	20-bit (Max)
	Data	8-bit
	Minimum bus cycle	1 system clock cycle
Interrupt	Vector interrupt	3 interrupt levels
Low-power consumption mode	STOP mode	
	HALT mode	

*1 : Maximum operating frequency is different from the guaranteed frequency.

2.1.1 Block Diagram

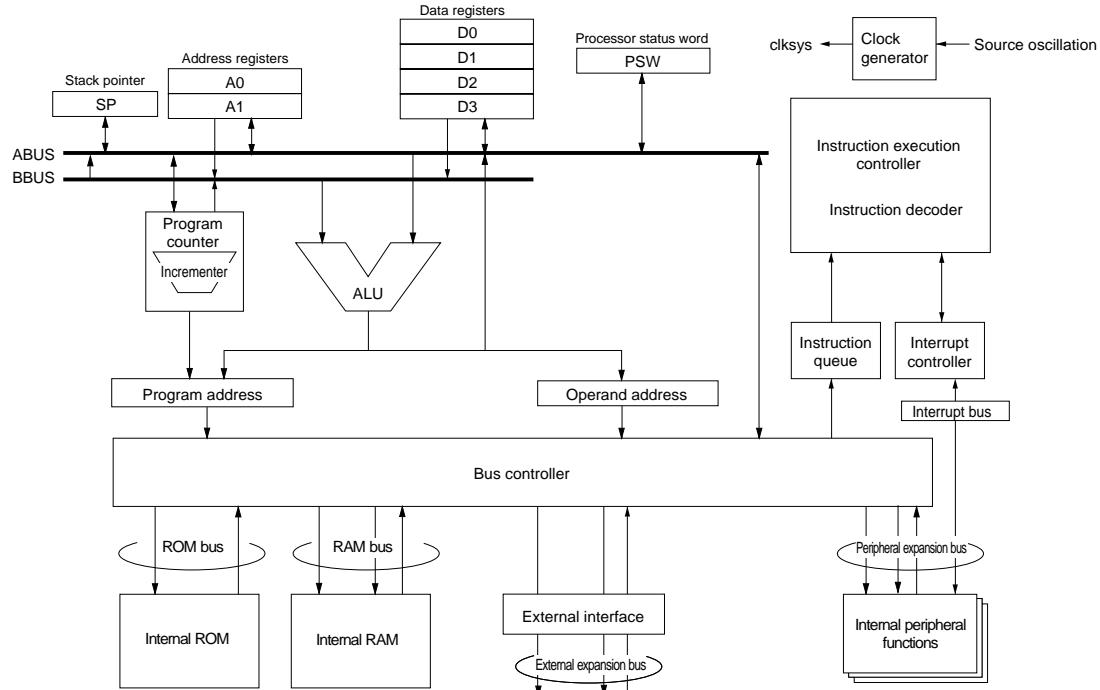


Figure:2.1.1 CPU Block Diagram

Table:2.1.2 Block Diagram and Function

Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic resonator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores up to 2 bytes of pre-fetched instructions.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ALU	Executes arithmetic operations, logic operations, shift operations, and calculates operand addresses for register relative indirect addressing mode.
Internal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Stores the addresses specifying memory for data transfer. Stores the base address for register relative indirect addressing mode.
Data register	Holds data for operations. Two 8-bit registers can be connected to form a 16-bit register.
Interrupt controller	Detects interrupt requests from peripheral functions and requests CPU shift to interrupt processing.
Bus controller	Controls connection of CPU internal bus and CPU external bus. Includes bus usage arbitration function.
Internal peripheral functions	Includes peripheral functions (timer, serial interface, A/D converter, D/A converter, etc.). Peripheral functions vary depending on the model.

2.1.2 CPU Control Registers

This LSI locates the peripheral circuit registers in memory space (0x03E00 to 0x03FFF) with memory mapped I/O. CPU control registers are also located in this memory space.

Table:2.1.3 CPU Control Registers

Registers	Address	R/W	Function	Pages
CPUM	0x03F00	R/W	CPU mode control register	II-45 II-57
MEMCTR	0x03F01	R/W	Memory control register	II-36
Reserved	0x03F04	-	(For test)	-
RCPSR	0x03FC3	R/W	ROM correction pointer specification register	II-28
RCCTR0	0x03FC4	R/W	ROM correction control register 0	II-29
AUCTR	0x03F07	R/W	Expanded Calculation Control Register	II-70
SBNKR	0x03F0A	R/W	Bank register for source address	II-22
DBNKR	0x03F0B	R/W	Bank register for destination address	II-23
Reserved	0x03F0F	-	(for test)	-
RCAPL	0x03FC0	R/W	ROM correction address register for lower 8 bits	II-30
RCAPM	0x03FC1	R/W	ROM correction address register for middle 8 bits	II-30
RCAPH	0x03FC2	R/W	ROM correction address register for upper 4 bits	II-30
Reserved	0x03FE0	-	(For debugger)	-
NMICR	0x03FE1	R/W	Non - maskable interrupt control register	III-24
xxICR	0x03FE2 to 0x03FFE	R/W	Maskable interrupt control register	III-25 to III-41
Reserved	0x03FFF	-	(For reading interrupt vector data on interrupt process)	-



Please do not access the reserved address (read-out / writing) .

2.1.3 Instruction Execution Controller

The instruction execution controller consists of four blocks: memory, instruction queue, instruction registers, and instruction decoder.

Instructions are fetched in 1-byte units, and temporarily stored in the 2-byte instruction queue. Transfer is made in 1-byte or half-byte units from the instruction queue to the instruction register to be decoded by the instruction decoder.

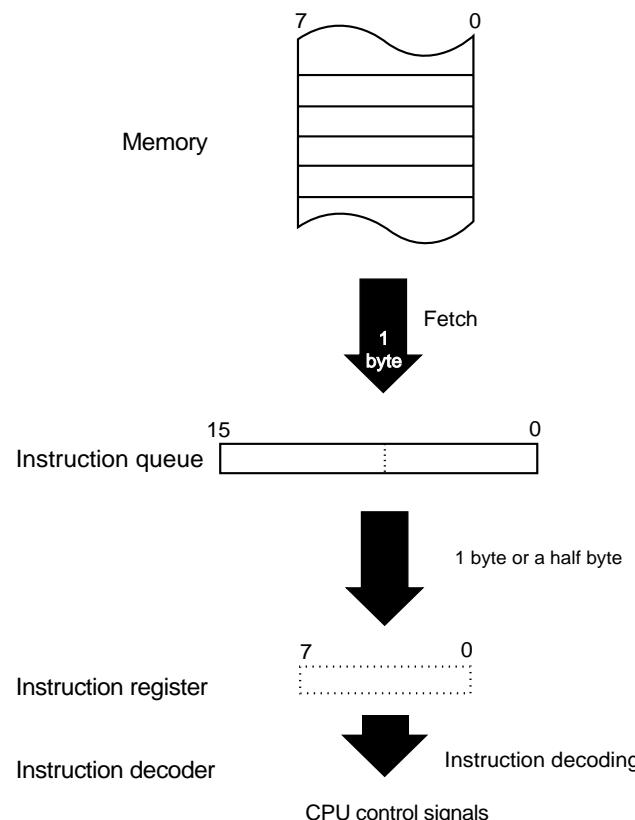


Figure:2.1.2 Instruction Execution Controller Configuration

2.1.4 Pipeline Process

Pipeline process means that reading and decoding are executed at the same time on different instructions, then instructions are executed without stopping. Pipeline process enables instruction execution continuously and faster. This process is executed with instruction queue and instruction decoder.

Instruction queue is buffer that fetches the second instruction in advance. That is controlled to fetch the next instruction when instruction queue is empty at each cycle on execution. At the last cycle of instruction execution, the first word (operation code) of executed next instruction is stored to instruction register. At that time, the next operand or operation code is fetched to instruction queue, so that the next instruction can be executed immediately, even if register direct (da) or immediate data (imm) is needed at the first cycle of the next instruction execution. But on some other instruction such as branch instruction, instruction queue becomes empty on the time that the next operation code to be executed is stored to instruction register at the last cycle. Therefore, only when instruction queue is empty, and direct address (da) or immediate data (imm) are needed, instruction queue keeps waiting for a cycle.

Instruction queue is controlled automatically by hardware so that there is no need to be controlled by software. But when instruction execution time is estimated, operation of instruction queue should be into consideration. Instruction decoder generates control signal at each cycle of instruction execution by micro program control. Instruction decoder uses pipeline process to decode instruction queue at one cycle before control signal is needed.

2.1.5 Registers for Address

Registers for address include program counter (PC), address registers (A0, A1), and stack pointer (SP)

■ Program Counter (PC)

This register gives the address of the currently executing instruction. It is 1 MB bits wide to provide access to a 21 address space in half byte(4-bit increments). The LSB of the program counter is used to indicate half byte instruction. The program counter after reset is stored from the value of vector table at the address of 0x04000.

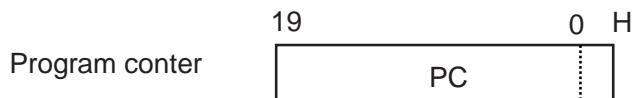


Figure:2.1.3 Program Counter

■ Address Registers (A0, A1)

These registers are used as address pointers specifying data locations in memory. They support the operations involved in address calculations (i.e. addition, subtraction and comparison). Those pointers are 2 bytes data. Transfers between these registers and memory are always in 16-bit units. Either odd or even address can be transferred. At reset, the value of address register is undefined.

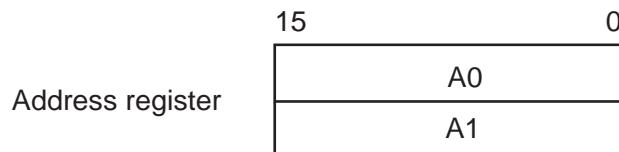


Figure:2.1.4 Address Registers

■ Stack Pointer (SP)

This register gives the address of the byte at the top of the stack. It is decremented during push operations and incremented during pop operations. At reset, the value of SP is undefined.

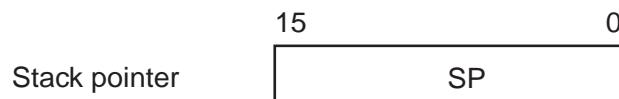


Figure:2.1.5 Stack Pointer

2.1.6 Registers for Data

Registers for data include four data registers (D0, D1, D2, D3).

■ Data Registers (D0, D1, D2, D3)

Data registers D0 to D3 are 8-bit general-purpose registers that support all arithmetic, logical and shift operations. All registers can be used for data transfers with memory. The four data registers may be paired to form the 16-bit data registers DW0 (D0+D1) and DW1 (D2+D3). At reset, the value of Dn is undefined.

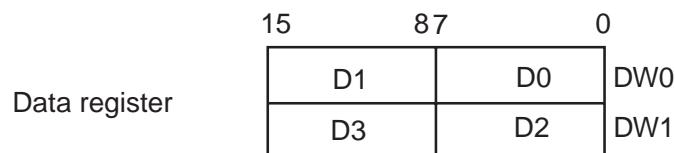


Figure:2.1.6 Data Registers

2.1.7 Processor Status Word

Processor status word (PSW) is an 8-bit register that stores flags for operation results, interrupt mask level, and maskable interrupt enable flag. PSW is automatically pushed onto the stack when an interrupt occurs and is automatically popped when return from the interrupt service routine.

■ Processor Status Word(PSW)

bp	7	6	5	4	3	2	1	0
Flag	BKD	MIE	IM1	IM0	VF	NF	CF	ZF
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	BKD	Bank disable flag 0: Bank addressing is enabled. 1: Bank addressing is disabled.
6	MIE	Maskable interrupt enable 0: All maskable interrupts are disabled. 1: (xxxLVn,xxxIE) for each interrupt is enabled.
5-4	IM1 IM0	Interrupt mask level Controls maskable interrupt acceptance.
3	VF	Overflow flag 0: Overflow does not occur. 1: Overflow occurs.
2	NF	Negative flag 0: MSB of operation results is "0". 1: MSB of operation results is "1".
1	CF	Carry flag 0: A carry or a borrow from MSB does not occur. 1: A carry or a borrow from MSB occurs.
0	ZF	Zero flag 0: Operation result is not "0". 1: Operation result is "0".

■ Zero Flag (ZF)

Zero flag (ZF) is set to "1", when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0".

■ Carry Flag (CF)

Carry flag (CF) is set to "1", when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0", when no carry or borrow occurs.

■ Negative Flag (NF)

Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value.

■ Overflow Flag (VF)

Overflow flag (VF) is set to "1", when the operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0". Overflow flag is used to handle a signed value.

■ Interrupt Mask Level (IM1 and IM0)

Interrupt mask level (IM1 and IM0) controls the maskable interrupt acceptance in accordance with the interrupt factor interrupt priority for the interrupt control circuit in the CPU. The two-bit control flag defines levels '0' to '3'. Level 0 is the highest mask level. The interrupt request will be accepted only when the level set in the interrupt level flag (xxxLV1 and xxxLV0) of the interrupt control register (xxxICR) is higher than the interrupt mask level. When the interrupt is accepted, the value of accepted interrupt level flag is set to IM1-IM0, and interrupts whose mask levels are the same or lower are rejected during the accepted interrupt processing.

Table:2.1.4 Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt level
	IM1	IM0		
Mask level 0	0	0	High	Non-maskable interrupt (NMI) only
Mask level 1	0	1	.	NMI, level 0
Mask level 2	1	0	.	NMI, level 0 to 1
Mask level 3	1	1	Low	NMI, level 0 to 2

■ Maskable Interrupt Enable (MIE)

Maskable interrupt enable flag (MIE) enables/disables acceptance of maskable interrupts by the CPU's internal interrupt acceptance circuit. The setting the flag to "1" enables maskable interrupts; the setting to "0" disables all maskable interrupts regardless of the interrupt mask level (IM1-IM0) setting in PSW. This flag is not changed by interrupts.

■ Bank disable flag (BKD)

Bank disable flag (BKD) enables/disables bank addressing of 64 KB unit. When this flag is set to "0", bank addressing is enabled and you can access to total 16 banks by setting the bank register value. When this flag is set to "1", bank addressing is disabled and the only area you can access is the first 64 KB. On an interrupt generation, BKD flag is automatically set to "1" and bank addressing is disabled. At returning from interrupt service routine, the value of BKD flag is returned to the previous one. (before the interrupt generation)



To enable bank addressing in an interrupt service routine, reset the BKD flag to "0" before accessing to data.



Make mascable interrupt enable flag (MIE) of processore status word (PSW) of prohibited all mascable interrupts (Set MIE flag to "0") before writing to interrupt control register (xxxICR). If writing to interrupt control register with setting MIE flag to "1", we can not guarantee normal operation.

2.1.8 Address Space

The address space of this LSI is 1 MB. (max.) The instruction and data areas are in the same area.

The instruction area can be used as linear address space. The data area needs bank specification in every 64 KB. (The initial value is first 64 KB space). The data described in this section includes RAM data and ROM table data.

The data area consists of an area of 256 bytes that supports efficient accesses with RAM short addressing and an area of 256 bytes that supports efficient accesses with I/O short addressing.

The memory control register controls the operation of the memory to be expanded.

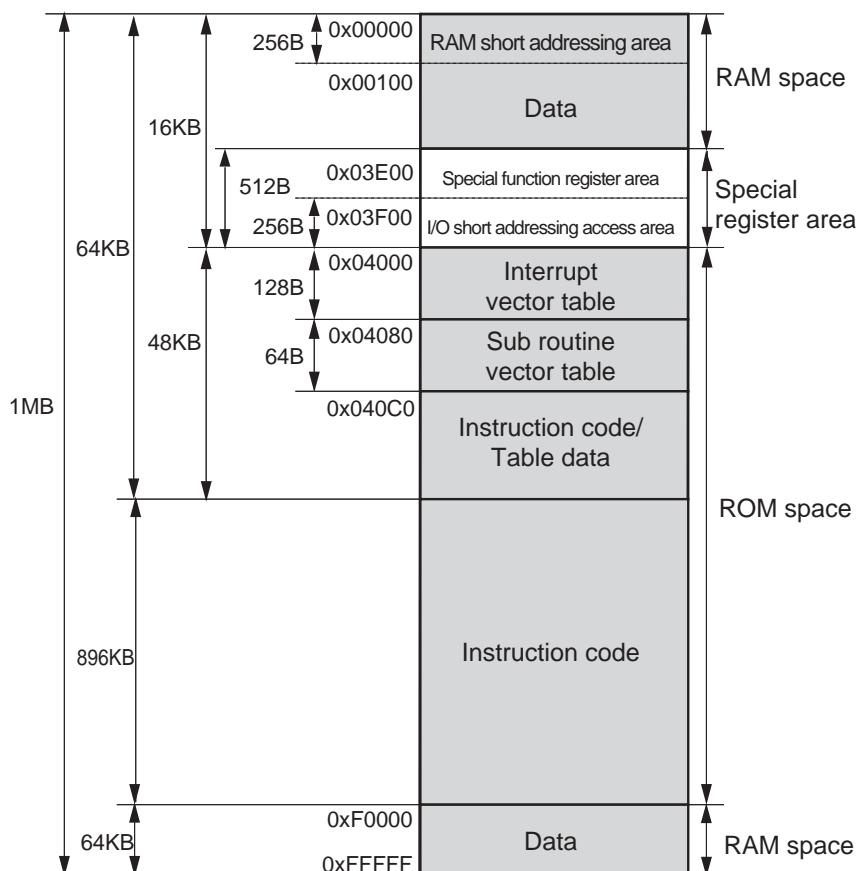


Figure:2.1.7 Address Space

2.1.9 Addressing Modes

This LSI supports the nine addressing modes.

Each instruction uses a combination of the following addressing

1. Register direct
2. Immediate
3. Register indirect
4. Register relative indirect
5. Stack relative indirect
6. Absolute
7. RAM short
8. I/O short
9. Handy

These addressing modes are well-suited for C language compilers. All of the addressing modes can be used for data transfer instructions. In modes that allow half-byte addressing, the relative value can be specified in half-byte (4-bit) increments, so that instruction length can be shorter. Handy addressing reuses the last memory address accessed. There are three instructions that can use this mode : MOV Dn, (HA) / MOVW DWn , (HA) / MOVW An , (HA). Combining handy addresssing with absolute addressing reduces code size. For transfer data between memory, 8 addressing modes ; register indirect, register relative indirect, stack relative indirect, absolute, RAM short, I/O short, handy can be used. For operation instruction, register direct and immediate can be used. Refer to instruction's manual for the MN101E series.



This LSI is designed for 8-bit data access. When 16-bit data access is carried out, 8-bit data access is performed twice from the lower address. It is possible to tranfer data in 16-bit increments with odd or all even addresses.

Table:2.1.5 Address Space

Addressing mode		Effective address	Explanation
Register direct	Dn/DWn An/SP PSW	—	Directly specifies the register. Only internal registers can be specified.
Immediate	imm4/imm8 imm16	—	Directly specifies the operand or mask value appended to the instruction code.
Register indirect	(An)	15 An 0	Specifies the address using an address register.
Register relative indirect	(d8,An)	15 An+d8 0	Specifies the address using an address register with 8-bit displacement.
	(d16,An)	15 An+d16 0	Specifies the address using an address register with 16-bit displacement.
	(d4,PC) (branch instructions only)	17 0 H PC+d4	*1 Specifies the address using the program counter with 4-bit displacement and H bit.
	(d7,PC) (branch instructions only)	17 0 H PC+d7	*1 Specifies the address using the program counter with 7-bit displacement and H bit.
	(d11,PC) (branch instructions only)	17 0 H PC+d11	*1 Specifies the address using the program counter with 11-bit displacement and H bit.
	(d12,PC) (branch instructions only)	17 0 H PC+d12	*1 Specifies the address using the program counter with 12-bit displacement and H bit.
	(d16,PC) (branch instructions only)	17 0 H PC+d16	*1 Specifies the address using the program counter with 16-bit displacement and H bit.
Stack relative indirect	(d4,SP)	15 SP+d4 0	Specifies the address using the stack pointer with 4-bit displacement.
	(d8,SP)	15 SP+d8 0	Specifies the address using the stack pointer with 8-bit displacement.
	(d16,SP)	15 SP+d16 0	Specifies the address using the stack pointer with 16-bit displacement.
Absolute	(abs8)	7 abs8 0	Specifies the address using the operand value appended to the instruction code. Optimum operand length can be used to specify the address.
	(abs12)	11 abs12 0	
	(abs16)	15 abs16 0	
	(abs18) (branch instructions only)	17 0 H abs18	*1
	(abs20) (branch instructions only)	19 0 H abs20	*1
RAM short	(abs8)	7 abs8 0	Specifies an 8-bit offset from the address 'x'00000'.
I/O short	(io8)	15 IOTOP+io8 0	Specifies an 8-bit offset from the top address ('x'03F00') of the special function register area.
Handy	(HA)	—	Reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combined use with absolute addressing reduces code size.

*1 H: half-byte bit

2.1.10 Machine Clock

Machine clock is generated based on the system clock (fs) dividing the source oscillation frequency. The machine clock is the base timing for control of CPU.

- Internal Memory Access (no wait cycle)

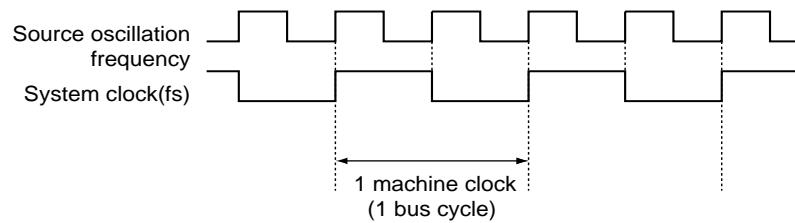


Figure:2.1.8 Machine Clock (no wait cycle)

- External Memory Access (0, 1, 2, 3 wait cycle)

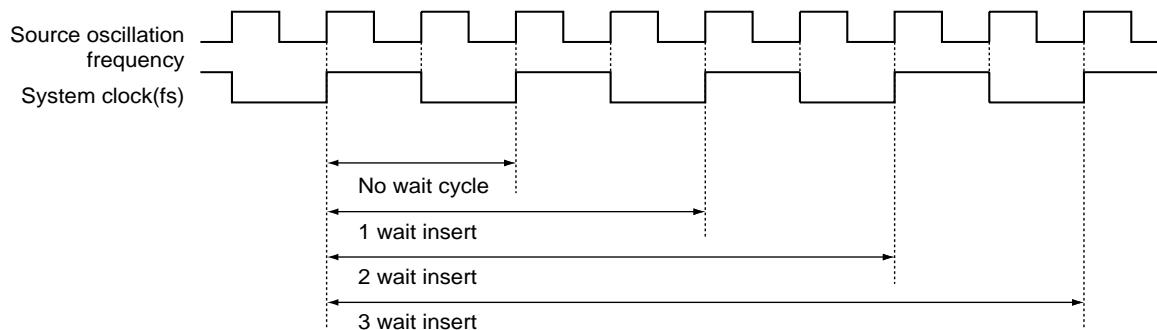


Figure:2.1.9 Machine Clock (memory wait cycle)



Wait cycle is set to fixed three wait cycle mode at reset start.



Division ratio of system clock (fs) differs depending on the CPUM register settings.
[Chapter 2. 2.6 Clock Switching]

2.2 Memory Space

2.2.1 Memory Mode

ROM is the read only area and RAM is the memory area which is readable/writable of data. In addition to these, peripheral resources such as memory-mapped special registers are allocated. The MN101E series supports two memory modes (single chip mode, memory expansion mode) in its memory model.

In single chip mode, the system consists of only internal memory. In memory expansion mode, ROM, RAM and external device for operation can be connected. This LSI supports single chip mode and memory expansion mode.

Table:2.2.1 Memory Mode Setup

Memory mode	MMOD pin	EXMEM flag (MEMCTR register)	EXADV3 to 1 flags (EXADV register)
Single chip mode	L	0	-
Memory expansion mode	L	1	1



Fix the MMOD pin always to "L" level. Do not change the settings of this pin also after reset release.

2.2.2 RAM Space

■ RAM Space

MN101E series has maximum 64 KB of RAM space.

RAM space is devided to be allocated to the address space. Mirror RAM space is provided for effective utilization of the devided RAM spaces.

RAM space: 0x00000 to 0x03DFF (15.5 KB) + 0xF3E00 to 0xFFFFF (48.5 KB) (maximum 64KB)

Mirror RAM space: 0xF0000 to 0xF3DFF = 0x00000 to 0x03DFF (Mapped to same RAM space)

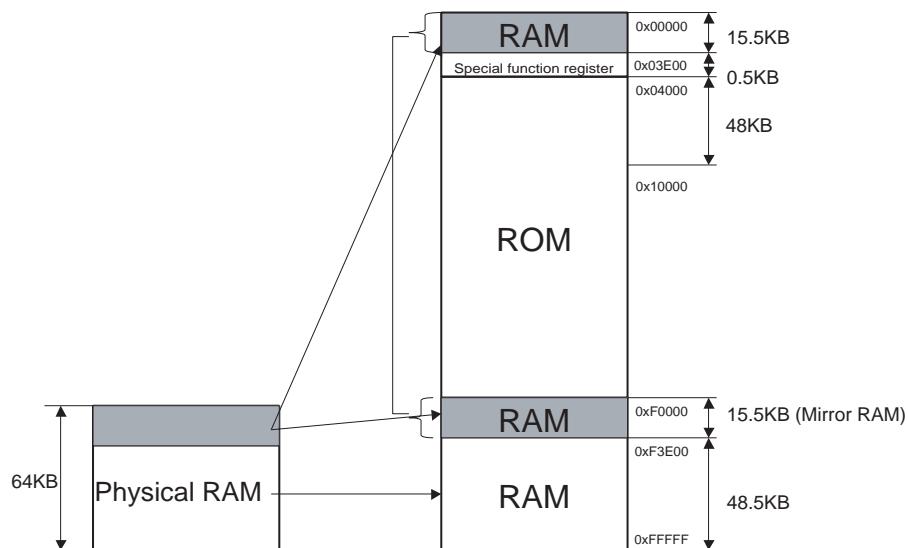


Figure:2.2.1 RAM Space

■ How to use mirror RAM Space

Sub routine A

Address bank 15

```
mov x'0F', (SBNKR) : Source side
mov x'0F', (DBNKR) : Destination side
Transfer data 15 between memories (1)
mov (x'XYZZ'), dn
mov dn, (x'ABCD') : x'XYZZ' → x'ABCD'
(x'ABCD', x'XYZZ' are address of abs16.)
```

Sub routine B (Address bank 0)

```
mov (x'ABCD'), d1 : Use mirror function (2)
```

Execute the same access ignoring the upper 4 bits.

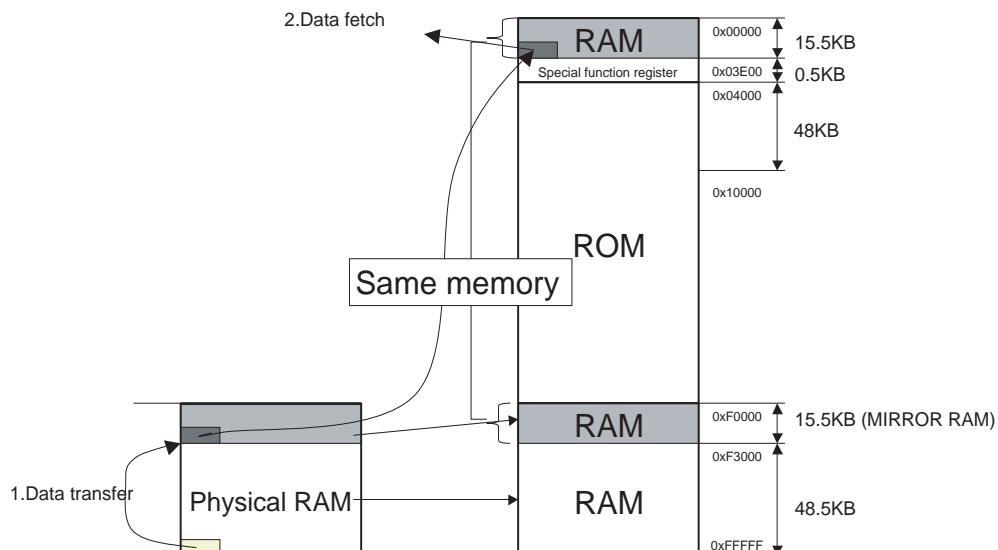


Figure:2.2.2 How to use mirror RAM Space

2.2.3 Single-chip Mode

In single-chip mode, the system consists of only internal memory. This is the optimized memory mode and allows construction of systems with the highest performance. The single-chip mode uses only internal ROM and internal RAM. The MN101E series devices offer up to 64 KB of RAM and up to 944 KB of ROM. The MN101E29G/F29G offers 6 KB of RAM and 128 KB of ROM.

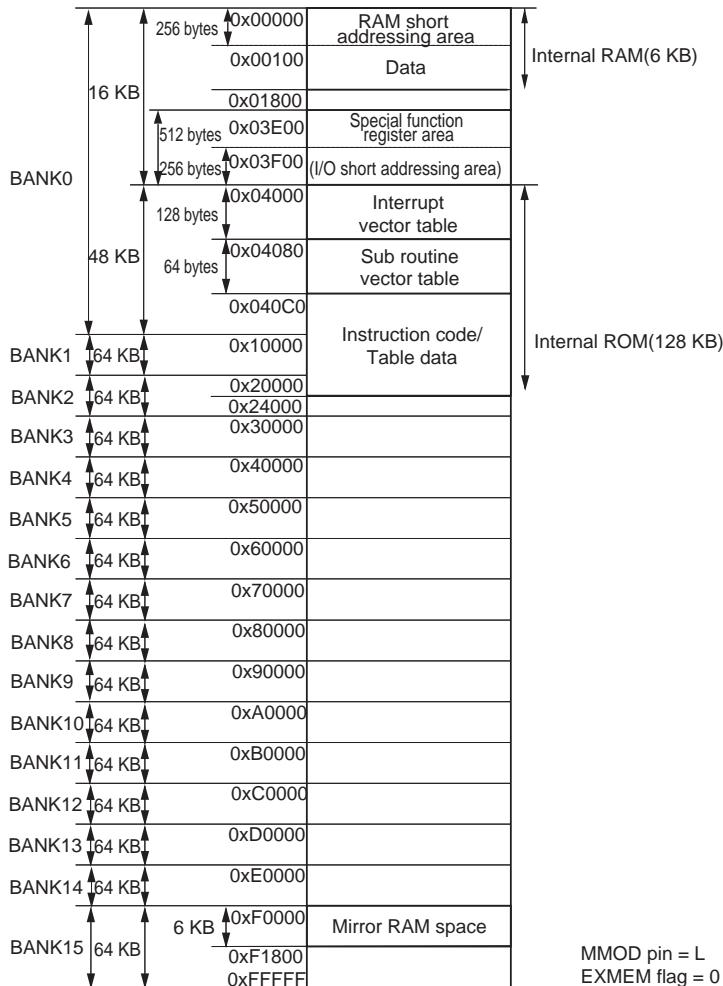


Figure:2.2.3 Single-chip Mode



The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before using.



It is not guaranteed to ensure proper operation in accessing to unimplemented spaces, such as internal ROM/RAM spaces without memory (ROM/RAM) and special register spaces without special register.

2.2.4 Memory Expansion Mode

The MN101E series can connect external ROM, RAM and external devices for operation in memory expansion mode. This is the mode to expand to external memory while using internal ROM and RAM.

Memory areas can be externally expanded as follows.

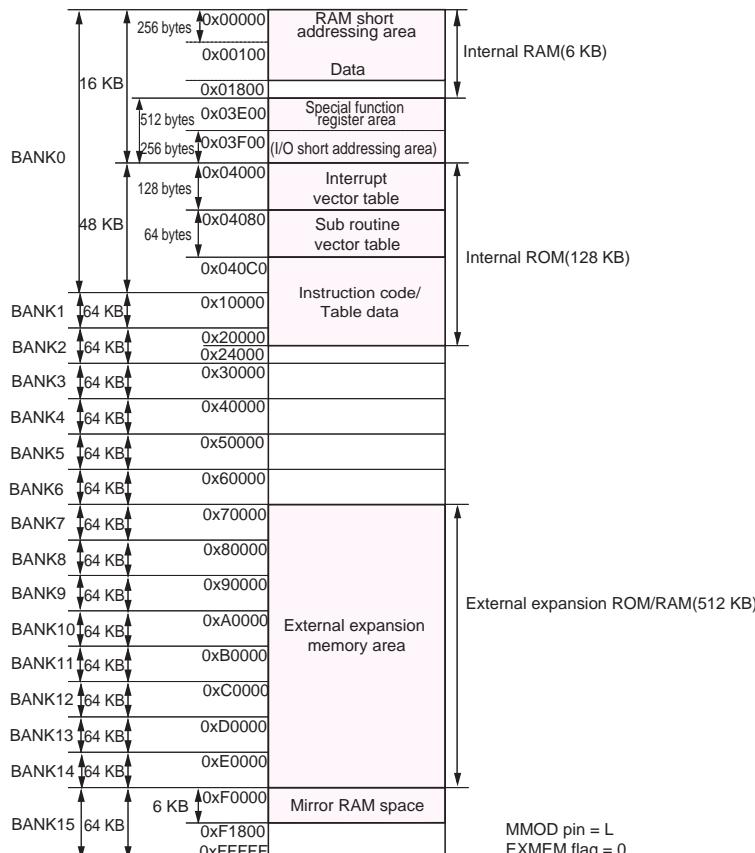


Figure:2.2.4 Memory Expansion Mode



The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before using.



If accessing the external memory area, execute with 100 ns or more of access time .



It is not guaranteed to ensure proper operation in accessing to unimplemented spaces, such as internal ROM/RAM spaces without memory (ROM/RAM) and special register spaces without special register.

2.2.5 Bank Function

CPU of MN101E series has basically 64 KB data area. On this LSI, data area can be expanded up to 16 banks (1 MB) based on units of 64KB with bank function.

Bank function can be used by setting the proper bank area to the bank register for source address (SBNKR) or the bank register for destination address (DBNKR). At reset, both of the SBNKR register and the DBNKR register indicate bank 0. Bank function is valid after setting bank disable flag (BKD), which is on the seventh bit of the processor status word (PSW), to 0.

Table:2.2.2 Address Range

SBA3 (DBA3)	SBA2 (DBA2)	SBA1 (DBA1)	SBA0 (DBA0)	Bank area	Address range
0	0	0	0	bank 0	0x00000 to 0x0FFFF
0	0	0	1	bank 1	0x10000 to 0x1FFFF
0	0	1	0	bank 2	0x20000 to 0x2FFFF
0	0	1	1	bank 3	0x30000 to 0x3FFFF
0	1	0	0	bank 4	0x40000 to 0x4FFFF
0	1	0	1	bank 5	0x50000 to 0x5FFFF
0	1	1	0	bank 6	0x60000 to 0x6FFFF
0	1	1	1	bank 7	0x70000 to 0x7FFFF
1	0	0	0	bank 8	0x80000 to 0x8FFFF
1	0	0	1	bank 9	0x90000 to 0x9FFFF
1	0	1	0	bank 10	0xA0000 to 0xAFFFF
1	0	1	1	bank 11	0xB0000 to 0xBFFFF
1	1	0	0	bank 12	0xC0000 to 0xCFFFF
1	1	0	1	bank 13	0xD0000 to 0xDFFFF
1	1	1	0	bank 14	0xE0000 to 0xEFFFF
1	1	1	1	bank 15	0xF0000 to 0xFFFFF



When bank area is changed at interrupt processing, pushing onto the stack or popping must be done by program, if it necessary.



While bank function is valid, I/O short instruction should be used for access to 0x03F00 to 0X03FFF in the special function register area (0x03E00 to 0x03FFF). For access to the memory space 0x13F00 to 0x13FFF, 0x23F00 to 0x23FFF, 0x33F00 to 0x33FFF, 0x43F00 to 0x43FFF, 0x53F00 to 0x53FFF, 0x63F00 to 0x63FFF, 0x73F00 to 0x73FFF, 0x83F00 to 0x83FFF, 0x93F00 to 0x93FFF, 0xA3F00 to 0xA3FFF, 0xB3F00 to 0xB3FFF, 0xC3F00 to 0xC3FFF, 0xD3F00 to 0xD3FFF, 0xE3F00 to 0xE3FFF, 0xF3F00 to 0xF3FFF, both instructions of register indirect and register relative indirect should be used.

[Chapter 2. 2.1.9. Addressing Modes]



Set the stack area to bank 0. The provided C-compiler for this series does not support the bank function.



Our linker supports the function that prevents data from straddling over bank boundaries. See "MN101E Series Cross-assembler User's Manual" for details.

■ Bank Register for Source Address (SBNKR:0x03F0A)

The SBNKR register is used to specify bank area for loading instruction from memory to register. Once this register is specified, bank control is valid for all addressing modes except I/O short instruction and stack relative indirect instruction.

[Chapter 2. 2.1.9. Addressing modes]

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SBA3	SBA2	SBA1	SBA0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3-0	SBA3-0	Bank for source address selection 0000: bank 0 0001: bank 1 0010: bank 2 0011: bank 3 0100: bank 4 0101: bank 5 0110: bank 6 0111: bank 7 1000: bank 8 1001: bank 9 1010: bank 10 1011: bank 11 1100: bank 12 1101: bank 13 1110: bank 14 1111: bank 15

■ Bank Register for Destination Address (DBNKR:0x03F0B)

The DBNKR register is used to specify bank area for storing instruction from register to memory. Once this register is specified, bank control is valid for all addressing modes except I/O short instruction, stack relative indirect instruction and bit manipulation instruction.

[Chapter 2. 2.1.9. Addressing modes]

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	DBA3	DBA2	DBA1	DBA0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3-0	DBA3-0	Bank for source address selection 0000:bank 0 0001:bank 1 0010:bank 2 0011:bank 3 0100:bank 4 0101:bank 5 0110:bank 6 0111:bank 7 1000:bank 8 1001:bank 9 1010:bank A 1011:bank B 1100:bank C 1101:bank D 1110:bank E 1111:bank F



Read, modify, write instruction such as bit manipulation (BSET, BCLR, BTST) depends on the value of the SBNKR register, both of for reading and writing.

2.2.6 Special Function Registers

This LSI locates the special function registers (I/O spaces) at the addresses 0x03E00 to 0x03FFF in memory space. The special function registers of this LSI are located as shown below.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
03E0X																
03E1X																
03E2X	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
03E3X	TM9BCL	TM9OC1L	TM9OCH	TM9PRIL	TM9PRIH	TM9ICL	TM9SEL1	TM9SEL2	TM9OC2L	TM9OC2H	TM9MD1	TM9MD2	TM9PR2L	TM9PR2H	TM9MD3	
03E4X																
03E5X	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
03E6X	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
03E7X	L00BUF	L00BUF	L00BUF	L04BUF	L04BUF	L06BUF	L07BUF	L08BUF	L09BUF	L09BUF	L0ABUF	L0CBUF	L0CBUF	L0EBUF	L0EBUF	L0FBUF
03E8X	LC10BUF	LC11BUF	LC12BUF	LC14BUF	LC15BUF	LC16BUF	LC17BUF	LC18BUF	LC19BUF	LC1ABUF	LC1BBUF					
03E9X	LCDMD1	LCDMD2	LCDMD3	LCCTR0	LCCTR1	LCCTR2	LCCTR3	LCCTR4	LCCTR5	LCCTR6	LCCTR7					
03EAx																
03EBX																
03ECX	AT00CNT0	AT00CNT1	AT00TRC	AT0MAP0L	AT0MAP0M	AT0MAP0H	AT0MAP1L	AT0MAP1M	AT0MAP1H							
03EDX	AT11CNT0	AT11CNT1	AT11TRC	AT1MAP0L	AT1MAP0M	AT1MAP0H	AT1MAP1L	AT1MAP1M	AT1MAP1H							
03EEX	P10MD	P10ND	P10SD	P10UD	P10MD	P10ND	P10MD	P10ND	P10MD							
03EFX	P00DC	P30DC	P40DC	P50DC	P60DC	P70DC	P80EV	P8SEV	P8SEV	Reserved	SCHMT1	SCHMT2	P8CNT1	P8CNT2	NF3CTR	NF4CTR
03F0X	CPUM	MENICTR	WDYCTR	DLYCTR	Reserved	ACTMD	AUCTR	SBMKR	DBMKR	Reserved	Reserved	Reserved	EXADV	EDGDT	LVLM	
03F1X	P00UT	P10UT	P20UT	P30UT	P40UT	P50UT	P60UT	P70UT	P80UT	P90UT	P90UT	P90UT	P90UT	P90UT	ACZCTR	XSEL
03F2X	P1IN	P2IN	P3IN	P4IN	P5IN	P6IN	P7IN	P8IN	P9IN	P9IN	P9IN	P9IN	P9IN	P9IN	IRQCNT	KEYT3_1MD KEYT3_2MD
03F3X	P0DIR	P1DIR	P2DIR	P3DIR	P4DIR	P5DIR	P6DIR	P7DIR	P8DIR	P9DIR	P9DIR	P9DIR	P9DIR	P9DIR	SELUD	IRQEXPEN
03F4X	P0PLUD	P1PLUD	P2PLUD	P3PLUD	P4PLUD	P5PLUD	P6PLUD	P7PLUD	P8PLUD	P9PLU	P9PLU	P9PLU	P9PLU	P9PLU	TM2MD	CK2MD
03F5X	TM0BC	TM1BC	TM0OC	TM1OC	TM0MD	TM1MD	CK0MD	CK1MD	TM2BC	TM3BC	TM3OC	TM3OC	TM3OC	TM3OC	TM3MD	CK3MD
03F6X	TM4BC	TM4OC	TM4AO	TM4MD	TM4MD	TM4MD	CK4MD	CK4MD	TM6BC	TM6MD						
03F7X	TM7BCL	TM7OC1L	TM7OCH	TM7PRIL	TM7PRIH	TM7ICL	TM7SEL1	TM7SEL2	TM7OC2L	TM7OC2H	TM7MD1	TM7MD2	TM7PR2L	TM7PR2H	TM7MD3	
03F8X	TM8BCL	TM8OC1L	TM8OCH	TM8PRIL	TM8PRIH	TM8ICL	TM8SEL1	TM8SEL2	TM8OC2L	TM8OC2H	TM8MD1	TM8MD2	TM8PR2L	TM8PR2H	TM8MD3	
03F9X	SC0SEL	SC0MD0	SC0MD1	SC0MD2	SC0MD3	SC0MD3	SC0MD3	SC0MD3	SC0SEL	SC1MD1	SC1MD2	SC1MD2	SC1MD2	SC1MD2	SC1MD2	SC1MD2
03FAx	SC2SEL	SC2MD0	SC2MD1	SC2MD2	SC2MD3	SC2MD3	SC2MD3	SC2MD3	SCASEL	SC3MD0	SC3MD1	SC3MD2	SC3MD2	SC3MD2	SC3MD2	SC3MD2
03FBX	SC4MD0	SC4MD1	SC4MD2	SC4MD3	SC4AD0	Reserved	SC4ASTRO	SC4ASTR1	RXBUFF4	TXBUFF4	SC5AD1	SC5AD0	SC5AD0	SC5AD0	SC5AD0	RXBUFF3
03FCX	RCAPL	RCAPM	RCAPH	RCPSR	RCCTR0	RCCTR0	RCCTR0	RCCTR0	SC5SEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SC5SEL
03FDX	ANCTR0	ANCTR1	ANCTR2	ANBUF0	ANBUF1	DACTR	DAD0	DAD0	DADR1	DADR2	DADR3	DADR3	DADR3	DADR3	DADR3	PLLONT
03FEY	NMICR	IRQ0ICR	IRQ1ICR	IRQ2ICR	IRQ3ICR	IRQ4ICR	IRQ5ICR	IRQ6ICR	TM1ICR	TM2ICR	TM3ICR	TM4ICR	TM5ICR	TM6ICR	TBICR	
03FFX	TM7OC2ICR	TM8OC2ICR	TM9OC2ICR	TM9ICR	TM9OC2ICR	TM9OC2ICR	TM9OC2ICR	TM9OC2ICR	SC2TICR	PERICR						

Figure:2.2.5 Register Map



Do not access registers described as “Reserved”. Otherwise, normal operation is not guaranteed.



Setup is different from each other according to the bp of each register. Follow the instructions described in “description” of each register

2.3 ROM Correction

2.3.1 Overview

This LSI can correct and change max 7 parts in a program on ROM both internal and external with ROM correction function. The correct program is read from the external to the internal RAM space by using the external EEPROM or by using the serial transmission. This function is valid to the system with the external EEPROM.

2.3.2 Correction Sequence

Program is corrected as following steps.

1. The instruction execution address is compared to the correction address.
2. Program counter is branched indirectly to the internal RAM address (the head address of the correct program) stored to the RC vector table (RCnV(L), RCnV(H)), after matching the above address. It is necessary to set the head address of the correct program as the address by a byte. This instruction needs 6 cycle.
3. The corrected program at the RAM area is executed.
4. Program counter is branched back to the program at ROM area.

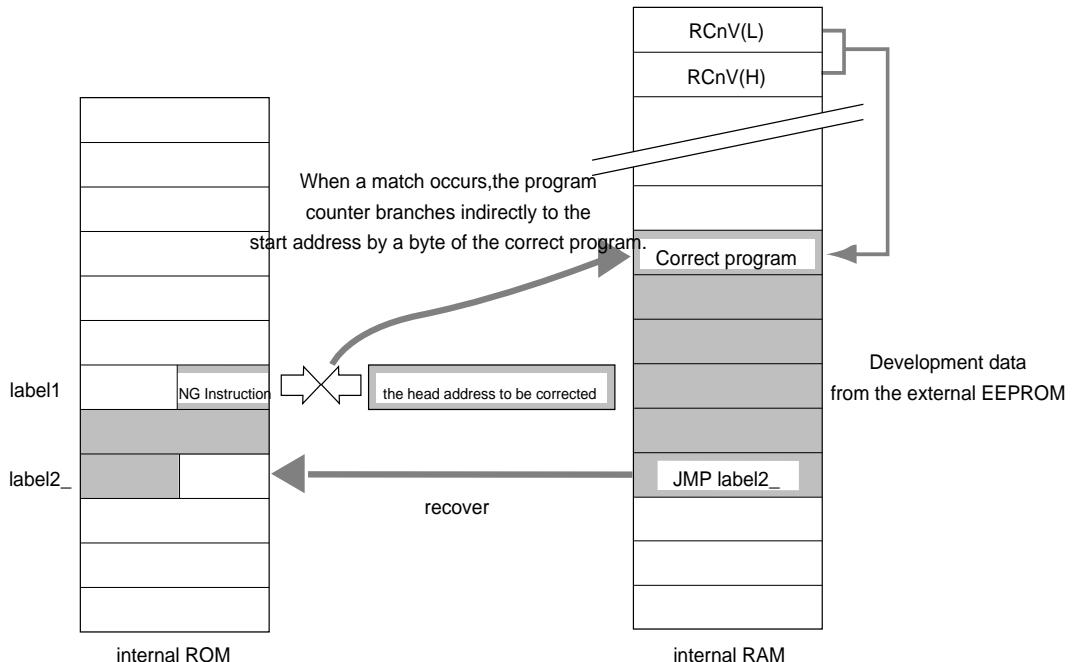


Figure:2.3.1 ROM Correction

The ROM correction setup procedure is as follows.

1. Specify the ROM correction pointer specification register (RCPSR).
2. Set the head address of the program to be corrected to the ROM correction address setting register (RCAP(H/M/L)).
3. Set the correct program at RAM area.
4. Set the head address of the correct program to RC vector table (RCnV(L), RCnV(H)).
5. Set the RCnEN flag of ROM correction control register (RCCTR0) to enable the ROM correction.



When the head address of the program to be corrected is the half-byte instruction, the ROM correction checks the execution instruction of the half-byte. Therefore, set the address by a byte to the ROM correction address setting register.



When the next instruction of the program to be corrected program last address is the instruction placed in half-byte address , the recover address should be set by half byte.

2.3.3 ROM Correction Control Register

ROM correction is controlled by ROM correction pointer specification register (RCPSR) , ROM correction control register (RCCTR0) and ROM correction address setting register (RCnAPL, RCnAPM, RCnAPH).

ROM correction pointer specification register (RCPSR) is the register which specifies the pointer of the ROM correction address register (RCAP (L/M/H)).ROM correction address setting register becomes effective by setting the value of the pointer n (RCnAP(L/M/H)) which is specified by RCPSR.

When setting a ROM correction address setting register, set up the ROM correction pointer specification register (RCPSR) first.

■ ROM correction pointer specification register (RCPSR:0x03FC3)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	Reserved	RCPSR2	RCPSR1	RCPSR0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3	Reserved	Always set to "0". *
2-0	RCPSR2 RCPSR1 RCPSR0	Specification of the ROM correction pointer 000:Address pointer 0 (RC0AP (L/M/H)) 001:Address pointer 1 (RC1AP (L/M/H)) 010:Address pointer 2 (RC2AP (L/M/H)) 011:Address pointer 3 (RC3AP (L/M/H)) 100:Address pointer 4 (RC4AP (L/M/H)) 101:Address pointer 5 (RC5AP (L/M/H)) 110:Address pointer 6 (RC6AP (L/M/H)) 111:Setting Prohibited



Always set "0" to the bp denoted by asterisk.

ROM correction control register (RCCTR0) enables/disables the ROM correction function to max 7 parts of the program to be corrected. When the RCnEN flag is set, the ROM correction is activated. And when the ROM address (the instruction execution address) reaches the set address to the ROM correction address setting register, it branches indirectly to the RAM address set on the RC vector table (RCnV(L), RCnV(H)). Set the RCnEN flag after setting the ROM correction address setting register.

■ ROM Correction Control Register0 (RCCTR0:0x03FC4)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	RC6EN	RC5EN	RC4EN	RC3EN	RC2EN	RC1EN	RC0EN
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0". *
6	RC6EN	Control of the ROM correction of the 6th address (RC6AP (L/M/H)) 0:Disable 1:Enable
5	RC5EN	Control of the ROM correction of the 5th address (RC5AP (L/M/H)) 0:Disable 1:Enable
4	RC4EN	Control of the ROM correction of the 4th address (RC4AP (L/M/H)) 0:Disable 1:Enable
3	RC3EN	Control of the ROM correction of the 3rd address (RC3AP (L/M/H)) 0:Disable 1:Enable
2	RC2EN	Control of the ROM correction of the 2nd address (RC2AP (L/M/H)) 0:Disable 1:Enable
1	RC1EN	Control of the ROM correction of the 1st address (RC1AP (L/M/H)) 0:Disable 1:Enable
0	RC0EN	Control of the ROM correction of the 0th address (RC0AP (L/M/H)) 0: Disable 1: Enable



ROM correction address is set for 4th or later command from command that enable the ROM correction control.



Always set "0" to the bp denoted by asterisk.

■ ROM correction address setting register(RCAPL,RCAPM,RCAPH)

The address in which the command to be corrected is stored is set up. The value to set up is written in the register specified by the ROM correction pointer specification register (RCPSR). Register of the pointer specified by RCPSR if the execution address of the set-up value and a command is in agreement, indirect branch will be carried out at the address set as RC vector table (RCnV (L), RCnV (H)). In enabling a ROM correction function, please set the RCnEN flag of RCCTR0 register as this register after setting up a desired address.

■ ROM correction address setting register for lower 8bits(RCAPL:0x03FC0)

bp	7	6	5	4	3	2	1	0
Flag	RCAPL7	RCAPL6	RCAPL5	RCAPL4	RCAPL3	RCAPL2	RCAPL1	RCAPL0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

■ ROM correction address setting register for middle 8 bits(RCAPM:0x03FC1)

bp	7	6	5	4	3	2	1	0
Flag	RCAPM7	RCAPM6	RCAPM5	RCAPM4	RCAPM3	RCAPM2	RCAPM1	RCAPM0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

■ ROM correction address setting register upper 4 bits(RCAPH:0x03FC2)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	RCAPH3	RCAPH2	RCAPH1	RCAPH0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W



Please do not perform the same address setup to two or more RCnAP (H/M/L) registers. When the same address is set up, the priority shown below is followed.
RC0AP>RC1AP>RC2AP>.....>RC6AP



ROM correction address is set for 4th or later command from command that enable the ROM correction control.

Here is the correspondence of ROM correction pointer specification register , the ROM correction address setting register, the ROM correction control register of ROM correction control flag and RC-vector table

	ROM correction pointer specification register	ROM correction address			ROM correction control flag	RC-vector table	
	RCPSR	RCAPL	RCAPM	RCAPH	RCCTR0	RCnV(L)	RCnV(H)
0th correction address	0000	RC0APL	RC0APM	RC0APH	RC0EN	0x0010	0x0011
1st correction address	0001	RC1APL	RC1APM	RC1APH	RC1EN	0x0012	0x0013
2nd correction address	0010	RC2APL	RC2APM	RC2APH	RC2EN	0x0014	0x0015
3rd correction address	0011	RC3APL	RC3APM	RC3APH	RC3EN	0x0016	0x0017
4th correction address	0100	RC4APL	RC4APM	RC4APH	RC4EN	0x0018	0x0019
5th correction address	0101	RC5APL	RC5APM	RC5APH	RC5EN	0x001A	0x001B
6th correction address	0110	RC6APL	RC6APM	RC6APH	RC6EN	0x001C	0x001D

2.3.4 ROM Correction Setup Example

■ Initial Routine with ROM Correction

The following routine should be set to correct the program. Also store the ROM correction setup and correct program to the external EEPROM, in advance.

Here is the steps for ROM correction execution.

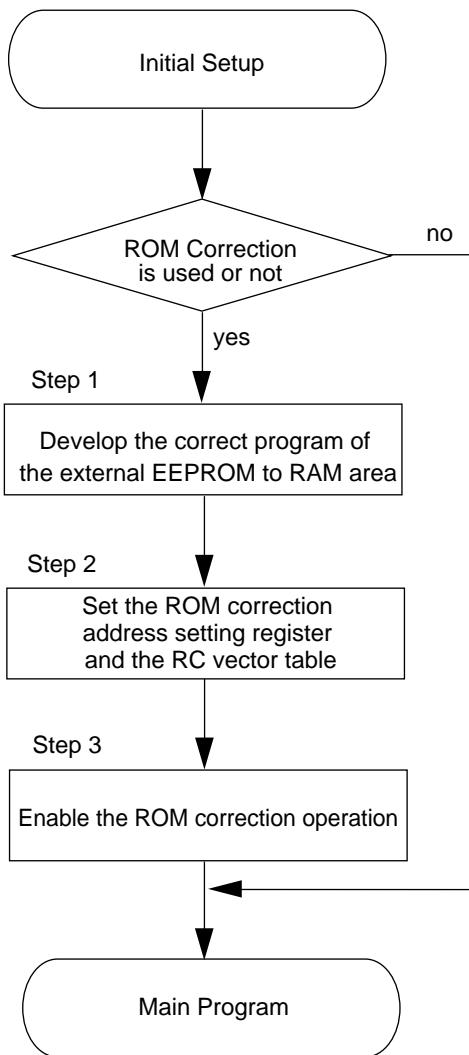


Figure:2.3.2 Initial Routine for ROM Correction

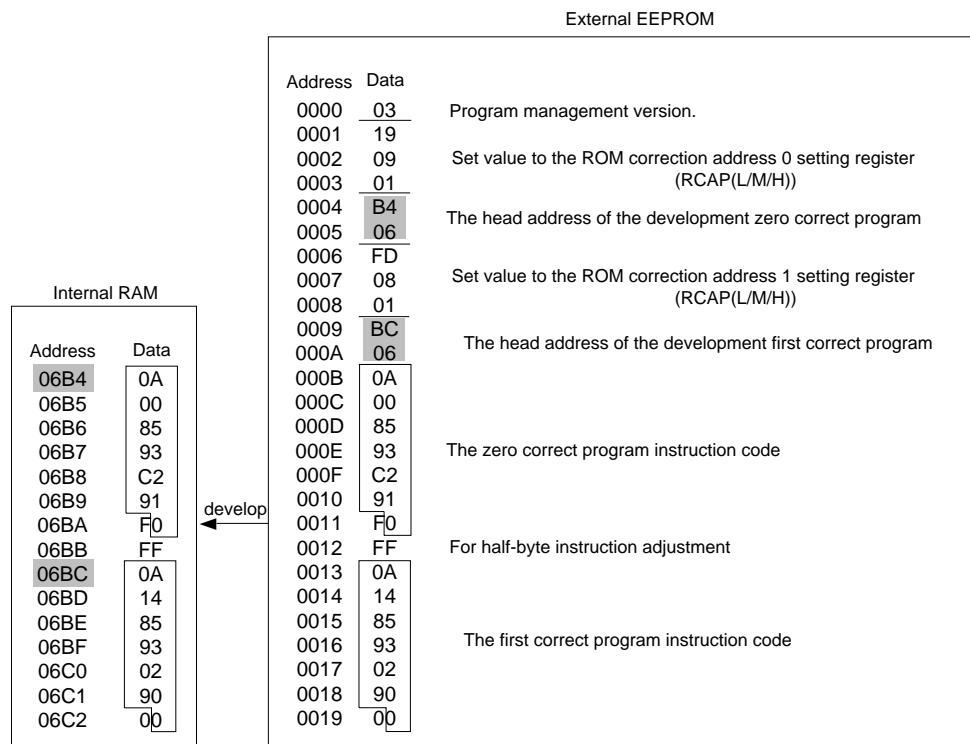
■ ROM Correction Setup Example

The setup procedure with ROM correction to correct 2 parts of program is shown below. For the step to execute the ROM correction, refer 2.3.2. Initial Routine for ROM correction on the previous page.

(STEP 1)

Develop the correct program of the external EEPROM to internal RAM area.

It is necessary to set the head address of the correct program as the address by a byte.



(STEP 2)

Set the ROM correction address setting register and the RC-vector table.

[Setup for the zeroth correction]

Specify the ROM correction pointer specification register (RCPSR).

RCPSR=0x00

Set the head address of the program to be corrected to the ROM correction address setting register (RC0AP)

RCAPL=0x19

RCAPM=0x09

RCAPH=0x01

(When the address is RCPSR=0x00, the value is set as the ROM correction address pointer 0 (RC0AP (L/M/H)).)

Set the internal RAM address 0x06B4 that stored zeroth correct program to the RC-vector table address (RC0V(L),RC0V(H)).

RC0V(L)=0xB4

RC0V(H)=0x06

The zero program to be corrected (internal ROM)

Address	The head address of the correction (the set value of RC0AP)		
	Data		
10916	D900A0	cbne	0, d1, 1091E
10919	A005	mov	50, d0
1091B	58	mov	d0, (a0)
1091C	8940	bra	10920
1091E	B4	sub	d0, d0

The address for recover

The zero correct program (internal RAM)

Address	The head address of the correction program (the set value of RC0V)		
	Data		
006B4	A000	mov	0, d0
006B6	58	mov	d0, (a0)
006B7	392C190	bra	1091C

The address for recover

[Setup for the first correction]

Specify the ROM correction pointer specification register (RCPSR).

RCPSR=0x01

Set the head address of the program to be corrected to the ROM correction address setting register (RC0AP)

RC1APL=0xFD

RC1APM=0x08

RC1APH=0x01

Set the internal RAM address 0x06BC that stored first correct program to the RC-vector table address (RC1V(L),RC1V(H)).

RC1V(L)=0xBC

RC1V(H)=0x06

The first program to be corrected (internal ROM)

Address	Data	The head address of the correction (the set value of RC1AP)	
108FC	85	sub	d1, d1
<u>108FD</u>	A011	mov	11, d0
108FF	58	mov	d0, (a0)
<u>10900</u>	EC1	addw	1, a0
<u>10901</u>	A081	mov	_Msyscom_edge, 0

The address for recover

The first correct program (internal RAM)

Address	Data	The head address of the correction program (the set value of RC1V)	
<u>006BC</u>	A041	mov	14, d0
006BE	58	mov	d0, (a0)
006BF	3920090	jmp	<u>10900</u>

The address for recover

(STEP 3)

Please set bit 0(RC0EN) , bit 1 (RC1EN) of ROM correction control register (RCCTR0) to "1."

After 4th or later command from command that enable the ROM correction control, the main program is started, the instruction fetched address and the set address to ROM correction address setting register (RCnAP) are always compared, then once they are matched program counter indirectly branches to the address in RAM area, that are stored to the RC vector table (RCnV).

the correction program in RAM area is executed.

Program counter recovers to the program in ROM area.

2.4 Bus Interface

2.4.1 Bus Controller

The MN101E series provides separate buses to the internal memory and internal peripheral circuits to reduce bus line loads and thus realize faster operation.

There are four such buses: ROM bus, RAM bus, peripheral expansion bus, and external expansion bus. They connect to the internal ROM, internal RAM, internal peripheral circuits, and external interfaces respectively. The bus control block controls the parallel operation of instruction read and data access, the access speed adjustment for low-speed external devices, and arbitration of bus access when using master devices on the external bus lines. A functional block diagram of the bus controller is given below.

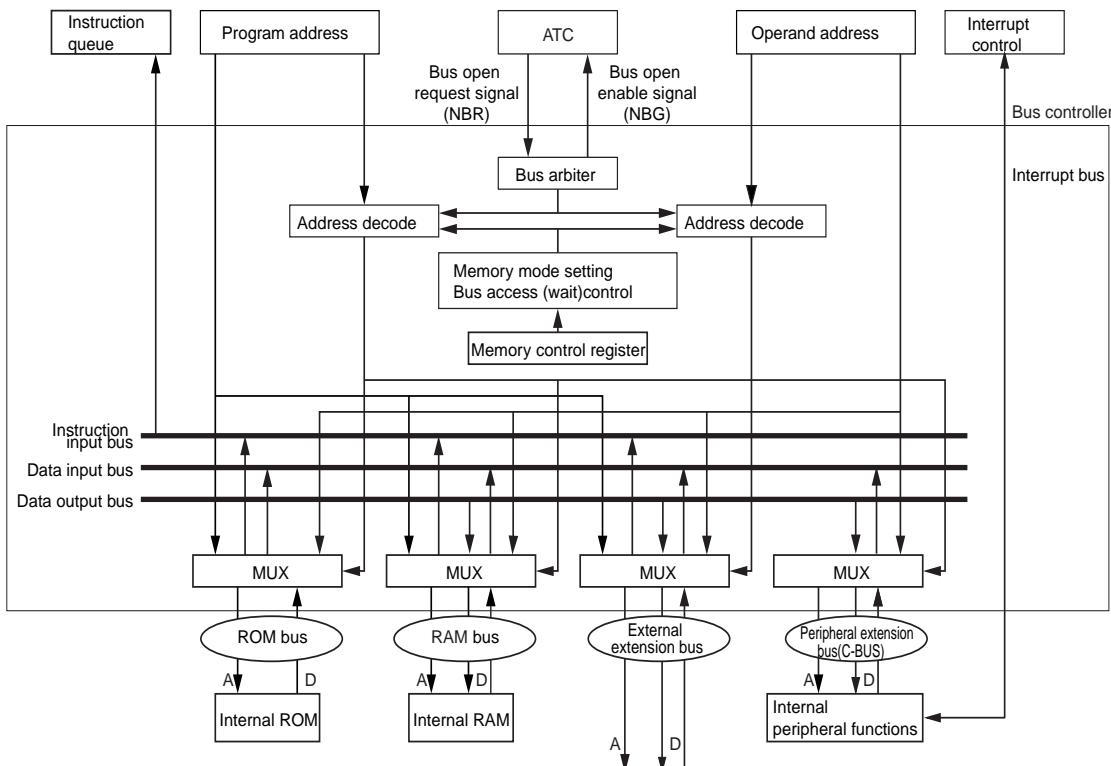


Figure:2.4.1 Functional Block Diagram of the Bus Controller

In memory expansion mode, the external expansion bus can access external device. Memory control register (MEMCTR) can be used to select the access mode, fixed wait cycle mode or handshake mode. Wait cycle setting to peripheral expansion bus, connected to internal peripheral circuits is available.

2.4.2 Control Registers

Bus interface is controlled by 2 registers : the memory control register (MEMCTR) and the expansion address control register (EXADV).

■ Memory Control Register (MEMCTR: 0x03F01)

bp	7	6	5	4	3	2	1	0
Flag	IOW1	IOW0	IVBM	EXMEM	EXWH	IRWE	EXW1	EXW0
At reset	1	1	0	0	1	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	IOW1 IOW0	Wait cycles when accessing special register area 00: No wait cycles 01: 1 wait cycle 10: 2 wait cycles 11: 3 wait cycles
5	IVBM	Base address specification for interrupt vector table 0:Interrupt vector base = 0x04000 1:Interrupt vector base = 0x00100
4	EXMEM	External memory expansion mode switching 0:Do not expand external memory 1:Expand external memory
3	EXWH	External memory fixed wait cycle mode or handshake mode switching 0:Handshake mode 1:Fixed wait cycle mode
2	IRWE	Software write set up for interrupt request flag 0:Even if data is written to each interrupt control (register (xxxICR), the state of the interrupt request flag (xxxIR) will not change. 1:Software write enable
1-0	EXW1 EXW0	Fixed wait cycles set up 00: No wait cycles 01: 1 wait cycle 10: 2 wait cycles 11: 3 wait cycles



The EXW1-EXW0 wait settings affect accesses to external devices in the processor mode and memory expansion mode. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles.



When changing EXW1, EXW0, and EXWH flag, execute the program with the change instruction allocated on the internal ROM or internal RAM.



The IOW1-IOW0 wait settings affect accesses to the special registers located at the addresses 0x03E00 to 0x03FFF. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is a function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. For this LSI, wait cycle setting is not always necessary. Select "no-wait cycle" in this LSI.



Automatic data transfer function (ATC0, ATC1) that accesses an external memory cannot be used in memory expansion mode.



Always set IRWE flag of memory control register (MEMCTR) to "0" except in writing IR with software. If operating interrupt control register xxxICR with software in setting IRWE flag to "1", the interrupt request flag which is set to "1" by interrupt source may be cleared to "0". For example, if giving the bit operation order to interrupt control register xxxICR, it executes bit operation to read-out 1 byte and writes it back. When the interrupt source occurs between reading out and writing back, IR flag may be cleared to "0" by mistake and then the interrupt source is missing. If IRWE flag is set to "0", the interrupt source will not be missing.



External expansion memory function does not guarantee AC timing. When using this function, refer to [Chapter 17 AC Timing Variable] and recommend the AC timing to be filled.



If accessing the external expansion memory area, execute with 5 MHz or less of access rate.

■ Expansion Address Control Register (EXADV: 0x03F1D)

bp	7	6	5	4	3	2	1	0
Flag	EXADV3	EXADV2	EXADV1	-	-	-	-	-
At reset	0	0	0	-	-	-	-	-
Access	R/W	R/W	R/W	-	-	-	-	-

bp	Flag	Description
7	EXADV3	"A19 to 16" address output enable during memory expansion mode. 0: Address output disabled 1: Address output enabled
6	EXADV2	"A15 to 12" address output enable during memory expansion mode. 0: Address output disabled 1: Address output enabled
5	EXADV1	"A11 to 8" address output enable during memory expansion mode. 0: Address output disabled 1: Address output enabled
4-0	-	-



In the memory expansion mode, unused address pins can be used as general ports.

2.4.3 Fixed Wait Cycle Mode

This mode accesses ROM, RAM, or other low-speed devices connected to the external expansion bus by inserting the number of wait cycles specified in the external fixed wait counter (EXW1-0) field of the memory control register (MEMCTR).

Fixed wait cycle mode is used to automatically insert the number of wait cycles specified by the fixed wait counter (EXW1-0) in the MEMCTR.

After reset, MEMCTR specifies the fixed wait cycle to three wait cycles. To change to handshake mode or to use a different number, modify the appropriate bits in MEMCTR.

2.4.4 External Memory Handshake Mode

External memory handshake mode uses the interlock control method in the data transfer sequence , with a transfer enable signals (NRE, NWE) and a data acknowledge signal (NDK).

External memory handshake mode adjusts the wait cycle for each external device that has a different access speed when the NDK generation circuit is provided for each device. CPU of this LSI keeps waiting until the reception of data acknowledge signal to ensure sufficient wait time so that external device can reception data with no error.



During single-chip mode, do not set the external memory handshake mode.

■ Access Timing with External Memory Fixed Wait Cycles

Access timing with 2 or 3 wait cycles follows the same pattern. The latter part of the cycle is extended and the timing is the same.

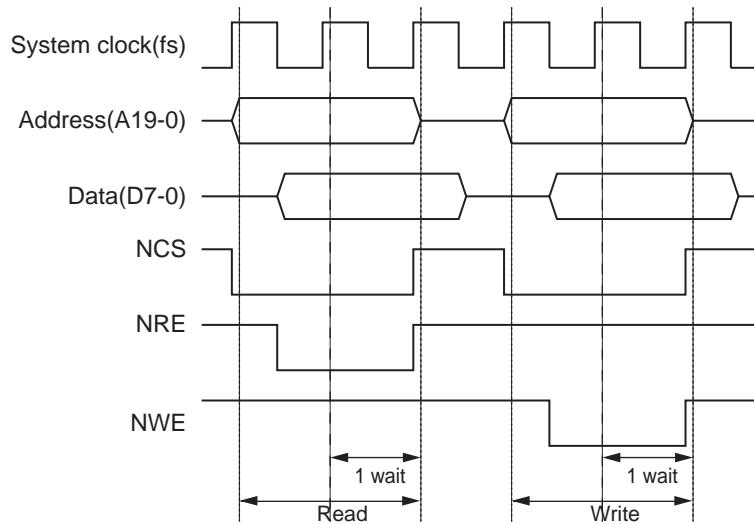


Figure:2.4.2 ROM and RAM Access Timing with fixed Wait Cycles

■ Access Timing with External Memory Handshake

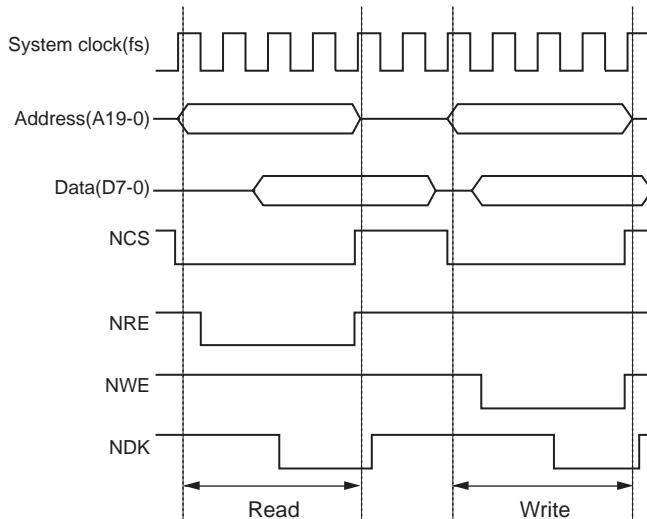


Figure:2.4.3 ROM and RAM Access Timing with Handshake



If accessing the external expansion memory area, execute with 5 MHz or less of access rate.

2.4.5 External Memory Connection Example

■ ROM Connection Example (memory expansion mode)

This example shows connection to 128 KB ROM.

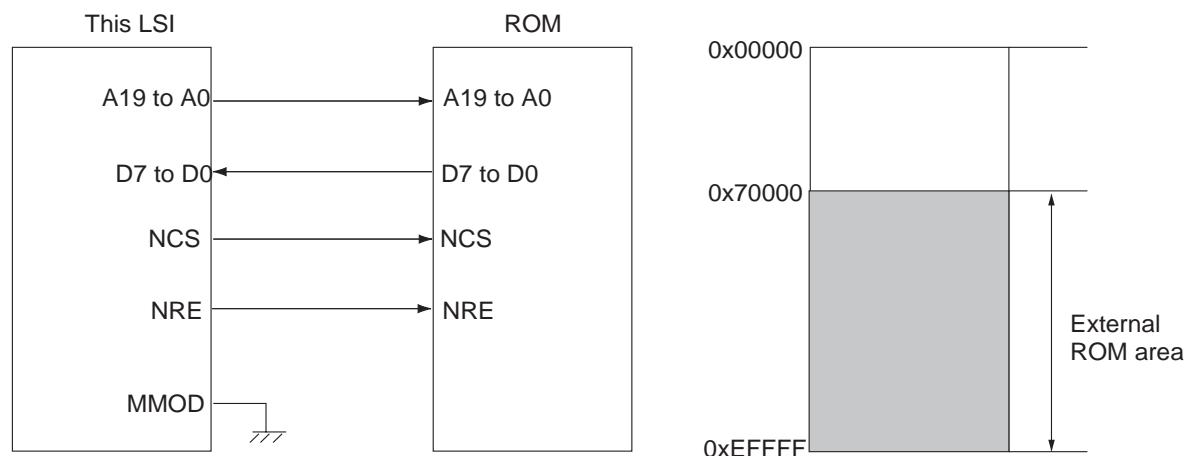


Figure 2.4.4 ROM Connection Example (memory expansion mode)

2.5 Standby Function

2.5.1 Overview

This LSI has two sets of system clock (fs) oscillator (high-speed oscillation, low speed oscillation) and PLL circuit to multiply high speed oscillation, for three CPU operating modes (NORMAL, PLL and SLOW), each with two standby modes (HALT and STOP). Power consumption can be decreased with using those modes.

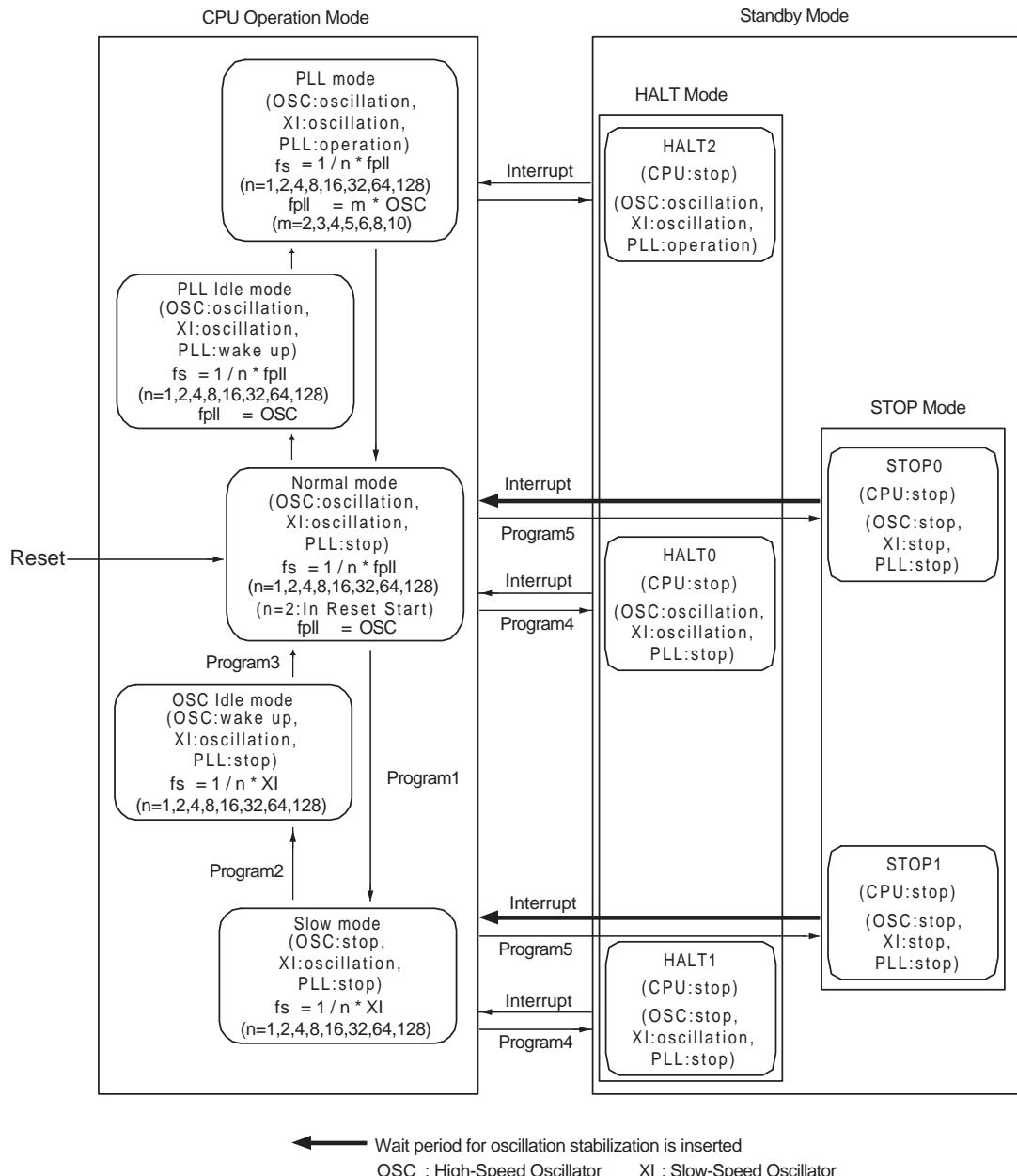


Figure:2.5.1 Transition Between Operation Modes

■ HALT Modes (HALT0, HALT1, HALT2)

The CPU stops operation. The oscillator or PLL are operating. An interrupt allows the CPU to operate.

The high and low-frequency oscillators operate in HALT0. When an interrupt occurs, HALT0 enters into the normal operation state (NORMAL).

Only the low-frequency oscillator operates in HALT1. When an interrupt occurs, HALT2 enters into the low-speed operation state (SLOW).

Both of the oscillators and PLL operate in HALT2. When an interrupt occurs, HALT2 enters into PLL modes.

■ STOP Modes (STOP0, STOP1)

The CPU and both of the oscillators stop operating.

An interrupt restarts the oscillators and, after allowing time for them to stabilize, returns the CPU to the previous CPU operating mode - that is, to NORMAL from STOP0 or to SLOW from STOP1.

■ SLOW Mode

This mode executes the software using the low-frequency clock. Since the high-speed oscillator is turned off, the device consumes less power while executing the software.

■ IDLE Modes (OSC-IDLE, PLL-IDLE)

The OSC-IDLE allows time for the high-speed oscillator to stabilize when the software is changing from SLOW to NORMAL mode.

The PLL-IDLE allows time for the clock from PLL to stabilize when the software is changing from NORMAL to PLL mode.

To reduce power dissipation in STOP and HALT modes, it is necessary to check the stability of both the output current from pins and port level of input pins. For output pins, the output level should match the external level or direction control should be changed to input mode. For input pins, the external level should be fixed.

This LSI has three system clock oscillation circuits. OSC or PLL is for high-frequency operation (NORMAL, PLL mode) and XI is for low-frequency operation (SLOW mode). Transition between NORMAL and SLOW modes or to standby mode is controlled by the CPU mode control register (CPUM). Reset and interrupts are the return factors from standby mode. A wait period is inserted for oscillation stabilization at reset and when returning from STOP mode, but not when returning from HALT mode. High/low-frequency oscillation mode is automatically returned to the same state as existed before entering standby mode.

■ PLL Mode (High-speed oscillation clock multiply)

The clock, which multiplies (2, 3, 4, 5, 6, 8, 10 multiplies) high-speed oscillator, is used as the high-speed clock. See [2.7 High-Speed Oscillation Clock Multiply Function] for how to use high-speed oscillation clock multiply function.



To stabilize the synchronization at the moment of switching clock frequency between high frequency oscillation (fpll) and low speed oscillation (fx), fpll should be set to 2.5 times or higher.



In OSC-IDLE state, the clock of the oscillator for high frequency operation (fosc) is oscillated, however, do not handle the peripheral functions with the fosc. Permit the fosc operation of the peripheral functions after the high frequency operation state is changed to NORMAL mode.



When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand and switch built-in ROM access method to the handshake. When usually access it within the range of exceed 10 MHz, it becomes impossible that can't read the ROM data and normal operation can't be guaranteed.

2.5.2 CPU Mode Control Register

Transition from one mode to another mode is controlled by the CPU mode control register (CPUM).

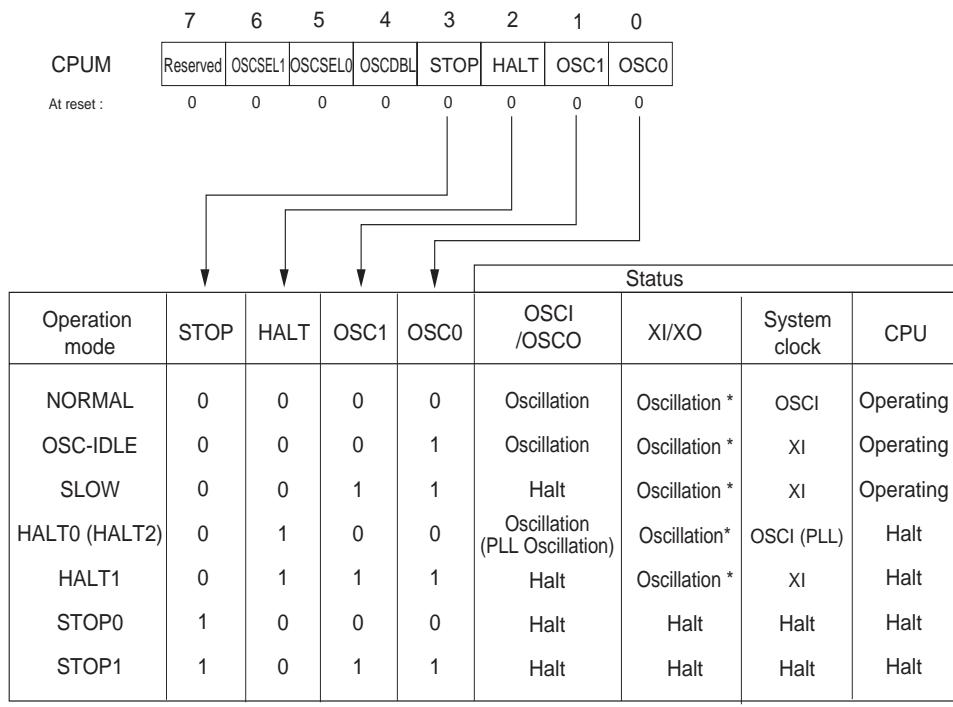


Figure 2.5.2. Growth Model Calibration (CPUM_2.2E02)

The next section discusses NORMAL, HALT, STOP, and the related

1. Clear the interrupt request flag (xxxIR) in the maskable interrupt control register (xxxICR), set the interrupt enable flag (xxxIE) for the return factor, and set the IE flag in the PSW.
 2. If the return factor is a maskable interrupt, set the MIE flag in the PSW to "1" and set the interrupt mask (IM) to a level permitting acceptance of the interrupt.
 3. Set CPUM to HALT or STOP mode



Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock switching function (OSCDBL, OSCSEL1 and OSCSEL0 flags) at the same time.



See section : 2.6 Clock switching for setup of bp 6-4 flags of the CPU mode control register (CPUM).



Set the IRWE flag of the memory control register (MEMCTR) to clear interrupt request flag by software. After clear interrupt request flag, must clear the IRWE flag.



The STOP, the HALT, the OSC1 or the OSC0 flags of the CPU mode control register (CPUM:0x3F00) should be used combination in Figure:2.5.2 only. The use of other combination is prohibited.

2.5.3 Transition between SLOW and NORMAL

This LSI has three CPU operating modes, NORMAL, PLL and SLOW. Transition from SLOW to NORMAL requires passing through OSC-IDLE mode.

A sample program for transition from NORMAL to SLOW mode is given below.

Program 1

```
MOV  x'03', D0      ; Set SLOW mode.  
MOV  D0, (CPUM)
```

Transition from NORMAL to SLOW mode, when the low-frequency clock has fully stabilized, can be done by writing to the CPU mode control register. In this case, transition through OSC-IDLE is not needed.



We recommend selecting the oscillation stabilization time of low-speed oscillation after consulting with oscillator manufacturers.



For transition from SLOW to NORMAL mode, the program must maintain the idle state until high-frequency clock oscillation is fully stable. In OSC-IDLE mode, the CPU operates on the low-frequency clock.



When SLOW mode, don't operate the peripheral circuits by a high-speed oscillation. A high-speed oscillation has stopped at the SLOW mode.

Sample program for transition from SLOW to NORMAL mode is given below.

Program 2

```
MOV  x'01', D0      ;Set IDLE mode.  
MOV  D0, (CPUM)
```

Program 3

```
MOV  x'0B', D0      ; A loop to keep approx. 6.7ms with low-frequency clock (32 kHz)  
LOOP ADD  -1, D0      ; Operation when changed to high-frequency clock (10 MHz).  
BNE   LOOP  
SUB   D0, D0      ; Set NORMAL mode  
MOV   D0,(CPUM)
```

2.5.4 Transition between NORMAL and PLL

This LSI has three CPU operating modes, NORMAL, PLL and SLOW. Transition from NORMAL to PLL requires passing through PLL-IDLE mode.

A sample program for transition from high-speed oscillation multiply mode to NORMAL mode is given below.

Program 1

```
BSET (XSEL) 2          ; Built-in ROM access method setting  
BCLR (PLLCNT) 1       ; Set NORMAL mode. (Use OSC oscillation)
```

Transition from PLL to NORMAL mode, when the high-speed multiply oscillation clock has fully stabilized, can be done by writing to the clock multiply circuit control register. In this case, transition through PLL-IDLE is not needed.

For transition from NORMAL to PLL mode, the program must maintain the idle state until high-speed multiply clock oscillation is fully stable. In PLL-IDLE mode, the CPU operates on the high-frequency clock.

Sample program for transition from NORMAL to PLL mode is given below.



When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand and switch built-in ROM access method to the handshake.

When usually access it within the range of exceed 10 MHz, it becomes impossible that can't read the ROM data and normal operation can't be guaranteed.

Program 2

```
MOV x'30', D0  
MOV D0, (PLLCNT) 1      ; Set PLL 4 multiplies  
BSET (PLLCNT) 0         ; Start PLL oscillation
```

Program 3

```
MOV x'43', D0          ; A loop to keep approx.100 µs with high-speed oscillation multiply clock (4 MHz)  
LOOP ADD -1, D0        ; Operation when changed to high-frequency clock (8 MHz).  
BNE LOOP  
BSET (PLLCNT)1         ; Select high-speed multiply clock use
```



Necessary time for steady operation of PLL is 100 µs. The stabilization waiting time is inserted by software.



Do neither multiplication setting of PLL nor oscillation start of PLL at the same time.

2.5.5 Transition to STANDBY Modes

The program initiates transitions from a CPU operating mode to the corresponding STANDBY (HALT/STOP) modes by specifying the new mode in the CPU mode control register (CPUM). Interrupts initiate the return to the former CPU operating mode.

Before initiating a transition to a STANDBY mode, however, the program must

1. Set the maskable interrupt enable flag (MIE) in the processor status word (PSW) to '0' to disable all maskable interrupts temporarily.
2. Set the interrupt enable flags (xxxIE) in the interrupt control registers (xxxICR) to '1' or '0' to specify which interrupts do and do not initiate the return from the STANDBY mode. Set MIE '1' to enable those maskable interrupts.

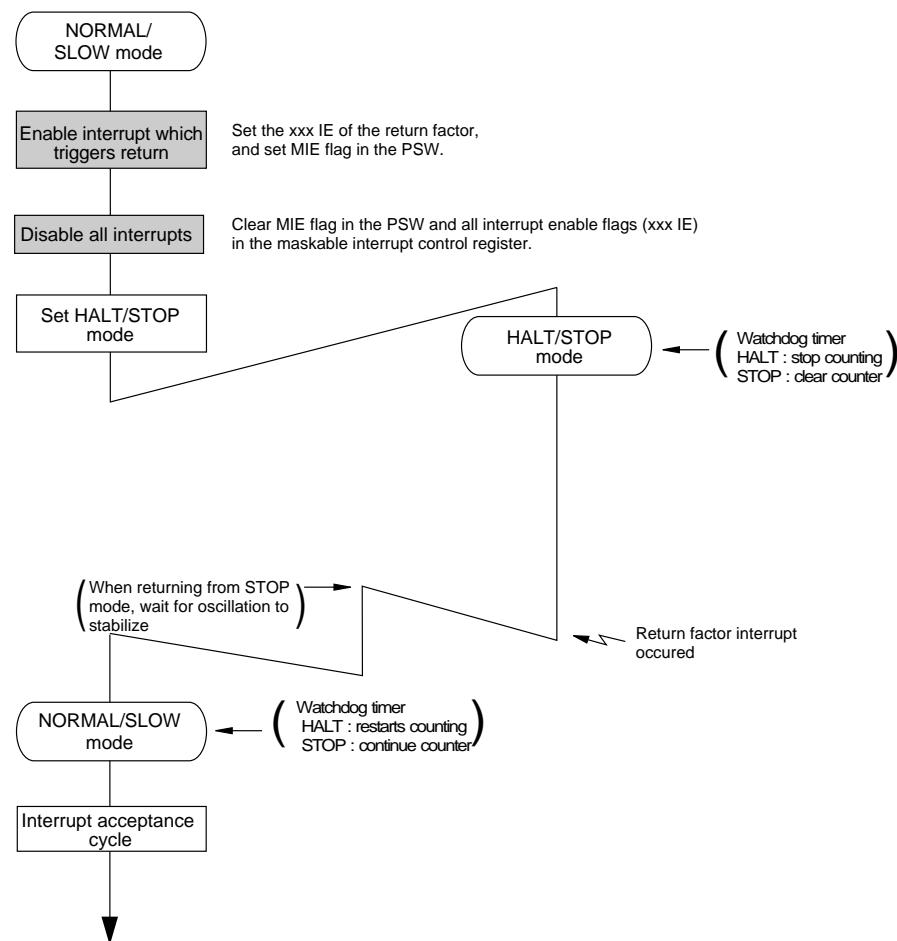


Figure:2.5.3 Transition to/from STANDBY Mode



If the interrupt is enabled but interrupt priority level of the interrupt to be used is not equal to or higher than the mask level in PSW before transition to HALT or STOP mode, it is impossible to return to CPU operation mode by maskable interrupt.



When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).

■ Transition to HALT modes

The system transfers from NORMAL mode to HALT0 mode, and from SLOW mode to HALT1 mode. The CPU stops operating, but the oscillators remain operational. There are two ways to leave a HALT mode: a reset or an interrupt. A reset produces a normal reset; an interrupt, an immediate return to the CPU state prior to the transition to the HALT mode. The watchdog timer, if enabled, resumes counting.

Program 4 MOV x'04', D0 MOV D0, (CPUM) NOP NOP NOP	; Set HALT mode. ; After written in CPUM, some NOP ; instructions (three or less) are ; executed.
--	--

■ Transition to STOP mode

The system transfers from NORMAL mode to STOP0 mode, and from SLOW mode to STOP1 mode. In both cases, oscillation and the CPU are both halted. There are two ways to leave a STOP mode: a reset or an interrupt.

On the transition to STOP mode, a counter of watchdog timer is cleared. On reconversion, the counting is started and oscillation stabilization wait is generated. After the reconversion to CPU operation, the counting is continued.

Program 5 MOV x'08', D0 MOV D0, (CPUM) NOP NOP NOP	; Set STOP mode. ; After written in CPUM, some NOP ; instructions (three or less) are ; executed.
--	--



Insert three NOP instructions right after the instruction of the transition to HALT, STOP mode.



Should transfer from PLL mode to STOP mode through Normal mode.



When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).



When can't ensure to generate the return interrupt sources after transmission request for standby mode (HALT/STOP) by setting to CPUM register, refer to [2.5.6 Attention of Transition to Standby Mode].

2.5.6 Attention of Transition to Standby Mode

When can't ensure to generate the return interrupt sources after transmission request for standby mode by setting to CPUM register, as don't transition to standby mode after the return interrupt is generated, execute the following processing.

```
# Standby Mode Transition Program
.

    MOV    x'08',    D1          ; STOP mode setting preparation
    MOV    psw,      D0
    OR     x'40',    D0
    MOV    D0,      psw         ; MIE flag setting
label_standby:
    MOV    D1,      (CPUM)     ; STOP mode setting
.

# Interrupt Processing Program
.

    PUSH   D0          ; Save of register
    PUSH   D1          ; Save of register
    MOV    (x'5', sp), D0
    AND    x'0F',    D0          ; Reduction of half byte information
    CMP    ah (label_standby), D0 ; Comparison of upper address for saving
    BNE    next program
    MOVW  (x'3', sp), DW0
    CMP    al (label_standby), DW0 ; Comparison of lower address for saving
    BNE    next program
    ADDW  x'02',    DW0          ; Instruction length of MOV dn, (CPUM)
    MOVW  DW0,      (x'3', sp) ; Change of address for saving
next_program:
    POP    D1
    POP    D0
```

2.5.7 Usage of Low-Frequency Clock

After releasing reset, this LSI does not oscillate low-frequency clock.

When using low-frequency clock, it must be set by the program.

When low-frequency clock (fx) is used as the clock source of transitions from NORMAL mode to SLOW mode, or the clock source of peripheral equipment such as Timer LCD, set the P90/XI, P91/XO pin to low-frequency oscillation pin with the low-speed oscillation selection register (XSEL). After the setting, with due consideration for oscillation stabilization wait time, use the low-frequency clock (fx) as the clock source of transitions to SLOW mode, or the clock source of peripheral equipment.

When using low-frequency clock, set the following:

(1) After releasing reset, set the bp5 of the low-speed oscillation selection register (XSEL) to “1”, and set the P90/XI, P91/XO pin to low-frequency oscillation pin. This will start low-frequency clock.

(2) Count the low-frequency oscillation stabilization wait time by the program.

(At the time, operation in NORMAL mode is not affected. In addition, when fpll (when pll is not used) or fx is used as the clock source of peripheral functions, it operates without any problem.)

(3) fx can be used as the clock source of transitions to SLOW mode, or the clock source of peripheral equipment.



Low-frequency oscillation should be stabled when using low-frequency clock. At least 4 counts of low-frequency clock is required for the stabilization. We recommend selecting the oscillation stabilization time after consulting with oscillator manufacturers.

Sample program prior to the usage of low-frequency clock is given below.

Program 6

```
MOV  x'20', (XSEL)      ; Set the P90/XI, P91/XO pin to low-frequency oscillation
MOV  x'FF', D0
LOOP ADD  -1, D0
BNE  LOOP              ; Loop to wait about 1.5 µs by 10 MHz
MOV  x'02', (TM0MD)    ; Select fx as the count clock of timer 0
MOV  x'03', (TM0OC)    ; Set interrupt generation cycle
MOV  x'82', (TM0ICR)   ; Enable timer 0 interrupt
BSET (TM0MD)3          ; Start counting of timer 0
.
.
.
; After interrupt, fx can be used
```

Low-speed oscillation is also used as P90, P91. At the slow mode, low-speed oscillation selection register (XSEL)

■ Low-speed oscillation selection register (XSEL : 0x03F2F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	XSEL	-	-	ROMHND	Reserved	Reserved
At reset	-	-	0	-	-	0	0	0
Access	-	-	R/W	-	-	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5	XSEL	P90/P91 I/O port, low-speed oscillation selection 0 : I/O port 1 : Low-speed oscillation
4-3	-	-
2	ROMHND	Built-in ROM area access switching 0 : Normal access 1 : Handshake
1-0	Reserved	Always set to "0" *



When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).



When operated with the system clock (f_s) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand and switch built-in ROM access method to the handshake.
When usually access it within the range of exceed 10 MHz, it becomes impossible that can't read the ROM data and normal operation can't be guaranteed.



Always set "0" to the bp denoted by asterisk.

2.5.8 Method for Accessing to Internal ROM

This LSI needs to set a method for accessing to internal ROM area with system clock frequency (fs).

The table below shows the relation between power supply voltage (V_{DD5}) and system clock (fs).

Table:2.5.1 The setting value of XSEL register

System clock (fs)	ROMHND flag
$fs < 10 \text{ MHz}$	0
$10 \text{ MHz} \leq fs \leq 20 \text{ MHz}$	1

■ Low-speed oscillation selection register (XSEL)

bp	7	6	5	4	3	2	1	0
Flag	-	-	XSEL	-	-	ROMHND	Reserved	Reserved
At reset	-	-	0	-	-	0	0	0
Access	-	-	R/W	-	-	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5	XSEL	P90/P91 I/O port, Low-speed oscillation selection 0 : I/O port 1 : Low-speed oscillation
4-3	-	-
2	ROMHND	Built-in ROM area access switching 0 : Normal access 1 : Handshake
1-0	Reserved	Always set to "0" *



Set the ROMHND flag in advance to select HANDSHAKE access when transition to the system clock frequency of the ROMHND flag settings described.



Clear the ROMHND flag and select normal access when operating with the system clock frequency of the ROMHND flag clearing described. The access timing to the internal ROM area improves.



Always set “0” to the bp denoted by asterisk.



Immediately after set “1” to the ROMHND flag (bp2) in the XSEL register, the NOP instruction is needed.

Description example of C program

```
asm("tbset (0x03F2F)2"); /*ROMHND flag setting*/  
asm("tnop");           /*elsewhere condition*/
```

When the program is compiled to enable the description of inline assembler (asm language), should be set the option of “-fenable-asm”.

Description example of assembler program

```
bset(0x03F2F)2      ;ROMHND flag setting  
nop                 ;elsewhere condition
```

2.6 Clock Switching

This LSI can select the best operation clock for system by switching clock cycle division factor by program. Division factor is determined by flag of the CPU mode control register (CPUM). At the highest-frequency, CPU can be operated in the same clock cycle to the external clock hence providing wider operating frequency range.

■ CPU Mode Control Register (CPUM : 0x03F00)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	OSCSEL1	OSCSEL0	OSCDBL	STOP	HALT	OSC1	OSC0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0". *
6-5	OSCSEL1 OSCSEL0	Clock Frequency 00: 1 01: 4 10: 16 11: 64
4	OSCDBL	Internal System Clock (fs) 0: Standard (Input the oscillation clock cycle divided by 2) 1: 2x-speed (Input the oscillation clock cycle)



See Figure:2.5.2 for setup of bp3-0 flags of the CPU mode control register (CPUM).



Always set "0" to the bp denoted by asterisk.

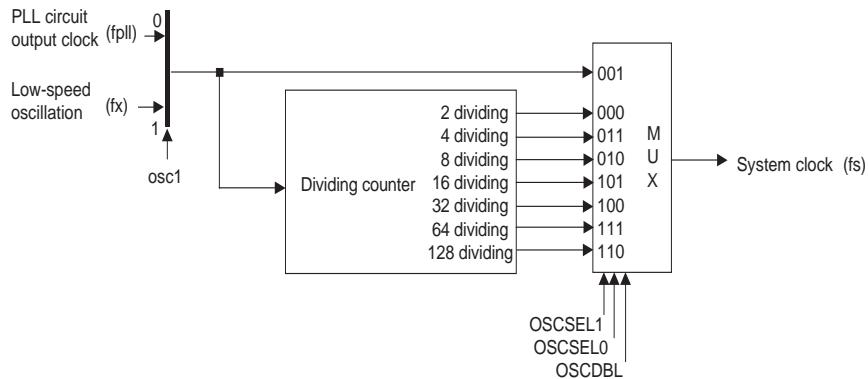


Figure:2.6.1 Clock Switching Circuit

Table:2.6.1 Division Factor Setting with Combination of OSCSEL and OSCDBL

OSCSEL1	OSCSEL0	OSCDBL	Oscillating frequency
0	0	0	2
0	0	1	1
0	1	0	8
0	1	1	4
1	0	0	32
1	0	1	16
1	1	0	128
1	1	1	64



Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock switching function (OSCDBL, OSCSEL1 and OSCSEL0 flags) at the same time.



OSCDBL, OSCSEL1 and OSCSEL0 flags can be set at the same time.



Set the dividing ratio of oscillation clock and transition to the operation mode to meet the operating condition (refer to Chapter 1 "Electrical Characteristics").



When system clock is over 10 MHz, set bp2 of XSEL register (0x03F2F) and change the access method to built-in ROM area to handshake.

2.7 High-Speed Oscillation Clock Multiply Function

High-speed oscillation clock multiply function is to generate a clock , 2/ 3/ 4/ 5/ 6/ 8/ 10-multiply of high-speed oscillation input from OSC1/OSC2. Also, PLL circuit output clock is defined as fpll. (This is used as clock source in each function such as timer or serial in Chapter 2 and after.)

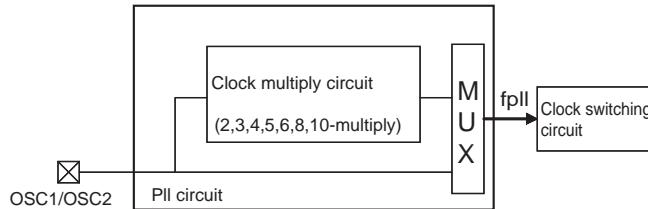


Figure:2.7.1 PLL Circuit

2.7.1 Control registers

- Clock Multiply Circuit Control Register (PLLCNT: 0x03FDF)

bp	7	6	5	4	3	2	1	0
Flag	PLLCK3	PLLCK2	PLLCK1	PLLCK0	-	-	PLLEN	PLLSTART
At reset	0	0	0	0	-	-	0	0
Access	R/W	R/W	R/W	R/W	-	-	R/W	R/W

bp	Flag	Description
7-4	PLLCK3-0	Specification of multiply number 4' h0: 2-multiply (Input frequency 4-7.5 MHz) 4' h1: 2-multiply (Input frequency 7.5-10 MHz) 4' h2: 3-multiply (Input frequency 4-5 MHz) 4' h3: 4-multiply (Input frequency 4-7.5 MHz) 4' h4: 4-multiply (Input frequency 7.5-10 MHz) 4' h5: 5-multiply (Input frequency 4-6 MHz) 4' h6: 5-multiply (Input frequency 6-8 MHz) 4' h7: 6-multiply (Input frequency 4-5 MHz) 4' h8: 8-multiply (Input frequency 4-5 MHz) 4' h9: 10-multiply (Input frequency 4 MHz) 4' h10-15: Setting prohibited
3-2	-	-
1	PLLEN	PLL clock enable 0: External high-speed oscillation (osc) operation 1: PLL clock operation
0	PLLSTART	PLL operation control 0: No PLL operation 1: PLL operation

2.7.2 Setup Example

■ Setup Example of High-Speed Oscillation Clock Multiply Function

By using high-speed oscillation clock multiply function, a clock, 2-multiply of high-speed oscillation clock, is set as fpll. An example setup procedure, with discription of each step is shown below.

Setup Procedure	Description
(1) Set the multiply number. PLLCKNT (0x03FDF) bp5-4: PLLCK1-0 = 00	(1) Select 2-multiply by setting the PLLCK flag of the high-speed oscillation clock multiply function control register (PLLCKNT).
(2) Start the PLL operation. PLLCKNT (0x03FDF) bp0 :PLLSTART = 1	(2) Start PLL operation by setting the PLLSTART flag to "1".
(3) MOV 0x43, D0 LOOP ADD -1, D0 BNE LOOP	(3) Wait PLL operation waiting time 100 μ s by software.(4 MHz)
(4) Switch the clock PLLCKNT (0x03FDF) bp1 :PLLEN = 1	(4) After PLL operation stabilization wait timer is completed, set the clock, which is 2-multiply of high-speed oscillation clock as fpll.



The setup described above can not be done at the same time. When set PLL, has to switch by above setting.



Switch in the bit order of (4) and (2) for transition to NORMAL mode.



The required time for PLL operation stabilization is 100 μ s. Insert stabilization time by software.



Do not change the setting of multiply number during PLL operation.



Don't set PLLSTART flag by the state of PLLEN flag = "0" of PLLCNT register.



Refer to [2.5 Standby Function] for operation mode transition.

The direct transition from the slow mode to the pll mode can not be enabled. Always transit via Normal mode.



When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand and switch built-in ROM access method to the handshake.

When usually access it within the range of exceed 10 MHz, it becomes impossible that can't read the ROM data and normal operation can't be guaranteed.



Block clocks, such as a timer and a serial which use fpll as a clock source, are multiplied by using high-speed oscillation clock multiply function.



The operation does not guaranteed if the system clock operates over 20MHz. Set the multiply number in 20MHz or lower range. If necessary, set the dividing with CPU mode register before PLL operates.

2.8 Reset

2.8.1 Reset operation

The CPU contents are reset and registers are initialized when the NRST pin is pulled to low.

■ Initiating a Reset

There are two methods to initiate a reset.

1. Drive the NRST pin low.

NRST pin should be held "low" for more than 100 μ s.

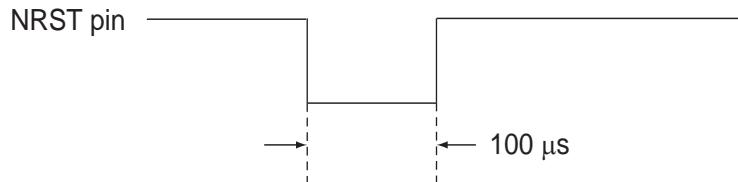


Figure:2.8.1 Minimum Reset Pulse Width

2. Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transferring to reset by program (software reset) can be executed.

If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.



This LSI is activated in NORMAL mode in which the base clock is external high-speed oscillation.



When NRST pin is connected to low power voltage detection circuit that gives pulse for enough low level time at sudden unconnected. And reset can be generated even if NRST pin is held "low" for less than 100 μ s, take notice of noise.



In this LSI, the oscillation (High-speed oscillation and Low speed oscillation) is stopped at reset.

■ Reset Sequence at the time of Power Supply Injection

This LSI is equipped with a power supply regulator.

External power supply stands up, and a regulator starts supply of a power supply later after about 100 us(max).

For a start period of a regulator, keep an NRST "L".

Refer to [Chapter I 1.7.4 Power Supply] for details.



When use power-on reset, it is necessary to keep NRST="L"(under 0.15 VDD5) till a regulator stands up. If the period keeping "L" is not enough, a regulator may not work properly.

[Setup example]

- 1)VDD5=5.0 V
- 2)VDD5 external power supply standing time(till VDD=2.2 V) = 4.4 ms
- 3)Regulator standing time=100 us(max)
- 4)R=10 kΩ(built-in pull-up Resistance value(min))

In this case
To keep NRST "L" during 6.45 ms, outside capacity need over 4.0 uF
from $V_{NRST}=V_{DD5} \times (1-\exp(-t/RC))$

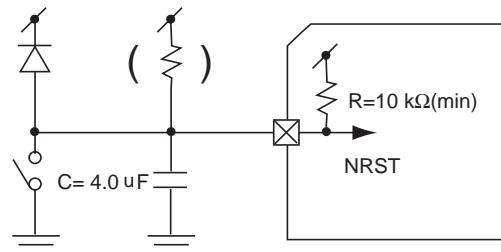


Figure:2.8.2 Reset Released Sequence

■ Sequence at Reset

1. When reset pin comes to high level from low level, the internal 14-bit counter (It can be used as watchdog timer, too.) starts its operation by system clock. The period from starting its count from its overflow is called oscillation stabilization wait time.
2. During reset, internal register and special function register are initiated.

Register	Address	R/W	Description	Initial value
PSW	-		Processor status word	0x00
PC	-		Program counter	Address stored in 0x04000
SP	-		Stack Pointer	undefined
An	-		Address register	undefined
Dn	-		Data register	undefined
CPUM	0x03F00	R/W	CPU mode control register	0x00
MEMCTR	0x03F01	R/W	Memory control register	0xCB
xxxICR	0x03FE2 to 0x03FFE	R/W	Maskable interrupt control register	0x00

3. After oscillation stabilization wait time, internal reset is released and program is started from the address written at address 0x4000 at interrupt vector table.

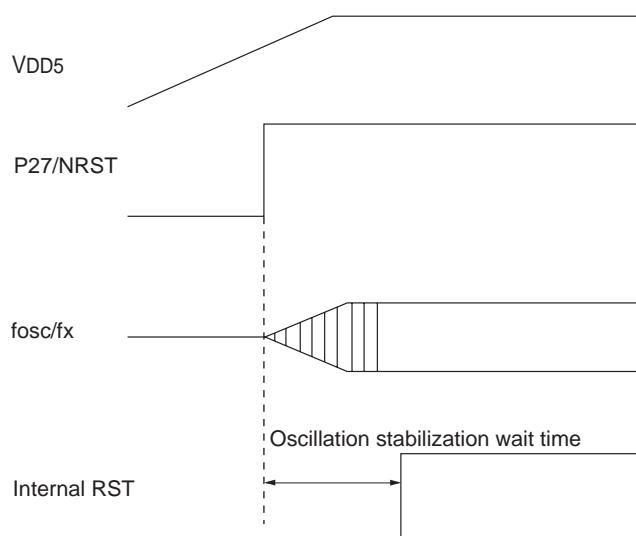


Figure:2.8.3 Reset Released Sequence



The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before used.

2.8.2 Oscillation Stabilization Wait time

Oscillation stabilization wait time is the period from the stop of oscillation circuit to the stabilization for oscillation. Oscillation stabilization wait time is automatically inserted at releasing from reset and at recovering from STOP mode. At recovering from STOP mode the oscillation stabilization wait time control register (DLYCTR) is set to select the oscillation stabilization wait time. At releasing from reset, oscillation stabilization wait time is fixed.

The timer that counts oscillation stabilization wait time is also used as a watchdog timer. That is used as a runaway detective timer at anytime except at releasing from reset and at recovering from STOP mode. Watchdog timer is initiated at reset and at STOP mode and starts counting from the initialize value (0x0000) when system clock (fs) is as clock source. After oscillation stabilization wait time, it continues counting as a watchdog timer.

■ Block Diagram of Oscillation Stabilization Wait Time (watchdog timer)

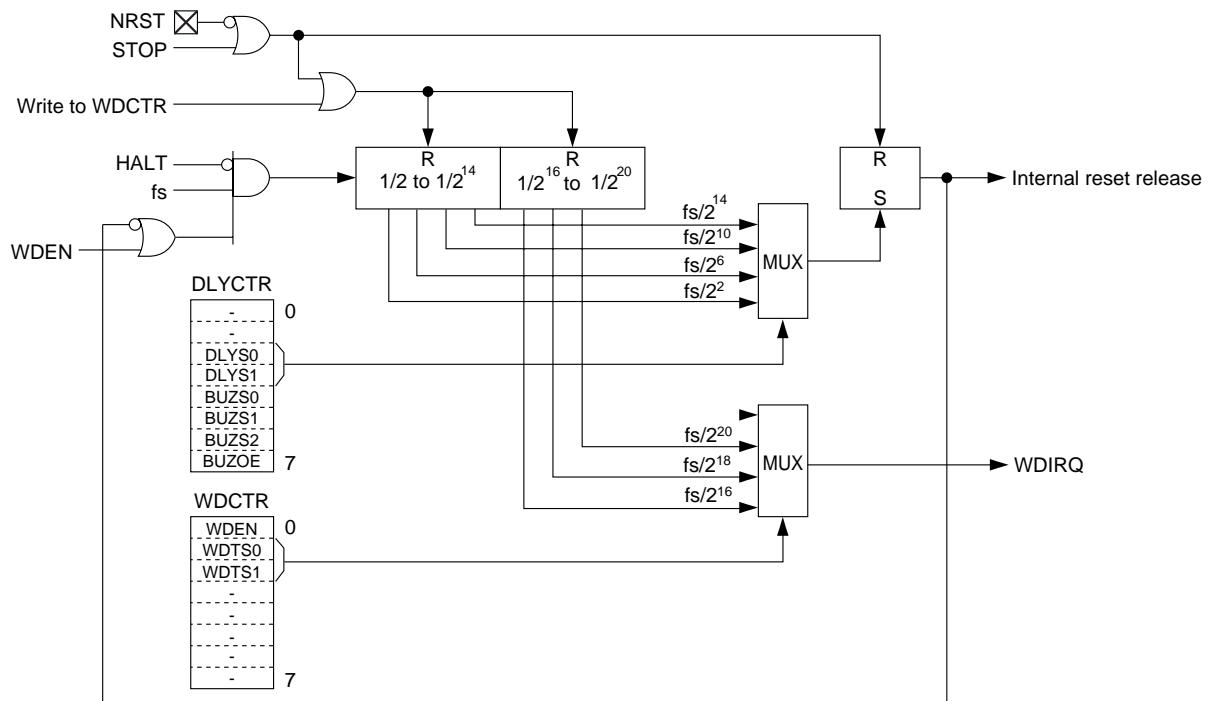


Figure:2.8.4 Block Diagram of Osillation Stabilization Wait Time (watchdog timer)

■ Oscillation Stabilization Wait Time Control Register (DLYCTR : 0x03F03)

bp	7	6	5	4	3	2	1	0
Flag	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-
At reset	0	0	0	0	0	0	-	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	-

bp	Flag	Description
7	BUZOE	Output selection 0:Portdata output 1:Buzzer output
6-4	BUZS2 BUZS1 BUZS0	Buzzer output frequency selection 000:fpll/2 ¹⁴ 001:fpll/2 ¹³ 010:fpll/2 ¹² 011:fpll/2 ¹¹ 100:ffpll/2 ¹⁰ 101:fpll/2 ⁹ 110:fx/2 ⁴ 111:fx/2 ³
3-2	DLYS1 DLYS0	Oscillation stabilization wait period selection 00:fs/2 ¹⁴ 01:fs/2 ¹⁰ 10:fs/2 ⁶ *1 11:s/2 ² *1
1-0	-	-



For the oscillation stabilization wait cycle required for high-speed/low-speed oscillation, which is set by DLYS 1-0 flags, it is recommended to consult the oscillator manufacturer for determining appropriate values.



See [Chapter 11 Buzzer] for setup of bp7-4 flags of the oscillation stabilization wait time control register (DLYCTR).



When recovering from STOP mode, more than 100 µs of oscillation stabilization wait cycle must be set for internal regulator output stabilization wait.

■ Control the Oscillation Stabilization Wait Time

At recovering from STOP mode, the bit 3-2 (DLYS1, DLYS0) of the oscillation stabilization wait time control register can be set to select the oscillation stabilization wait time from 2^{14} , 2^{10} , 2^6 , $2^2 \times$ system clock. The DLYCTR register is also used for controlling of buzzer functions.

At releasing from reset, the oscillation stabilization wait time is fixed to " $2^{14} \times$ system clock". System clock is determined by the CPU mode control register (CPUM).

Table:2.8.1 Oscillation Stabilization Wait Time

DLYS1	DLYS0	Oscillation stabilization wait time
0	0	$2^{14} \times$ System clock
0	1	$2^{10} \times$ System clock
1	0	$2^6 \times$ System clock
1	1	$2^2 \times$ System clock



Please set the value by which an oscillation circuit is stabilized enough to the waiting cycle for oscillation stability.

2.9 Summary of Auto Reset Functions

2.9.1 Summary of Auto Reset Functions

This LSI has a built-in type 1 auto reset circuit that detects low voltage.
Auto reset function can be selected with ATRST pin (11 pin)

- In using auto reset --- ATRST pin (11 pin) : V_{DD5} level fixed
- In not using auto reset --- ATRST pin (11 pin) : V_{SS} level fixed

When detecting a low voltage at auto reset function, NRST pin automatically becomes "L" level and reset operation is executed. When power supply voltage reaches reset cancellation voltage (VRST), NRST pin automatically becomes "H" and reset is cancelled.

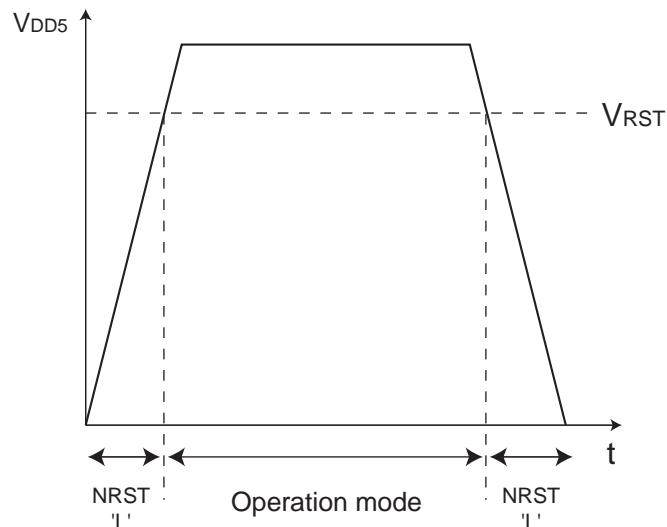


Figure:2.9.1 Auto Reset Detection Voltage



Refer to [Chapter I 1.5.7 Auto Reset Characteristics] for VRST



When use the auto reset function, "L" level input to NRST pin has to keep at least 100 μ s or more. Connect external capacitors and design the substrate with which above-mentioned requirement is met.

2.10 Extended Calculation Instruction

2.10.1 Overview

This LSI contains the functions of 16-bit x 16-bit and 32-bit/16-bit calculation in addition to the existing calculation functions which can be executed by MN101C series. The executable calculation and execution cycles are as follows:

Table:2.10.1 List of Extended Calculation Functions

Calculation	Instruction	Operation	Execution cycle	PSW Flag variation			
				V F	N F	C F	Z F
16-bit x 16-bit multiplication (unsigned)	MOV 1,(0x3F07) Extended calculation macro instruction MULWU	DW0 * DW1→{DW1, DW0}	13 cycles	0	✓	0	✓
16-bit x 16-bit multiplication (signed)	MOV 2,(0x3F07) Extended calculation macro instruction MULW	DW0 * DW1→{DW1, DW0}	13 cycles	0	✓	0	✓
32-bit/16-bit division (unsigned)	MOV 4,(0x3F07) Extended calculation macro instruction DIVWU	{DW1, DW0}/A0→DW0…DW1	14 cycles	✓	✓	0	✓

✓: flag varies.

VF: The value is 0 when the division result can be expressed with the unsigned 16-bit, and otherwise is 1. When zero divide is executed, the value is 1. When the value is 1, the calculation ends in 6 executing cycles.

The value is always 0 in case of multiplication.

NF: The value is 1 when the MSB of multiplication/division result is 1. It is 0 when the MSB of the result is 0.

However, when VF is 1, the value is undefined.

CF: Always 0.

ZF: The value is 1 when the multiplication/division result is 0, and otherwise is 0.

However, when VF is 1, the value is undefined.

Refer to Chapter 2 2.11 Extended Calculation Macro Instruction

2.10.2 Extended Calculation Control Register

Extended calculation can be executed by setting the extended calculation control flag after setting the multiplier to DW0, the multiplicand to DW1, the divisor to A0, and the dividend to DW1 and DW0 respectively.

■ Expanded Calculation Control Register (AUCTR:0x03F07)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	AUDIVU	AUMUL	AUMULU
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	W	W	W

bp	Flag	Description
7-3	-	-
2	AUDIVU	Unsigned division execution 0: Disabled 1: Enabled
1	AUMUL	Signed multiplication execution 0: Disabled 1: Enabled
0	AUMULU	Unsigned multiplication execution 0: Disabled 1: Enabled

When calculation is finished, each flag is cleared to “0” by hardware.



Don't set a number of bits at the same time.

2.10.3 Execution of Extended Calculation

■ Execution of 16-bit x 16-bit multiplication (unsigned)

1. Store the multiplier to DW0 register and the multiplicand to DW1 register.
2. Execute MOV 1, (0x03F07) (Extended calculation macro instruction MULWU).
3. The value of the unsigned 16-bit of DW0 register is multiplied by the unsigned 16-bit of DW1 register. Then the upper 16-bit of the result (32-bit) is stored in DW1 register and the lower 16-bit is stored in DW0 register.

■ Execution of 16-bit x 16-bit multiplication (signed)

1. Store the multiplier to DW0 register and the multiplicand to DW1 register.
2. Execute MOV 2, (0x03F07) (Extended calculation macro instruction MULW).
3. The value of the signed 16-bit of DW0 register is multiplied by the signed 16-bit of DW1 register. Then the upper 16-bit of the results (32-bit) is stored in DW1 register and the lower 16-bit register is stored in DW0 register.

■ Execution of 32-bit / 16-bit division (unsigned)

1. Store the upper 16-bit of the dividend to DW1 register, the lower 16-bit of the dividend to DW0 register, and the divisor to A0 register.
2. Execute MOV 4, (0x03F07) (Extended calculation macro instruction DIVWU).
3. The value of the unsigned 32-bit which is stored in the DW1 register (upper 16-bit) and DW0 register (lower 16-bit) is divided by the value of the unsigned 16-bit of A0 register. Then the quotient 16-bit of the result is stored in DW0 register and the residue 16-bit of the result is stored in DW1 register.



VF is 1 when the division result cannot be expressed with the unsigned 16-bit or zero divide is executed.



When VF is 1, the calculation ends in 6 execution cycles. In this case, the result is undefined.

2.11 Extended Calculation Macro Instruction

Extended calculation macro instruction can be generated by specifying machine dependence option -mmuldivw by compiler of MN101C/MN101E series.

2.11.1 About Extended Calculation Macro Instruction

■ About this Table

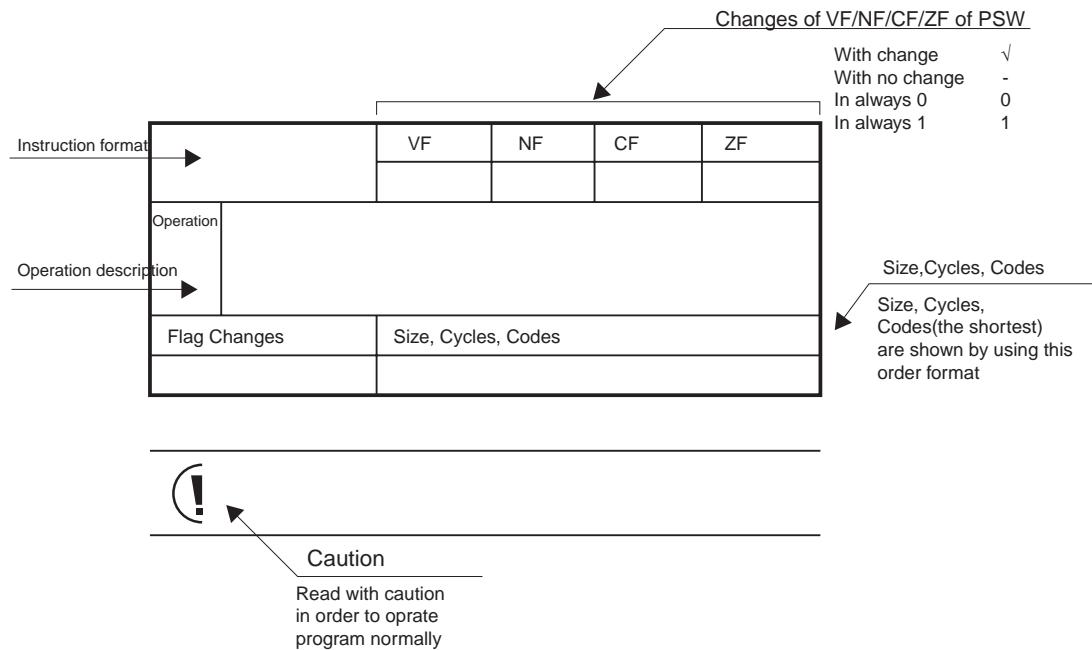


Figure:2.11.1 About this Table

■ Sign

*	Multiplication
/	Division
→	Substitution
...	Residue
{DW1,DW0}	32 bit data (high 16 bits in DW1 register and low 16 bits in DW0 register are stored)

2.11.2 MULWU

MULWU		VF	NF	CF	ZF
		0	✓	0	✓
Operation	DW0 *DW1 → {DW1, DW0}				
Multiplies the unsigned 16-bit value of DW0 register by the unsigned 16-bit value or DW1 register, and store the upper 16-bit of the result (32-bit) in the DW1 register and the lower 16-bit of the result in the DW0 register.					
Flag Changes		Size, Cycles, Codes			
VF: 0 NF: Set if the MSB of the result is 1, reset otherwise. CF: 0 ZF: Set if the result is 0, reset otherwise.		6 nibbles 13 cycles 0000 0010 0111 0000 0001 0000			



Store the multiplier to DW0 register and the multiplicand to DW1 register before executing this instruction.



This instruction is a macro instruction. The following operation is actually executed:

MOV 1, (0x03F07); Set 1 to AUCTR register (address 0x03F07)

With this instruction, the address used in the handy addressing mode is updated to 0x03F07.

The updating example of handy addresses is as follows:

_CODE section code, pulic, 0

```

    mov      (0x100), d0
    mulwu
    mov      d0, (HA)           ; HA value is updated and
                                ; 0x03F07 address is accessed

    mov      (0x100), d0
    add      1, d0
    mov      d0, (HA)           ; access to HA value 0x100 address

```

2.11.3 MULW

MULW		VF	NF	CF	ZF
		0	✓	0	✓
Operation	DW0 *DW1 → {DW1, DW0}				
	Multiplies the unsigned 16-bit value of DW0 register by the unsigned 16-bit value or DW1 register, and store the upper 16-bit of the result (32-bit) in the DW1 register and the lower 16-bit of the result in the DW0 register.				
Flag Changes		Size, Cycles, Codes			
VF: 0 NF: Set if the MSB of the result is 1, reset otherwise. CF: 0 ZF: Set if the result is 0, reset otherwise.		6 nibbles 13 cycles 0000 0010 0111 0000 0010 0000			



Store the multiplier to DW0 register and the multiplicand to DW1 register before executing this instruction.



This instruction is a macro instruction. The following operation is actually executed:

MOV 2, (0x03F07);set 2 to AUCTR register (address 0x03F07)

With this instruction, the address used in the handy addressing mode is updated to 0x03F07.

The updating example of handy addresses is as follows:

```
_CODE section code, public, 0

    mov    (0x100), d0
    mulwu
    mov    d0, (HA)      ; HA value is updated and
                         ; 0x03F07 address is accessed

    mov    (0x100), d0
    add    1, d0
    mov    d0, (HA)      ; access to HA value 0x100 address
```

2.11.4 DIVWU

DIVWU		VF	NF	CF	ZF
Operation	{DW1, DW0}/A0 → DW0...DW1	√	√	0	√
Flag Changes		Size, Cycles, Codes			
If VF is 0 VF:0 (if the quotient is an unsigned 16-bit value) NF:Set if the MSB of the quotient is 1, reset otherwise. CF:0 ZF:Set if the MSB of the quotient is 0, reset otherwise.	If VF is 1 VF:1 (if the quotient is not an unsigned 16-bit value) NF:Undefined CF:0 ZF:Undefined	6 nibbles 14 cycles 0000 0010 0111 0000 0100 0000			



Set the upper 16-bit of the dividend to DW1 register, the lower 16-bit of the dividend to DW0 register, and the divisor to A0 register.



This instruction is a macro instruction. The following operation is actually executed:

MOV 4, (0x03F07) ; Set 4 to AUCTR register (address 0x03F07)

With this instruction, the address used in the handy addressing mode is updated to 0x03F07.
The updating example of handy addresses is as follows:

```
_CODE section code, public, 0

    mov    (0x100), d0
    mulwu
    mov    d0, (HA)      ; HA value is updated and
                         ; 0x03F07 address is accessed

    mov    (0x100), d0
    add    1, d0
    mov    d0, (HA)      ; access to HA value 0x100 address
```



VF is 1 when the division result cannot be expressed with the unsigned 16-bit or zero divide is executed.



When VF is 1, the calculation ends in 6 execution cycles. In this case, the result is undefined.

3

Chapter 3 Interrupts

3.1 Overview

This LSI speeds up interrupt response with circuitry that automatically loads the branch address to the corresponding interrupt service routine from an interrupt vector table: reset, non-maskable interrupts (NMI), 6 maskable peripheral interrupts, and 21 internal interrupts.

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance determination (only maskable interrupt), interrupt acceptance (hardware processing) and return (RTI instruction). After the interrupt is accepted, the program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack. Handy addressing data (HA) is saved onto the stack so that it may not be influenced by the interrupt. And an interrupt handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted. Least 12 machine cycles before execution, and 11 machine cycles for the return from interrupt.

Each interrupt has a interrupt control register, which controls the interrupts. Interrupt control register consists of the interrupt level field (LV1 to 0), interrupt enable flag (IE), and interrupt request flag (IR).

Interrupt request flag (IR) is set to "1" by an interrupt request, and cleared to "0" by the interrupt acceptance. This flag is managed by hardware, but can be rewritten by software.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. There is no interrupt enable flag in non-maskable interrupt (NMI). Once this interrupt request flag is set, it is accepted without any conditions. Interrupts enable flag is set in maskable interrupt. Interrupt enable flag of maskable interrupt is valid when the maskable interrupt enable flag (MIE flag) of PSW is "1".

Maskable interrupts have vector numbers by hardware, but their priority can be changed by setting interrupt level field. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. Maskable interrupts are accepted when its level is higher than the interrupt mask level (IM1 to 0) of PSW. Non-maskable interrupts are always accepted, regardless of the interrupt mask level.

3.1.1 Functions

Table:3.1.1 Interrupt Functions

Interrupt type		Reset (interrupt)	Non-maskable interrupt	Maskable interrupt
Vector number		0	1	2 to 30
Table address	IVBM = 0	0x04000	0x04004	0x04008 to 0x04078
	IVBM = 1		0x00104	0x00108 to 0x00178
Starting address		Address specified by vector address		
Interrupt level		-	-	Can be set to levels 0 to 2 by software
Interrupt factor		External Reset pin input	Errors detection, Program interrupt (PI)	External pin input internal peripheral function
Generated operation		Direct input to CPU	Input to CPU from non-maskable interrupt control register (NMICR)	Input interrupt request level set in interrupt level flag (xxxLVn) of maskable interrupt control register (xxxICR) to CPU.
Accept operation		Always accepts	Always accepts	Acceptance only by the interrupt control of the register (xxxICR) and the maskable interrupt enable, the interrupt mask level in PSW.
Machine cycles until accepted		Least 6 Machine cycles + oscillation stabilization wait time	Least 12	Least 12
PSW status after acceptance		All flags are cleared to "0"	The interrupt mask level flag in PSW is cleared to "00"	Values of the interrupt level flag (xxxLVn) are set to the interrupt mask level (masking all interrupt requests with the same or the lower priority).

3.1.2 Block Diagram

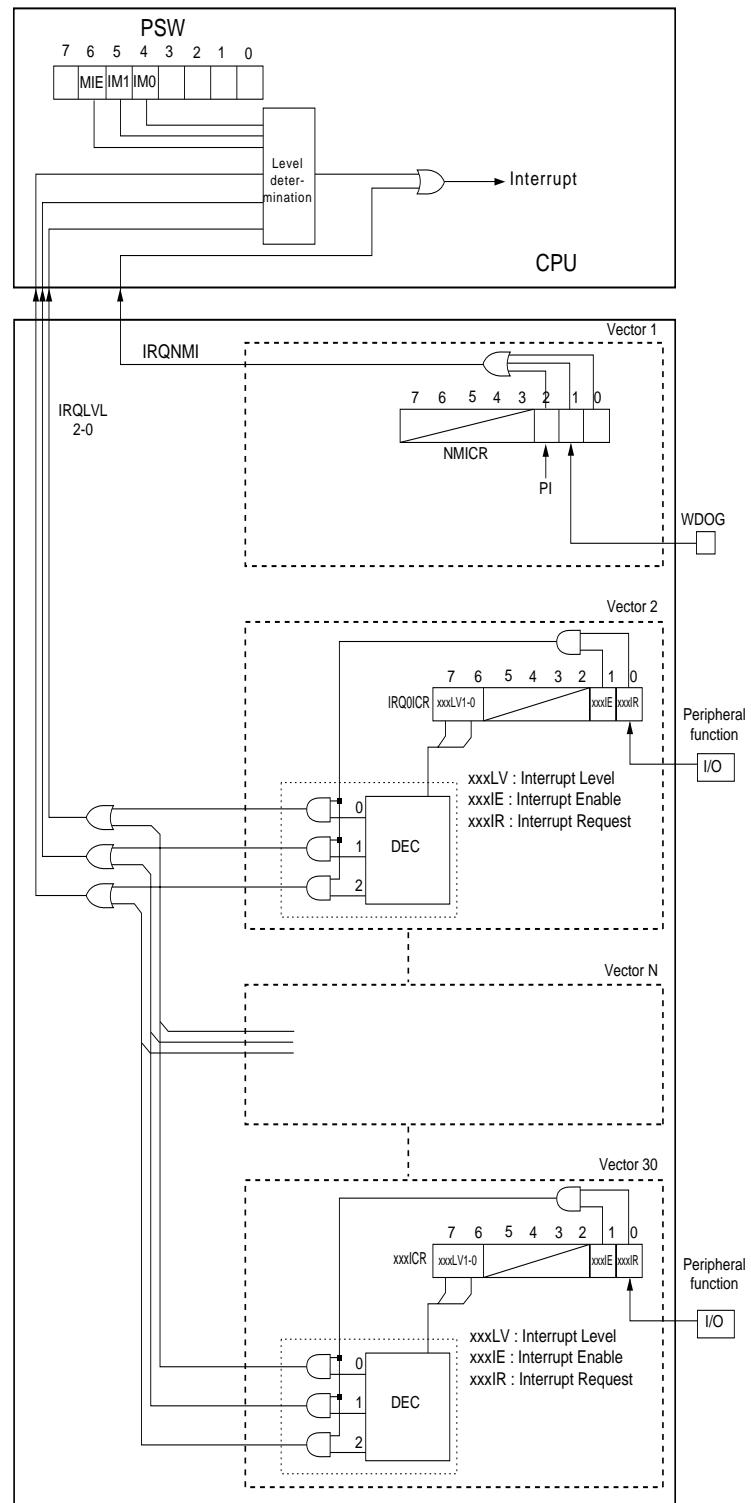


Figure:3.1.1 Interrupt Block Diagram

3.1.3 Operation

■ Interrupt Processing Sequence

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance determination (only maskable interrupt), interrupt acceptance (hardware processing), and return (RTI instruction). The program counter (PC) and processor status word (PSW) and hard addressing data (HA) are saved onto the stack, and program is branched to the address specified by the corresponding interrupt vector. An interrupt handler ends by restoring the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

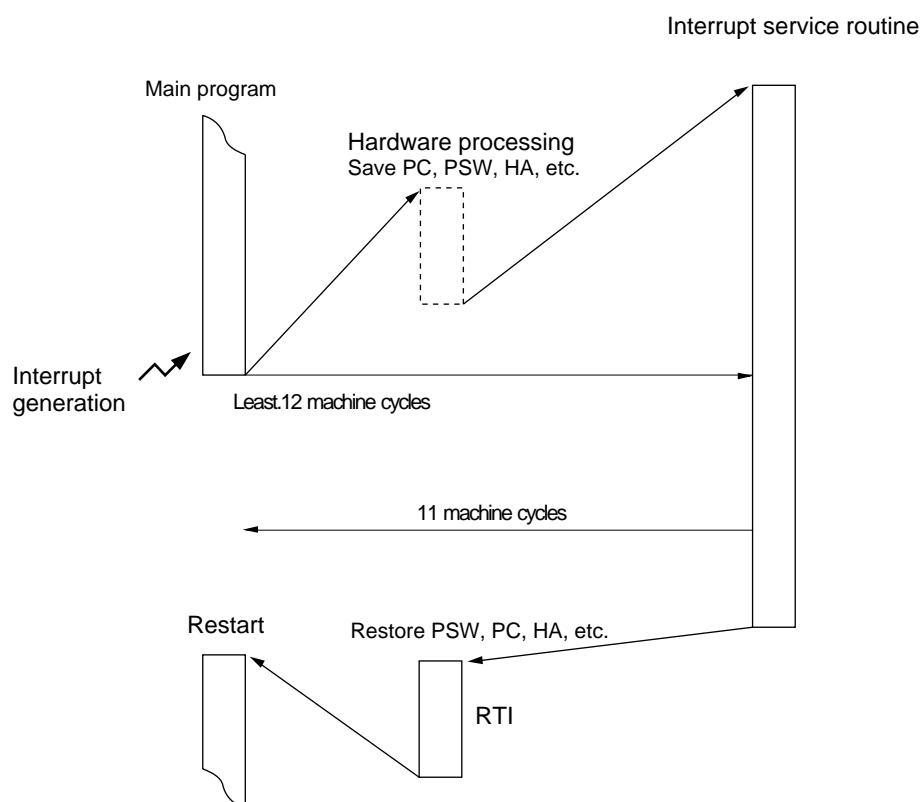


Figure:3.1.2 Interrupt Processing Sequence

The interrupt request flag (xxxIR) of maskable interrupt control register (xxxICR) is cleared by hardware when interrupt is accepted. the interrupt request flags of non-maskable interrupt control register (NMICR) is not cleared by hardware.

■ Interrupt Group and Vector Addresses

Table:3.1.2 shows the list of interrupt vector addresses and interrupt group.

Table:3.1.2 Interrupt Vector Addresses and Interrupt Group

Vector number	Vector addresses		Interrupt group (interrupt factor)	Control register (address)	
	IVBM = 0	IVBM = 1			
0	0x04000	0x00100	Reset	-	-
1	0x04004	0x00104	Non-maskable interrupt	NMI	NMICR 0x03FE1
2	0x04008	0x00108	External Interrupt 0	IRQ0	IRQ0ICR 0x03FE2
3	0x0400C	0x0010C	External Interrupt 1	IRQ1	IRQ1ICR 0x03FE3
4	0x04010	0x00110	External Interrupt 2	IRQ2	IRQ2ICR 0x03FE4
5	0x04014	0x00114	External Interrupt 3	IRQ3	IRQ3ICR 0x03FE5
6	0x04018	0x00118	External Interrupt 4	IRQ4	IRQ4ICR 0x03FE6
7	0x0401C	0x0011C	External Interrupt 5	IRQ5	IRQ5ICR 0x03FE7
8	0x04020	0x00120	Timer 0 interrupt	TM0IRQ	TM0ICR 0x03FE8
9	0x04024	0x00124	Timer 1 interrupt	TM1IRQ	TM1ICR 0x03FE9
10	0x04028	0x00128	Timer 2 interrupt	TM2IRQ	TM2ICR 0x03FEA
11	0x0402C	0x0012C	Timer 3 interrupt	TM3IRQ	TM3ICR 0x03FEB
12	0x04030	0x00130	Timer 4 interrupt	TM4IRQ	TM4ICR 0x03FEC
13	0x04034	0x00134	Timer 6 interrupt	TM6IRQ	TM6ICR 0x03FED
14	0x04038	0x00138	Time base interrupt	TBIRQ	TBICR 0x03FEE
15	0x0403C	0x0013C	Timer 7 interrupt	TM7IRQ	TM7ICR 0x03FEEF
16	0x04040	0x00140	Timer 7 compare 2-match interrupt	TM7OC2IRQ	TM7OC2ICR 0x03FF0
17	0x04044	0x00144	Timer 8 interrupt	TM8IRQ	TM8ICR 0x03FF1
18	0x04048	0x00148	Timer 8 compare 2-match interrupt	TM8OC2IRQ	TM8OC2ICR 0x03FF2
19	0x0404C	0x0014C	Timer 9 interrupt	TM9IRQ	TM9ICR 0x03FF3
20	0x04050	0x00150	Timer 9 compare 2-match interrupt	TM9OC2IRQ	TM9OC2ICR 0x03FF4
21	0x04054	0x00154	Reserved	-	Reserved 0x03FF5
22	0x04058	0x00158	Reserved	-	Reserved 0x03FF6
23	0x0405C	0x0015C	Serial 0 UART transmission interrupt	SC0TIRQ	SC0TICR 0x03FF7
24	0x04060	0x00160	Serial 1 UART transmission interrupt	SC1TIRQ	SC1TICR 0x03FF8
25	0x04064	0x00164	Serial 2 UART reception interrupt	SC2RIRQ	SC2RICR 0x03FF9
26	0x04068	0x00168	Serial 2 UART transmission interrupt	SC2TIRQ	SC2TICR 0x03FFA
27	0x0406C	0x0016C	Serial 3 UART transmission interrupt	SC3TIRQ	SC3TICR 0x03FFB
28	0x04070	0x00170	Serial 4 interrupt	SC4IRQ	SC4ICR 0x03FFC
29	0x04074	0x00174	A/D conversion interrupt	ADIRQ	ADICR 0x03FFD
30	0x04078	0x00178	Peripheral group interrupt	PERIIRQ	PERIICR 0x03FFE

■ Interrupt Level and Priority

This LSI allocated vector numbers and interrupt control registers (except reset interrupt) to each interrupt. The interrupt level (except reset interrupt, non-maskable interrupt) can be set by software, per each interrupt group. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. For example, if a vector 3 set to level 1 and a vector 4 set to level 1 request interrupt simultaneously, vector 3 will be accepted.

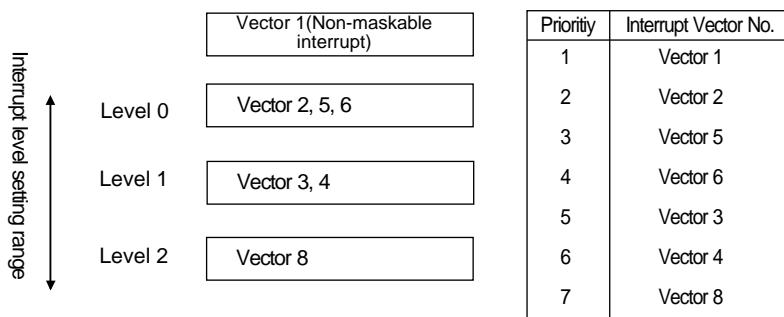


Figure:3.1.3 Interrupt Priority Outline

Table:3.1.3 Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt level
	IM1	IM0		
Mask level 0	0	0	Highest	Non-maskable interrupt (NMI) only
Mask level 1	0	1	High	NMI, level 0
Mask level 2	1	0	Low	NMI, level 0 to 1
Mask level 3	1	1	Lowest	NMI, level 0 to 2

■ Determination of Maskable Interrupt Acceptance

The following is the procedure from interrupt request input to acceptance.

1. The interrupt request flag (xxxIR) in the corresponding external interrupt control register (IRQnICR) and internal interrupt control register (xxxICR) are set to "1".
2. When the interrupt enable flag (xxxIE) corresponding to the interrupt request flag is "1", the information of the level set to the interrupt level flag (xxxLV1-0) is output to the CPU as an interrupt request signal.
3. The interrupt request is accepted if the output interrupt request signal has a higher priority than the level set in the interrupt mask level (IM1-0) of the processor status word (PSW) and the interrupt enable flag (MIE) of PSW is "1" (enabled).
4. After acceptance of an interrupt, the interrupt request flag (xxxIR) is cleared by hardware. However, the interrupt enable flag (xxxIE) is not cleared.

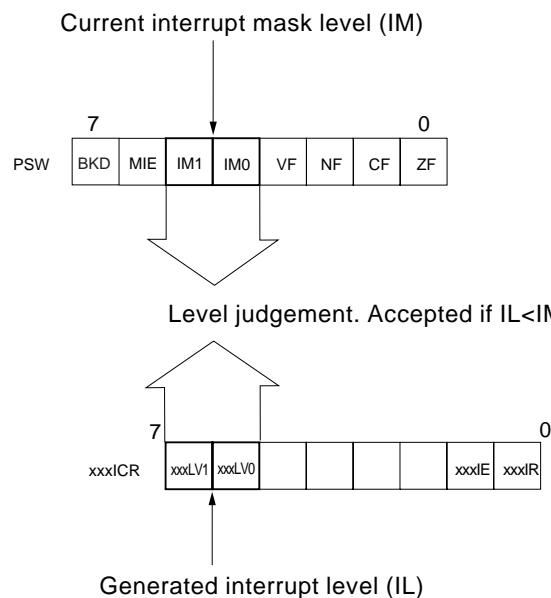


Figure:3.1.4 Determination of Interrupt Acceptance



Acceptance of an interrupt does not reset the corresponding interrupt enable flag (xxxIE) to "0".



After accept of an interrupt, interrupt of same source is disregarded until interrupt request flag (xxxIR) is cleared to "0" by hardware.

■ Maskable interrupt Enable (MIE) and Interrupt Mask level (IM1-0) in PSW

MIE = "0" and maskable interrupts are disabled when:

- MIE in the PSW is reset to "0" by a program
- BE instruction is executed. (BKD is reset and MIE is reset)
- Reset is detected.

MIE = "1" and maskable interrupts are enabled when:

- MIE in the PSW is reset to "1" by a program
- BD instruction is executed. (BKD is set and MIE is set)

The interrupt mask level (IM = IM1 - IM0) in the processor status word (PSW) changes when:

- The program alters it directly, A reset initializes it to 0 (00b), maskable interrupt is accepted (the interrupt level becomes the interrupt mask level).
- A reset initializes it to 0 (00b).
- Maskable interrupt is accepted (the interrupt level becomes the interrupt mask level).
- Execution of the RTI instruction at the end of an interrupt service routine restores the processor status word (PSW) and thus the previous interrupt mask level.
- Non-Maskable interrupt is accepted (it to 0 (00b)).



The maskable interrupt enable (MIE) flag of processor status word (PSW) is not set to "0" when accepting interrupts.



Non-maskable interrupts have priority over maskable ones.



As for the BE instruction and BD instruction, refer to the appendices [18.4 Instruction Set] at the end of the book.

■ Interrupt Acceptance Operation (Hardware Processing)

When accepting an interrupt, this LSI hardware saves the handy addressing data, the return address from the program counter, and the processor status word (PSW) to the stack and branches program to the interrupt handler using the starting address in the vector table. The following is the hardware processing sequence invoked by interrupt acceptance.

1. the stack pointer (SP) is updated.

$SP - 6 \rightarrow SP$

2. The contents of the program counter (PC)-i.e., the return address- are saved to the stack.

$PC\ bits\ 7\ to\ 0 \rightarrow Address\ (SP + 1)$

$PC\ bits\ 15\ to\ 8 \rightarrow Address\ (SP + 2)$

$PC\ bits\ 19\ to\ 16,\ and\ H \rightarrow Address\ (SP + 3)$

3. The contents of the handy addressing data (HA) are saved to the stack.

$Lower\ half\ of\ HA \rightarrow Address\ (SP + 4)$

$Upper\ half\ of\ HA \rightarrow Address\ (SP + 5)$

4. The contents of the PSW are saved to the stack.

$PSW \rightarrow Address\ (SP)$

5. The interrupt level (xxxLVn) for the interrupt is copied to the interrupt mask IMn in the PSW.

$Interrupt\ level\ (xxxLVn) \rightarrow IMn$

6. BKD flag of the PSW is reset (When accepting interrupts, the bank register always address the first 64KB.)

7. The hardware branches program to the address in the vector table.

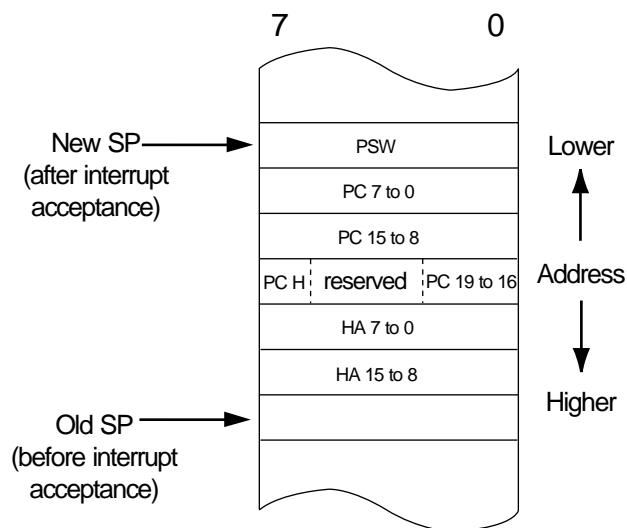


Figure:3.1.5 Stack Operation during Interrupt Acceptance

■ Interrupt Return Operation (RTI Instruction)

An interrupt handler ends by restoring the contents of any registers saved to the stack during processing by the POP instruction and other means, and the RTI instruction restores the program to the point at execution was interrupted.

The following is the processing sequence invoked by the RTI instruction.

1. The contents of the PSW are restored from the stack. (SP)
2. The contents of the program counter (PC) -i.e., the return address- are restored from the stack. (SP + 1 to SP + 3)
3. The contents of the handy addressing data (HA) are restored from the stack. (SP + 4, SP+ 5)
4. The stack pointer is updated. $SP+6 \rightarrow SP$
5. Execution branches program to the address in the program counter.

The handy addressing data is an internal register used by the handy addressing function. The hardware saves its contents to the stack to prevent the interrupt from interfering with operation of the function.



Registers such as data register, or address register are not saved, so that PUSH instruction from program should be used to save them onto stack, if necessary.

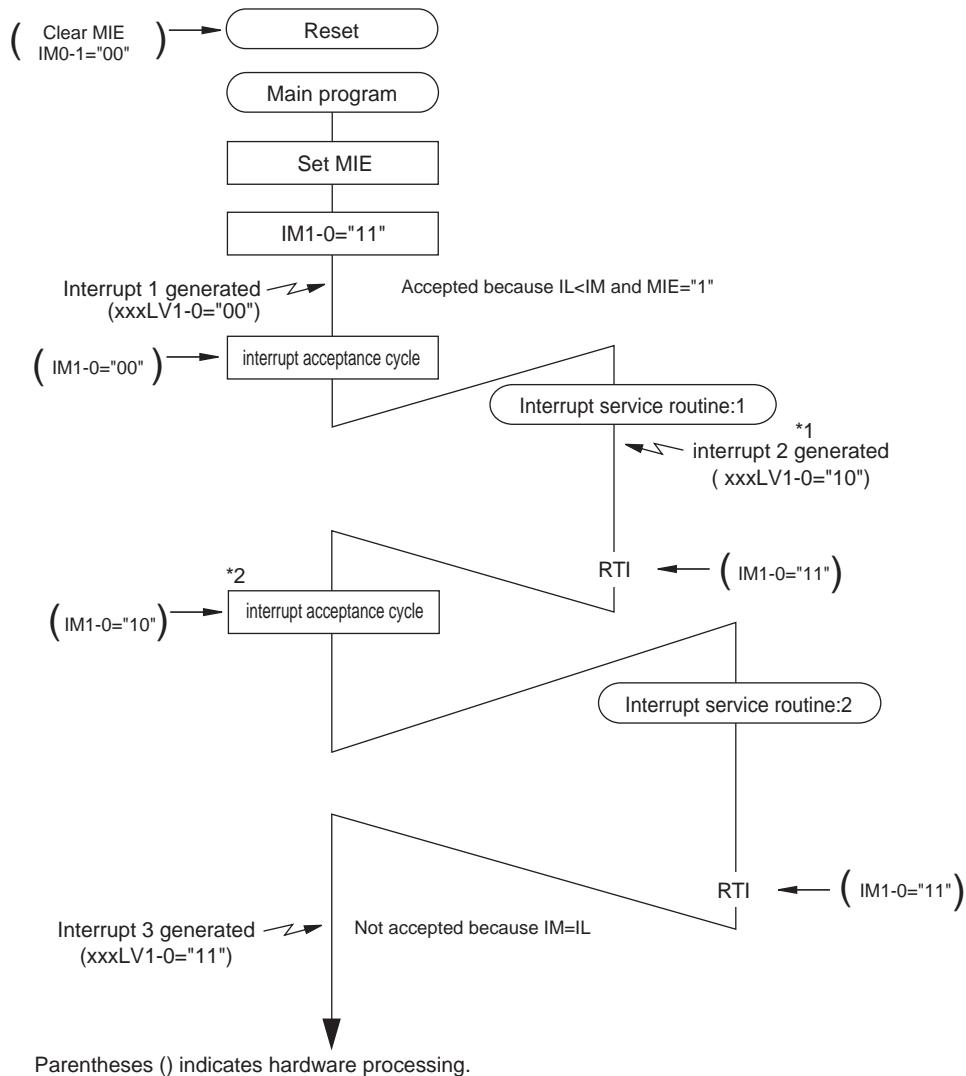


The address bp6 to bp4, when program counter (PC [bit19 to bit16, bitH]) are saved to the stack, are reserved. Do not change it by program.

■ Maskable Interrupt

The following is the processing sequence when the lower priority level interrupt occurs while processing the higher priority level interrupt.

(Higher priority level interrupt: $\text{xxxLV1-0} = "00"$, Lower priority level interrupt: $\text{xxxLV1-0} = "10"$)



*1: If during the processing of the first interrupt, an interrupt request with an interrupt level (IL) numerically lower than the interrupt mask (IM) arrives, it is accepted as a nested interrupt. If $IL > IM$, however, the interrupt is not accepted.

*2: The second interrupt, postponed because its interrupt level (IL) was numerically greater than the interrupt mask (IM) for the first interrupt service routine, is accepted when the first interrupt handler returns.

Figure:3.1.6 Processing Sequence for Maskable Interrupts

■ Multiplex Interrupt of Maskable Interrupt

When this LSI accepts an interrupt, it automatically disables acceptance of subsequent interrupts with the same or lower priority level. When the hardware accepts an interrupt, it copies the interrupt level (xxxLVn) for the interrupt to the interrupt mask (IM) in the PSW. As a result, subsequent interrupts with the same or lower priority levels are automatically masked. Only interrupts with higher priority levels are accepted. The net result is that interrupts are normally processed in decreasing order of priority. It is, however, possible to alter this arrangement.

1. To disable interrupt nesting
 - Reset the MIE bit in the PSW to "0".
 - Raise the priority level of the interrupt mask (IM) in the PSW.
2. To enable interrupts with lower priority than the currently accepted interrupt
 - Lower the priority level or the interrupt mask (IM) in the PSW.



Multiplex interrupts are only enabled for interrupts with levels higher than the PSW interrupt mask level (IM).



It is possible to forcibly rewrite IM to accept an interrupt with a priority lower than the interrupt being processed, but be careful of stack overflow.



Do not operate the maskable interrupt control register (xxxICR) when multiple interrupts are enabled. If operation is necessary, first clear the PSW MIE flag.

Figure:3.1.7 shows the processing sequence of the multiple interrupt.

(multiple interrupt: $\text{xxxLV1 to 0} = "10"$, $\text{xxxLV1 to 0} = "00"$)

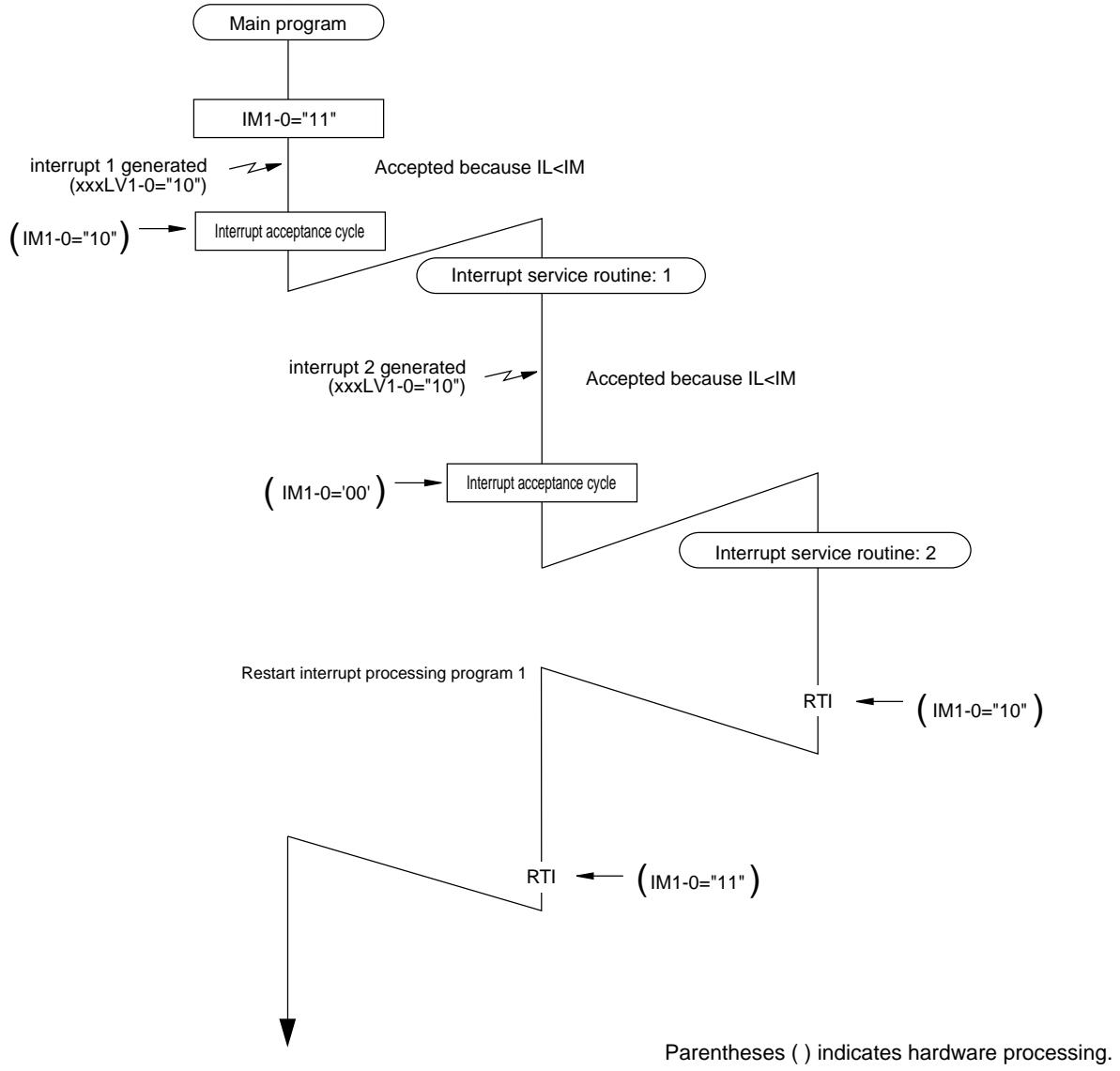


Figure:3.1.7 Processing Sequence for Maskable Interrupts

■ Multiple Interrupt of Non-maskable

On the acceptance of nmi interrupt, when other nmi interrupt factor is generated, this interrupt is processed right away. Also, when the same nmi interrupt factor is generated before nmi interrupt flag is be soft cleared, it is not accepted. (Unless nmi interrupt clears the flag by the soft, the following same nmi interrupt is not accepted and valid.)

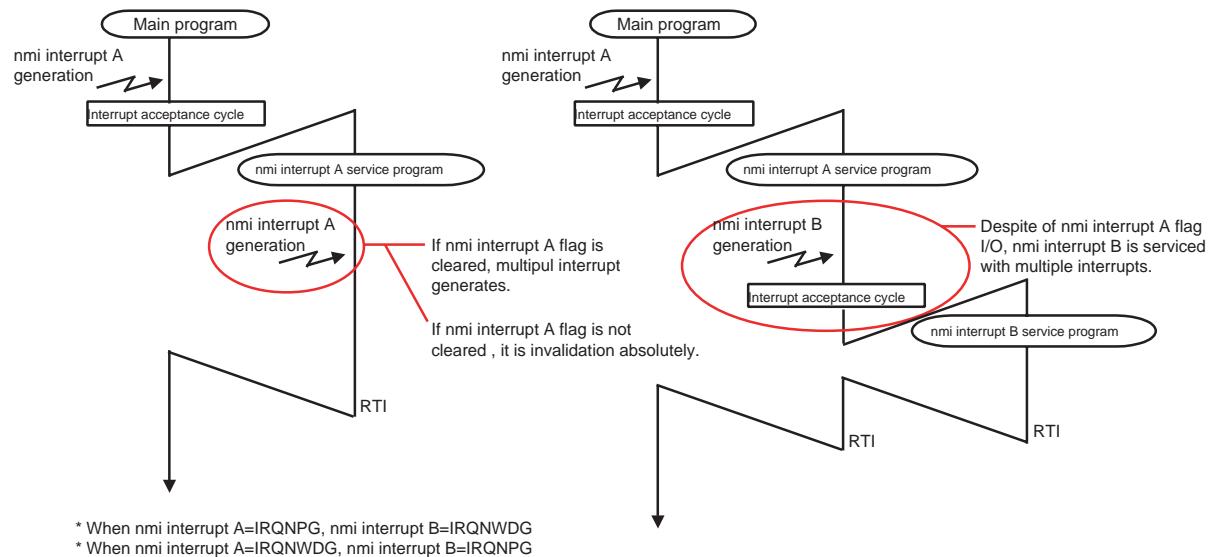


Figure:3.1.8 Processing Sequence for Non-maskable Interrupts

3.1.4 Maskable Interrupt Control Register Setup

■ Interrupt Request Flag (IR) Setup by the Software

The interrupt request flag is operated by the hardware. That is set to "1" when any interrupt factor is generated, and cleared to "0" when the interrupt is accepted. If you want to operate it by the software, the IRWE flag of MEMCTR should be set to "1".

■ Maskable Interrupt Control Register Setup Procedure

A setup procedure of the flags of maskable interrupt control register set by the hardware and the software shows as follows;

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp6:MIE =0	(1) Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2) Select the interrupt factor.	(2) Select the interrupt factor such as interrupt edge selection, or timer interrupt cycle change.
(3) Enable the interrupt request flag to be rewritten. MEMCTR(0x03F01) bp2:IRWE =1	(3) Set the IRWE flag of MEMCTR to enable the interrupt request flag to be rewritten. This is necessary only when the interrupt request flag is changed by the software.
(4) Rewrite the interrupt request flag. xxxICR bp0:xxxIR	(4) Rewrite the interrupt request flag (xxxIR) of the interrupt control register (xxxICR). (the flag may already be set, so clear it.)
(5) Disable the interrupt request flag to be rewritten. MEMCTR(0x03F01) bp2:IRWE =0	(5) Clear the IRWE flag so that interrupt request flag can not be rewritten by the software.
(6) Set the interrupt level. xxxICR bp7-6:xxxLV1-0 PSW bp5-4:IM1-0	(6) Set the interrupt level by the xxxLV1 - 0 flag of the interrupt control register (xxxICR). Set the IM1 - 0 flag of PSW.
(7) Enable the interrupt. xxxICR bp1:xxxIE =1	(7) Set the xxxIE flag of the interrupt control register (xxxICR) to enable the interrupt.
(8) Enable all maskable interrupts. PSW bp6:MIE =1	(8) Enable all maskable interrupts. PSW bp6:MIE =1



Interrupt request flag of interrupt control register is set by interrupt generation, the edge switching and others, regardless of the xxxIE flag. Clear the flag referring to the setup procedures (3) to (5).



Always set IRWE flag of memory control register (MEMCTR) to "0" except in writing IR with software. If operating interrupt control register xxxICR with software in setting IRWE flag to "1", the interrupt request flag which is set to "1" by interrupt source may be cleared to "0". For example, if giving the bit operation order to interrupt control register xxxICR, it executes bit operation to read-out 1 byte and writes it back. When the interrupt source occurs between reading out and writing back, IR flag may be cleared to "0" by mistake and then the interrupt source is missing. If IRWE flag is set to "0", the interrupt source will not be missing.



Make processor status word (PSW) and maskable interrupt enable flag (MIE) of prohibited all maskable interrupts (Set MIE flag to "0") before writing to interrupt control register (xxxICR). If writing to interrupt control register with setting MIE flag to "1", we can not guarantee normal operation.

3.1.5 Internal Interrupt Extended Interrupt Control Register Setup

■ Interrupt Request Flag (IRQEXPDT) Setup by the Software

The internal interrupt extended interrupt request flag is set by hardware/software and cleared by software. When any interrupt factor is generated, it is set to "1", and the interrupt is accepted.

When an interrupt factor corresponding to the internal interrupt extended input control register (IRQEXPEN) setting is generated and "1" is written in the corresponding flag, a maskable interrupt factor will be generated.

Setting this flag to "1" by software also generates an interrupt.

Unlike the xxxIR flag of the interrupt control register (xxxICR), this flag is not cleared by hardware. In order to accept an interrupt again, clear the appropriate flag by writing "1" within the interrupt process program.

The following shows the flag status, write data and flag status after writing.

Flag status	Write data	Flag after writing	Flag change
0	0	0	No change
0	1	1	Flag set
1	0	1	No change
1	1	0	Flag clear



To initialize (clear) all flags, read the register contents first, and write the contents to the register.

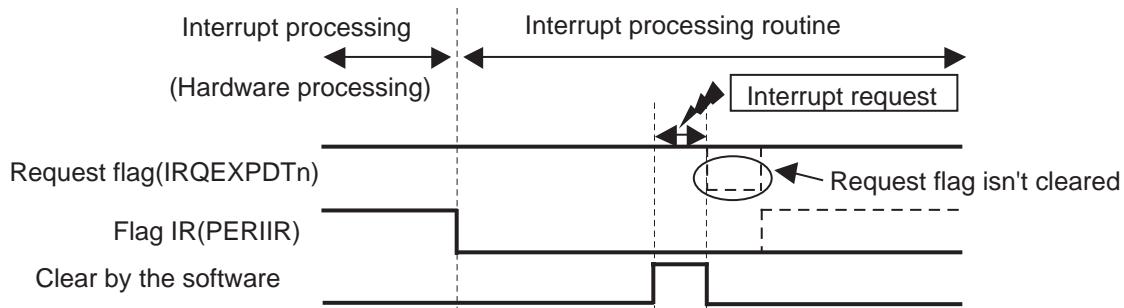


The internal interrupt extended interrupt request flag is not cleared by hardware. Clear the appropriate flag by writing "1" within the interrupt process program to accept an interrupt again.



When interrupt request of same bit and above-mentioned request flag by the software is generated at the same time after the request flag was set, the set of request flag is given to priority and isn't cleared by the software(request flag is setting). At the time, IR flag (PERIIR) isn't set.

When the request flag is set, interrupt request of same bit isn't accepted. After the request flag is cleared by the software, has to confirm that request flag was cleared.



■ Interrupt Flag Setup Procedure

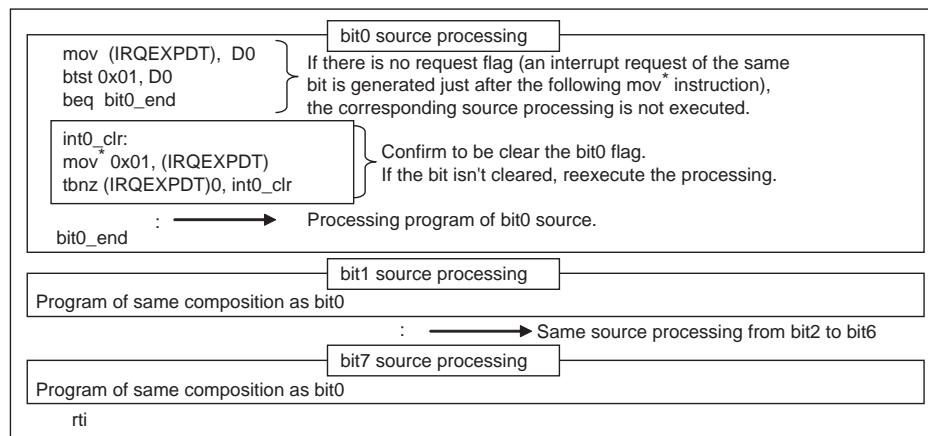
The following shows a setup procedure of the internal interrupt extended interrupt control register;

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp6:MIE =0	(1) Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2) Enable writing of the interrupt request flag. MEMCTR(0x03F01) bp2:IRWE =1	(2) Set the IRWE flag of the memory control register (MEMCTR) to enable writing of the interrupt request flag by software. This is necessary only when the interrupt request flag is changed by software.
(3) Disable the interrupt PERIICR(0x03FFE) bp1:PERIIE =0	(3) Disable the interrupt by clearing the PERIIE flag of the interrupt control register (PERIICR).
(4) Set the extended input IRQEXPEN(0x03F4E) bp6-0:IRQEXPEN6-0 =1011011	(4) Enable the extended interrupt by setting the IRQEXPEN6-0 flags of the internal interrupt extended input control register (IRQEXPEN).
(5) Clear the extended interrupt request flag IRQEXPDT(0x03F4F) bp6-0:IRQEXPDT6-0	(5) Read the IRQEXPDT6-0 flags of the internal interrupt extended interrupt factor holding register (IRQEXPDT) and write the contents to clear the flags. It clears by this method because there is a possibility that internal interrupt extended interrupt factor holding register has already been set.
(6) Clear the interrupt request flag PERIIRQ(0x03FFE) bp0:PERIIR =0	(6) Clear the PERIIR flag of the interrupt control register (PERIIRQ). It clears by this method because there is a possibility that interrupt request flag has already been set.
(7) Disable writing of the interrupt request flag. MEMCTR(0x03F01) bp2:IRWE =0	(7) Clear the IRWE flag to disable writing of the interrupt request flag by software.
(8) Enable the interrupt PERIICR(0x03FFE) bp1:PERIIE =1	(8) Set the PERIIE flag of the interrupt control register (PERIIRQ) to enable the interrupt.
(9) Enable all maskable interrupts. PSW bp6:MIE =1 [Interrupt acceptance]	(9) Set the MIE flag of the PSW to enable the maskable interrupt. Read the flags of the internal interrupt extended interrupt factor holding register (IRQEXPDT) and determine the interrupt source by software.



Extended interrupt request flag (IRQEXPDT) is set by interrupt generation regardless of setting of internal interrupt extended input control register (IRQEXPEN). Clear the flag referring to the setup procedures (3) to (5).

■ Example of Internal Interrupt Extended Interrupt Processing Program



3.2 Control Registers

3.2.1 Registers List

Table:3.2.1 Interrupt Control Registers

Register	Address	R/W	Functions	Page
NMICR	0x03FE1	R/W	Non-maskable interrupt control register	III-24
IRQ0ICR	0x03FE2	R/W	External interrupt 0 control register	III-25
IRQ1ICR	0x03FE3	R/W	External interrupt 1 control register	III-25
IRQ2ICR	0x03FE4	R/W	External interrupt 2 control register	III-25
IRQ3ICR	0x03FE5	R/W	External interrupt 3 control register	III-25
IRQ4ICR	0x03FE6	R/W	External interrupt 4 control register	III-25
IRQ5ICR	0x03FE7	R/W	External interrupt 5 control register	III-25
TM0ICR	0x03FE8	R/W	Timer 0 interrupt control register	III-26
TM1ICR	0x03FE9	R/W	Timer 1 interrupt control register	III-26
TM2ICR	0x03FEA	R/W	Timer 2 interrupt control register	III-26
TM3ICR	0x03FEB	R/W	Timer 3 interrupt control register	III-26
TM4ICR	0x03FEC	R/W	Timer 4 interrupt control register	III-26
TM6ICR	0x03FED	R/W	Timer 6 interrupt control register	III-26
TBICR	0x03FEE	R/W	Time base interrupt control register	III-27
TM7ICR	0x03FEF	R/W	Timer 7 interrupt control register	III-28
TM7OC2ICR	0x03FF0	R/W	Timer 7 compare 2-match interrupt control register	III-29
TM8ICR	0x03FF1	R/W	Timer 8 interrupt control register	III-30
TM8OC2ICR	0x03FF2	R/W	Timer 8 compare 2-match interrupt control register	III-31
TM9ICR	0x03FF3	R/W	Timer 9 interrupt control register	III-32
TM9OC2ICR	0x03FF4	R/W	Timer 9 compare 2-match interrupt control register	III-33
Reserved	0x03FF5/6	R/W	Reserved register	III-34
SC0TICR	0x03FF7	R/W	Serial 0 UART transmission interrupt control register	III-35
SC1TICR	0x03FF8	R/W	Serial 1 UART transmission interrupt control register	III-35
SC2RICR	0x03FF9	R/W	Serial 2 UART reception interrupt control register	III-36
SC2TICR	0x03FFA	R/W	Serial 2 UART transmission interrupt control register	III-37
SC3TICR	0x03FFB	R/W	Serial 3 UART transmission interrupt control register	III-38
SC4ICR	0x03FFC	R/W	Serial 4 interrupt control register	III-39
ADICR	0x03FFD	R/W	A/D conversion interrupt control register	III-40
PERIICR	0x03FFE	R/W	Peripheral group interrupt control register	III-41
IRQEXPEN	0x03F4E	R/W	Internal interrupt extended input control register	III-42
IRQEXPDT	0x03F4F	R/W	Internal interrupt extended interrupt factor holding register	III-43

R/W: Readable / Writable.



If the interrupt level flag (xxxLVn) is set to "level 3", its vector is disabled, regardless of interrupt enable flag and interrupt request flag.



Make processor status word (PSW) and mascable interrupt enable flag (MIE) of prohibited all mascable interrupts (Set MIE flag to "0") before writing to interrupt control register (xxx-ICR). If writing to interrupt control register with setting MIE flag to "1", we can not guarantee normal operation.

3.2.2 Interrupt Control Registers

The interrupt control registers include the non-maskable interrupt control register (NMICR), and maskable interrupt control register. The maskable interrupt control register consists of the external interrupt control register (IRQnICR) and the internal interrupt control registers (xxxICR).

■ Non-maskable Interrupt Control Register (NMICR:0x03FE1)

The non-maskable interrupt control register (NMICR) is stored in the non maskable interrupt request. When the non-maskable interrupt request is generated, the interrupt is accepted regardless of the interrupt mask level (IMn) of PSW. The hardware then branches program to the address stored at location 0x04004 in the interrupt vector table. The watchdog timer overflow interrupt request flag (IRQNWDG) is set to "1" when the watchdog timer overflows. The program interrupt request flag (IRQNPG) is set to "1" when the undefined instruction is executed.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	IRQNPG	IRQNWDG	Reserved
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
2	IRQNPG	Program interrupt request flag 0:No interrupt request 1:Interrupt request generated
1	IRQNWDG	Watchdog interrupt request flag 0:No interrupt request 1:Interrupt request generated
0	Reserved	Always set to "0" *



When the undefined instruction is going to be executed, this LSI generates the non-maskable interrupt at the same time of the setting of the program interrupt request flag IRQNPG.
When the setting of the IRQNPG flag is confirmed by the non-maskable interrupt process program, the soft reset is recommended by outputting "0" to the reset pin (P27).



Always set "0" to the bp denoted by *.

■ External Interrupt 0 to 5 Control Registers (IRQ0ICR to IRQ5ICR:0x03FE2 to 0x03FE7)

External interrupt 0 to 5 control registers (IRQ0ICR to IRQ5ICR) control interrupt levels of external interrupts 0 to 5, active edge, interrupt enable, and interrupt request. Interrupt control registers should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	IRQnLV1	IRQnLV0	REDGn	-	-	-	IRQnIE	IRQnIR
At reset	0	0	0	-	-	-	0	0
Access	R/W	R/W	R/W	-	-	-	R/W	R/W

bp	Flag	Description
7-6	IRQnLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5	REDGn	External interrupt valid edge flag (at the standby mode) 0 : Falling edge (low level) 1 : Rising edge (high level)
4-2	-	-
1	IRQnIE	External interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	IRQnIR	External interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Timer 0 to 4, 6 Interrupt Control Registers (TM0ICR to TM4ICR, TM6ICR:0x03FE8 to 0x03FED)

Timer 0 to 4, 6 interrupt control registers (TM0ICR to TM4ICR, TM6ICR) control interrupt levels of timer 0 to 4, 6 interrupts, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TMnLV1	TMnLV0	-	-	-	-	TMnIE	TMnIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TMnLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TMnIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TMnIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Time Base Interrupt Control Register (TBICR:0x03FEE)

Time base interrupt control register (TBICR) controls interrupt level of time base interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TBLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TBIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TBIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Timer 7 Interrupt Control Register (TM7ICR:0x03FEF)

Timer 7 interrupt control register (TM7ICR) controls interrupt level of timer 7 interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TM7LV1	TM7LV0	-	-	-	-	TM7IE	TM7IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TM7LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TM7IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TM7IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Timer 7 Compare 2-Match Interrupt Control Register (TM7OC2ICR:0x03FF0)

Timer 7 compare 2-match interrupt control register (TM7OC2ICR) controls interrupt level of timer 7 compare 2-match interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TM7OC2LV1	TM7OC2LV0	-	-	-	-	TM7OC2IE	TM7OC2IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TM7OC2LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TM7OC2IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TM7OC2IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Timer 8 Interrupt Control Register (TM8ICR:0x03FF1)

Timer 8 interrupt control register (TM8ICR) controls interrupt level of timer 8 interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TM8LV1	TM8LV0	-	-	-	-	TM8IE	TM8IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TM8LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TM8IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TM8IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Timer 8 Compare 2-Match Interrupt Control Register (TM8OC2ICR:0x03FF2)

Timer 8 compare 2-match interrupt control register (TM8OC2ICR) controls interrupt level of timer 8 compare 2-match interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TM8OC2LV1	TM8OC2LV0	-	-	-	-	TM8OC2IE	TM8OC2IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TM8OC2LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TM8OC2IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TM8OC2IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated



Do not word access to timer 8 compare 2-match interrupt control register (TM8OC2ICR)

■ Timer 9 Interrupt Control Register (TM9ICR:0x03FF3)

Timer 9 interrupt control register (TM9ICR) controls interrupt level of timer 9 interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TM9LV1	TM9LV0	-	-	-	-	TM9IE	TM9IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TM9LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TM9IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TM9IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Timer 9 Compare 2-Match Interrupt Control Register (TM9OC2ICR:0x03FF4)

Timer 9 compare 2-match interrupt control register (TM9OC2ICR) controls interrupt level of timer 9 compare 2-match interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	TM9OC2LV1	TM9OC2LV0	-	-	-	-	TM9OC2IE	TM9OC2IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	TM9OC2LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	TM9OC2IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	TM9OC2IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Reserved Register (Reserved:0x03FF5, 0x03FF6)

Always set to “0”.

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	-	-	-	-	Reserved	Reserved
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	Reserved	Always set to “0”.
5-2	-	-
1-0	Reserved	Always set to “0”.



Always set to “0”.

- Serial 0, 1 UART Transmission Interrupt Control Registers (SC0TICR to SC1TICR:0x03FF7 to 0x03FF8)

Serial 0, 1 UART transmission interrupt control registers (SC0TICR to SC1TICR) control interrupt levels of Serial 0, 1 UART transmission interrupts, interrupt enable, and interrupt request. Interrupt control registers should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	SCnTLV1	SCnTLV0	-	-	-	-	SCnTIE	SCnTIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	SCnTLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	SCnTIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	SCnTIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Serial 2 UART Reception Interrupt Control Register (SC2RICR:0x03FF9)

Serial 2 UART reception interrupt control register (SC2RICR) controls interrupt level of serial 2 UART reception interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	SC2RLV1	SC2RLV0	-	-	-	-	SC2RIE	SC2RIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	SC2RLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	SC2RIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	SC2RIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Serial 2 UART Transmission Interrupt Control Register (SC2TICR:0x03FFA)

Serial 2 UART transmission interrupt control register (SC2TICR) controls interrupt level of serial 2 UART transmission interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	SC2TLV1	SC2TLV0	-	-	-	-	SC2TIE	SC2TIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	SC2TLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	SC2TIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	SC2TIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Serial 3 UART Transmission Interrupt Control Register (SC3TICR:0x03FFB)

Serial 3 UART transmission interrupt control register (SC3TICR) controls interrupt level of serial 3 UART transmission interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	SC3TLV1	SC3TLV0	-	-	-	-	SC3TIE	SC3TIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	SC3TLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	SC3TIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	SC3TIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Serial 4 Interrupt Control Register (SC4ICR:0x03FFC)

Serial 4 interrupt control register (SC4ICR) controls interrupt level of serial 4 interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	SC4LV1	SC4LV0	-	-	-	-	SC4IE	SC4IR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	SC4LV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	SC4IE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	SC4IR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ A/D Conversion Interrupt Control Register (ADICR:0x03FFD)

A/D conversion interrupt control register (ADICR) controls interrupt level of A/D conversion interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	ADLV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	ADIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	ADIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated

■ Peripheral Function Group Interrupt Control Register (PERIICR:0x03FFE)

Peripheral group interrupt control register (PERIICR) controls interrupt level of peripheral group interrupt, interrupt enable, and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	PERILV1	PERILV0	-	-	-	-	PERIIE	PERIIR
At reset	0	0	-	-	-	-	0	0
Access	R/W	R/W	-	-	-	-	R/W	R/W

bp	Flag	Description
7-6	PERILV1-0	Interrupt level flag This flag sets the interrupt level 0 to 3 for interrupt requests.
5-2	-	-
1	PERIIE	Interrupt enable flag 0 : Disable interrupt 1 : Enable interrupt
0	PERIIR	Interrupt request flag 0 : No interrupt request 1 : Interrupt request generated



Peripheral Function Group Interrupt can not be used as a returning source from the standby mode.

■ Internal Interrupt Extended Input Control Register (IRQEXPEN:0x03F4E)

Internal interrupt extended input control register (IRQEXPEN) controls factor of peripheral group interrupt. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	Reserved	IRQEXPEN6	IRQEXPEN5	IRQEXPEN4	IRQEXPEN3	IRQEXPEN2	IRQEXPEN1	IRQEXPEN0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0". *
6	IRQEXPEN6	ATC1 interrupt enable flag 0: Disable 1: Enable
5	IRQEXPEN5	ATC0 interrupt enable flag 0: Disable 1: Enable
4	IRQEXPEN4	Serial 5 interrupt enable flag 0: Disable 1: Enable
3	IRQEXPEN3	Serial 4 stop condition interrupt enable flag 0: Disable 1: Enable
2	IRQEXPEN2	Serial 3 UART reception interrupt enable flag 0: Disable 1: Enable
1	IRQEXPEN1	Serial 1 UART reception interrupt enable flag 0: Disable 1: Enable
0	IRQEXPEN0	Serial 0 UART reception interrupt enable flag 0: Disable 1: Enable



Peripheral Function Group Interrupt can not be used as a returning source from the standby mode.



Always set "0" to the bp denoted by *.

■ Internal Interrupt Extended Interrupt Factor Holding Register (IRQEXPDT:0x03F4F)

Internal interrupt extended interrupt factor holding register (IRQEXPEN) holds a factor of peripheral group interrupt. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". Refer to 3.1.4 for the setting procedure of the flags.

bp	7	6	5	4	3	2	1	0
Flag	Reserved	IRQEXPDT6	IRQEXPDT5	IRQEXPDT4	IRQEXPDT3	IRQEXPDT2	IRQEXPDT4	IRQEXPDT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0". *
6	IRQEXPDT6	ATC1 interrupt request flag 0 : No interrupt request 1 : Interrupt request generated
5	IRQEXPDT5	ATC0 interrupt request flag 0 : No interrupt request 1 : Interrupt request generated
4	IRQEXPDT4	Serial 5 interrupt request flag 0 : No interrupt request 1 : Interrupt request generated
3	IRQEXPDT3	Serial 4 stop condition interrupt request flag 0 : No interrupt request 1 : Interrupt request generated
2	IRQEXPDT2	Serial 3 UART reception interrupt request flag 0 : No interrupt request 1 : Interrupt request generated
1	IRQEXPDT1	Serial 1 UART reception interrupt request flag 0 : No interrupt request 1 : Interrupt request generated
0	IRQEXPDT0	Serial 0 UART reception interrupt request flag 0 : No interrupt request 1 : Interrupt request generated



Peripheral Function Group Interrupt can not be used as a returning source from the standby mode.

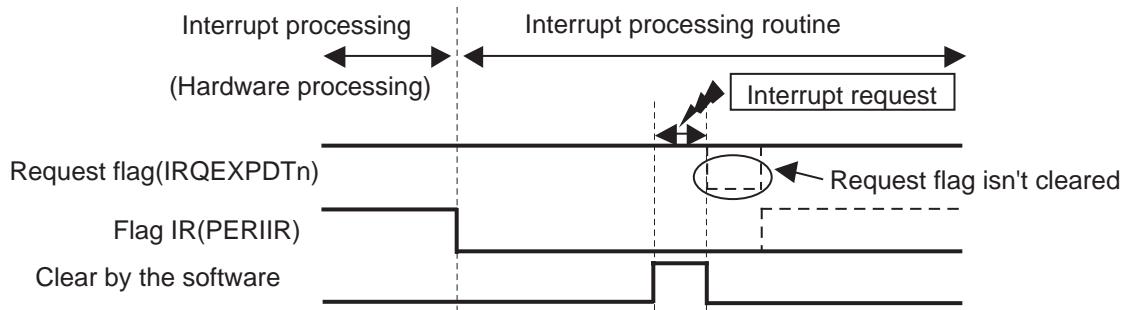


Always set "0" to the bp denoted by *.



When interrupt request of same bit and above-mentioned request flag by the software is generated at the same time after the request flag was set, the set of request flag is given to priority and isn't cleared by the software(request flag is setting). At the time, IR flag (PERIIR) isn't set.

When the request flag is set, interrupt request of same bit isn't accepted. After the request flag is cleared by the software, has to confirm that request flag was cleared.



3.2.3 Internal Interrupt Extended Interrupt Interface Block Diagram

■ Internal Interrupt Extended Interrupt Interface Block Diagram

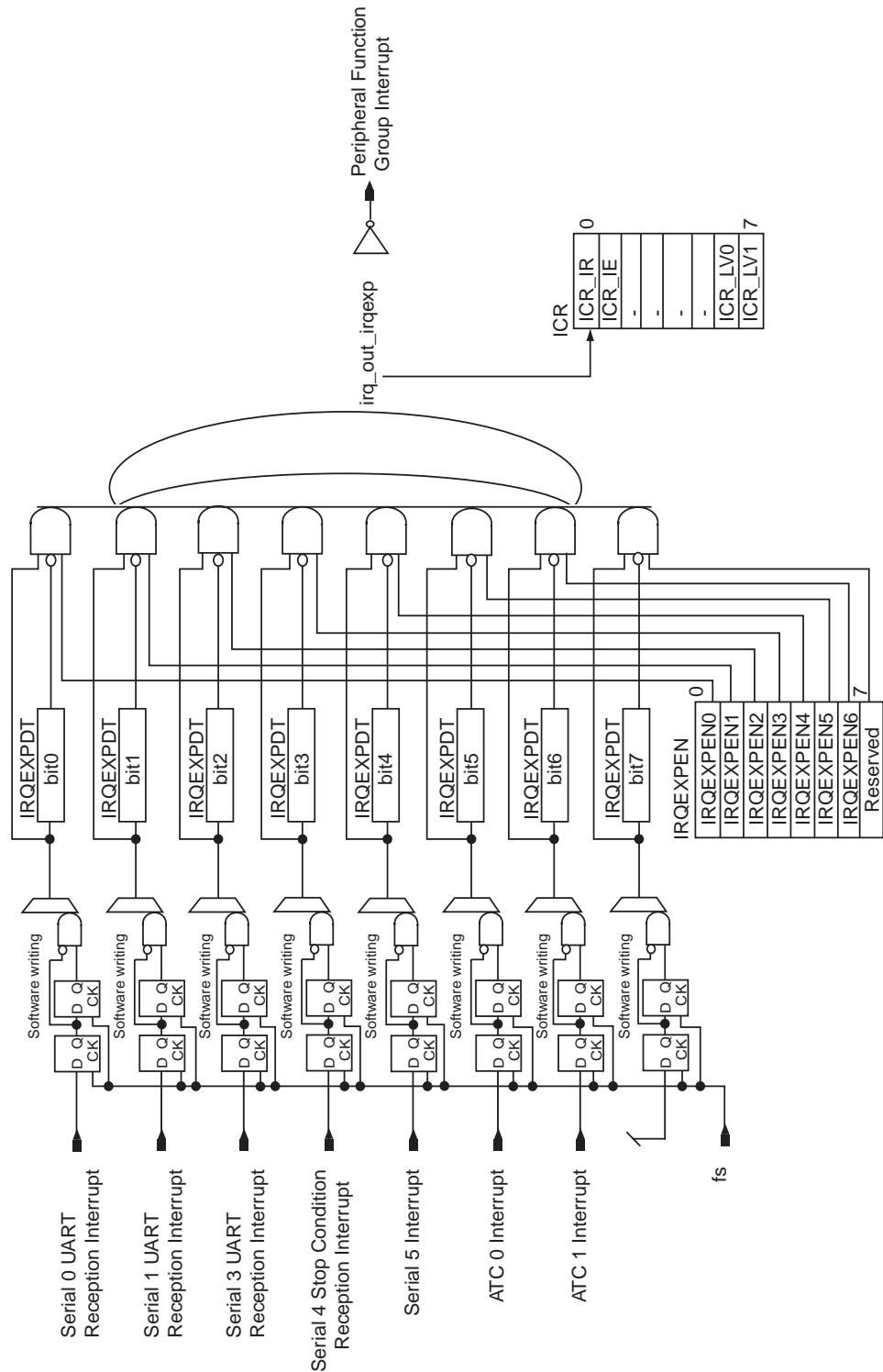


Figure:3.2.1 Internal Interrupt Extended Interrupt Interface Block Diagram

3.3 External Interrupts

There are 6 external interrupts in this LSI. The circuit (external interrupt interface), operates the external interrupt input signal, is built-in between the external interrupt input pin and the external interrupt block. This external interrupt interface can manage to do with any kind of external interrupts.

3.3.1 Overview

Table:3.3.1 shows the list of functions which external interrupts 0 to 5 are used.

Table:3.3.1 External Interrupt Functions

	External interrupt input pin	Programmable active edge interrupt	Both edges interrupt	built-in Noise filter	Sampling count	AC zero cross detection	Key input interrupt	Level interrupt
External interrupt 0	P20	O	-	O	-	O	-	-
External interrupt 1	P21	O	-	O	-	O	-	-
External interrupt 2	P22	O	O	O	O	-	-	O
External interrupt 3	P23	O	O	O	O	-	-	O
External interrupt 4	P24	O	O	O	-	-	-	O
External interrupt 5	P50 to P57	O	O	-	-	-	O	-



Because the external interrupt event , key event and AC zero-cross is acknowledged by the rising of the system clock (fs), the pulse which is shorter than the system clock (fs) cycle is neglected.

3.3.2 Block Diagram

■ External Interrupt 0 Block Diagram

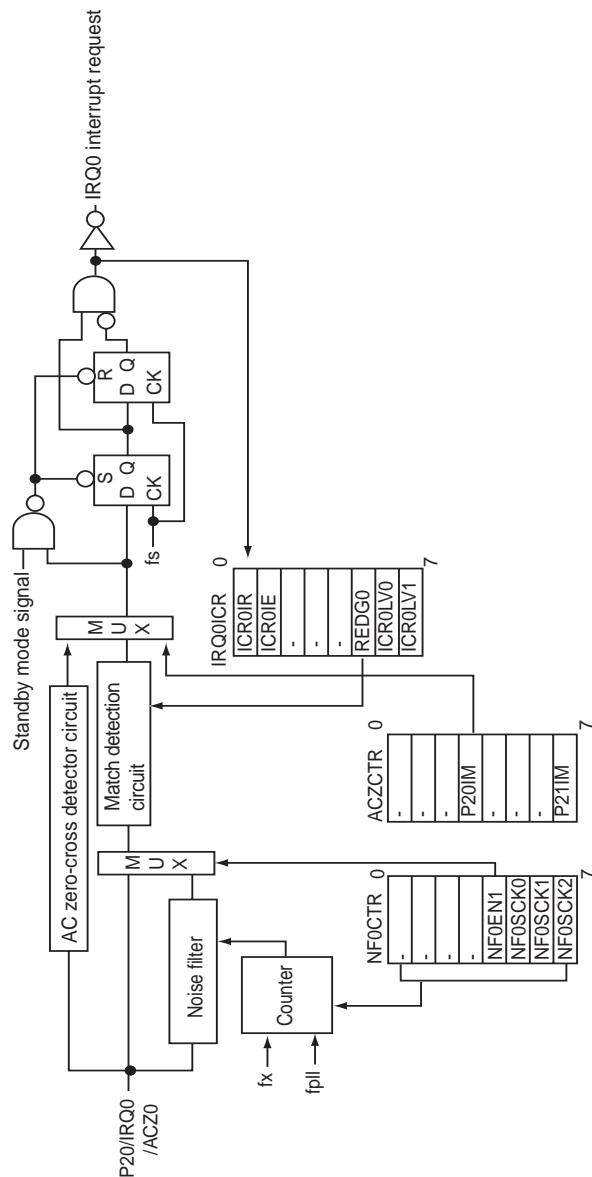


Figure:3.3.1 External Interrupt 0 Block Diagram

■ External Interrupt 1 Block Diagram

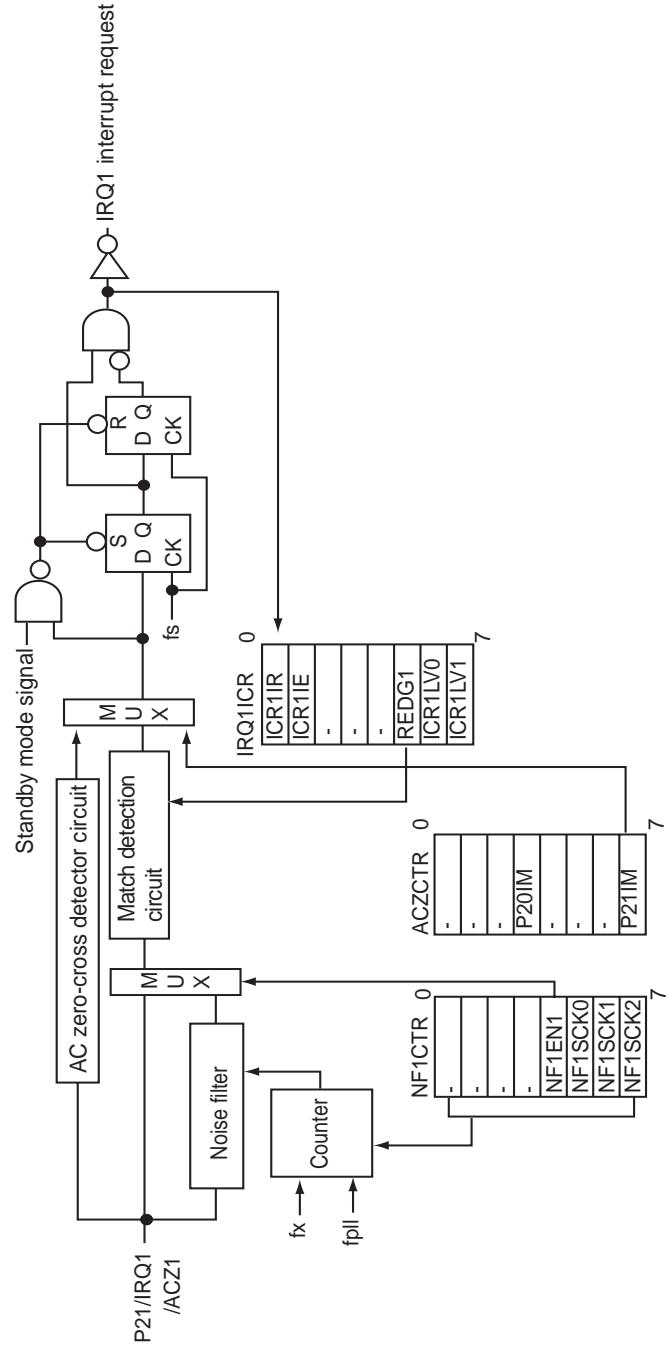


Figure:3.3.2 External Interrupt 1 Block Diagram

■ External Interrupt 2 Block Diagram

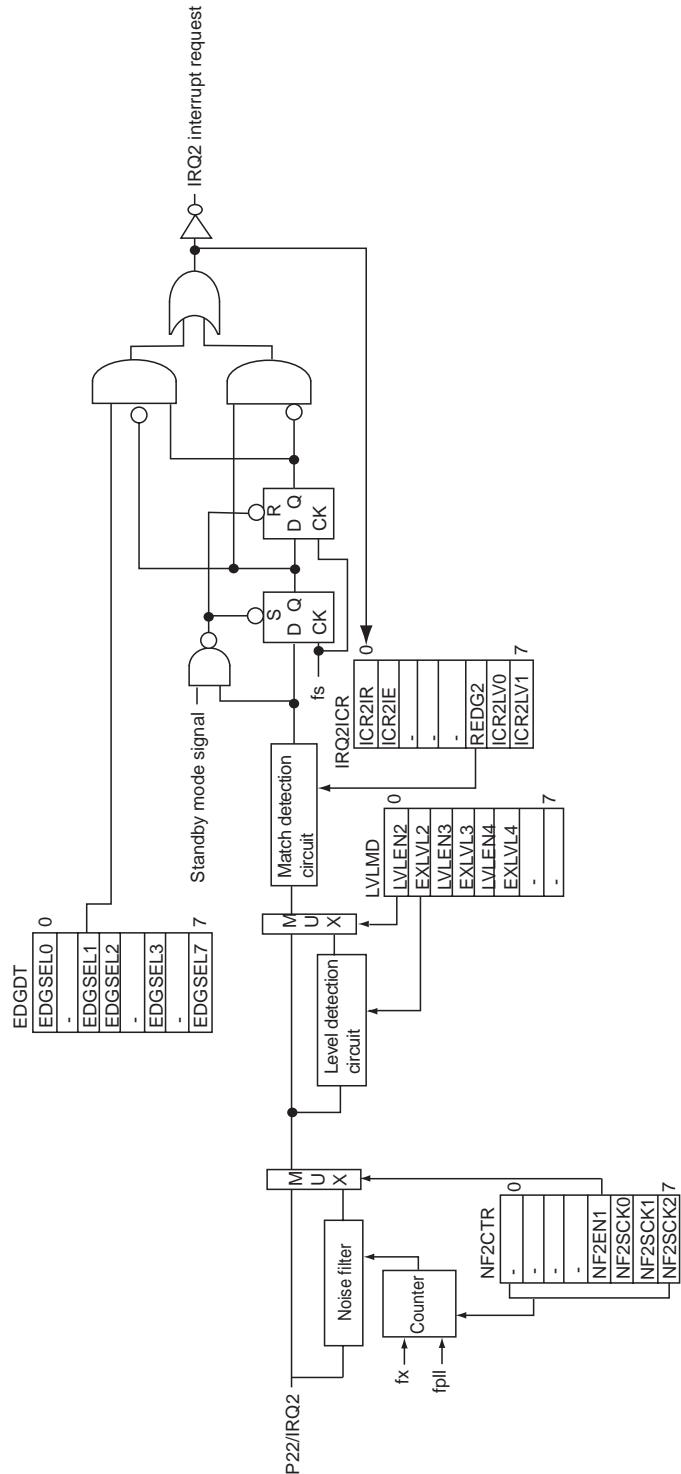


Figure:3.3.3 External Interrupt 2 Block Diagram

■ External Interrupt 3 Block Diagram

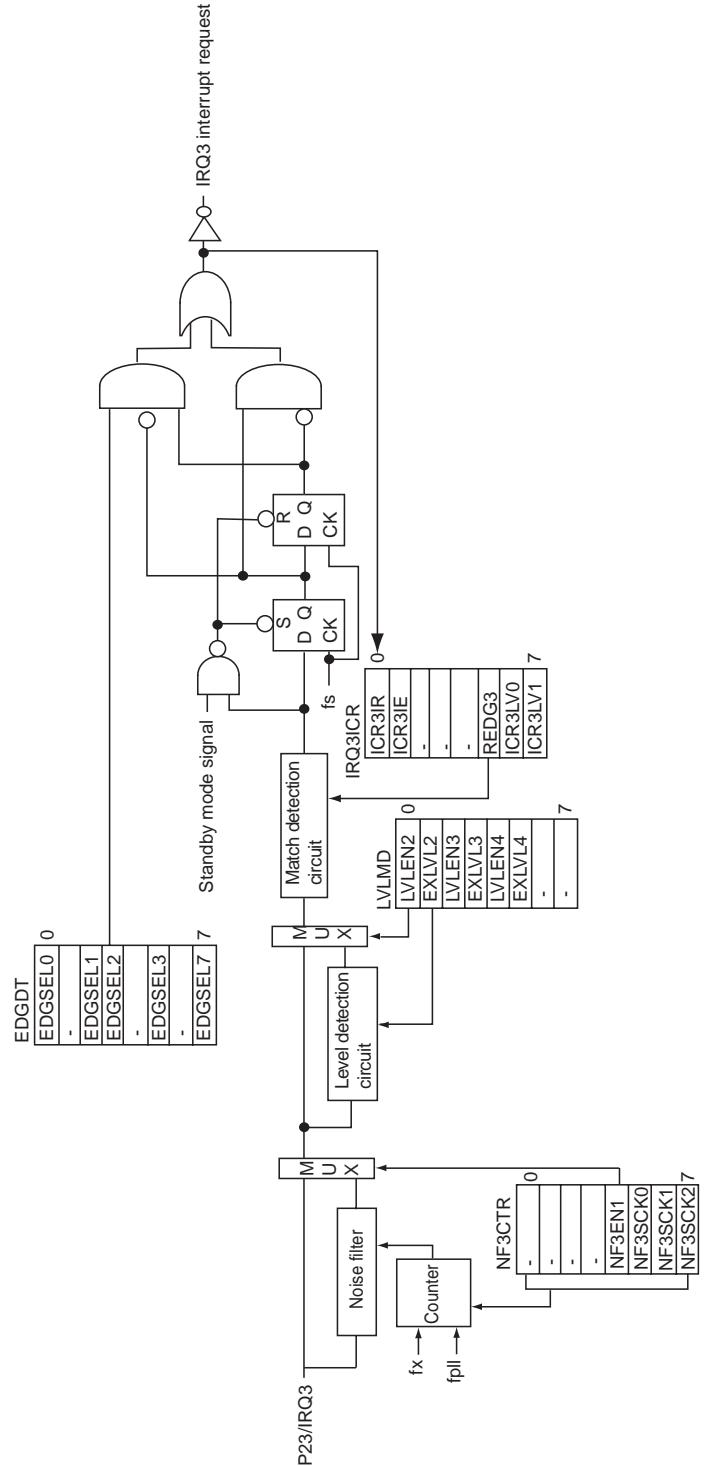


Figure:3.3.4 External Interrupt 3 Block Diagram

■ External Interrupt 4 Block Diagram

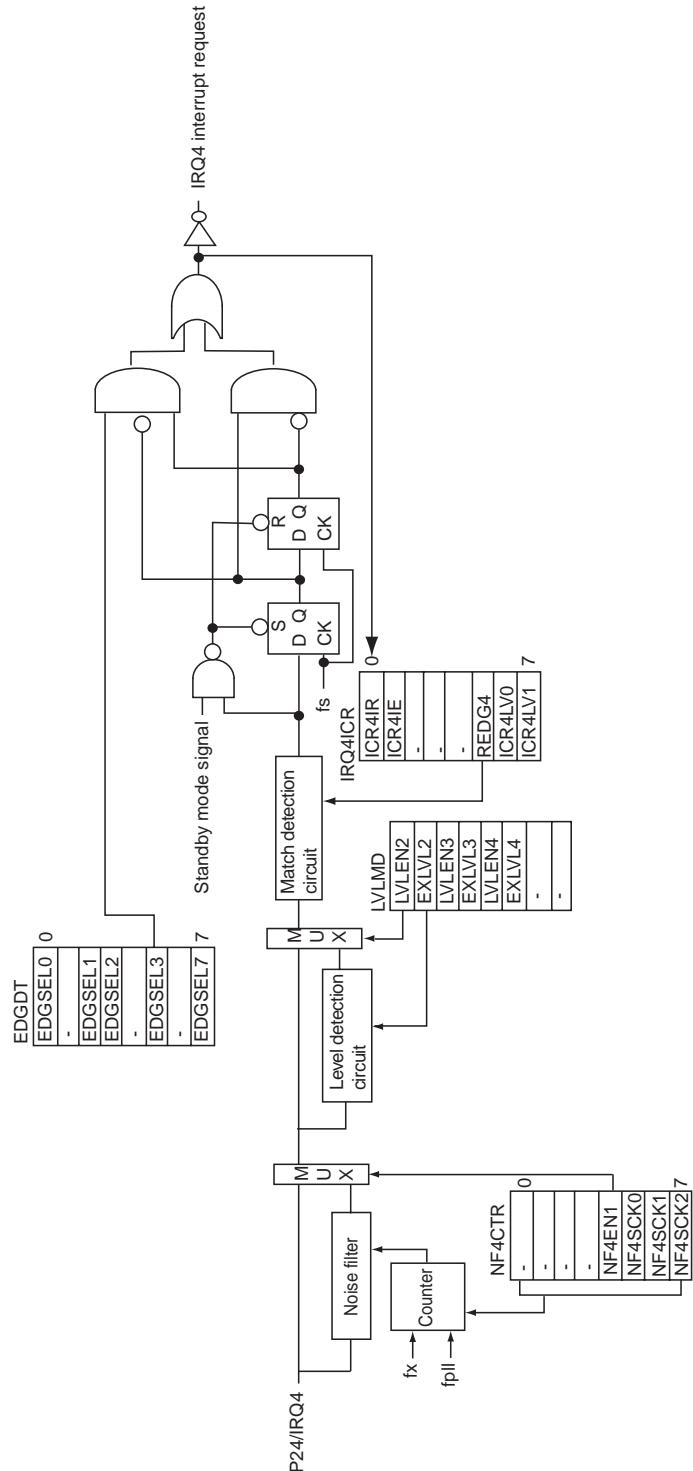


Figure:3.3.5 External Interrupt 4 Block Diagram

■ External Interrupt 5 Block Diagram

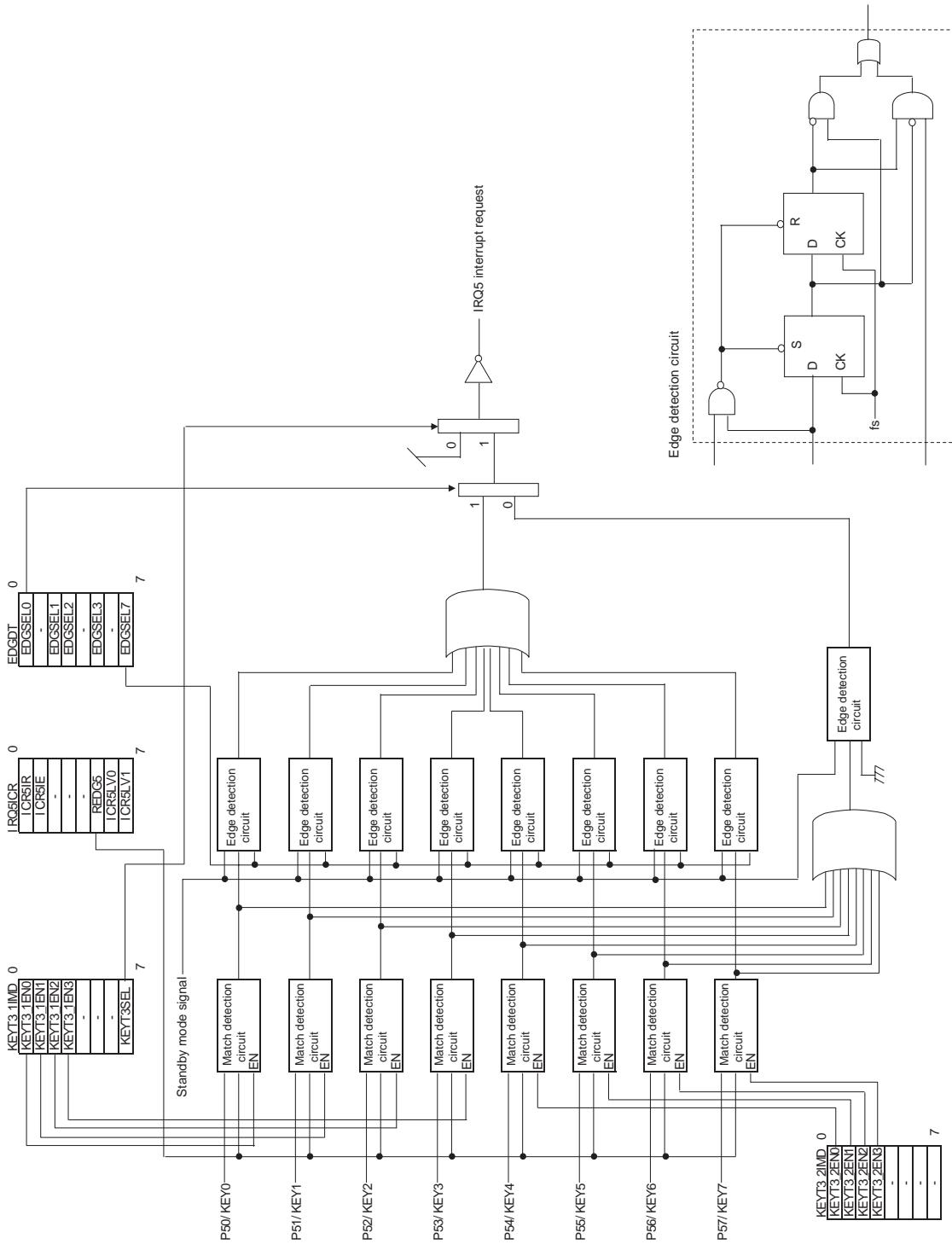


Figure:3.3.6 External Interrupt 5 Block Diagram

3.3.3 External Interrupt Control Registers

The external interrupts 0 to 5 respectively generate interrupt requests by the external interrupt input signals which pass each external interrupt interface 0 to 5.

External interrupt interfaces 0 to 5 are controlled by the external interrupt control register (IRQnICR). The external interrupt interfaces 0 and 1 are controlled by AC zero-cross detector interrupt register (ACZCTR) and noise filter control register (NF0CTR, NF1CTR). The external interrupt interfaces 2 to 4 are controlled by the both edges interrupt control register (EDGDT) and noise filter control register (NF2CTR, NF3CTR, NF4CTR). The external interrupt interface 5 is controlled by the key interrupt control register 1 (KEYT3_1IMD) and key interrupt control register 2 (KEYT3_2IMD).

The following table shows the list of registers which controls external interrupt 0 to 5

Table:3.3.2 External Interrupt Control Register

External interrupt	Register	Address	R/W	Function	Page
External interrupt 0	IRQ0ICR	0x03FE2	R/W	External interrupt 0 control register	III-25
	IRQCNT	0x03F3D	R/W	External interrupt set register	III-55
	NF0CTR	0x03EEB	R/W	Noise filter 0 control register	III-56
	ACZCTR	0x03F2E	R/W	AC zero-cross detector interrupt register	III-57
External interrupt 1	IRQ1ICR	0x03FE3	R/W	External interrupt 1 control register	III-25
	IRQCNT	0x03F3D	R/W	External interrupt set register	III-55
	NF1CTR	0x03ECC	R/W	Noise filter 1 control register	III-56
	ACZCTR	0x03F2E	R/W	AC zero-cross detector interrupt register	III-57
External interrupt 2	IRQ2ICR	0x03FE4	R/W	External interrupt 2 control register	III-25
	IRQCNT	0x03F3D	R/W	External interrupt set register	III-55
	NF2CTR	0x03EED	R/W	Noise filter 2 control register	III-56
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-58
	LVLMD	0x03F1F	R/W	External interrupt enable input switching control register	III-60
External interrupt 3	IRQ3ICR	0x03FE5	R/W	External interrupt 3 control register	III-25
	IRQCNT	0x03F3D	R/W	External interrupt set register	III-55
	NF3CTR	0x03EEE	R/W	Noise filter 3 control register	III-56
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-58
	LVLMD	0x03F1F	R/W	External interrupt enable input switching control register	III-60
External interrupt 4	IRQ4ICR	0x03FE6	R/W	External interrupt 4 control register	III-25
	IRQCNT	0x03F3D	R/W	External interrupt set register	III-55
	NF4CTR	0x03EEF	R/W	Noise filter 4 control register	III-56
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-58
	LVLMD	0x03F1F	R/W	External interrupt enable input switching control register	III-60

External interrupt	Register	Address	R/W	Function	Page
External interrupt 5	IRQ5ICR	0x03FE7	R/W	External interrupt 5 control register	III-25
	IRQCNT	0x03F3D	R/W	External interrupt set register	III-55
	KEYT3_1IMD	0x03F3E	R/W	Key interrupt control register 1	III-61
	KEYT3_2IMD	0x03F3F	R/W	Key interrupt control register 2	III-62
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-58
	LVLMD	0x03F1F	R/W	External interrupt enable input switching control register	III-60

R/W: Readable / Writable.

■ External Interrupt Set Register (IRQCNT: 0x03F3D)

External interrupt set register (IRQCNT) sets whether to enable external interrupts 0 to 4 or not.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P24EN	P23EN	P22EN	P21EN	P20EN
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	P24EN	0: Disable 1: Enable
3	P23EN	0: Disable 1: Enable
2	P22EN	0: Disable 1: Enable
1	P21EN	0: Disable 1: Enable
0	P20EN	0: Disable 1: Enable

Change flags at step (2) in 3.1.4 Maskable Interrupt Control Register Setup.

■ Noise Filter 0 to 4 Control Registers (NF0CTR to NF4CTR:0x03EEB to 0x03EEF)

Noise filter 0 to 4 control registers (NF0CTR to NF4CTR) set the noise remove function to IRQ0 and it also sets the sampling cycle of noise remove function.

bp	7	6	5	4	3	2	1	0
Flag	NFnSCK2	NFnSCK1	NFnSCK0	NFnEN1	Reserved	Reserved	Reserved	Reserved
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	NFnSCK2-0	IRQn noise sampling frequency 000: fpll 001: fpll/2 ⁵ 010: fpll/2 ⁶ 011: fpll/2 ⁷ 100: fpll/2 ⁸ 101: fpll/2 ⁹ 110: fpll/2 ¹⁰ 111: fx
4	NFnEN1	0: External interrupt n 1: Noise filter ON
3-0	Reserved	Always set to "0" *1

Change flags at step (2) in 3.1.4 Maskable Interrupt Control Register Setup.



Always set "0" to the bp denoted by *1.

■ AC Zero-Cross Detector Interrupt Register (ACZCTR:0x03F2E)

AC zero-cross detector interrupt register (ACZCTR) is used to set zero-cross detection function to IRQ0 and IRQ1.

bp	7	6	5	4	3	2	1	0
Flag	P21IM	-	-	-	P20IM	-	-	-
At reset	0	-	-	-	0	-	-	-
Access	R/W	-	-	-	R/W	-	-	-

bp	Flag	Description
7	P21IM	IRQ1 ACZ Input enable flag 0:ACZ input disable 1:ACZ input enable
6-4	-	-
3	P20IM	IRQ0 ACZ Input enable flag 0:ACZ input disable 1:ACZ input enable
2-0	-	-

Change flags at step (2) in 3.1.4 Maskable Interrupt Control Register Setup.

■ Both Edges Interrupt Control Register (EDGDT:0x03F1E)

Bp 2,3,5 of both edges interrupt control register (EDGDT) select interrupt edges of IRQ2 to 4. With this register, the edge to generate the interrupts is selected; both edges or the edge which is specified by the external interrupt control register (IRQ2ICR, IRQ3ICR, IRQ4ICR). When the edge detection circuit in the key interrupt block is used with bit common/bit independant or bit independant, the edge to generate the interrupt is selected; both edges or the edge which is specified by the external interrupt control register (IRQ5ICR) with the register selecting IRQ5 key interrupt edge.

bp	7	6	5	4	3	2	1	0
Flag	EDGSEL7	-	EDGSEL3	-	EDGSEL2	EDGSEL1	-	EDGSEL0
At reset	0	-	0	-	0	0	-	0
Access	R/W	-	R/W	-	R/W	R/W	-	R/W

bp	Flag	Description
7	EDGSEL7	IRQ5 Key interrupt both edges operation selection (Enable at bp:0 EDGSEL0="1") 0:Programmable active edge interrupt selection (Specified with IRQ5ICR bp:5 REDG5) 1:Both edges interrupt selection
6	-	-
5	EDGSEL3	IRQ4 both edges interrupt selection 0:Programmable active edge interrupt selection (Specified with IRQ4ICR bp:5 REDG4) 1:Both edges interrupt selection
4	-	-
3	EDGSEL2	IRQ3 both edges interrupt selection 0:Programmable active edge interrupt selection (Specified with IRQ3ICR bp:5 REDG3) 1:Both edges interrupt selection
2	EDGSEL1	IRQ2 both edges interrupt selection 0:Programmable active edge interrupt selection (Specified with IRQ2ICR bp:5 REDG2) 1:Both edges interrupt selection
1	-	-
0	EDGSEL0	IRQ5 Key interrupt selection 0:Key input Edge detection circuit bit common * 1:Key input Edge detection circuit bit independant

Change flags at step (2) in [3.1.4 Maskable Interrupt Control Register Setup].

* Detail of operation refers to [3.3.7 Key Input Interrupt].



If the key input edge detection circuit is selected bit common with EDGSEL0 flag, the interrupt request signal can be generated by inputting OR of the match detection circuit output of the enable key input. While the match is detected with one enable key input, if the match is detected with other enable key input, the interrupt request signal is not generated.



If the key input edge detection circuit is selected bit independant with EDGSEL0 flag, the edge detection circuit is used with each enable key input. Ths means even though the match is detected with one enable key input, if the match is detected with other enable key input, the interrupt request signal is generated



EDGSEL7 flag is enable only when the key input edge detection circuit is selected bit independant with EDGSEL0 flag. When the key input edge detection circuit bit common is selected with EDGSEL0 flag, key interrupt turns to the programmable active edge in spite of the value of EDGSEL7.

■ External Interrupt Enable Input Switching Control Register (LVLMD:0x03F1F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	EXLVL4	LVLEN4	EXLVL3	LVLEN3	EXLVL2	LVLEN2
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5	EXLVL4	External interrupt 4 Enable Input Level setup (Enable at bp:4 LVLEN4="1") 0:L level 1:H level
4	LVLEN4	External interrupt 4 Enable Input setup 0:Edge 1:Level
3	EXLVL3	External interrupt 3 Enable Input Level setup (Enable at bp:3 LVLEN3="1") 0:L level 1:H level
2	LVLEN3	External interrupt 3 Enable Input setup 0:Edge 1:Level
1	EXLVL2	External interrupt 2 Enable Input Level setup (Enable at bp:2 LVLEN2="1") 0:L level 1:H level
0	LVLEN2	External interrupt 2 Enable Input setup 0:Edge 1:Level

Change flags at step (2) in [3.1.4 Maskable Interrupt Control Register Setup].

■ Key Interrupt Control Register 1 (KEYT3_1IMD:0x03F3E)

Key interrupt control register 1 (KEYT3_1IMD) selects the type of the interrupt which is to be accepted (key interrupt or external interrupt IRQ5. This register can select which pin should accept the key interrupt from port 5 in 1-bit unit.

bp	7	6	5	4	3	2	1	0
Flag	KEYT3SEL	-	-	-	KEYT3_1EN3	KEYT3_1EN2	KEYT3_1EN1	KEYT3_1EN0
At reset	0	-	-	-	0	0	0	0
Access	R/W	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7	KEYT3SEL	Interrupt source selection 0:Disable key interrupt 1:Enable key interrupt
6-4	-	-
3	KEYT3_1EN3	KEY3 interrupt selection 0:Disable 1:Enable
2	KEYT3_1EN2	KEY2 interrupt selection 0:Disable 1:Enable
1	KEYT3_1EN1	KEY1 interrupt selection 0:Disable 1:Enable
0	KEYT3_1EN0	KEY0 interrupt selection 0:Disable 1:Enable

Change flags at step (2) in [3.1.4 Maskable Interrupt Control Register Setup].

■ Key Interrupt Control Register 2 (KEYT3_2IMD:0x03F3F)

Key interrupt control register 2 (KEYT3_2IMD) can select which pin should accept the key interrupt from port 5 in 1-bit unit.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	KEYT3_2EN3	KEYT3_2EN2	KEYT3_2EN1	KEYT3_2EN0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3	KEYT3_2EN3	KEY7 interrupt selection 0:Disable 1:Enable
2	KEYT3_2EN2	KEY6 interrupt selection 0:Disable 1:Enable
1	KEYT3_2EN1	KEY5 interrupt selection 0:Disable 1:Enable
0	KEYT3_2EN0	KEY4 interrupt selection 0:Disable 1:Enable

Change flags at step (2) in [3.1.4 Maskable Interrupt Control Register Setup].

3.3.4 Programmable Active Edge Interrupt

■ Programmable Active Edge Interrupts (External Interrupts 0 to 5)

The programmable active edge interrupt can select the rising/falling edge about the signal which is input from the external interrupt input pin and generate the interrupt at the selected edge. Also, if the value which is set to the external interrupt valid edge specify flag and the level of the external interrupt pin are matched, it is possible from the standby mode.



At the standby mode, if the value that is set to the external interrupt valid specified flag and the external interrupt pin level are matched, the interrupt is generated.

[Chapter 3 3.3.10 External Interrupt At The Standby Mode]

■ Programmable Active Edge Interrupt Setup Example (External Interrupts 0 to 5)

External interrupt 0 (IRQ0) is generated at the rising edge of the input signal from P20.

The table below shows a setup example.

Setup Procedure	Description
(1) Set the external interrupt IRQCNT(0x03F3D) bp0:P20EN=1	(1) Set the P20EN flag of the external interrupt set register (IRQCNT) to "1" to set P20 to an external interrupt.
(2) Specify the interrupt active edge IRQ0ICR(0x03FE2) bp5:REDG0 =1	(2) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the rising edge as the active edge for interrupts.
(3) Set the interrupt level IRQ0ICR(0x03FE2) bp7-6:IRQ0LV1-0 =10	(3) Set the interrupt priority level in the IRQ0LV1 to 0 flag of the IRQ0ICR register. When the interrupt request flag may already be set, the interrupt request flag (IRQ0IR) must be cleared. [Chapter 3 3.1.4 Maskable Interrupt Control Register Setup]
(4) Enable the interrupt IRQ0ICR(0x03FE2) bp1:IRQ0IE =1	(4) Set the IRQ0IE flag of the IRQ0ICR register to "1" enable the interrupt.



The interrupt request flag can be set in switching the interrupt edge, so specify the interrupt valid edge before the interrupt permission.

When the interrupt request flag may already be set, the interrupt request flag (IRQ0IR) must be cleared.



To use the external interrupt pin as interrupt function, it should be pull-up in advance, so that unknown value is not input. If unknown value is input to pin, through current flow.

3.3.5 Both Edges Interrupt

■ Both Edges Interrupt (External Interrupts 2 to 5)

Both edges interrupt can generate interrupt at both the falling edge and the rising edge by the input signal from external input pins. Also, if the value which is set to the external interrupt valid edge specify flag and the level of the external interrupt pin are matched, it is possible from the standby mode.



At the standby mode, if the value that is set to the external interrupt valid specified flag and the external interrupt pin level are matched, the interrupt is generated.
[Chapter 3 3.3.10. External Interrupt At The Standby Mode]

■ Both Edges Interrupt Setup Example (External Interrupts 2 to 5)

External interrupt 2 (IRQ2) is generated at the both edges of the input signal from P22 pin.

The table below shows a setup example.

Setup Procedure	Description
(1) Set the external interrupt IRQCNT(0x03F3D) bp2:P22EN=1	(1) Set the P22EN flag of the external interrupt set register (IRQCNT) to "1" to set P22 to an external interrupt.
(2) Select the both edges interrupt EDGDT (0x03F1E) bp2:EDGSEL2 =1	(2) Set the EDGSEL2 flag of the both edges interrupt control register (EDGDT) to "1" to select the both edges interrupt.
(3) Set the interrupt level IRQ2ICR (0x03FE4) bp7-6:IRQ2LV1-0 =10	(3) Set the interrupt level by the IRQ2LV1 to 0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR). [Chapter 3 3.1.4 Maskable Interrupt Control Register Setup]
(4) Enable the interrupt IRQ2ICR (0x03FE4) bp1:IRQ2IE =1	(4) Set the IRQ2IE flag of the IRQ2ICR register to "1" to enable the interrupt.



When the both edges interrupt is selected, the interrupt request is generated at the both edge, regardless of the REDGn flag of the external interrupt control register (IRQnICR) and EDGSEL0 of the both edges interrupt control register (EDGDT).



The interrupt request flag may be set at switching the interrupt edge. So, clear the interrupt request flag before the interrupt acceptance. Also, select the both edges interrupt before the interrupt acceptance.



To use the external interrupt pin as interrupt function, it should be pull-up in advance, so that unknown value is not input. If unknown value is input to pin, through current flow.

3.3.6 Level Interrupt

■ Level Interrupt (External interrupts 2, 3, and 4)

The level interrupt can select the input level H or input level L about the signal which is input from the external interrupt input pin and generate the interrupt at the selected edge. It is possible from the standby mode.

■ Level Interrupt Example (External interrupts 2, 3, and 4)

External interrupt 2 (IRQ2) is generated at the H level of the input signal from P22.

The table below shows a setup example of IRQ2.

Setup Procedure	Description
(1) Specify the interrupt valid edge IRQ2ICR (0x03FE4) bp5:REDG2 =1	(1) Set the REDG2 flag of the external interrupt 0 control register (IRQ2ICR) to "0" and specify the rising edge as the valid edge.
(2) Specify the interrupt valid input LVLMD (0x03F1F) bp1 :EXLVL2 =1	(2) Set the EXLVL flag of the external interrupt valid input switching control register (LVLMD) to "1" to specify the interrupt valid input level as the level interrupt (H level).
(3) Enable the level interrupt LVLMD (0x03F1F) bp0:LEVEN2 =1	(3) Set the LEVEN2 flag of the external interrupt valid input switching control register (LVLMD) to "1" to specify the interrupt valid input level as the level interrupt (H level).
(4) Set the interrupt level IRQ2ICR (0x03FE4) bp7-6:IRQ2LV1-0 =10	(4) Set the interrupt priority level in the IRQ2LV1 to 0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR). Refer to [Chapter III 3.1.4 Maskable Interrupt Control Register Setup]
(5) Enable the interrupt IRQ2ICR (0x03FE4) bp1:IRQ2IE =1	(5) Set the IRQ2IE flag of the IRQ2ICR register to "1" enable the interrupt.

External interrupt 2 is generated at the H level of the input signal from P22.



Set the external interrupt valid input level equal to the polarity of the interrupt valid edge.
External interrupt valid input level = H level Interrupt valid edge=rising edge
External interrupt valid input level = L level Interrupt valid edge=falling edge



The interrupt request flag can be set at switching the interrupt edge, so specify the interrupt valid edge before the interrupt permission.



When using the level interrupt function, an interrupt may occur after the interrupt process program ends.
When using the level interrupt function, set the request flag to interrupt disabled within the interrupt process program.



At the standby mode, if the value that is set to the external interrupt valid specified flag and the external interrupt pin level are matched, the interrupt is generated. (refer to figure 3-3-1 to 3-3-6.)
So when “flag is 0 and pin is 0” or “flag is 1 and pin is 1” before standby, interrupt is generated at the standby mode and CPU can be returned.

3.3.7 Key Input Interrupt

■ Key Input Interrupt (External Interrupt 5)

This LSI can set port 5 (P50 to P57) pin by 1 bit to key input pin. An interrupt can be generated at the falling edge, if at least 1 key input pin outputs low level. Also, if the key input pin becomes low level, it is possible to return from the standby mode.

When rising edge is set by the external interrupt 5 (ICR5IRQ), the key input default state is changed from "L" to "H".



Key input pin should be pull-up in advance, so that unknown value is not input.

■ Key Input Interrupt Setup Example (External Interrupt 5)

After (P50 to P53) pin of port 5 are set to key input pins and key is input (low level), the external interrupt 5 (IRQ5) is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the key input to input P5DIR(0x03F35) bp7-0:P5DIR7-0=00000000	(1) Set the P5DIR7-0 flag of the port5 direction control register(P5DIR) to "00000000" and set P50 to P57 pin to the input pin
(2) Set the pull-up resistor SELUD(0x03F4C) bp5 :P5DWN =0 P5PLUD(0x03F45) bp7-0:P5PLUD7-0=00001111	(2) Set the P5DWN flag of the SELUD register to "0". and, Set P5PLUD7-0 flag of port 5 pull up resistor control register (P5PLUD) to "00001111" to add pull up resistor to the P50 to P53 pins.
(3) Select the key input interrupt KEYT3_1IMD (0x03F3E) bp7:KEYT3_1SEL =1	(3) Set KEYT3SEL flag of the key interrupt register(KEYT3_1IMD) to "1" to select the key interrupt as the external interrupt5 source.
(4) Select the key input pin KEYT3_1IMD(0x03F3E) bp3-0:KEYT3_1EN3-0=1111	(4) Set KEYT3_1EN3-0 flags of the key interrupt register (KEYT3_1IMD) to "1111" to set the P50 to P53 pins as the key input pins.
(5) Specify the interrupt valid edge EDGDT(0x03F1E) bp7:EDGSEL7=0 bp0:EDGSEL0=0	(5) Set the EDGSEL7 and 0 flags of the EDGDT register to "0" to specify the interrupt valid input to Level.
(6) Set the interrupt level IRQ5ICR(0x03FE7) bp7-6:IRQ5LV1-0=10	(6) Set the interrupt level by the IRQ5LV1 to 0 flag of the IRQ5ICR register. If the interrupt request flag has been already set, clear the request flag. [Chapter 3 3.1.4 Maskable Interrupt Control Register Setup]
(7) Enable the interrupt IRQ5ICR(0x0) bp1:IRQ5IE=1	(7) Set the IRQ5IE flag of the IRQ5ICR register to "1" to enable the interrupt.

*Above (3) and (4) can be set at the same time.

If there is at least one input signal, from the P50 to P53 pins, shows “L” level, the external interrupt 5 is generated at the falling edge.



The key input should be setup before the interrupt is accepted.

3.3.8 Noise Filter

■ Noise Filter (External Interrupts 0 to 4)

Noise filter reduces noise by sampling the input waveform from the external interrupt pins (IRQ0 to 4). Its sampling cycle can be selected from 8 types (f_{PLL} , $f_{PLL}/2^5$, $f_{PLL}/2^6$, $f_{PLL}/2^7$, $f_{PLL}/2^8$, $f_{PLL}/2^9$, $f_{PLL}/2^{10}$, f_x).

■ Noise Filter Selection (External Interrupts 0 to 4)

Noise remove function can be selected by setting the NFnEN1 flag of the noise filter control register (NFnCTR) to "1".

Table:3.3.3 Addition of Noise Remove Function

NFnEN1	IRQn input (P2n)
0	IRQn noise filter OFF
1	IRQn noise filter ON

■ Sampling Cycle Setup (External Interrupts 0 to 4)

The sampling cycle of noise remove function can be set by the NFnSCK2-0 flags of the NFnCTR register.

Table:3.3.4 Sampling Cycle / Time of Noise Remove Function

NFnSCK2-0	Sampling cycle	$f_{PLL}=10\text{ MHz}, f_x=32\text{ kHz}$	
000	f_{PLL}	10 MHz	100 ns
001	$f_{PLL}/2^5$	312.5 kHz	3.2 μs
010	$f_{PLL}/2^6$	156.25 kHz	6.4 μs
011	$f_{PLL}/2^7$	78.12 kHz	12.8 μs
100	$f_{PLL}/2^8$	39.06 kHz	25.6 μs
101	$f_{PLL}/2^9$	19.53 kHz	51.20 μs
110	$f_{PLL}/2^{10}$	9.76 kHz	102.40 μs
111	f_x	32 kHz	31.25 μs

■ Noise Remove Function Operation (External Interrupts 0 to 4)

After sampling the input signal to the external interrupt pins (IRQ0 to 4) with the set sampling time, if the same level comes continuously three times, that level is sent to the inside of LSI. If the same level does not come continuously three times, the previous level is sent.

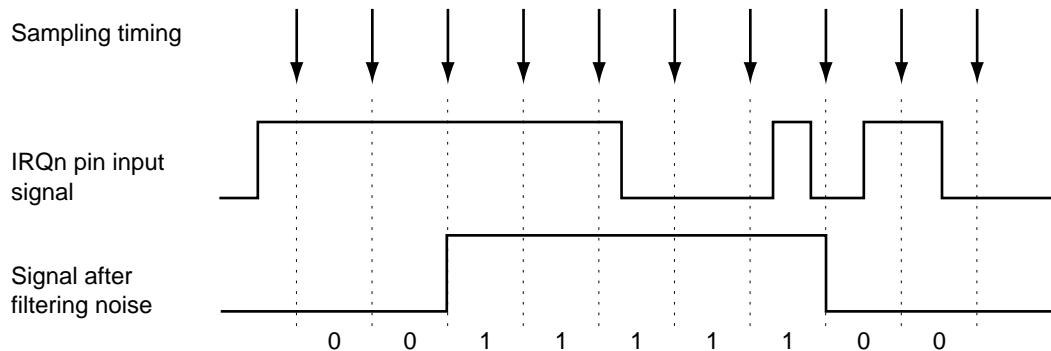


Figure:3.3.7 Noise Remove Function Operation



Noise filter cannot be used at STOP mode and HALT mode.
Set the NFnEN1 flag to "0" when using IRQ0 to 4 for recovering from STANDBY mode.

■ Noise Filter Setup Example (External Interrupt 0)

Noise remove function is added to the input signal from P20 pin to generate the external interrupt 0 (IRQ0) at the rising edge. The sampling clock is set to $fs/2^8$, and the operation state is $fs = 10$ MHz. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) External interrupt setup IRQCNT (0x03F3D) bp0:P20EN =1	(1) Set the P20EN flag of the external interrupt setting register (IRQCNT) to "1" to set P20 to external interrupt.
(2) Specify the interrupt valid edge IRQ0ICR (0x03FE2) bp5:REDG0 =1	(2) Set the REDG0 flag of the external interrupt 0control register (IRQ0ICR) to "1" to specify the interrupt valid edge to the rising edge.
(3) Select the sampling clock NF0CTR(0x03EEB) bp7-5:NF0SCK2-0=000	(3) Select the sampling clock to $f_{PLL}/2^8$ by the NF0SCK2 to 0 flags of the noise filter control register (NF0CTR).
(4) Set the noise filter operation NF0CTR (0x03EEB) bp4:NF0EN1 =1	(4) Set the NF0EN1 flag of the NF0CTR register to "1" to add the noise filter operation.
(5) Set the interrupt level IRQ0ICR (0x03FE2) bp7-6:IRQ0LV1-0 =10	(5) Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [Chapter 3 3.1.4 Maskable Interrupt Control Register Setup]
(6) Enable the interrupt IRQ0ICR (0x03FE2) bp1:IRQ0IE =1	(6) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

*Above (3) and (4) can be set at the same time.

The input signal from P20 pin outputs the interrupt factor at the edge that is followed to the programmable active edge after passing through the noise filter.



The noise filter should be setup before the interrupt is enabled.



The external interrupt pins are recommended to be pull-up in advance, so that unknown value is not input.

3.3.9 AC Zero-Cross Detector

This LSI has AC zero-cross detector circuit. The P20/ACZ0 pin and P21/ACZ1 pin are the input pins of AC zero-cross detector circuit. AC zero-cross detector circuit output the high level when the input level is at the middle, and outputs the low level at other level.

■ AC Zero-Cross Detector (External Interrupt 0)

AC zero-cross detector sets to the high level when the input signal (P20/ACZ0 pin, P21/ACZ1 pin) is at intermediate range by AC zero-cross detector circuit. At the other level, set to the low level. AC zero-cross detector is set by setting the P20IM and P21IM flags of the AC zero-cross detector interrupt control register (ACZCTR) to "1". Also, if the AC zero-cross detector signal becomes high level, it is possible from the standby mode.

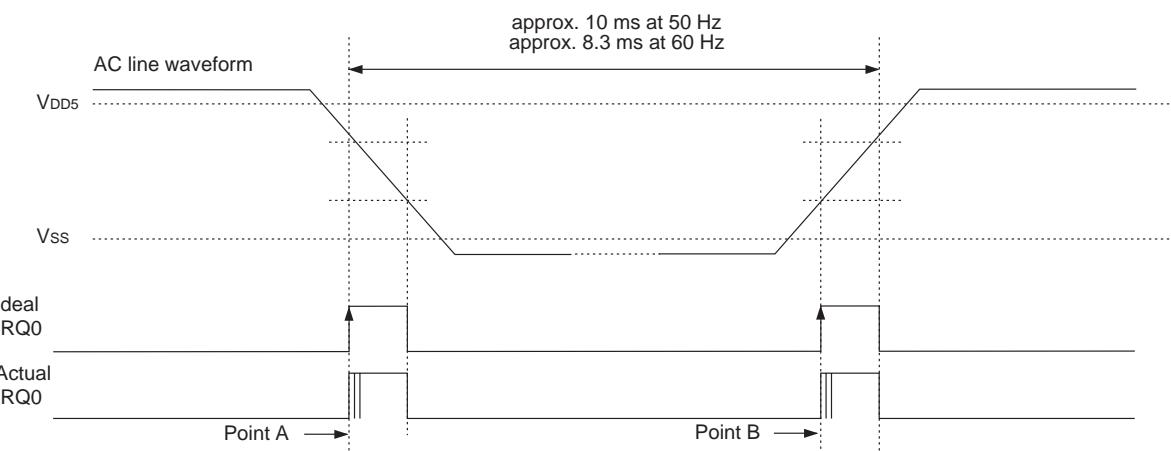


Figure 3.3.8 AC Line Waveform and IRQ0 Generation Timing

Actual IRQ0 interrupt request is generated several times at crossing the AC line waveform and the intermediate level (point A and B). So, the filtering operation by the program is needed.



The interrupt request is generated at the rising edge of the AC zero-cross detector signal.



The interrupt request is output at "H" level of the AC zero-cross detector signal at the standby mode.

■ AC Zero-Cross Detector Setup Example (External Interrupt 1)

AC zero-cross detector generates the IRQ1 external interrupt 1 by using P21/ACZ1 pin.

An example of the setup procedure, with a description of each step is shown below.

If the input level signal which is input from P21/ACZ1 pin cross with the intermediate level, the external interrupt 1 is generated.

Setup Procedure	Description
(1) Set the external interrupt IRQCNT(0x03F3D) bp0:P21EN=1	(1) Set the P21EN flag of the external interrupt set register (IRQCNT) to "1" to set P21 to an external interrupt.
(2) Select the AC zero-cross detector signal ACZCTR(0x03F2E) bp7:P21IM=1	(2) Set the P21IM flag of the AC zero-cross detector interrupt control register (ACZCTR) to "1" to select the AC zero-cross detector signal as the external interrupt 1 generation factor.
(3) Set the interrupt level IRQ1ICR(0x03FE3) bp7-6:IRQ1LV1-0=10	(3) Set the interrupt level by the IRQ1LV1 to 0 flags of the IRQ1ICR register. If the interrupt request flag has been already set, clear the interrupt request flag(IRQ1IR) . [Chapter 3 3.1.4. Maskable Interrupt Control Register Setup]
(4) Enable the interrupt IRQ1ICR(0x03FE3) bp1:IRQ1IE=1	(4) Set the IRQ1IE flag of the IRQ1ICR register to "1" to enable the interrupt.

3.3.10 External Interrupt At The Standby Mode

■ External Interrupt at the Standby Mode (External Interrupts 0 to 5)

It is possible from the standby mode by the external interrupt.

At the standby mode, when the value which is set to the external interrupt valid edge specify flag and external interrupt pin level are matched, the interrupt is generated. Therefore, be aware of the value of external interrupt valid edge specify flag and the external interrupt pin level at the transition to the standby mode. If the value which is set to the external interrupt valid edge specify flag and the external interrupt pin level are matched at the transition to the standby mode, it recovers from the standby mode right away.

■ Setup Examples of the External Interrupt at the Standby Mode.

The generation of the external interrupt 0 (IRQ0) can recover from STOP mode by the low level signal which is input from the external interrupt.

Setup Procedure	Description
(1) Specify the interrupt valid edge IRQ0ICR (0x03FE2) bp5:REDG0 =0	(1) Set the REDG0 of the external interrupt 0 control register (IRQ0ICR) to "0" to specify the interrupt valid edge to the falling edge.

- (2) Set the external interrupt pin
 The external interrupt 0 pin is pulled-up in advance.
- (3) Set the external interrupt
 IRQCNT(0x03F3D)
 bp0:P20EN=1

- (4) Set the interrupt level
 IRQ0ICR (0x03FE2)
 bp7-6:IRQ0LV1-0 =10

- (5) Enable the interrupt
 IRQ0ICR (0x03FE2)
 bp1:IRQ0IE =1

- (6) Set the STOP mode
 CPUM (0x03F00)
 bp3:STOP =1

- (2) The value of the REDG0 flag of the IRQ0ICR register and the external interrupt pin level is different.
- (3) Set the P20EN flag of the external interrupt set register (IRQCNT) to "1" to set P20 to an external interrupt.
- (4) Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register.
 If the interrupt request has been already set, clear the interrupt request flag (IRQ0IR).
- (5) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
- (6) Transfer to the STOP mode by setting STOP flag of the CPU mode control register (CPUM) to "1".
 [Chapter 2. 2.5.5. Transition to Standby Modes]

If the low level of the signal is input to the external interrupt 0 pin, then, the value of the external interrupt valid edge specify flag and the external interrupt 0 pin are matched, the external interrupt 0 is accepted and recover from the STOP mode.



Recovering from the STOP mode is done when the oscillation stabilization wait time which is set at the oscillation stabilization wait control register (DLYCTR) is passed after the acceptance of the external interrupt. [Chapter 2. 2.8.2. Oscillation Stabilization Wait Time]

4

Chapter 4 I/O Ports

4.1 Overview

4.1.1 I/O Port Overview

A total of 90 pins on this LSI, including those shared with special function pins, are allocated for the I/O ports of port 0, port 1, port 2, port 3, port 4, port 5, port 6, port 7, port 8, port 9, port A and port B.

4.1.2 I/O Port Status at Reset

Table:4.1.1 I/O port status at reset (single chip mode)

Port	I/O mode	Pull-up/pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up/pull-down resistor	I/O port
Port 1	Input mode	No pull-up/pull-down resistor	I/O port
Port 2	Input mode	P27: Pull-up resistor Others: No pull-up resistor	I/O port
Port 3	Input mode	No pull-up/pull-down resistor	I/O port
Port 4	Input mode	No pull-up/pull-down resistor	I/O port
Port 5	Input mode	No pull-up/pull-down resistor	I/O port
Port 6	Input mode	No pull-up/pull-down resistor	I/O port
Port 7	Input mode	No pull-up/pull-down resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port 9	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up resistor	I/O port
Port B	Input mode	No pull-up resistor	I/O port



The values of pull-up/pull-down resistors should be calculated in the following ways based on the electrical characteristics in LSI User's Manual of each model.

How to determine pull-up resistor value

- ex) When pins maintain the low level guaranteed performance from the electrical characteristics,
and at $V_{DD5}=5$ V, $V_{IN}=V_{SS}$
input current is Min=-50 μ A, Typ=-100 μ A, Max=-500 μ A.
(- means current passing from microcontroller.) When convert the above values to resistor value, typ = 50 k Ω .
Note that this value varies wildly depending on the temperature.
In temperature variation from -40 °C to 85 °C,
the resistor value varies from Min=10 k Ω to Max=100 k Ω .

How to determine pull-down resistor value

- ex) When pins maintain the high level guaranteed performance from the electrical characteristics,
and at $V_{DD5}=5$ V, $V_{IN}=V_{DD5}$
input current is Min=50 μ A, Typ=100 μ A, Max=500 μ A.
When convert the above values to resistor value, typ = 50 k Ω .
Note that this value varies wildly depending on the temperature.
In temperature variation from -40 °C to 85 °C,
the resistor value varies from Min=10 k Ω to Max=100 k Ω .
-

4.2 Control Registers

Each port is controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU) or the pull-up/pull-down resistor control register (SELUD, PnPLUD) and registers that control special function pin (PnOMD, PnIMD, PnSYO, PnSEV, PnCNT, EXADV, PnODC). The following table shows the list of registers.

Table:4.2.1 I/O Port Control Registers List

Register	Address	R/W	Function	Page
P0OUT	0x03F10	R/W	Port 0 output register	IV-9
P0IN	0x03F20	R	Port 0 input register	IV-10
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-10
P0PLUD	0x03F40	R/W	Port 0 pull-up/pull-down resistor control register	IV-10
P0OMD	0x03EE0	R/W	Port 0 output mode register	IV-11
P0ODC	0x03EF0	R/W	Port 0 Nch open-drain control register	IV-12
P0LED	0x03EE3	R/W	Port 0 LED control register	IV-13
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-14
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-15
P1OUT	0x03F11	R/W	Port 1 output register	IV-25
P1IN	0x03F21	R	Port 1 input register	IV-26
P1DIR	0x03F31	R/W	Port 1 direction control register	IV-26
P1PLUD	0x03F41	R/W	Port 1 pull-up/pull-down resistor control register	IV-26
P1OMD	0x03EE1	R/W	Port 1 output mode register	IV-27
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-28
BUZSEL	0x03EE2	R/W	Buzzer output control register	IV-29
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-30
P2OUT	0x03F12	R/W	Port 2 output register	IV-39
P2IN	0x03F22	R	Port 2 input register	IV-40
P2DIR	0x03F32	R/W	Port 2 direction control register	IV-40
P2PLUD	0x03F42	R/W	Port 2 pull-up/pull-down resistor control register	IV-40
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-41
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-42
P3OUT	0x03F13	R/W	Port 3 output register	IV-51
P3IN	0x03F23	R	Port 3 input register	IV-52
P3DIR	0x03F33	R/W	Port 3 direction control register	IV-52
P3PLUD	0x03F43	R/W	Port 3 pull-up/pull-down resistor control register	IV-52
P3ODC	0x03EF1	R/W	Port 3 Nch open-drain control register	IV-53
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-54

Register	Address	R/W	Function	Page
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-55
P4OUT	0x03F14	R/W	Port 4 output register	IV-65
P4IN	0x03F24	R	Port 4 input register	IV-65
P4DIR	0x03F34	R/W	Port 4 direction control register	IV-66
P4PLUD	0x03F44	R/W	Port 4 pull-up/pull-down resistor control register	IV-66
P4ODC	0x03EF2	R/W	Port 4 Nch open-drain control register	IV-67
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-68
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-69
P5OUT	0x03F15	R/W	Port 5 output register	IV-79
P5IN	0x03F25	R	Port 5 input register	IV-80
P5DIR	0x03F35	R/W	Port 5 direction control register	IV-80
P5PLUD	0x03F45	R/W	Port 5 pull-up/pull-down resistor control register	IV-80
P5ODC	0x03EF3	R/W	Port 5 Nch open-drain control register	IV-81
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-82
BUZSEL	0x03EE2	R/W	Buzzer output control register	IV-83
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-84
P6OUT	0x03F16	R/W	Port 6 output register	IV-92
P6IN	0x03F26	R	Port 6 input register	IV-93
P6DIR	0x03F36	R/W	Port 6 direction control register	IV-93
P6PLUD	0x03F46	R/W	Port 6 pull-up/pull-down resistor control register	IV-93
P6OMD	0x03EE4	R/W	Port 6 output mode register	IV-94
P6ODC	0x03EF4	R/W	Port 6 Nch open-drain control register	IV-94
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-95
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-96
P7OUT	0x03F17	R/W	Port 7 output register	IV-107
P7IN	0x03F27	R	Port 7 input register	IV-107
P7DIR	0x03F37	R/W	Port 7 direction control register	IV-108
P7PLUD	0x03F47	R/W	Port 7 pull-up/pull-down resistor control register 0	IV-108
P7ODC	0x03EF5	R/W	Port 7 Nch open-drain control register	IV-109
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection control register1	IV-110
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-111
P8OUT	0x03F18	R/W	Port 8 output register	IV-122
P8IN	0x03F28	R	Port 8 input register	IV-123
P8DIR	0x03F38	R/W	Port 8 direction control register	IV-123
P8PLU	0x03F48	R/W	Port 8 pull-up resistor control register	IV-123
P8OMD1	0x03EE5	R/W	Port 8 output mode register 1	IV-124
P8CNT1	0x03EFB	R/W	Port 8 output control register 1	IV-125

Register	Address	R/W	Function	Page
P8CNT2	0x03EFC	R/W	Port 8 output control register 2	IV-126
P8SY0	0x03EF7	R/W	Port 8 synchronous output control register 1	IV-126
P8SEV	0x03EF8	R/W	Port 8 synchronous output event selection register 1	IV-127
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection control register 2	IV-127
P9OUT	0x03F19	R/W	Port 9 output register	IV-137
P9IN	0x03F29	R	Port 9 input register	IV-138
P9DIR	0x03F39	R/W	Port 9 direction control register	IV-138
P9PLU	0x03F49	R/W	Port 9 pull-up resistor control register	IV-138
P9OMD	0x03EE7	R/W	Port 9 output mode register 1	IV-139
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection control register 2	IV-139
PAOUT	0x03F1A	R/W	Port A output register	IV-145
PAIN	0x03F2A	R	Port A input register	IV-146
PADIR	0x03F3A	R/W	Port A direction control register	IV-146
PAPLU	0x03F4A	R/W	Port A pull-up resistor control register	IV-146
PAOMD	0x03EE6	R/W	Port A output mode register	IV-147
PAIMD	0x03EE8	R/W	Port A input mode register	IV-148
PACNT	0x03EF6	R/W	Port A output control register	IV-149
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection control register 2	IV-150
PBOUT	0x03F1B	R/W	Port B output register	IV-160
PBIN	0x03F2B	R	Port B input register	IV-160
PBDIR	0x03F3B	R/W	Port B direction control register	IV-161
PBPLU	0x03F4B	R/W	Port B pull-up resistor control register	IV-161
PBIMD	0x03EE9	R/W	Port B input mode register	IV-162
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection control register 2	IV-163

R/W: Readable/Writable

4.3 Port 0

4.3.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 0 direction control register (P0DIR) to “1” and write the value of the port 0 output register (P0OUT).

To read input data of pin, set the control flag of the port 0 direction control register (P0DIR) to “0” and read the value of the port 0 input register (P0IN).

Each bit can be set individually as either an input or output by the port 0 I/O direction control register (P0DIR). The control flag of the port 0 direction control register (P0DIR) is set to “1” for output mode, and “0” for input mode.

Each bit can be set individually if pull-up (or pull-down) resistor is added or not, by the port 0 pull-up/pull-down resistor control register (P0PLUD). Set the control flag of the port 0 pull-up/pull-down resistor control register (P0PLUD) to “1” to add pull-up (or pull-down) resistor.

Port 0 can be selected to add pull-up or pull-down resistor by bp0 of the pull-up/pull-down resistor selection register (SELUD).

For P01, P02, P04 and P06, each bit can be selected individually as Nch open-drain output by the port 0 Nch open-drain control register (P0ODC). The control flag of the port 0 Nch open-drain control register (P0ODC) is set to “1” for Nch open-drain output, and “0” for push-pull output.

■ Special Function Pin Setup

P00 is also used as I/O pin of timer 7.

P01 is also used as I/O pin of timer 8.

P02 is also used as I/O pin of timer 9.

P03 is also used as the output pin of timer 0, timer 2 and remote control carrier. I/O mode by each bit can be selected by the port 0 output mode register (P0OMD). The port 0 output mode register (P0OMD) is set to “1” to output the special function data, and “0” to use as the general port.

The bp3 of the remote control carrier output control register (RMCTR) is set to “0” for the timer output, and “1” for the remote control carrier output.

P00 is also used as the input pin of the serial 1 reception data and UART 1 reception data. When the SC1SBIS flag of the serial interface 1 mode register 1 (SC1MD1) is “1”, P01 is the input pin of serial data.

P01 is also used as the I/O pin of serial 1 transmission/reception data and the output pin of UART 1 transmission data. When the SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is “1”, P00 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 0 Nch open-drain control register (P0ODC) output can be selected by setting the Port 0 Nch open-drain control register (P0ODC).

P02 is also used as the I/O pin of serial 1 clock. When the SC1SBTS flag of the serial interface 1 mode register 1 (SC1MD1) is “1”, P02 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 0 Nch open-drain control register (P0ODC).

P04 is also used as the I/O pin of serial 3 transmission/reception data and the output pin of UART3 transmission data. When the SC3SBOS flag of the serial interface 3 mode register 1 (SC3MD1) is “1”, P04 is the serial data I/

O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 0 Nch open-drain control register (P0ODC).

P05 is also used as the input pin of the serial 3 reception data and the UART3 reception data. When the SC3SBIS flag of the serial interface 3 mode register 1 (SC3MD1) is "1", P05 is the serial data input pin.

P06 is also used as the serial 3 clock I/O pin. When the SC0SBTS flag of the serial interface 3 mode register 1 (SC3MD1) is "1", P04 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 0 Nch open-drain control register (P0ODC).

P00 to P07 are also used as the LED0 to 7 output pins. The output mode by each bit can be selected by the large current pin control register (POLED). When the large current pin control register (POLED) is "1", P00 to P07 are the large current output pins. (Nch-Tr.), and "0", P00 to P07 are the normal current output pins.

Combined with the large current pin control register (POLED), the output of the general port can be large current.

P07 is also used as analog A output.

4.3.2 Registers

Table:4.3.1 shows registers that control the port 0.

Table:4.3.1 Port 0 Control Register

Registers	Address	R/W	Function	Page
P0OUT	0x03F10	R/W	Port 0 output register	IV-9
P0IN	0x03F20	R	Port 0 input register	IV-10
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-10
P0PLUD	0x03F40	R/W	Port 0 pull-up/pull-down resistor control register	IV-10
P0OMD	0x03EE0	R/W	Port 0 output mode register	IV-11
P0ODC	0x03EF0	R/W	Port 0 Nch open-drain control register	IV-12
P0LED	0x03EE3	R/W	Port 0 LED control register	IV-13
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-14
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-15

R/W:Readable/Writable

- Port 0 Output Register (P0OUT: 0x03F10)

bp	7	6	5	4	3	2	1	0
Flag	P0OUT7	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	P0OUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 0 Input Register (P0IN: 0x03F20)

bp	7	6	5	4	3	2	1	0
Flag	P0IN7	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	P0IN7-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 0 Direction Control Register (P0DIR: 0x03F30)

bp	7	6	5	4	3	2	1	0
Flag	P0DIR7	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P0DIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 0 Pull-up/Pull-down Resistor Control Register (P0PLUD: 0x03F40)

bp	7	6	5	4	3	2	1	0
Flag	P0PLUD7	P0PLUD6	P0PLUD5	P0PLUD4	P0PLUD3	P0PLUD2	P0PLUD1	P0PLUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P0PLUD7-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 0 Output Mode Register (P0OMD: 0x03EE0)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P0OMD4	P0OMD3	P0OMD2	P0OMD1	P0OMD0
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	P0OMD4	P03 special function setting 0:TM0IOB/RMOUTB 1:TM2IOB
3	P0OMD3	I/O port, TM0IOB/TM2IOB/RMOUTB selection 0:Port P03 1:TM0IOB/TM2IOB/RMOUTB
2	P0OMD2	I/O port, TM9IOB selection 0:Port P02 1:TM9IOB
1	P0OMD1	I/O port, TM8IOB selection 0:Port P01 1:TM8IOB
0	P0OMD0	I/O port, TM7IOB selection 0:Port P00 1:TM7IOB

■ Port 0 Nch Open-drain Control Register (P0ODC:0x03EF0)

bp	7	6	5	4	3	2	1	0
Flag	-	P0ODC6	-	P0ODC4	-	P0ODC2	P0ODC1	-
At reset	-	0	-	0	-	0	0	-
Access	-	R/W	-	R/W	-	R/W	R/W	-

bp	Flag	Description
7	-	-
6	P0ODC6	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
5	-	-
4	P0ODC4	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
3	-	-
2-1	P0ODC2-1	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
0	-	-

■ Port 0 LED Control Register (P0LED:0x03EE3)

bp	7	6	5	4	3	2	1	0
Flag	P0LED7	P0LED6	P0LED5	P0LED4	P0LED3	P0LED2	P0LED1	P0LED0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	P0LED7	LED 7 (Large current output) selection 0:Normal output 1:LED 7 (Large current output)
6	P0LED6	LED 6 (Large current output) selection 0:Normal output 1:LED 6 (Large current output)
5	P0LED5	LED 5 (Large current output) selection 0:Normal output 1:LED 5 (Large current output)
4	P0LED4	LED 4 (Large current output) selection 0:Normal output 1:LED 4 (Large current output)
3	P0LED3	LED 3 (Large current output) selection 0:Normal output 1:LED 3 (Large current output)
2	P0LED2	LED 2 (Large current output) selection 0:Normal output 1:LED 2 (Large current output)
1	P0LED1	LED 1 (Large current output) selection 0:Normal output 1:LED 1 (Large current output)
0	P0LED0	LED 0 (Large current output) selection 0:Normal output 1:LED 0 (Large current output)

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.3.3 Block Diagram

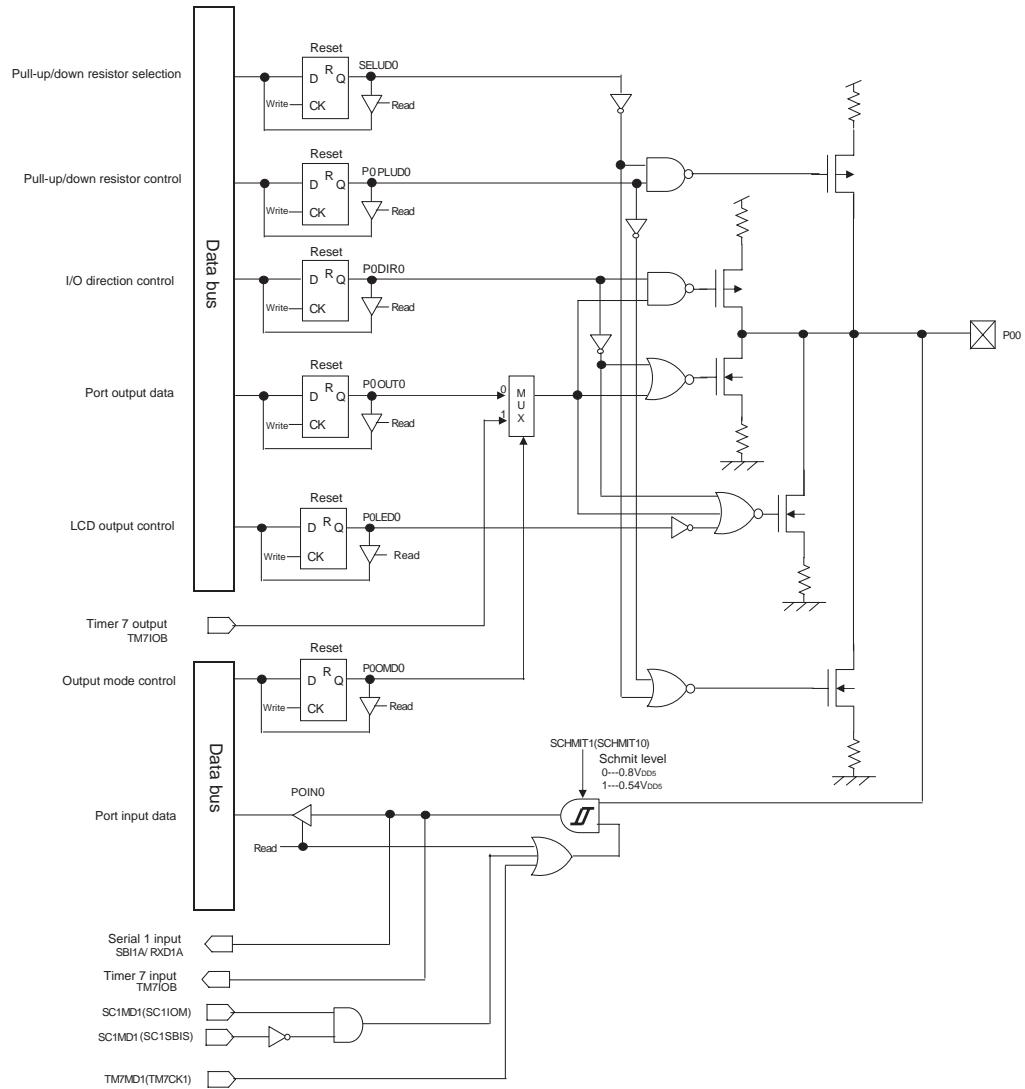


Figure:4.3.1 Block Diagram (P00)

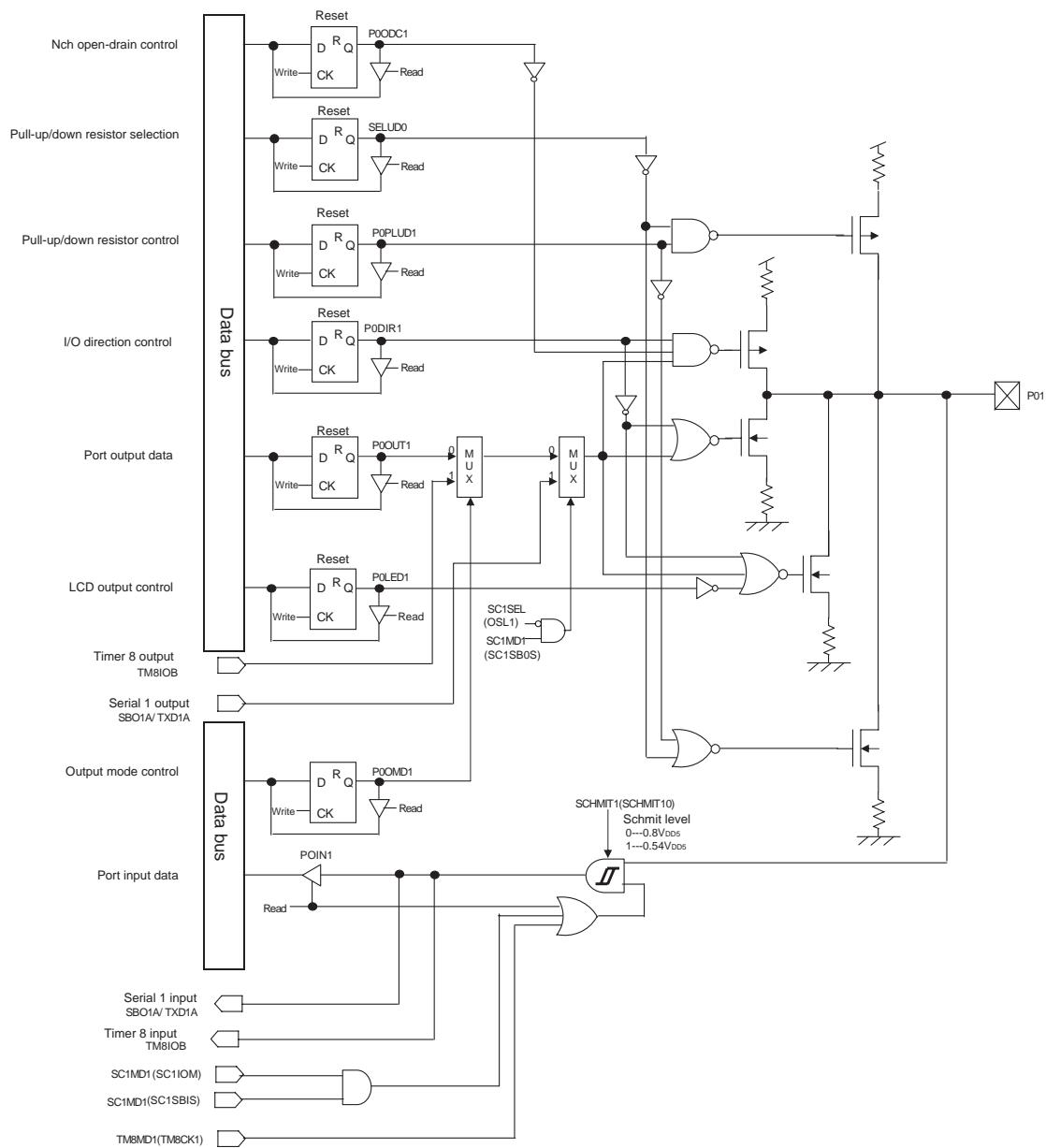


Figure:4.3.2 Block Diagram (P01)

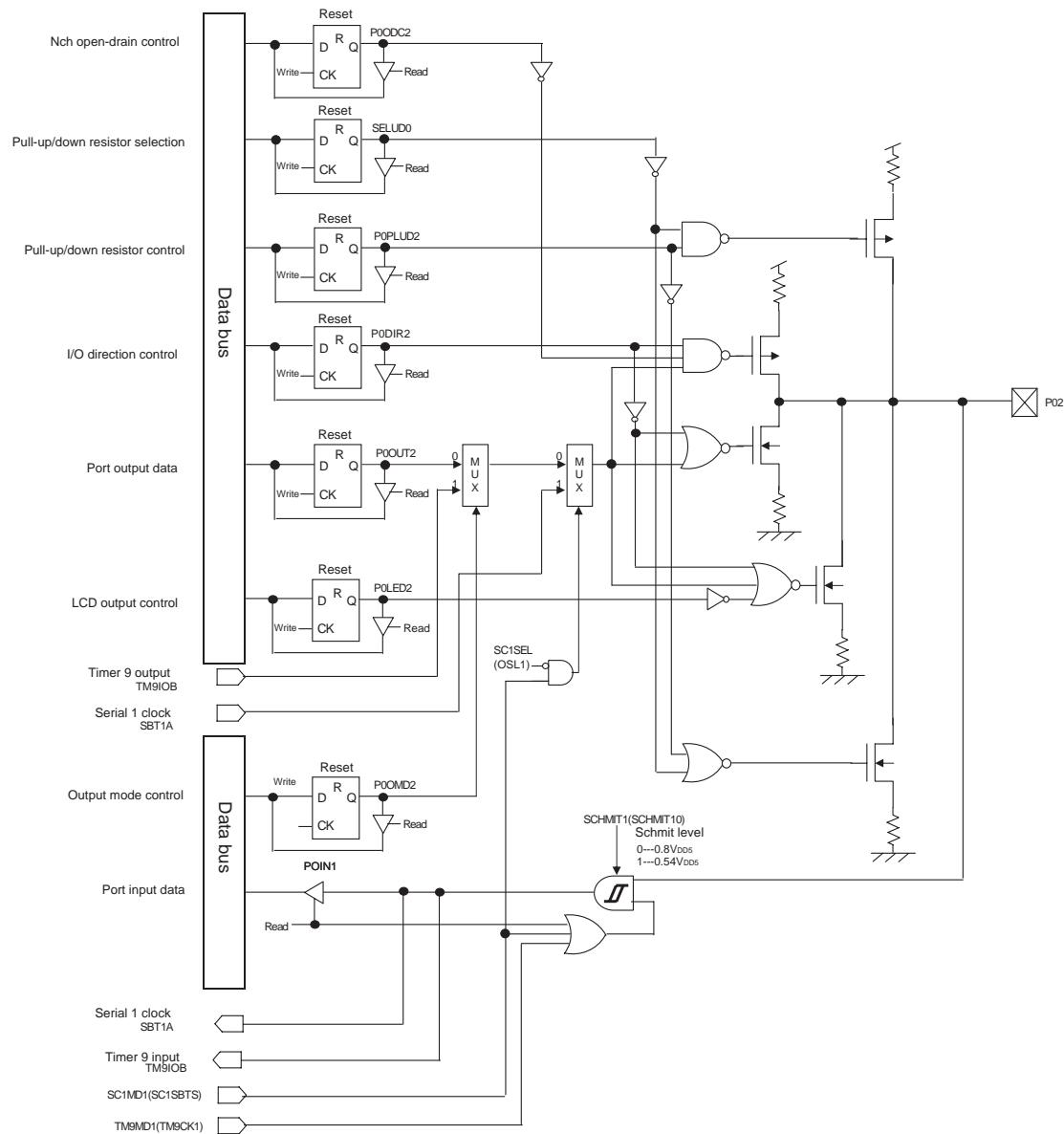


Figure:4.3.3 Block Diagram (P02)

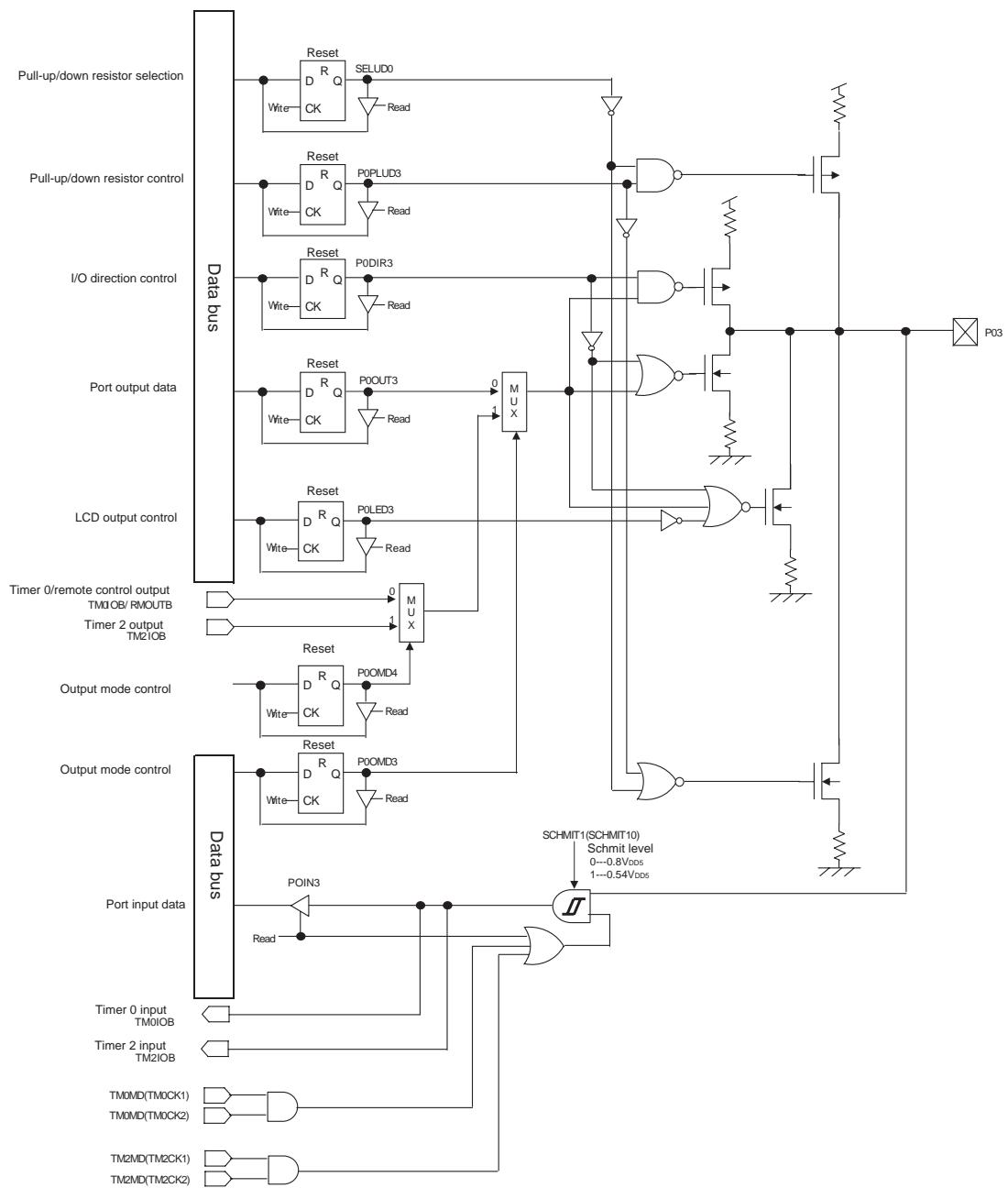


Figure:4.3.4 Block Diagram (P03)

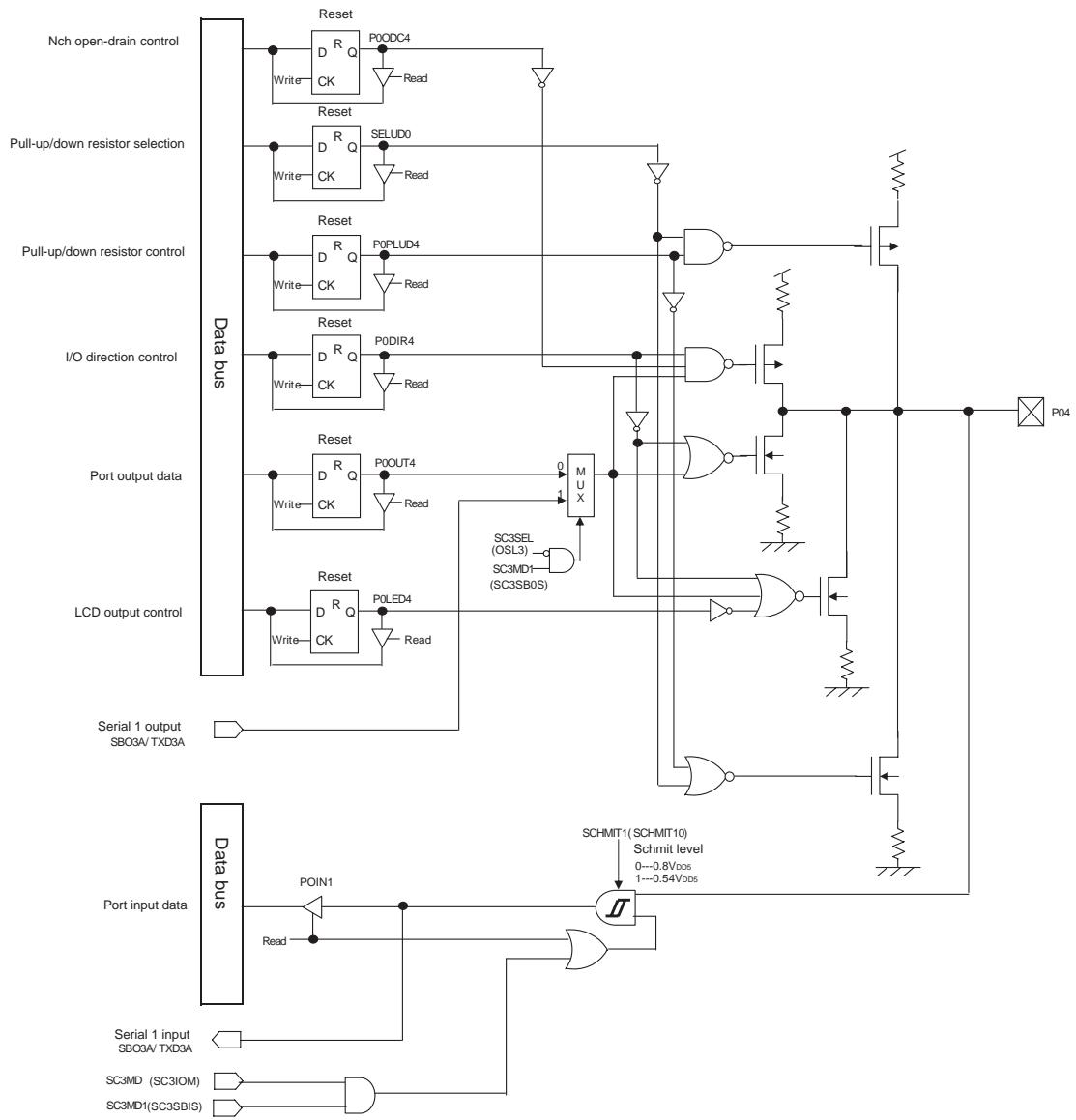


Figure:4.3.5 Block Diagram (P04)

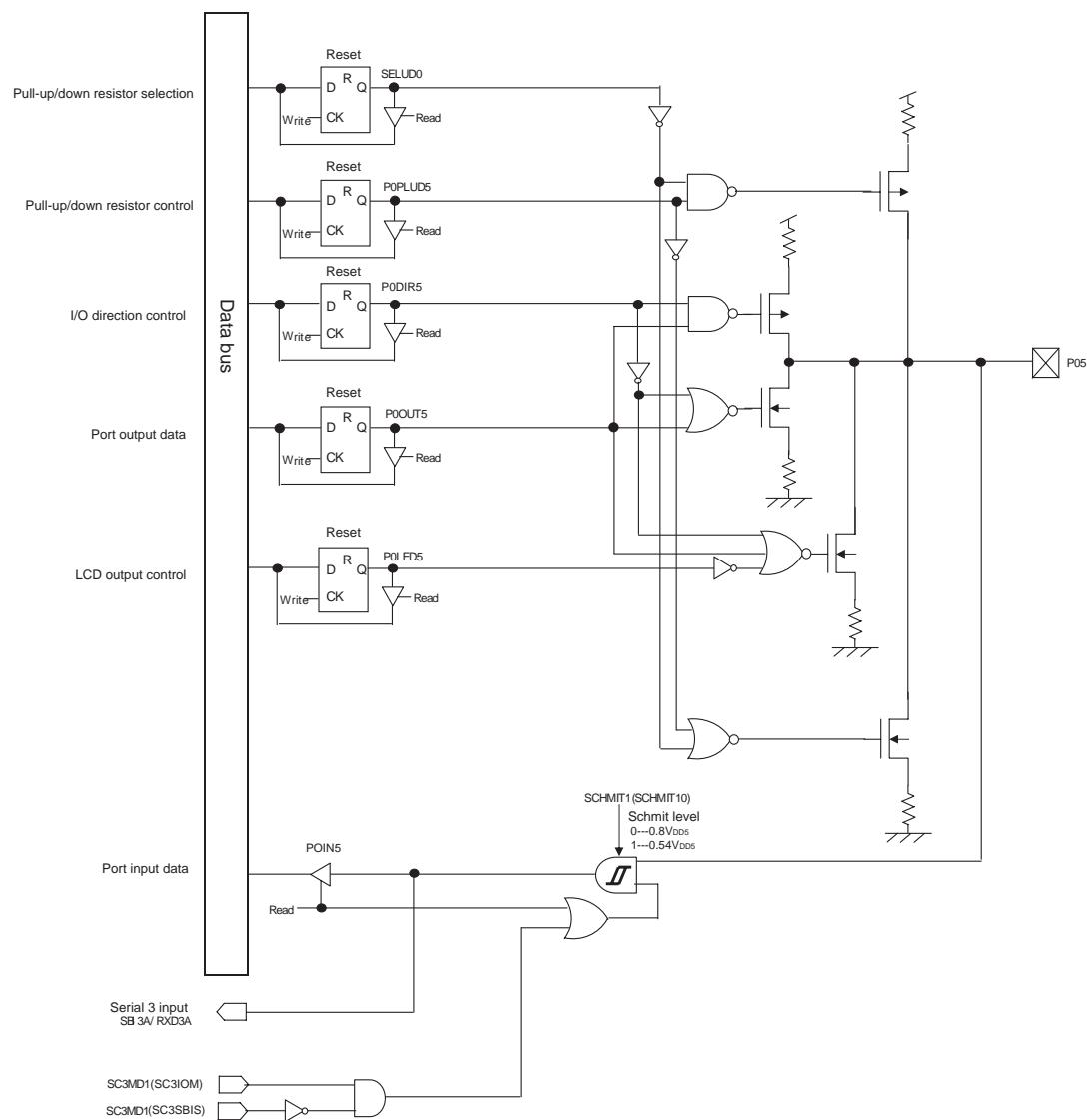


Figure:4.3.6 Block Diagram (P05)

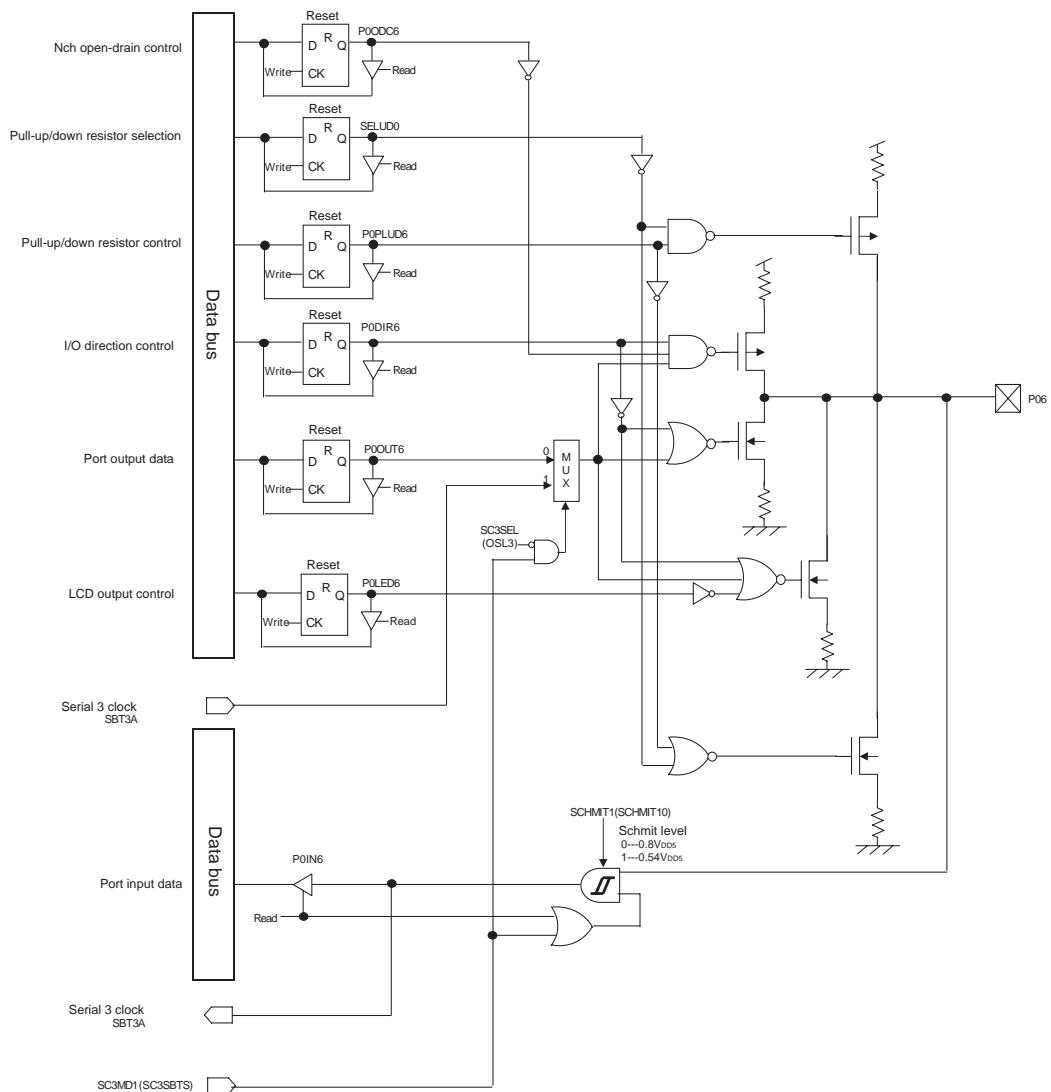


Figure:4.3.7 Block Diagram (P06)

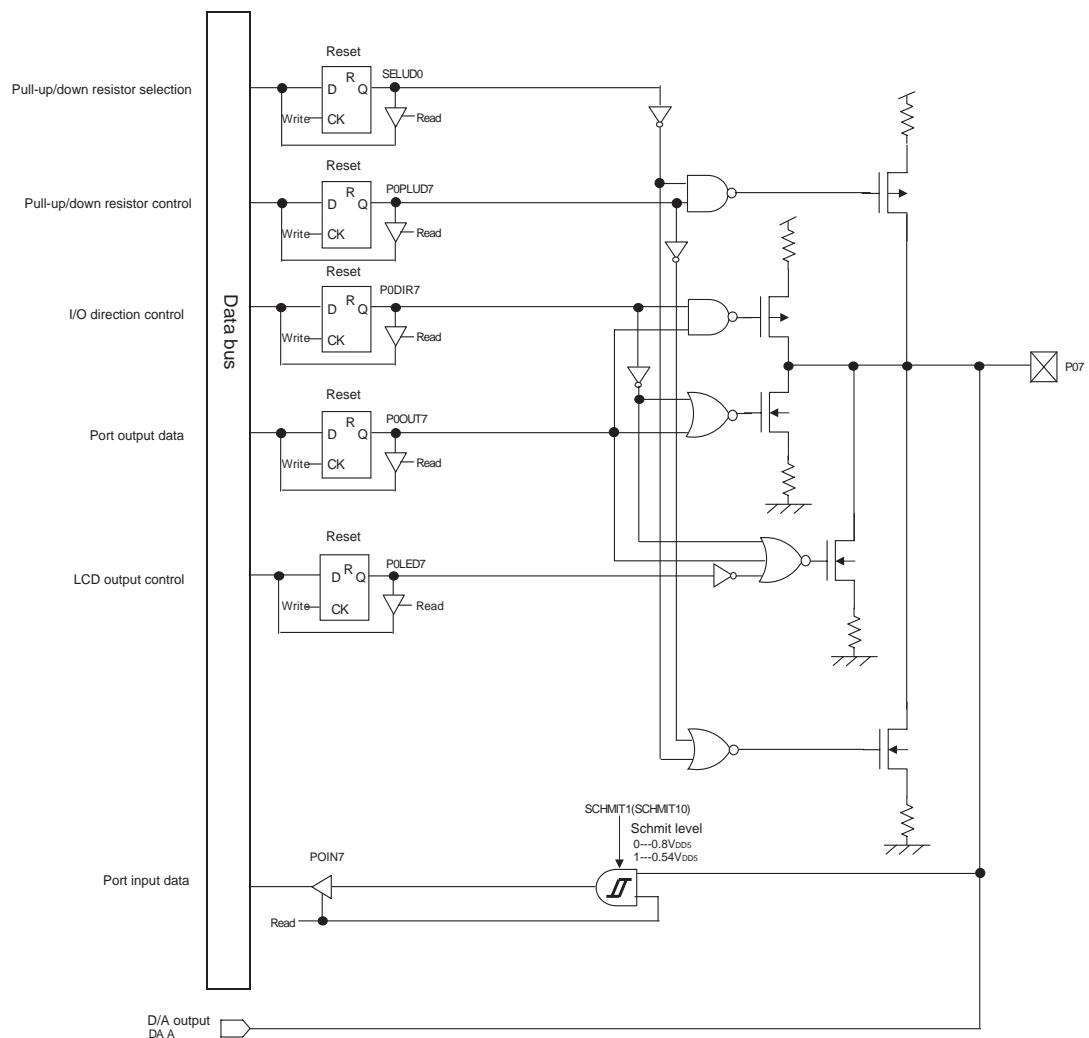


Figure:4.3.8 Block Diagram (P07)

4.4 Port 1

4.4.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 1 direction control register (P1DIR) to "1" and write the value of the port 1 output register (P1OUT).

To read input data of pin, set the control flag of the port 1 direction control register (P1DIR) to "0" and read the value of the port 1 input register (P1IN).

Each bit can be set individually as either an input or output by the port 1 I/O direction control register (P1DIR). The control flag of the port 1 direction control register (P1DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up or pull-down resistor is added or not, by the port 1 pull-up/pull-down resistor control register (P1PLUD). Set the control flag of the port 1 pull-up/pull-down resistor control register (P1PLUD) to "1" to add pull-up or pull-down resistor.

Port 1 can be selected to add pull-up or pull-down resistor by bp1 of the pull-up/pull-down resistor selection register (SELUD).

■ Special Function Pin Setup

P10 is also used as timer 0 I/O pin and remote control carrier output pin. Each bit can be selected individually as output mode by the bp0 of the port 1 output mode register (P1OMD). The port 1 output mode register (P1OMD) is set to "1" for the special function data output, and "0" for the general port.

The bp7 of the remote control carrier output control register (RMCTR) is set to "1" and the bp2 of the port 1 output mode register (P1OMD) is set to "1" for the remote control carrier output.

P11 is also used as timer 2 I/O pin.

P12 is also used as timer 1 I/O pin.

P13 is also used as timer 3 I/O pin.

P14 is also used as timer 4 I/O pin. Each bit can be selected individually as I/O mode by the port 1 output mode register (P1OMD). The port 1 output mode register (P1OMD) is set to "1" for the special function data I/O, and "0" for the general port.

P15 is also used as timer 7/buzzer B I/O pin.

P16 is also used as timer 8/Reverse buzzer B I/O pin. Each bit can be selected individually as output mode by the port 1 output mode register (P1OMD) and the buzzer selection register (BUSZEL). The port 1 output mode register (P1OMD) is set to "1" for the special function data output, and "0" for the general port.

P10 to P16 are also used as LCD segment output pin. SEG 49 to 43 pins can be selected when the flag of the bp1 to 0 of the LCD output control register 7 (LCCTR7) and the flag of 7 to 3 of the LCD output control register 6 (LCCTR6). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

4.4.2 Registers

Table:4.4.1 shows registers that control the port 1.

Table:4.4.1 Port 1 Control Register

Registers	Address	R/W	Function	Page
P1OUT	0x03F11	R/W	Port 1 output register	IV-25
P1IN	0x03F21	R	Port 1 input register	IV-26
P1DIR	0x03F31	R/W	Port 1 direction control register	IV-26
P1PLUD	0x03F41	R/W	Port 1 pull-up/pull-down resistor control register	IV-26
P1OMD	0x03EE1	R/W	Port 1 output mode register	IV-27
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-28
BUZSEL	0x03EE2	R/W	Buzzer output control register	IV-29
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-30

R/W:Readable/Writable

- Port 1 Output Register (P1OUT: 0x03F11)

bp	7	6	5	4	3	2	1	0
Flag	-	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
At reset	-	x	x	x	x	x	x	x
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P1OUT6-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 1 Input Register (P1IN: 0x03F21)

bp	7	6	5	4	3	2	1	0
Flag	-	P1IN6	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0
At reset	-	x	x	x	x	x	x	x
Access	-	R	R	R	R	R	R	R

bp	Flag	Description
7	-	-
6-0	P1IN6-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 1 Direction Control Register (P1DIR: 0x03F31)

bp	7	6	5	4	3	2	1	0
Flag	-	P1DIR6	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P1DIR6-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 1 Pull-up/Pull-down Resistor Control Register (P1PLUD: 0x03F41)

bp	7	6	5	4	3	2	1	0
Flag	-	P1PLUD6	P1PLUD5	P1PLUD4	P1PLUD3	P1PLUD2	P1PLUD1	P1PLUD0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P1PLUD6-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 1 Output Mode Register (P1OMD: 0x03EE1)

bp	7	6	5	4	3	2	1	0
Flag	-	P1OMD6	P1OMD5	P1OMD4	P1OMD3	P1OMD2	P1OMD1	P1OMD0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6	P1OMD6	I/O port, Timer/buzzer output selection 0:Port P16 1:TM8IOC/buzzer output
5	P1OMD5	I/O port, Timer/buzzer output selection 0:Port P15 1:TM7IOC/buzzer output
4	P1OMD4	I/O port, TM4IOC selection 0:Port P14 1:TM4IOC
3	P1OMD3	I/O port, TM3IOC selection 0:Port P13 1:TM3IOC
2	P1OMD2	I/O port, TM1IOC selection 0:Port P12 1:TM1IOC
1	P1OMD1	I/O port, TM2IOC selection 0:Port P11 1:TM2IOC
0	P1OMD0	I/O port, TM0IOC/RMOUTC selection 0:Port P10 1:TM0IOC/RMOUTC

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Buzzer Output Control Register (BUZSEL: 0x03EE2)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	BUZSEL4	BUZSEL3	BUZSEL2	BUZSEL1	-
At reset	-	-	-	0	0	0	0	-
Access	-	-	-	R/W	R/W	R/W	R/W	-

bp	Flag	Description
7-5	-	-
4	BUZSEL4	Buzzer (Reverse) output selection 0:Port P54 1:NBUZZERA
3	BUZSEL3	Buzzer output selection 0:Port P53 1:BUZZERA
2	BUZSEL2	Control with P10MD6 0:TM8IOC 1:NBUZZERB
1	BUZSEL1	Buzzer (Reverse) output selection 0:TM7IOC 1:BUZZERB
0	-	-

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.4.3 Block Diagram

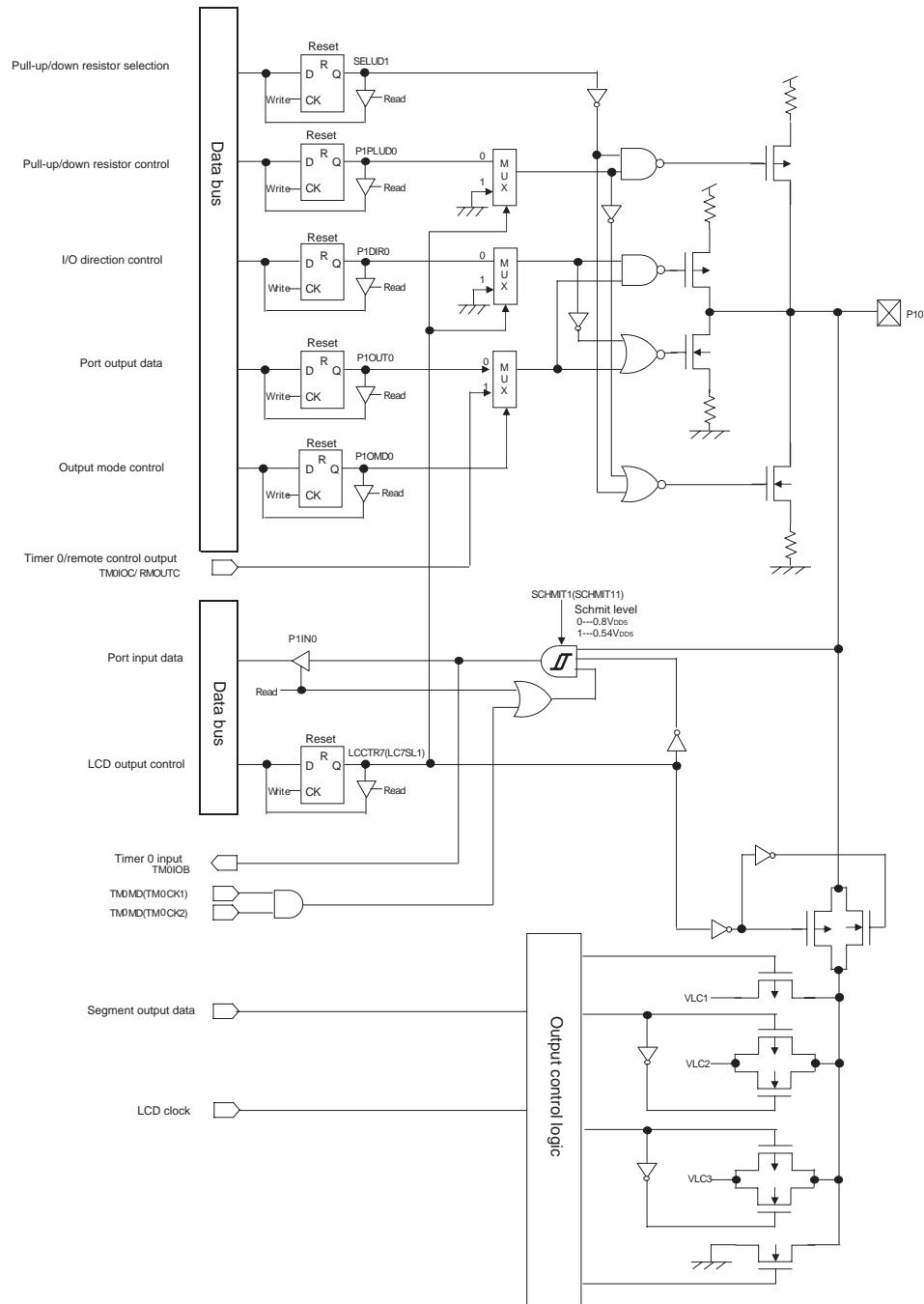


Figure:4.4.1 Block Diagram (P10)

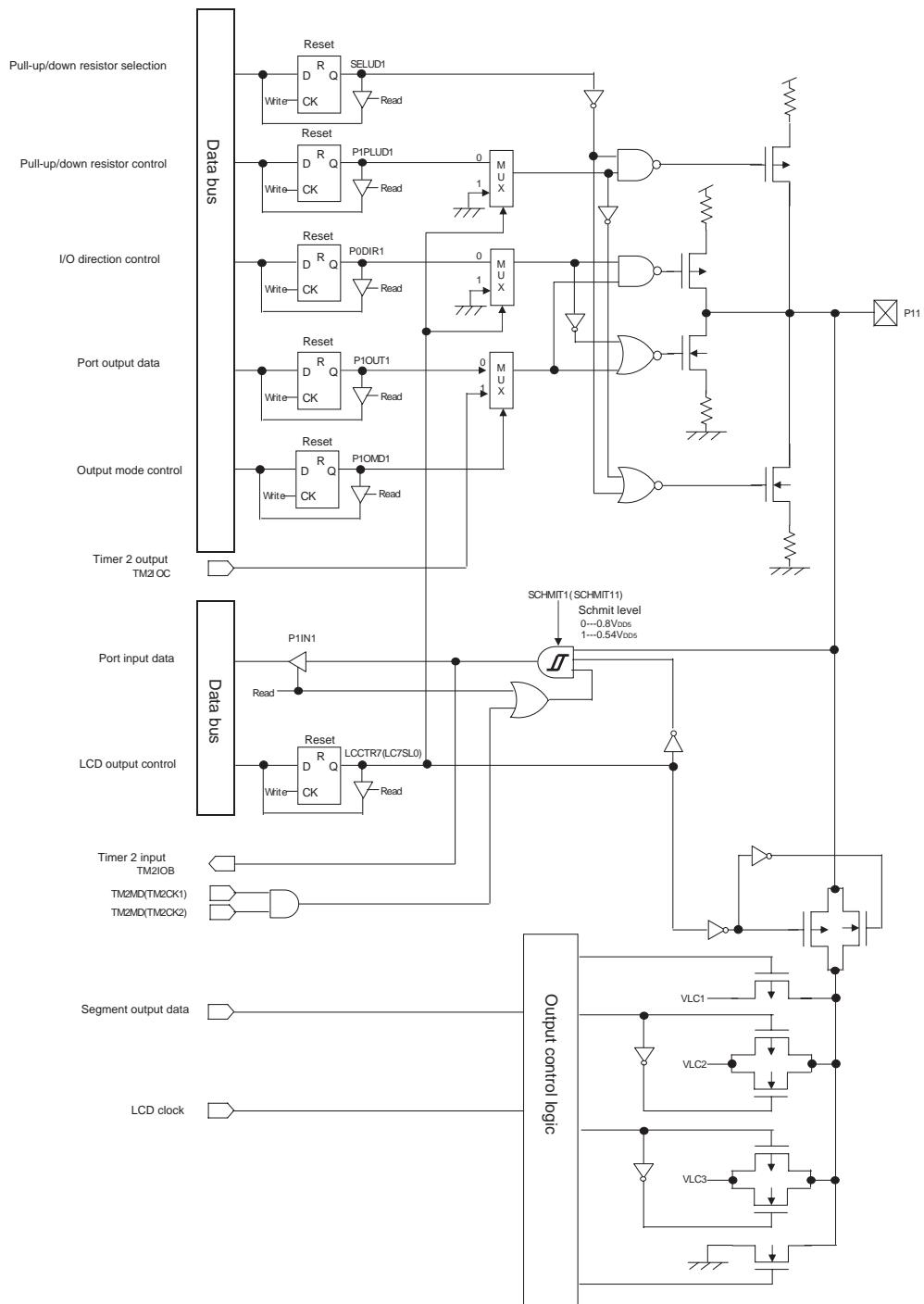


Figure:4.4.2 Block Diagram (P11)

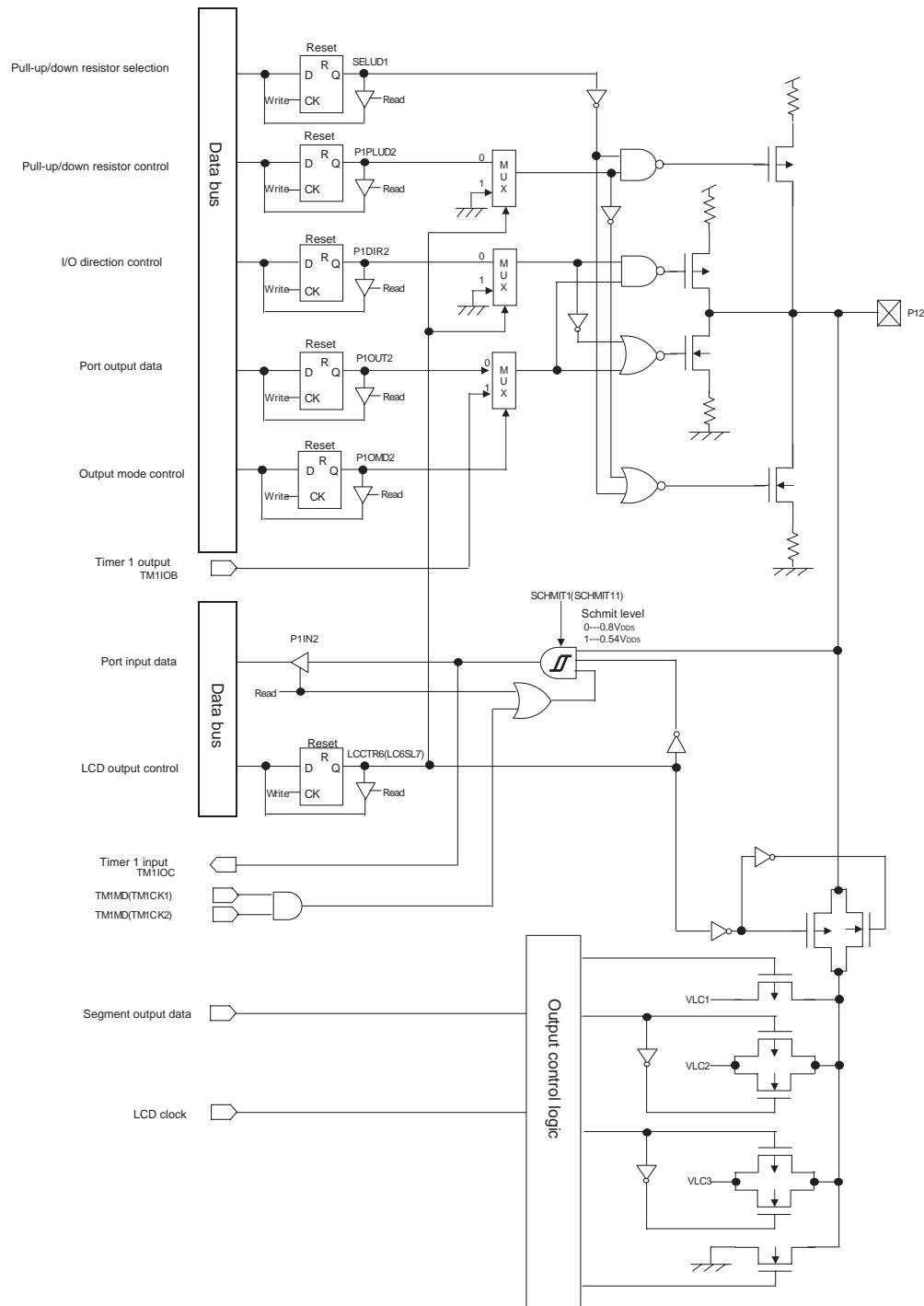


Figure:4.4.3 Block Diagram (P12)

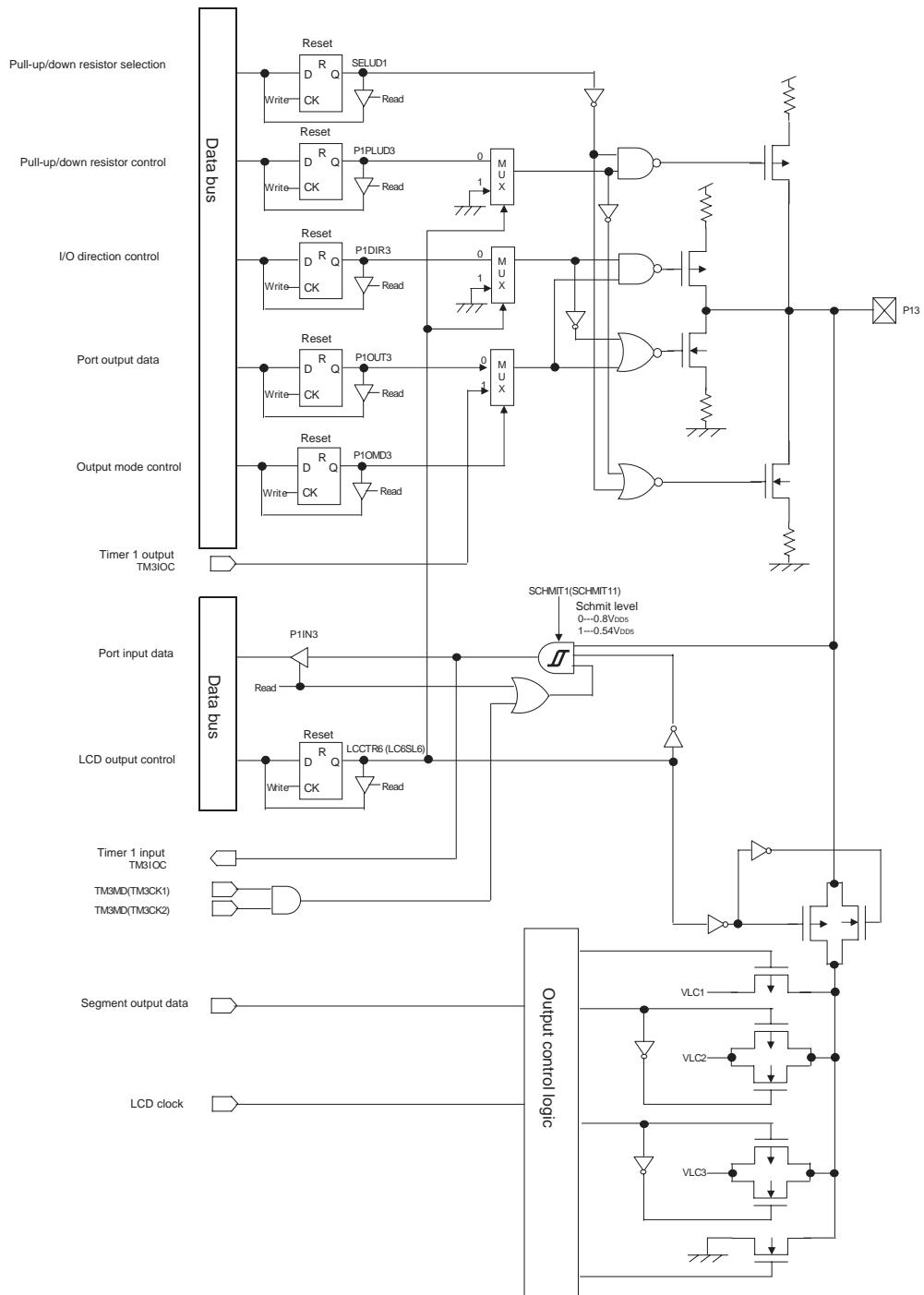


Figure:4.4.4 Block Diagram (P13)

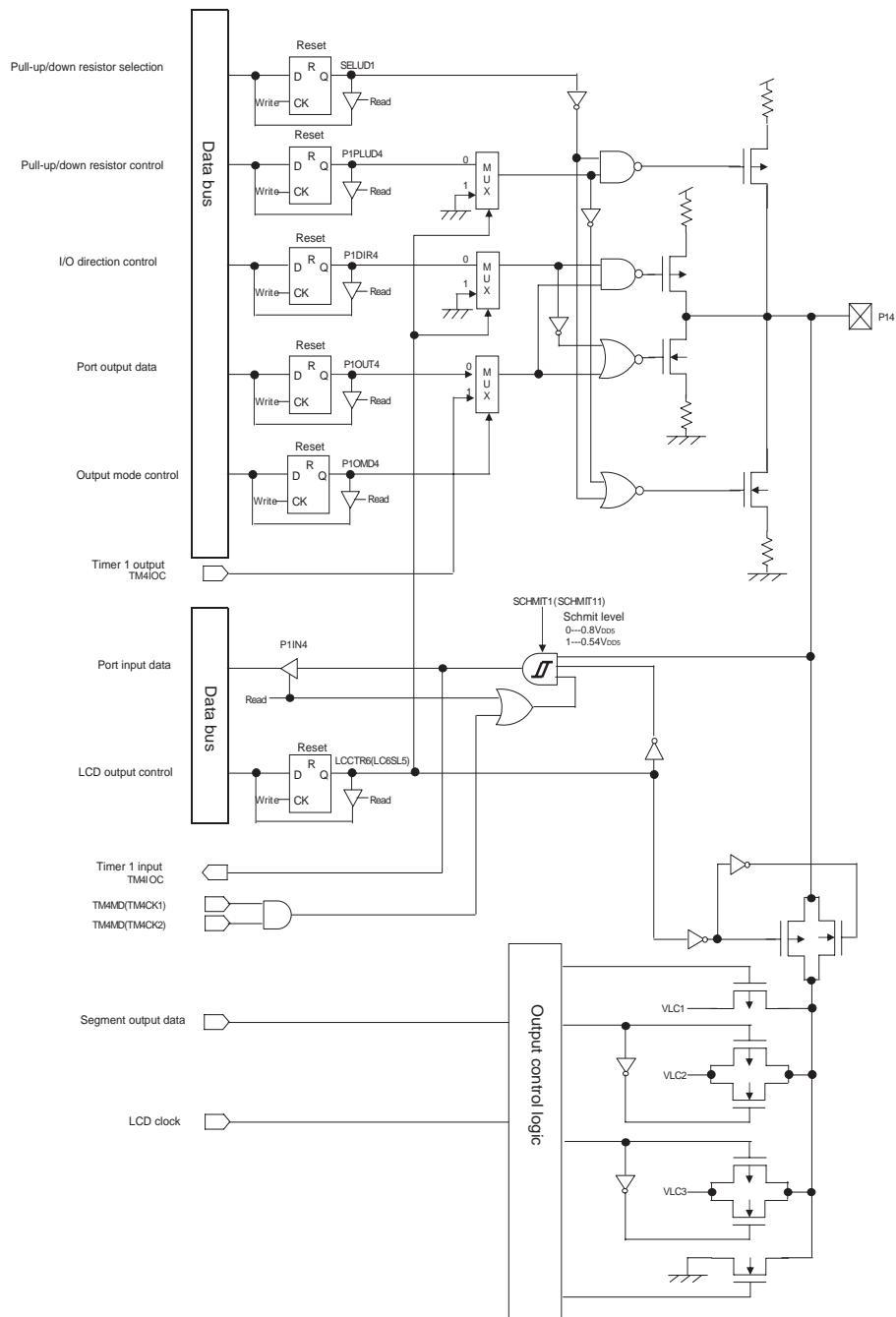


Figure:4.4.5 Block Diagram (P14)

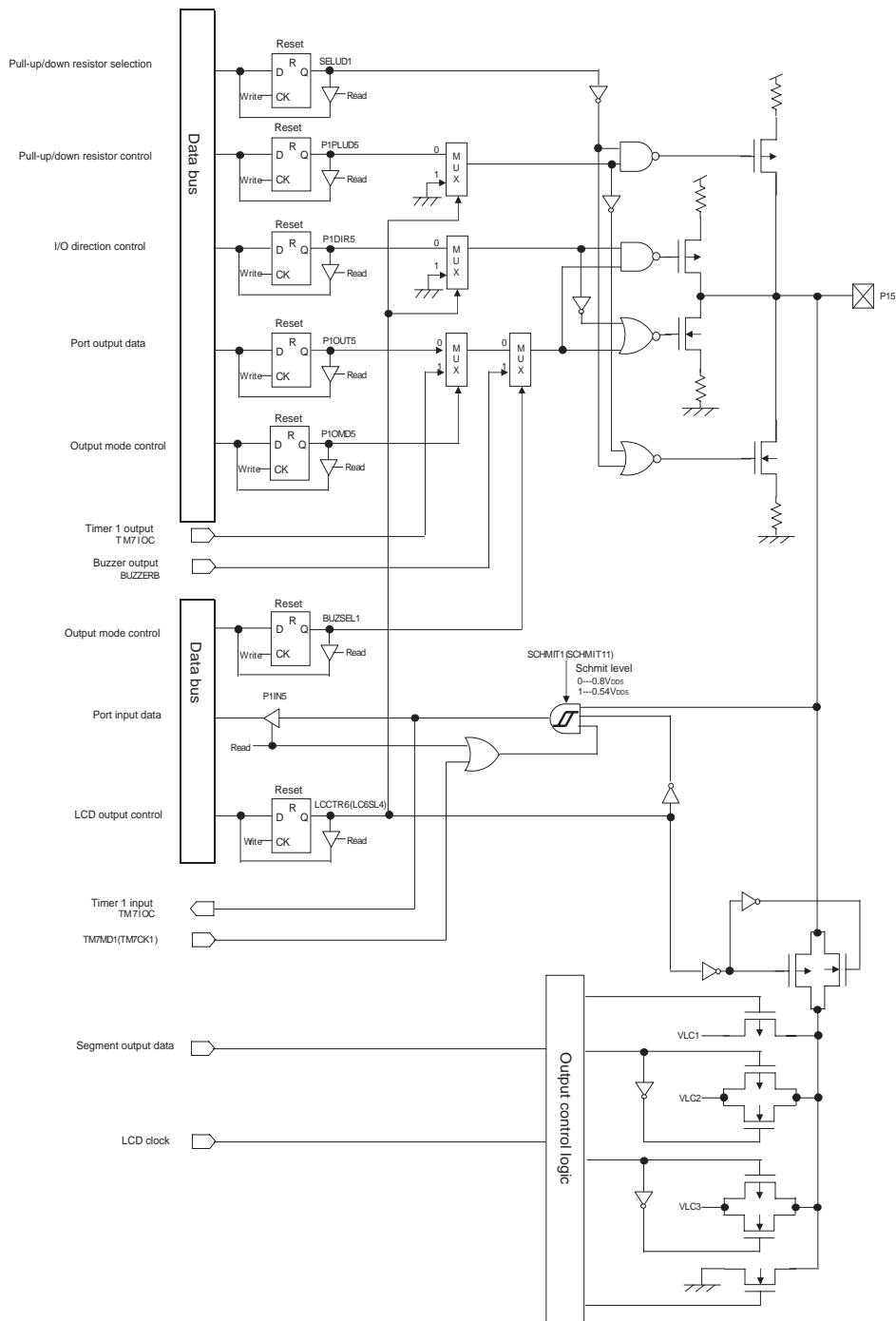


Figure:4.4.6 Block Diagram (P15)

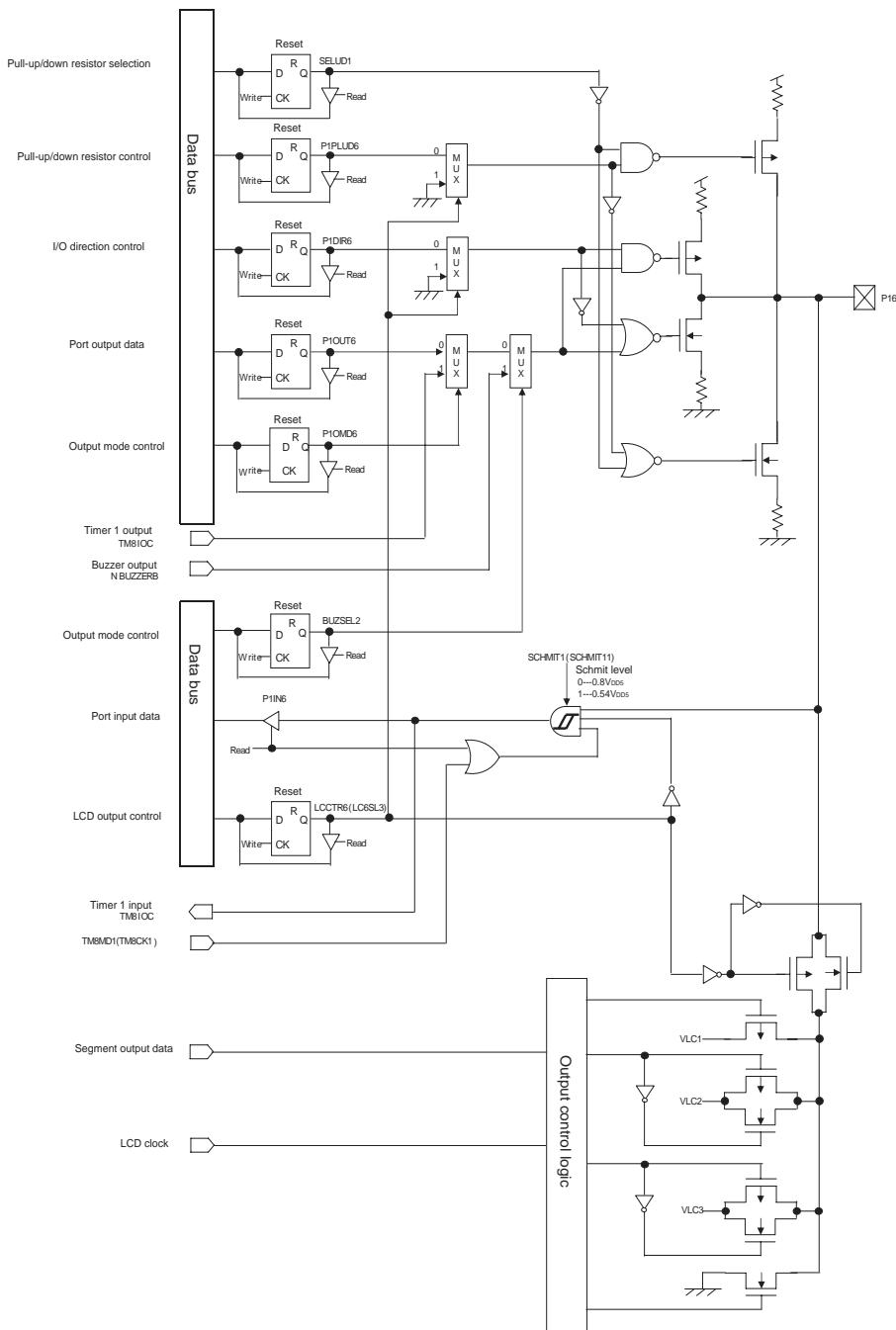


Figure:4.4.7 Block Diagram (P16)

4.5 Port 2

4.5.1 Description

■ General Port Setup

To output data to pins, set the control flag of the port 2 direction control register (P2DIR) to "1" and write the data to the port 2 output register (P2OUT).

To read input data of pins, set the control flag of the port 2 direction control register (P2DIR) to "0" and read the value of the port 2 input register (P2IN). Each bit can be set individually as either an input or output by the port 2 I/O direction control register (P2DIR). The control flag of the port 2 direction control register (P2DIR) is set to "1" for output mode, and "0" for input mode.

Added/non-added of the pull-up (or pull-down) resistor of each bit can be set by the port 2 pull-up resistor control register (P2PLUD). Set the control flag of the port 2 pull-up/pull-down resistor control register (P2PLUD) to "1" to add the pull-up (or pull-down) resistor.

Port 2 can be selected to add pull-up or pull-down resistor by bp2 of the pull-up/pull-down resistor selection register (SELUD).

P27 is the reset pin. To add soft reset, write "0" to bp7 of the port 2 output register (P2OUT). P27 is always added of pull-up resistor.

■ Special Function Pin Setup

P20 to P24 are also used as the external interrupt pin.

P20, 21 is also used as input pin of the AC zero-cross. To use the detection function of AC zero-cross, set the bp7, 3 of the AC zero-cross detection interrupt control register (ACZCTR) to "1", and read out the value of port 2 input register (P2IN).

P20 to P24 are also used as LCD segment output pin. SEG 54 to 50 pins can be selected when the flag of the bp6 to 2 of the LCD output control register 7 (LCCTR7). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

4.5.2 Registers

Table:4.5.1 shows the registers that control the port 2.

Table:4.5.1 Port 2 Control Register

Registers	Address	R/W	Function	Page
P2OUT	0x03F12	R/W	Port 2 output register	IV-39
P2IN	0x03F22	R	Port 2 input register	IV-40
P2DIR	0x03F32	R/W	Port 2 direction control register	IV-40
P2PLUD	0x03F42	R/W	Port 2 pull-up/pull-down resistor control register	IV-40
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-41
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-42

R/W:Readable/Writable

- Port 2 Output Register (P2OUT: 0x03F12)

bp	7	6	5	4	3	2	1	0
Flag	P2OUT7	-	-	P2OUT4	P2OUT3	P2OUT2	P2OUT1	P2OUT0
At reset	1	-	-	x	x	x	x	x
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	P2OUT7	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)
6-5	-	-
4-0	P2OUT4-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 2 Input Register (P2IN: 0x03F22)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0
At reset	-	-	-	x	x	x	x	x
Access	-	-	-	R	R	R	R	R

bp	Flag	Description
7-5	-	-
4-0	P2IN4-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 2 Direction Control Register (P2DIR: 0x03F32)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P2DIR4	P2DIR3	P2DIR2	P2DIR1	P2DIR0
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4-0	P2DIR4-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 2 Pull-up/pull-down Resistor Control Register (P2PLUD: 0x03F42)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P2PLUD4	P2PLUD3	P2PLUD2	P2PLUD1	P2PLUD0
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4-0	P2PLUD4-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.5.3 Block Diagram

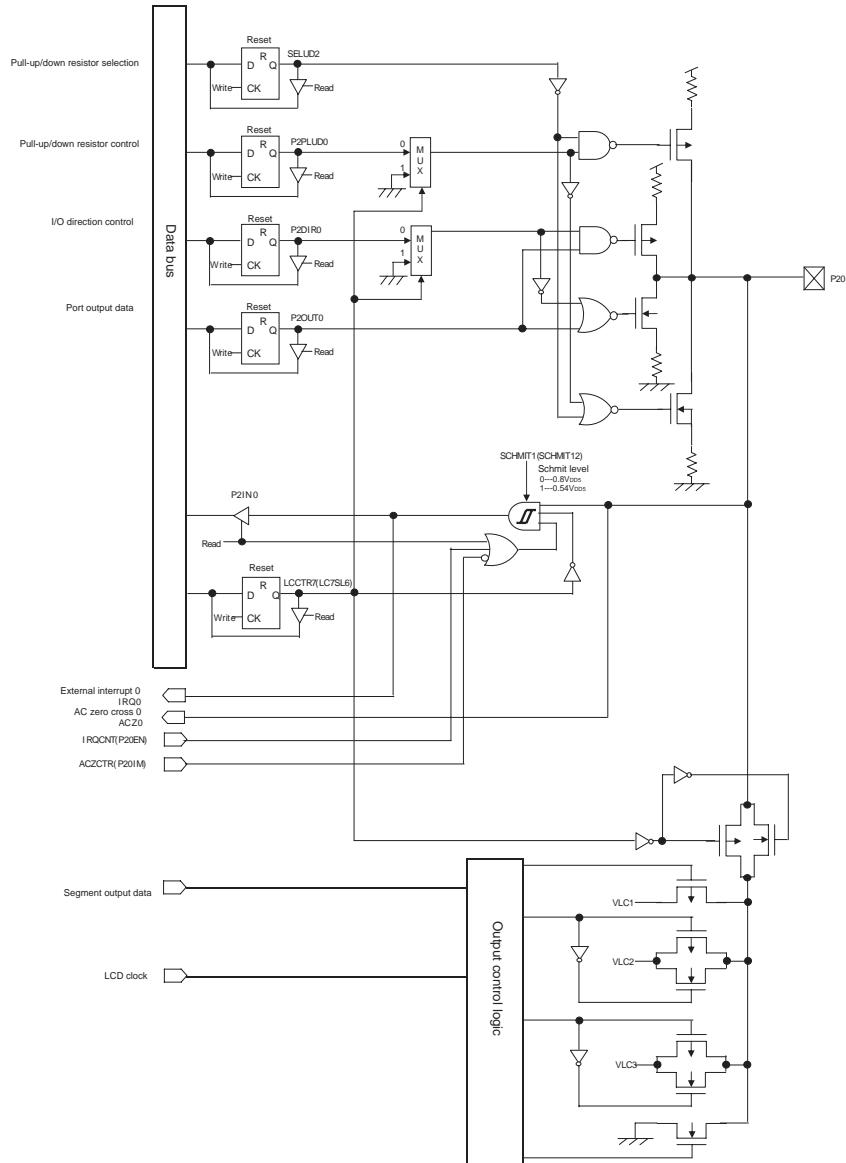


Figure:4.5.1 Block Diagram (P20)

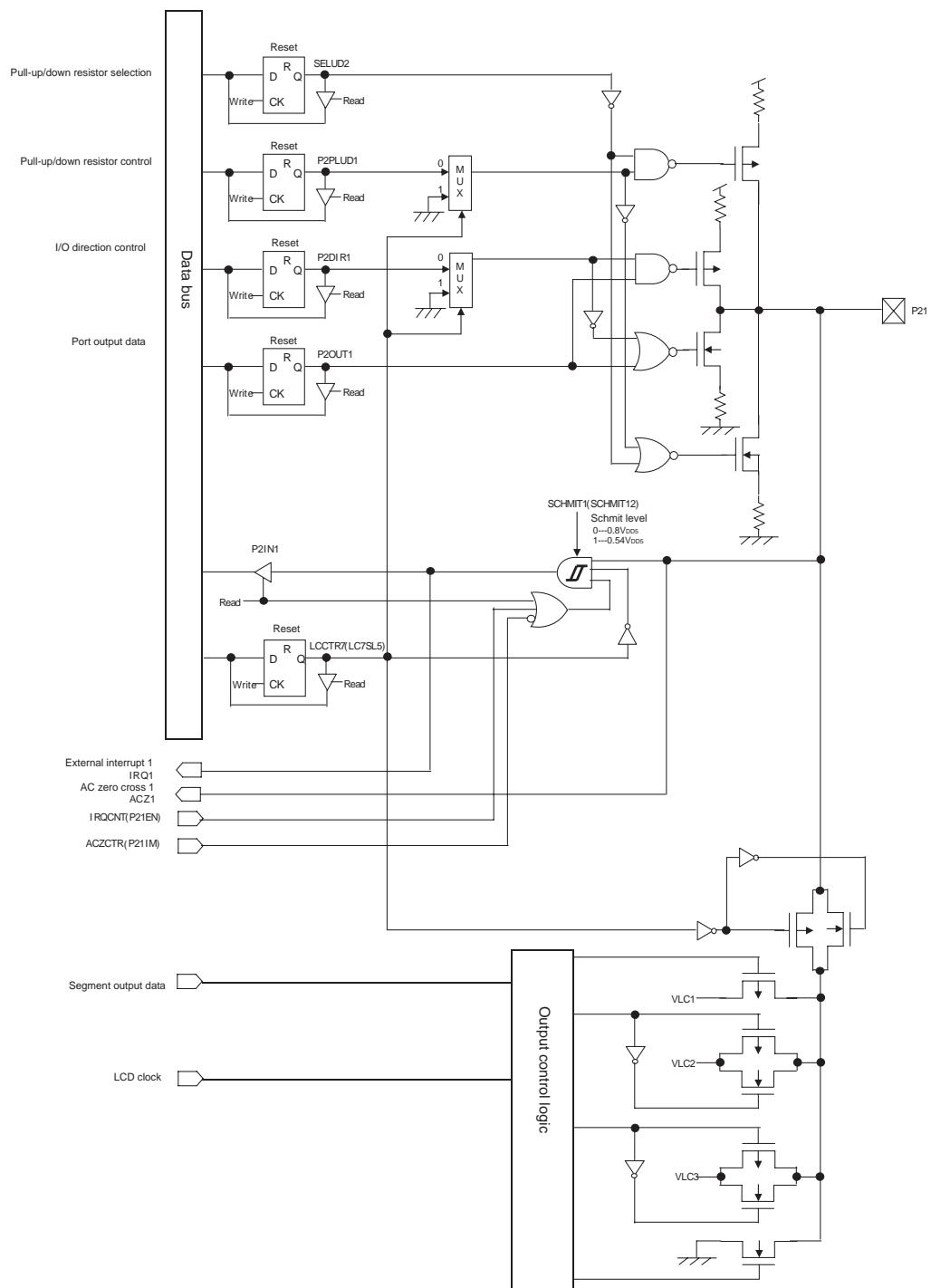


Figure:4.5.2 Block Diagram (P21)

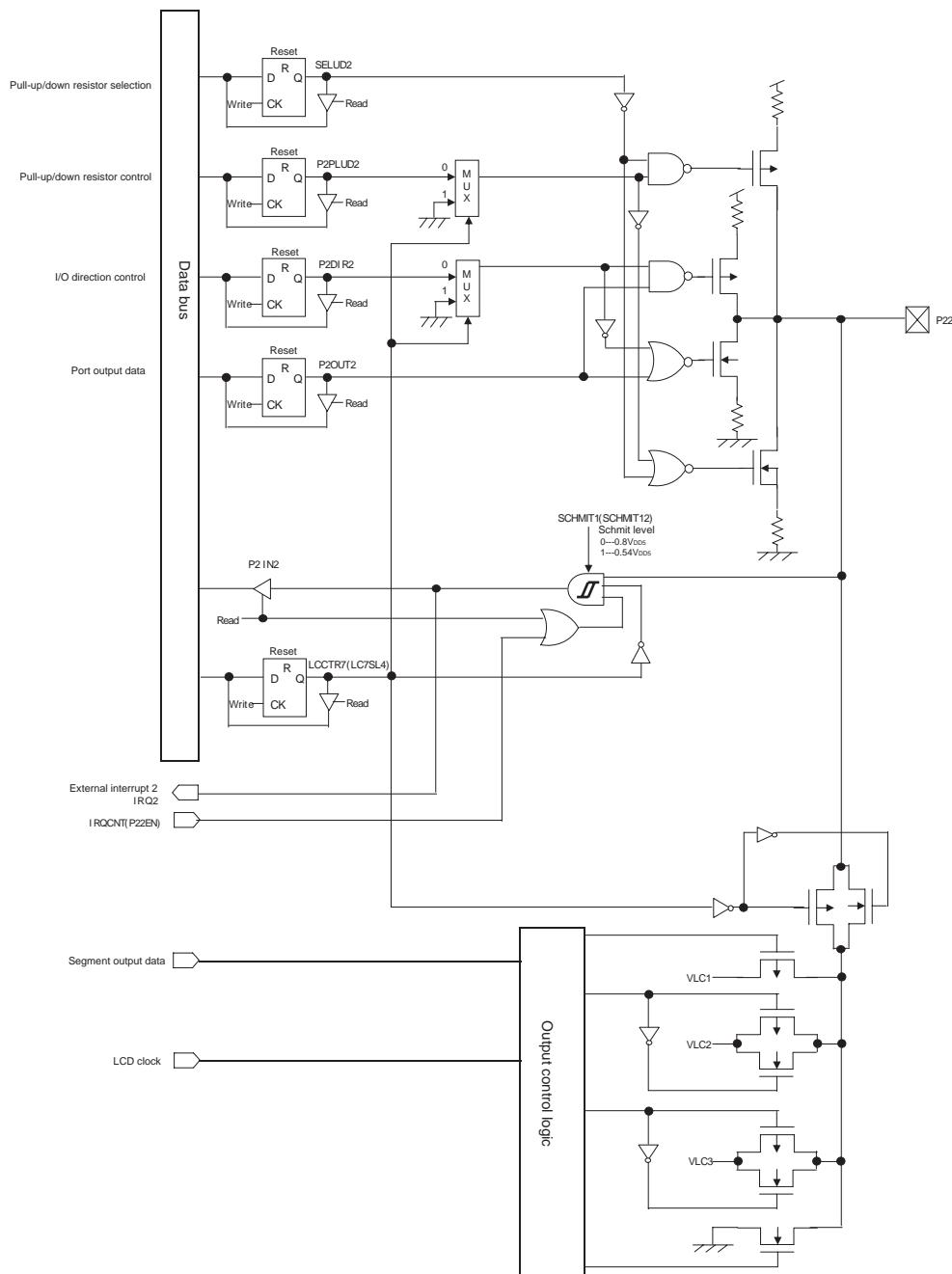


Figure:4.5.3 Block Diagram (P22)

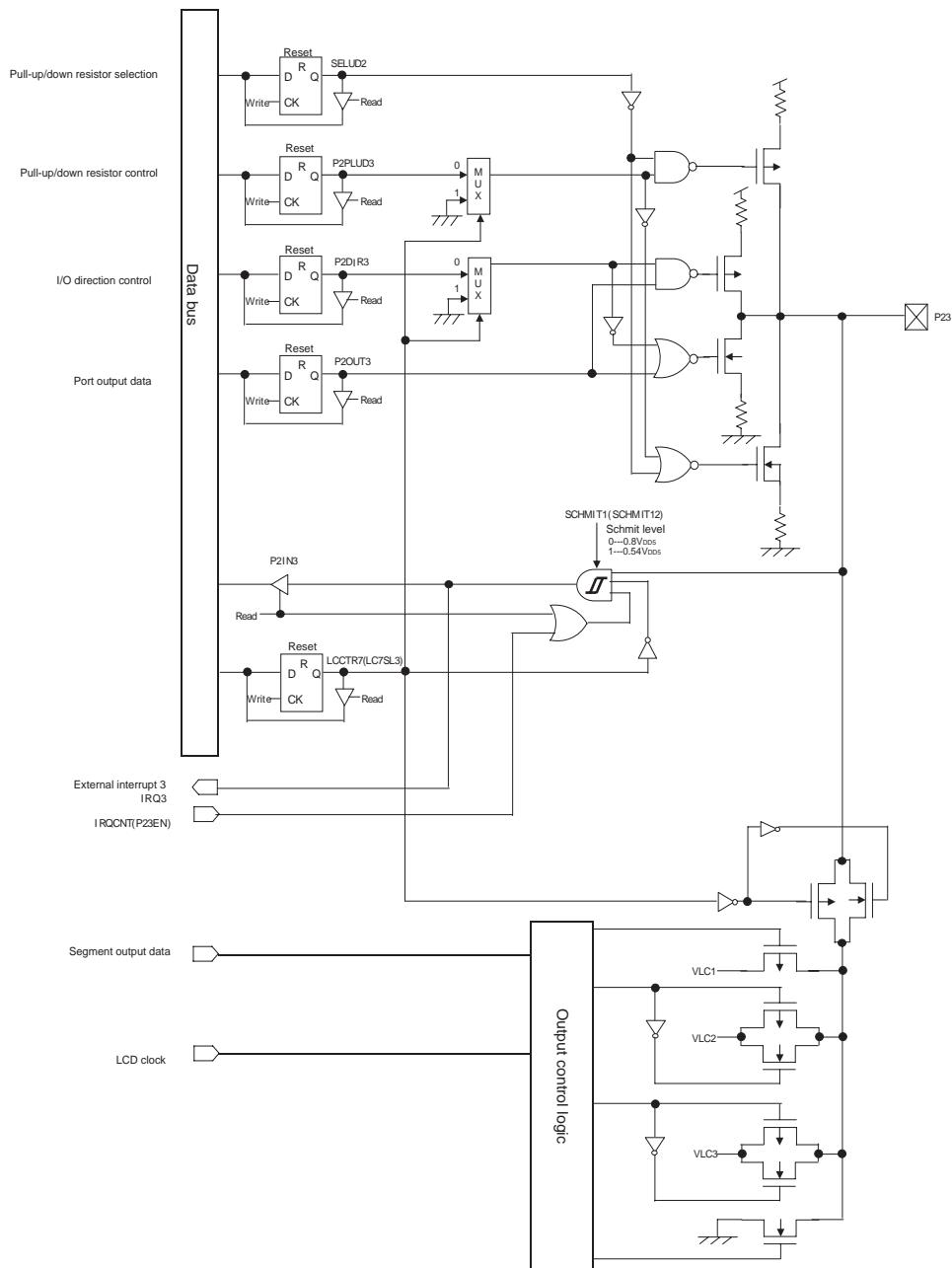


Figure:4.5.4 Block Diagram (P23)

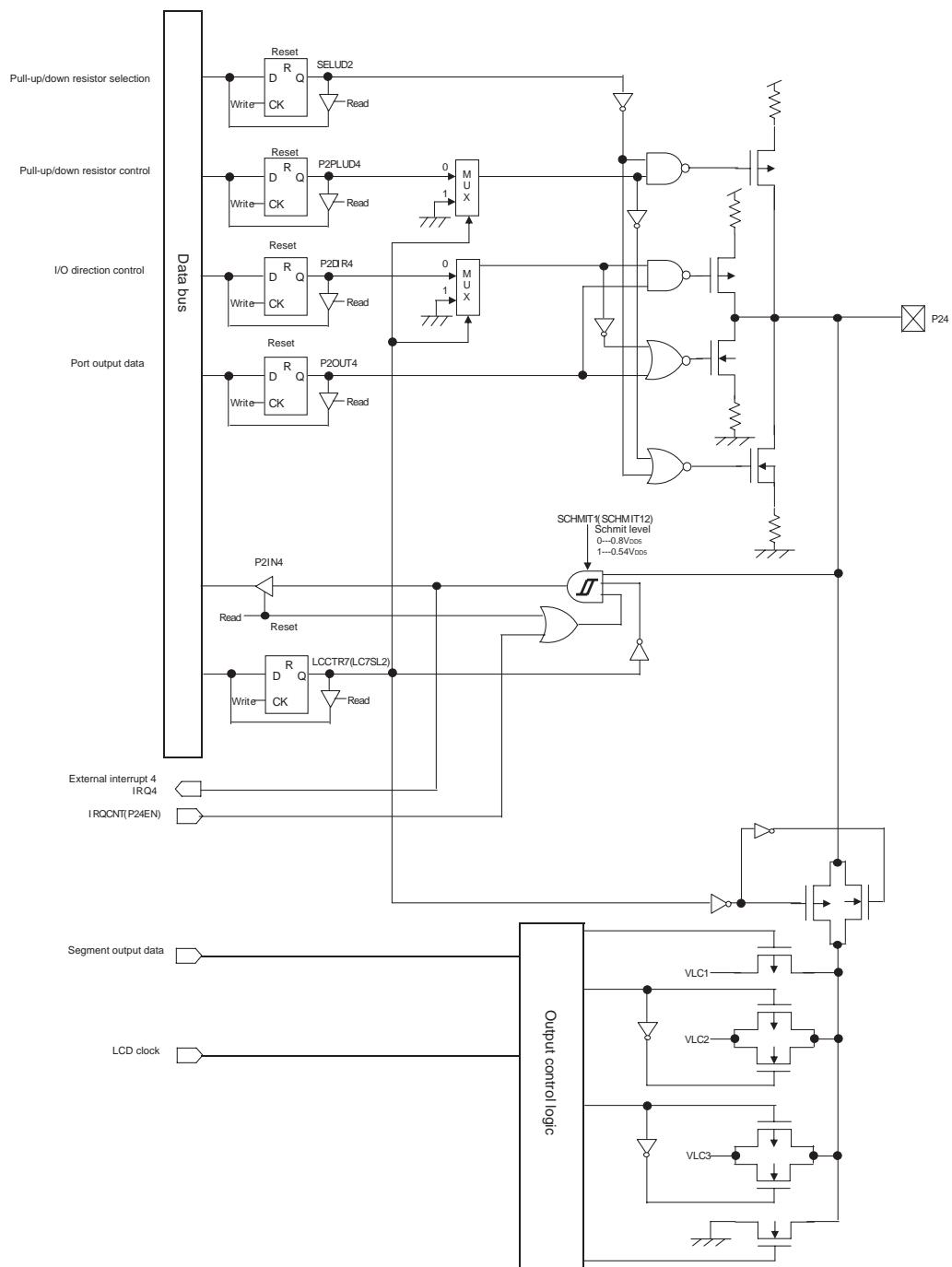


Figure:4.5.5 Block Diagram (P24)

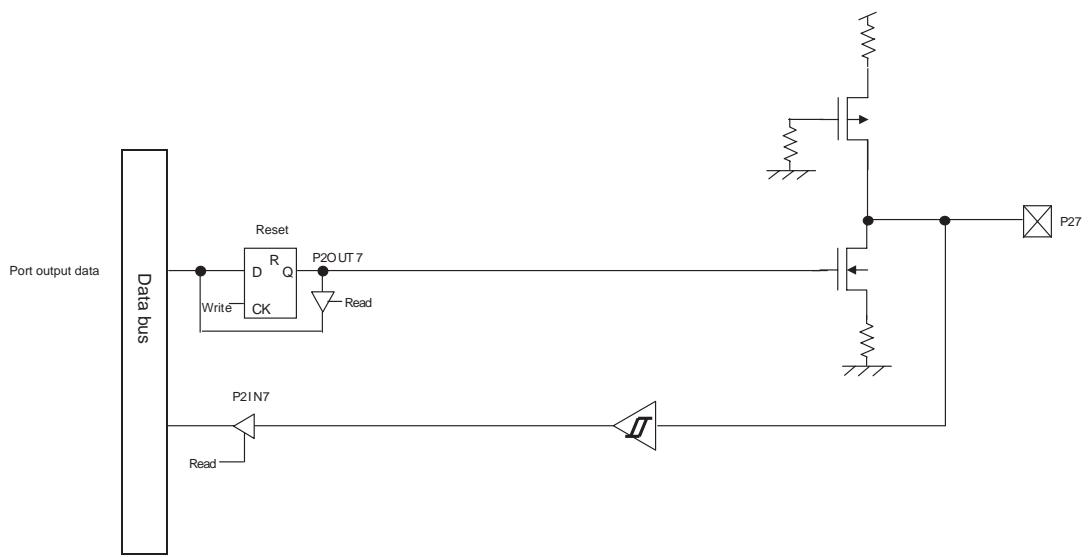


Figure:4.5.6 Block Diagram (P27)

4.6 Port 3

4.6.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 3 direction control register (P3DIR) to “1” and write the value of the port 3 output register (P3OUT).

To read input data of pin, set the control flag of the port 3 direction control register (P3DIR) to “0” and read the value of the port 3 input register (P3IN).

Each bit can be set individually as either an input or output by the port 3 I/O direction control register (P3DIR). The control flag of the port 3 direction control register (P3DIR) is set to “1” for output mode, and “0” for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 3 pull-up/pull-down resistor control register (P3PLUD). Set the control flag of the port 3 pull-up/pull-down resistor control register (P3PLUD) to “1” to add pull-up (or pull-down) resistor.

Port 3 can be selected to add pull-up or pull-down resistor by bp3 of the pull-up/pull-down resistor selection register (SELUD).

For P30, P32, P33, and P34, each bit can be selected individually as Nch open-drain output by the port 3 Nch open-drain control register (P3ODC). The port 3 Nch open-drain control register (P3ODC) is set to “1” for Nch open-drain output, and “0” for push-pull output.

■ Special Function Pin Setup

P30 to P36 are also used as LCD segment output pin. SEG 42 to 36 pins can be selected when the flag of the bp2 to 0 of the LCD output control register 6 (LCCTR6) and the flag of the bp7 to 4 of the LCD output control register 5 (LCCTR5). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P30 is also used as the I/O pin of serial 2 transmission/reception data and the output pin of UART 2 transmission data. When the SC2SBOS flag of the serial interface 2 mode register 1 (SC2MD1) is “1”, P30 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 3 Nch open-drain control register (P3ODC) output can be selected by setting the Port 0 Nch open-drain control register (P3ODC).

P31 is also used as the input pin of the serial 2 reception data and UART 2 reception data. When the SC2SBIS flag of the serial interface 2 mode register 1 (SC2MD1) is “1”, P31 is the input pin of serial data.

P32 is also used as the I/O pin of serial 2 clock. When the SC2SBTS flag of the serial interface 2 mode register 1 (SC2MD1) is “1”, P32 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 3 Nch open-drain control register (P3ODC).

P33 is also used as the I/O pin of serial 4 transmission/reception data and the IIC4 transmission/reception data. When the SC4SBOS flag of the serial interface 4 mode register 1 (SC4MD1) is “1”, P33 is the serial data I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 3 Nch open-drain control register (P3ODC).

P34 is also used as the I/O pin of serial 4 clock transmission/reception data and the output pin of IIC4 clock transmission data. When the SC4SBTS flag of the serial interface 4 mode register 1 (SC4MD1) is “1”, P34 is the serial data I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 3 Nch open-drain control register (P3ODC).

P35 is also used as the input pin of the serial 4 reception data. When the SC4SBIS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", P35 is the input pin of serial data.

4.6.2 Registers

Table:4.6.1 shows registers that control the port 3.

Table:4.6.1 Port 3 Control Register

Registers	Address	R/W	Function	Page
P3OUT	0x03F13	R/W	Port 3 output register	IV-51
P3IN	0x03F23	R	Port 3 input register	IV-52
P3DIR	0x03F33	R/W	Port 3 direction control register	IV-52
P3PLUD	0x03F43	R/W	Port 3 pull-up/pull-down resistor control register	IV-52
P3ODC	0x03EF1	R/W	Port 3 Nch open-drain control register	IV-53
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-54
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-55

R/W:Readable/Writable

- Port 3 Output Register (P3OUT: 0x03F13)

bp	7	6	5	4	3	2	1	0
Flag	-	P3OUT6	P3OUT5	P3OUT4	P3OUT3	P3OUT2	P3OUT1	P3OUT0
At reset	-	x	x	x	x	x	x	x
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P3OUT6-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 3 Input Register (P3IN: 0x03F23)

bp	7	6	5	4	3	2	1	0
Flag	-	P3IN6	P3IN5	P3IN4	P3IN3	P3IN2	P3IN1	P3IN0
At reset	-	x	x	x	x	x	x	x
Access	-	R	R	R	R	R	R	R

bp	Flag	Description
7	-	-
6-0	P3IN6-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 3 Direction Control Register (P3DIR: 0x03F33)

bp	7	6	5	4	3	2	1	0
Flag	-	P3DIR6	P3DIR5	P3DIR4	P3DIR3	P3DIR2	P3DIR1	P3DIR0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P3DIR6-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 3 Pull-up/Pull-down Resistor Control Register (P3PLUD: 0x03F43)

bp	7	6	5	4	3	2	1	0
Flag	-	P3PLUD6	P3PLUD5	P3PLUD4	P3PLUD3	P3PLUD2	P3PLUD1	P3PLUD0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P3PLUD6-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 3 Nch Open-drain Control Register (P3ODC:0x03EF1)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P3ODC4	P3ODC3	P3ODC2	-	P3ODC0
At reset	-	-	-	0	0	0	-	0
Access	-	-	-	R/W	R/W	R/W	-	R/W

bp	Flag	Description
7-5	-	-
4-2	P3ODC4-2	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
1	-	-
0	P3ODC0	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.6.3 Block Diagram

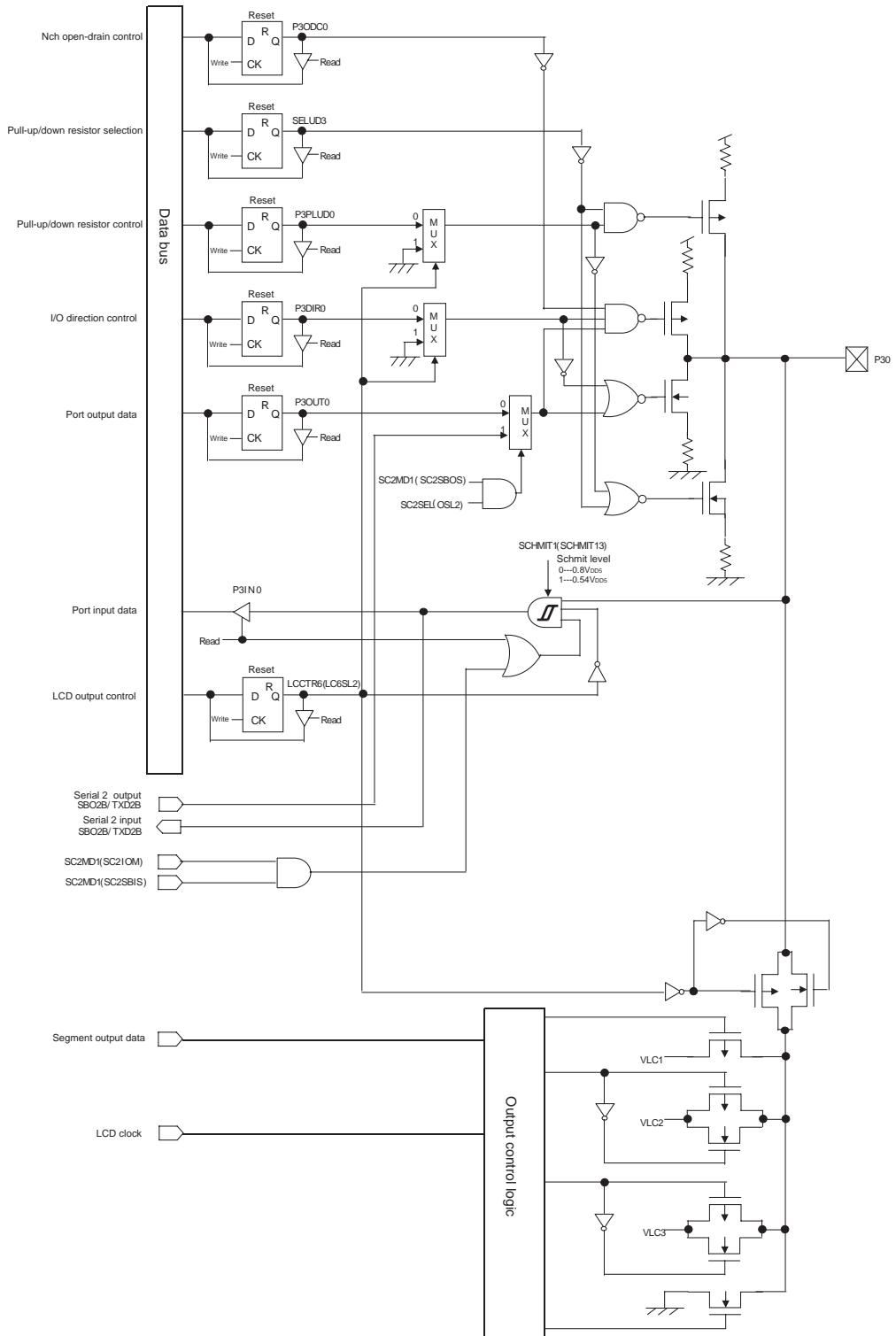


Figure:4.6.1 Block Diagram (P30)

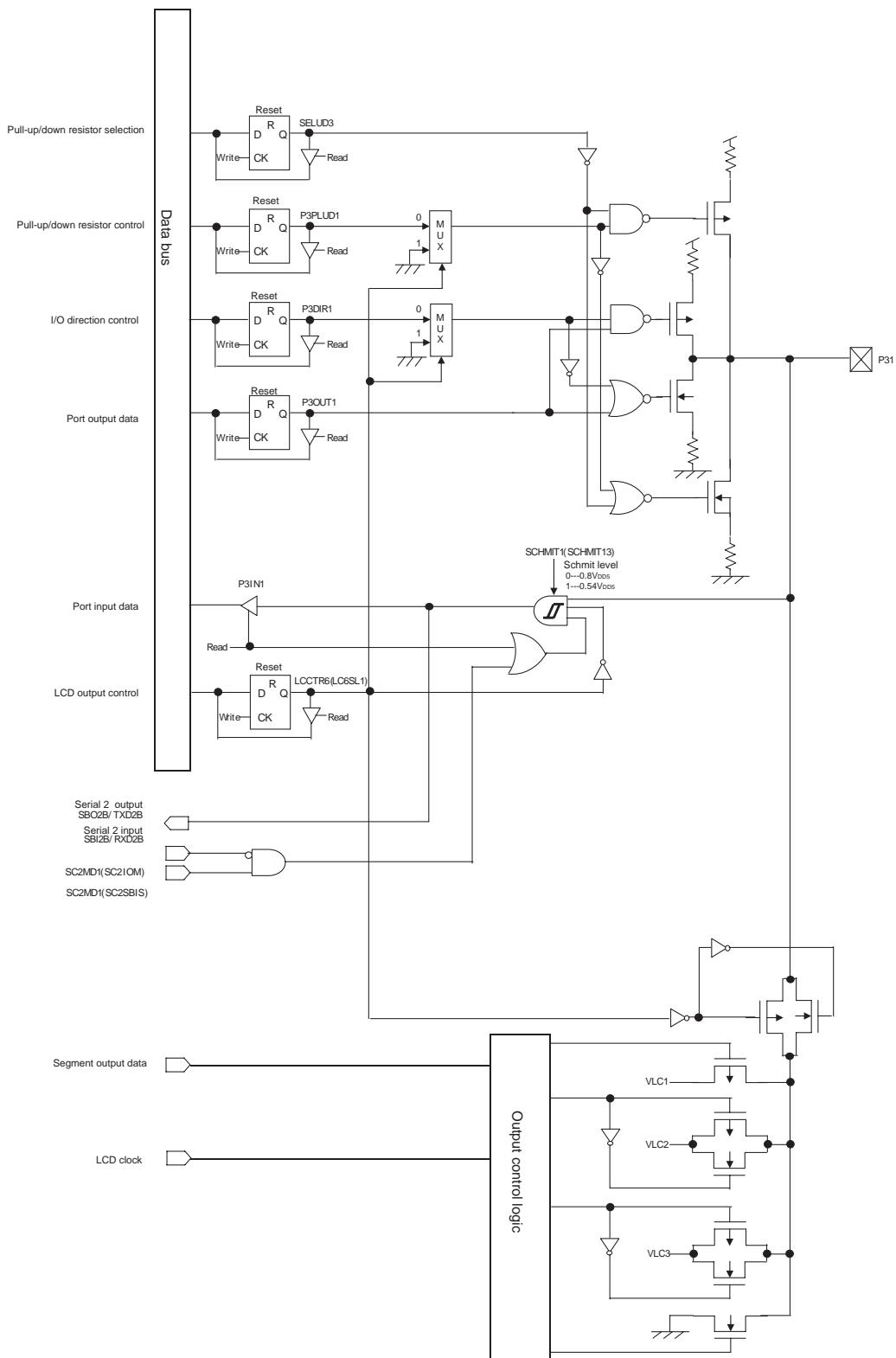


Figure:4.6.2 Block Diagram (P31)

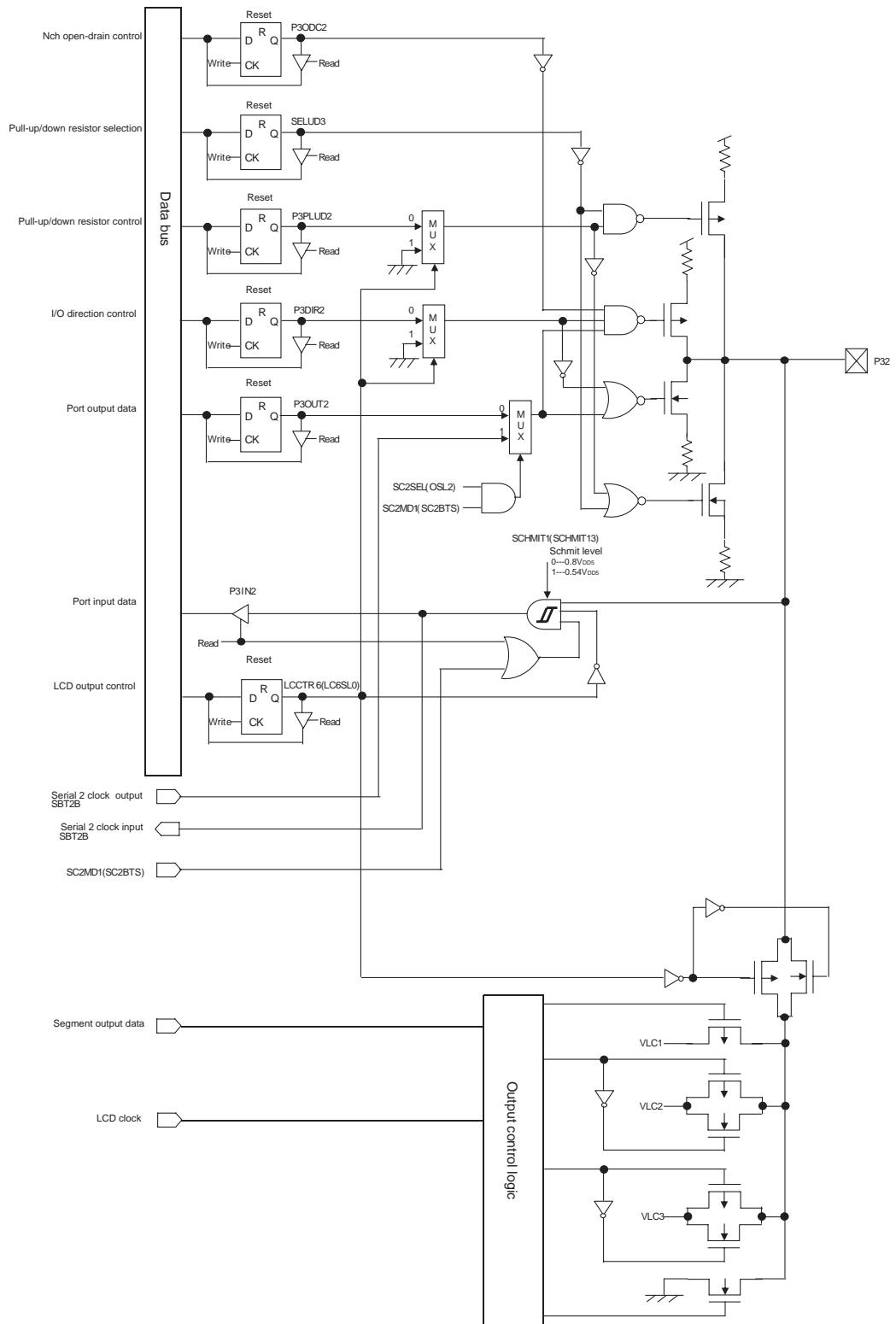


Figure:4.6.3 Block Diagram (P32)

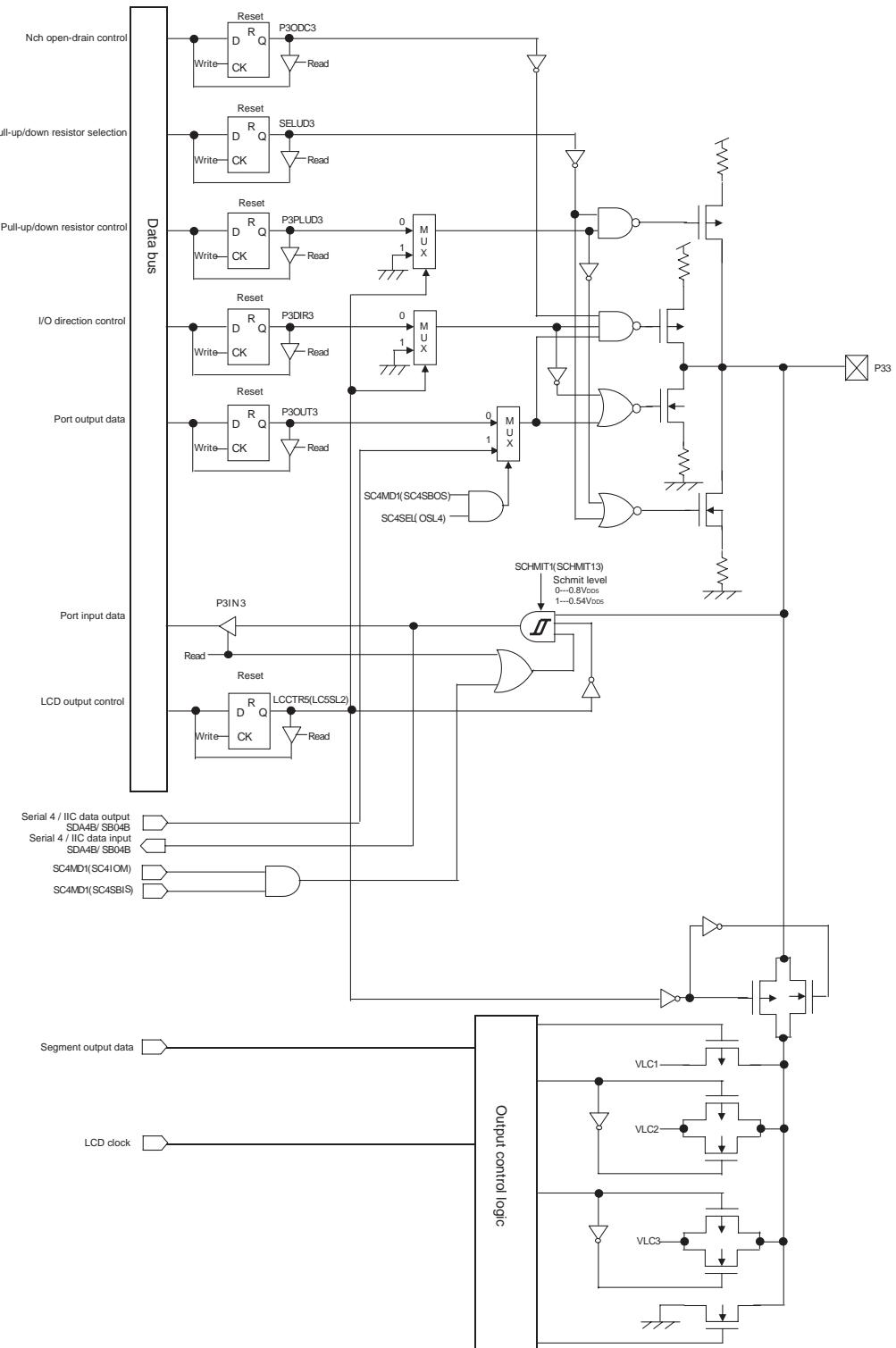


Figure:4.6.4 Block Diagram (P33)

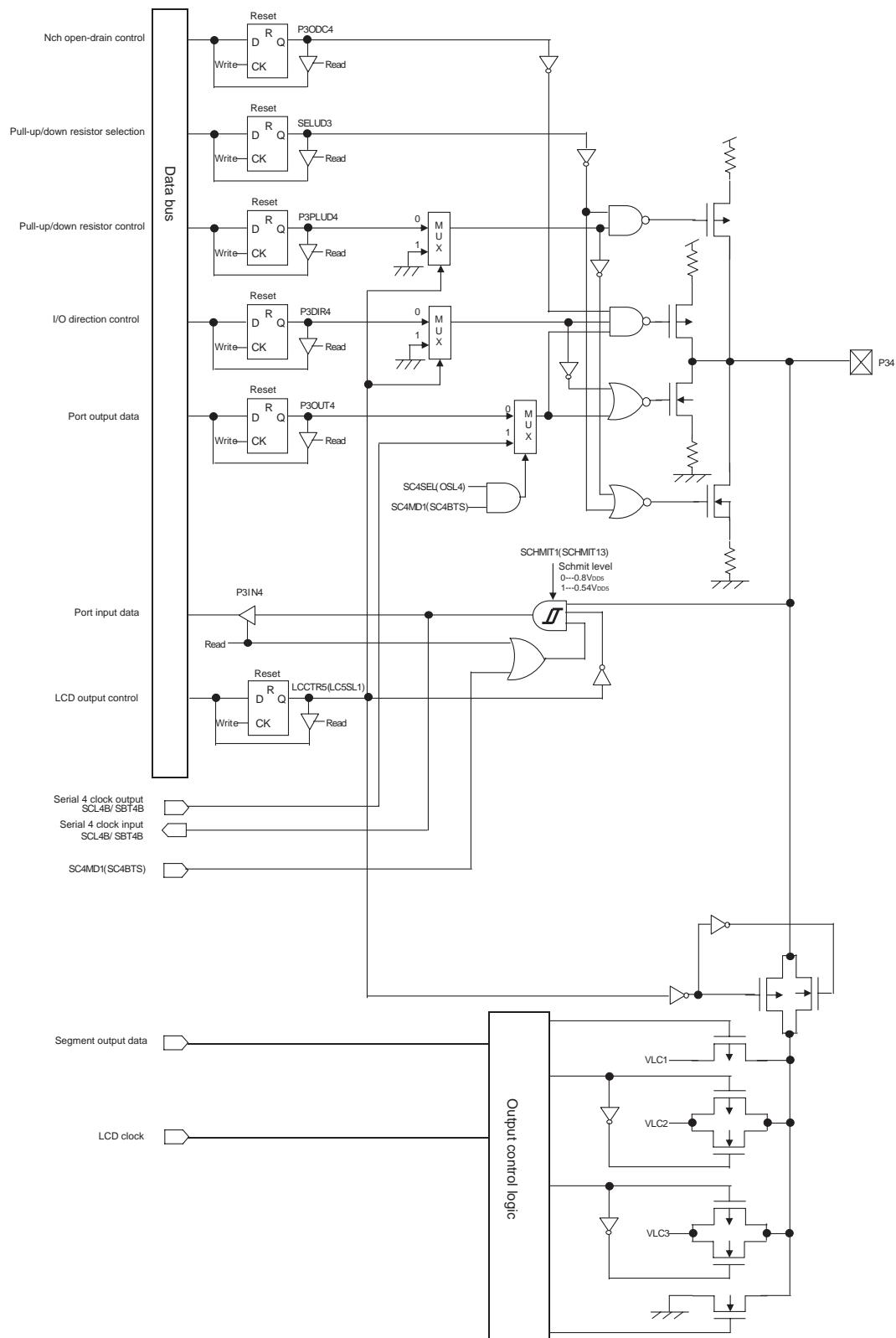


Figure:4.6.5 Block Diagram (P34)

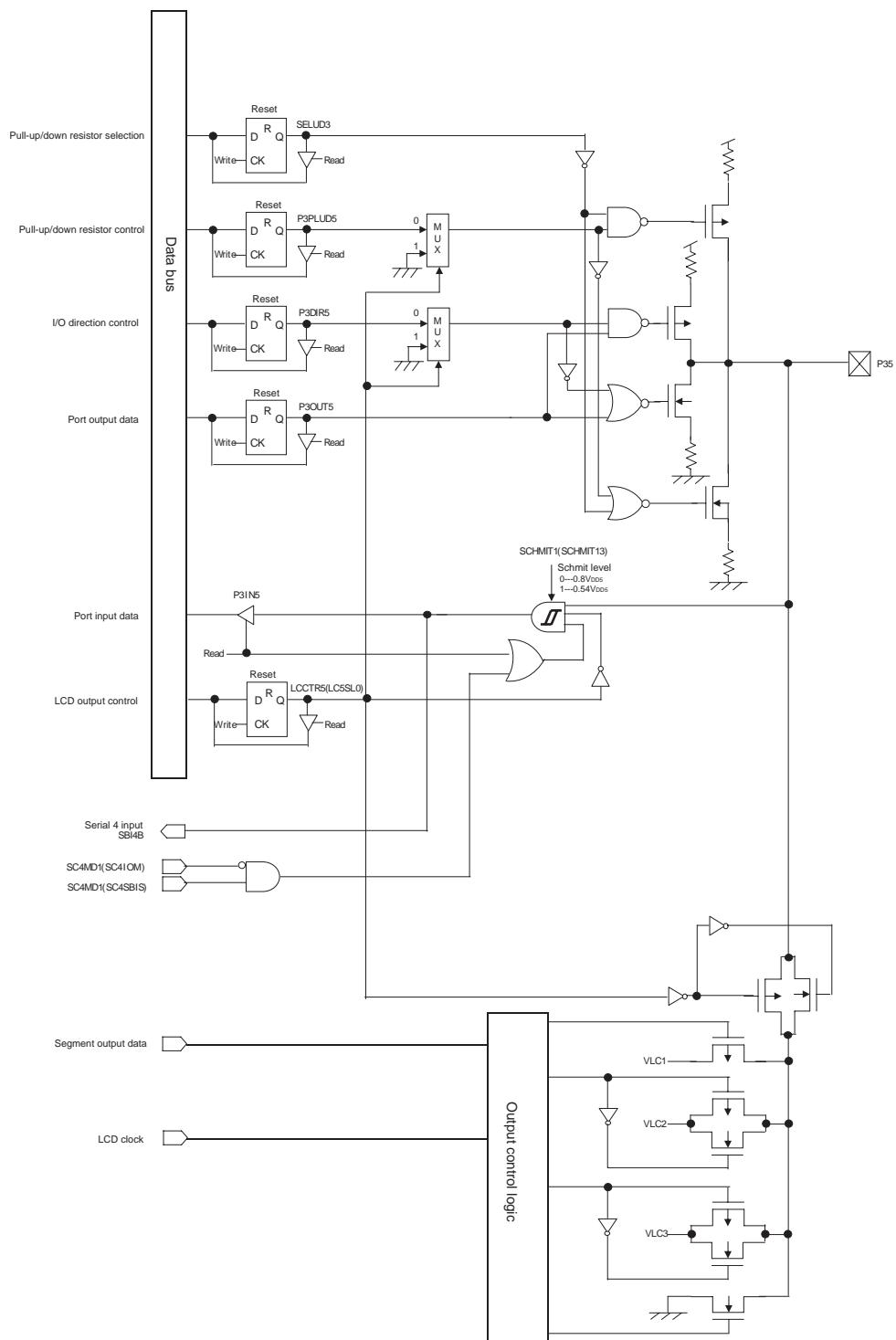


Figure:4.6.6 Block Diagram (P35)

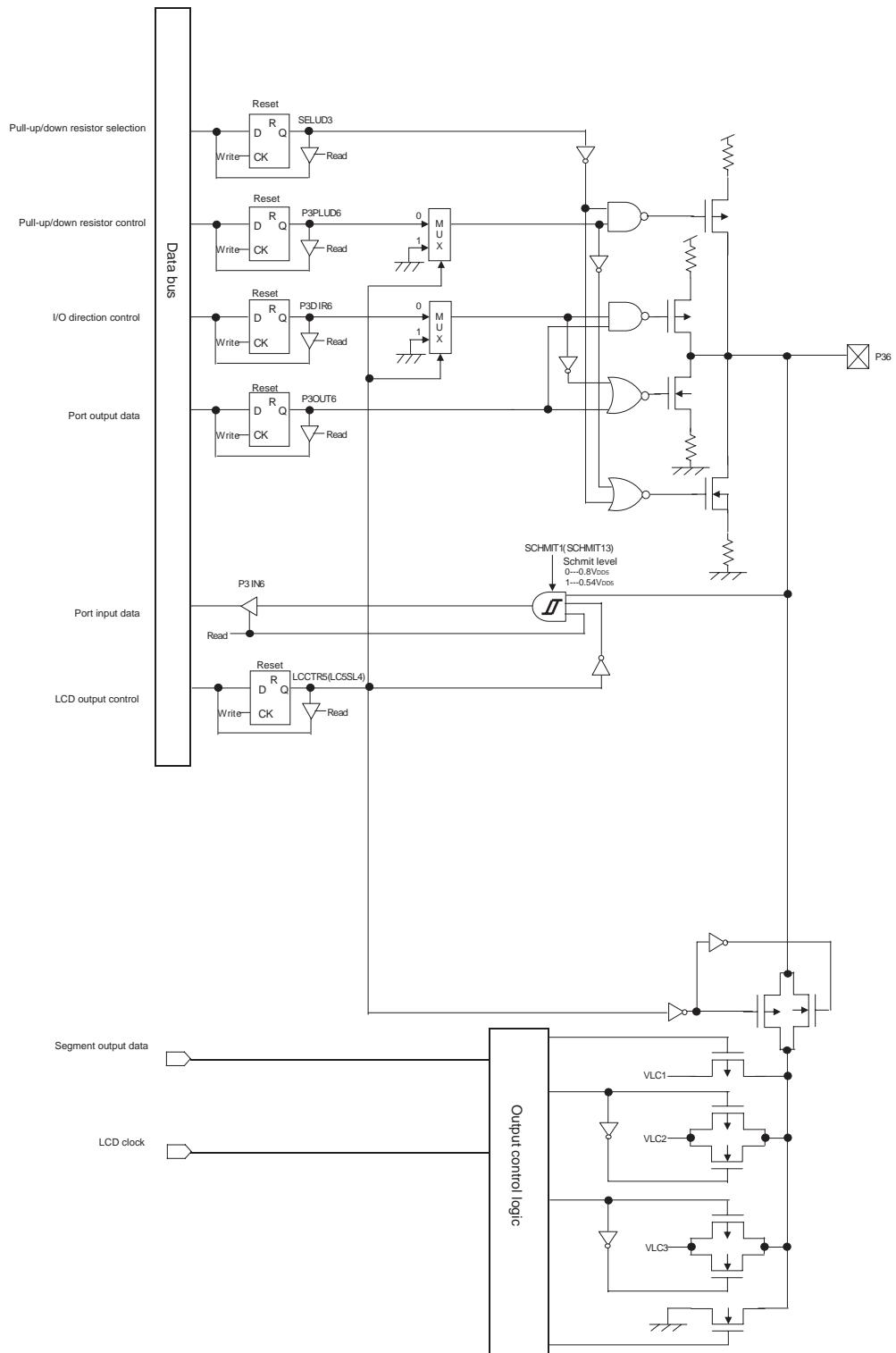


Figure:4.6.7 Block Diagram (P36)

4.7 Port 4

4.7.1 Description

■ General Port Setup

To output data to pins, set the control flag of the port 4 direction control register (P4DIR) to "1" and write the data to the port 4 output register (P4OUT).

To read input data of pins, set the control flag of the port 4 direction control register (P4DIR) to "0" and read the value of the port 4 input register (P4IN).

Each bit can be set individually as either an input or output by the port 4 I/O direction control register (P4DIR). The control flag of the port 4 direction control register (P4DIR) is set to "1" for output mode, and "0" for input mode.

Added/non-added of the pull-up resistor of each bit can be set by the port 4 pull-up or pull-down resistor control register (P4PLUD). Set the control flag of the port 4 pull-up or pull-down resistor control register (P4PLUD) to "1" to add the pull-up or pull-down resistor.

Port 4 can be selected to add pull-up or pull-down resistor by bp4 of the pull-up/pull-down resistor selection register (SELUD).

For P40, P42 to P43 and P45 to P47 each bit can be selected individually as Nch open-drain output by the port 4 Nch open-drain control register (P4ODC). The port 4 Nch open-drain control register (P4ODC) is set to "1" for Nch open-drain output, and "0" for push-pull output.

■ Special Function Pin Setup

P40 to P47 are also used as LCD segment output pin. SEG 35 to 28 pins can be selected when the flag of the bp3 to 0 of the LCD output control register 5 (LCCTR5) and the flag of the bp7 to 4 of the LCD output control register 4 (LCCTR4). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P40 is also used as the I/O pin of serial 3 transmission/reception data and the output pin of UART 3 transmission data. When the SC3SBOS flag of the serial interface 3 mode register 1 (SC3MD1) is "1", P40 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 4 Nch open-drain control register (P4ODC).

P41 is also used as the input pin of the serial 3 reception data and UART 3 reception data. When the SC3SBIS flag of the serial interface 3 mode register 1 (SC3MD1) is "1", P41 is the input pin of serial data.

P42 is also used as the I/O pin of serial 3 clock. When the SC0SBTS flag of the serial interface 3 mode register 1 (SC3MD1) is "1", P42 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 4 Nch open-drain control register (P4ODC).

P43 is also used as the I/O pin of serial 0 transmission/reception data and the output pin of UART0 transmission data. When the SC0SBOS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P43 is the serial data I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 4 Nch open-drain control register (P4ODC).

P44 is also used as the input pin of serial 0 reception data and the UART0 reception data. When the SC0SBIS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P44 is the serial data I/O pin.

P45 is also used as the I/O pin of the serial 0 clock data. When the SC0SBTS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P45 is the I/O pin of serial clock. Push-pull output or Nch open-drain output can be selected by setting the Port 4 Nch open-drain control register (P4ODC).

P46 is also used as the I/O pin of the serial 5 transmission/reception data. When the SEL12C flag or the I2CMON flag of the serial interface 5 address setting register 1 (SC5AD1) is "1", P46 is the I/O pin of serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 4 Nch open-drain control register (P4ODC).

P47 is also used as the serial 5 clock input pin. When the SEL12C flag or the I2CMON flag of the serial interface 5 address setting register 1 (SC5AD1) is "1", P47 is the serial clock input pin. Push-pull output or Nch open-drain output can be selected by setting the Port 4 Nch open-drain control register (P4ODC).

4.7.2 Registers

Table:4.7.1 shows the registers that control the port 4.

Table:4.7.1 Port 4 Control Register

Registers	Address	R/W	Function	Page
P4OUT	0x03F14	R/W	Port 4 output register	IV-65
P4IN	0x03F24	R	Port 4 input register	IV-65
P4DIR	0x03F34	R/W	Port 4 direction control register	IV-66
P4PLUD	0x03F44	R/W	Port 4 pull-up/pull-down resistor control register	IV-66
P4ODC	0x03EF2	R/W	Port 4 Nch open-drain control register	IV-67
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-68
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-69

R/W:Readable/Writable

- Port 4 Output Register (P4OUT: 0x03F14)

bp	7	6	5	4	3	2	1	0
Flag	P4OUT7	P4OUT6	P4OUT5	P4OUT4	P4OUT3	P4OUT2	P4OUT1	P4OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	P4OUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

- Port 4 Input Register (P4IN: 0x03F24)

bp	7	6	5	4	3	2	1	0
Flag	P4IN7	P4IN6	P4IN5	P4IN4	P4IN3	P4IN2	P4IN1	P4IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	P4IN7-0	Input data 0:Pin is L(V _{SS} level) 1:Pin is H(V _{DD5} level)s

■ Port 4 Direction Control Register (P4DIR: 0x03F34)

bp	7	6	5	4	3	2	1	0
Flag	P4DIR7	P4DIR6	P4DIR5	P4DIR4	P4DIR3	P4DIR2	P4DIR1	P4DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P4DIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 4 Pull-up/pull-down Resistor Control Register (P4PLUD: 0x03F44)

bp	7	6	5	4	3	2	1	0
Flag	P4PLUD7	P4PLUD6	P4PLUD5	P4PLUD4	P4PLUD3	P4PLUD2	P4PLUD1	P4PLUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P4PLUD7-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 4 Nch Open-drain Control Register (P4ODC:0x03EF2)

bp	7	6	5	4	3	2	1	0
Flag	P4ODC7	P4ODC6	P4ODC5	-	P4ODC3	P4ODC2	-	P4ODC0
At reset	0	0	0	-	0	0	-	0
Access	R/W	R/W	R/W	-	R/W	R/W	-	R/W

bp	Flag	Description
7-5	P4ODC7-5	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
4	-	-
3-2	P4ODC3-2	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
1	-	-
0	P4ODC0	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.7.3 Block Diagram

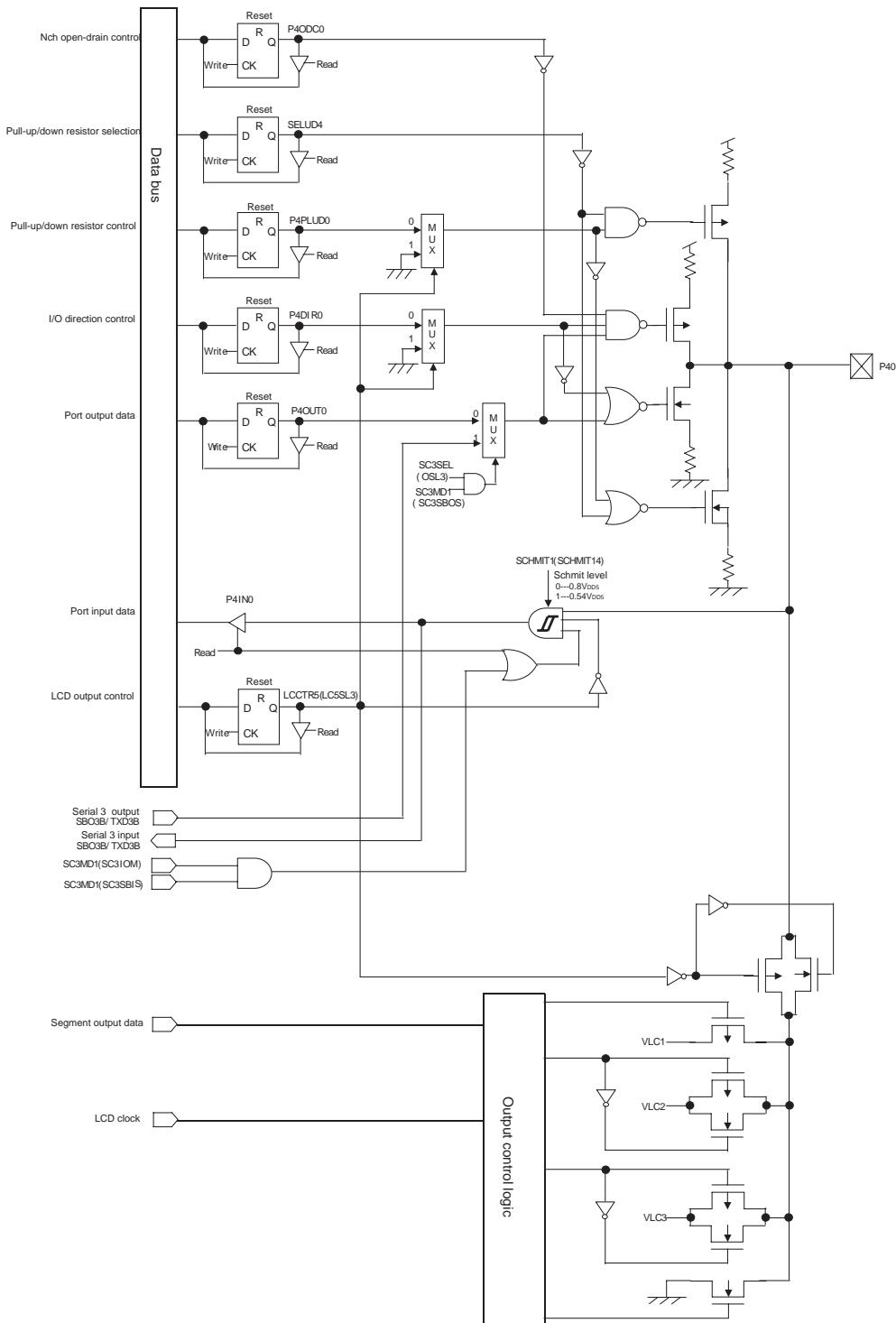


Figure:4.7.1 Block Diagram (P40)

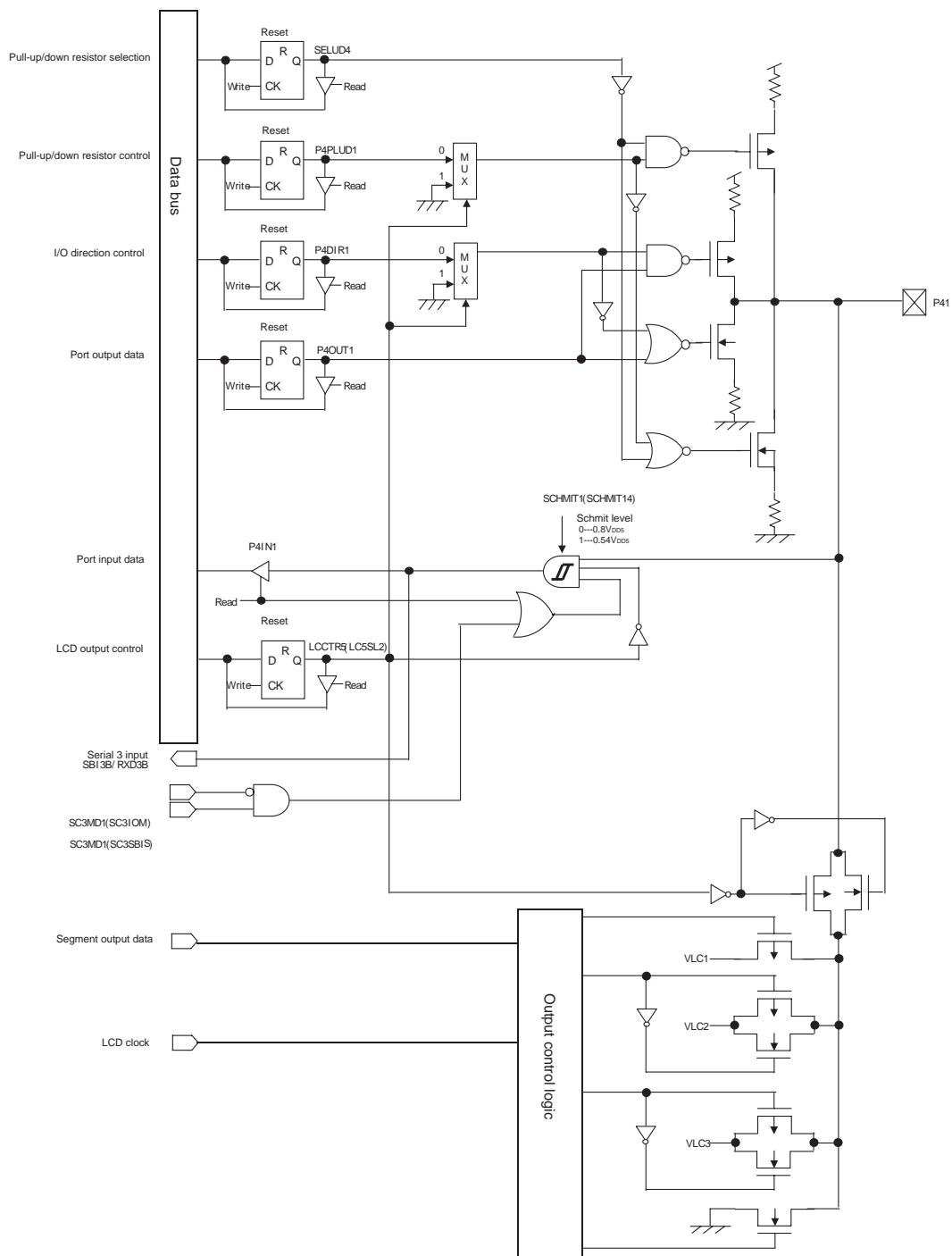


Figure:4.7.2 Block Diagram (P41)

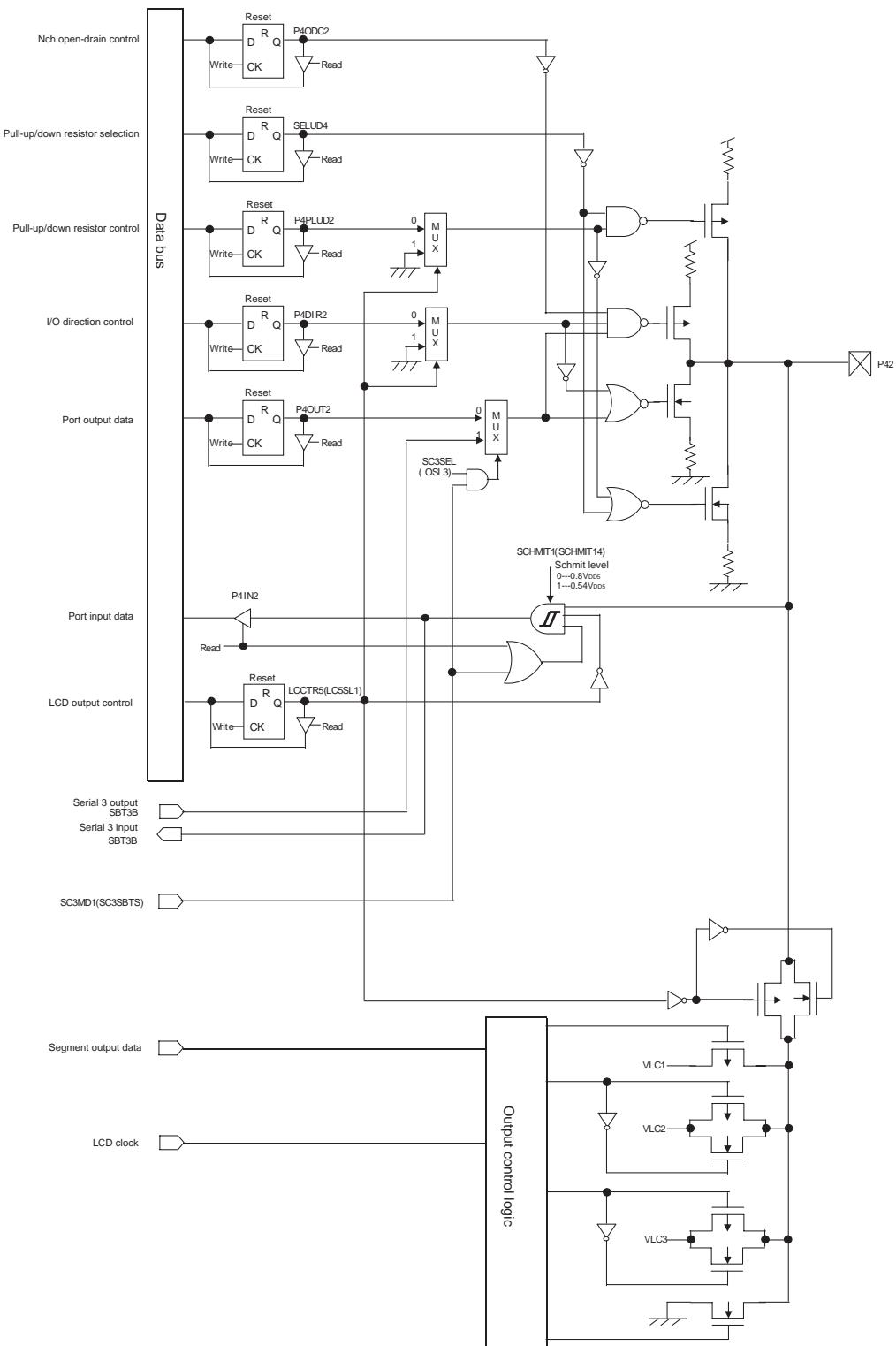


Figure:4.7.3 Block Diagram (P42)

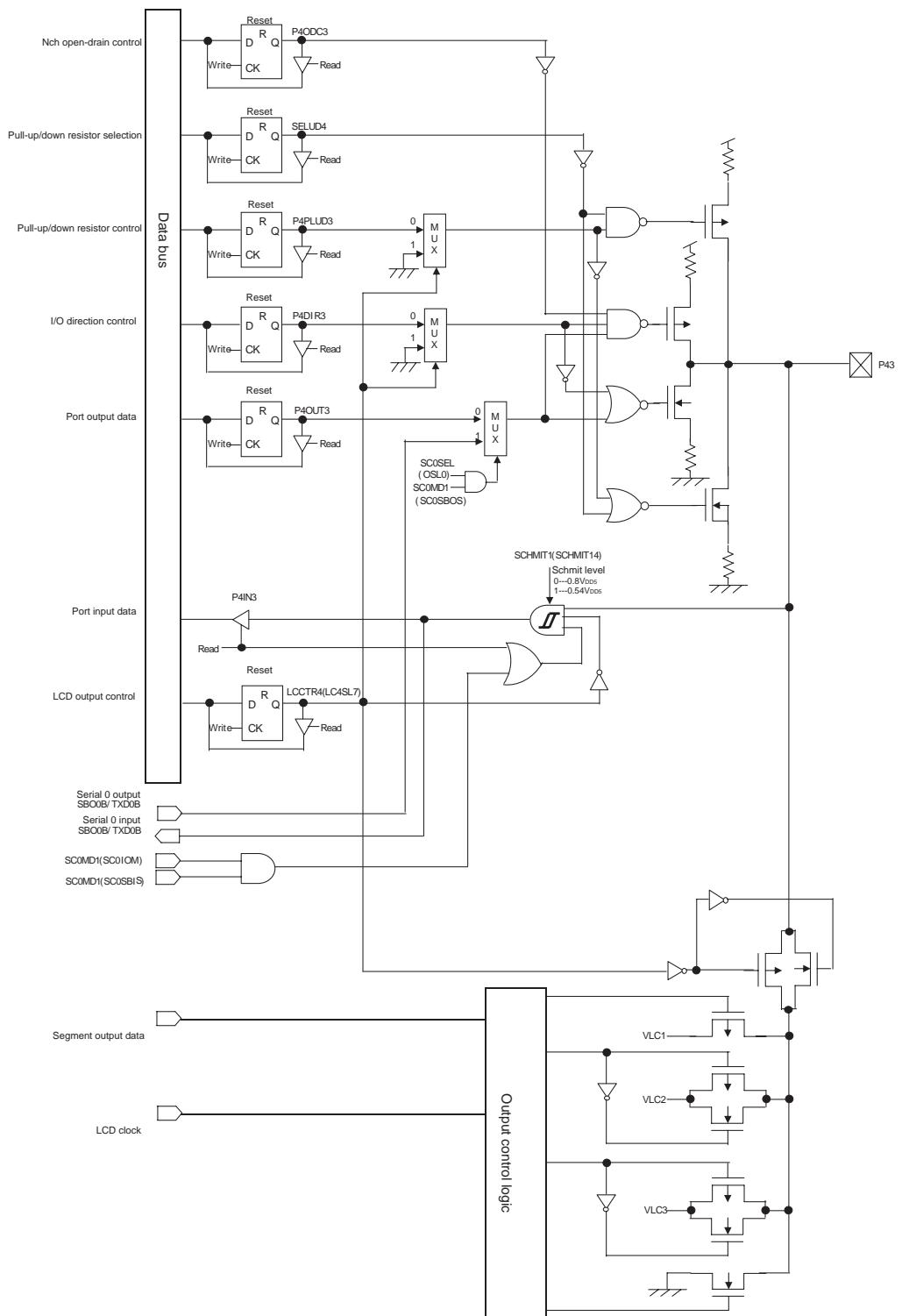


Figure:4.7.4 Block Diagram (P43)

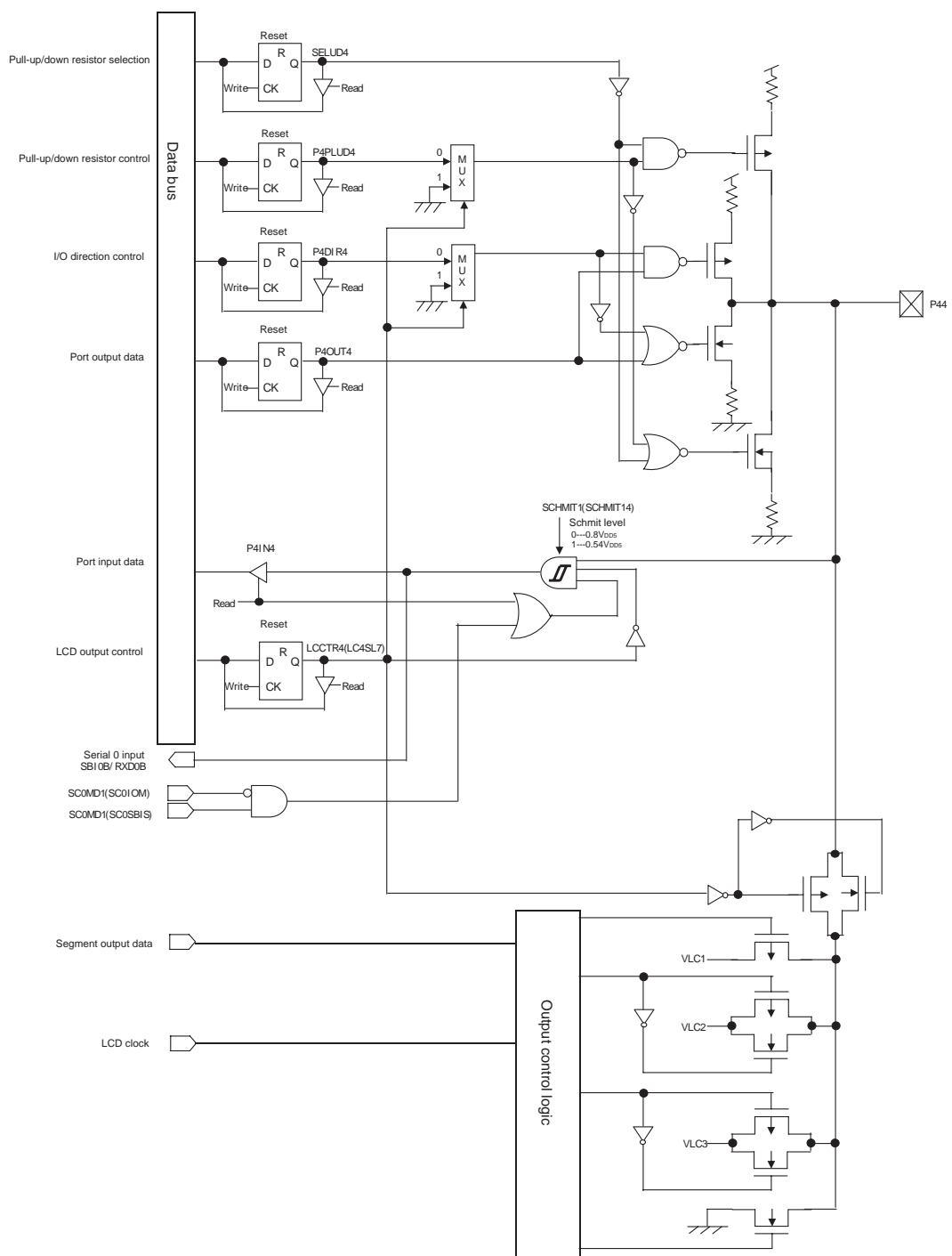


Figure:4.7.5 Block Diagram (P44)

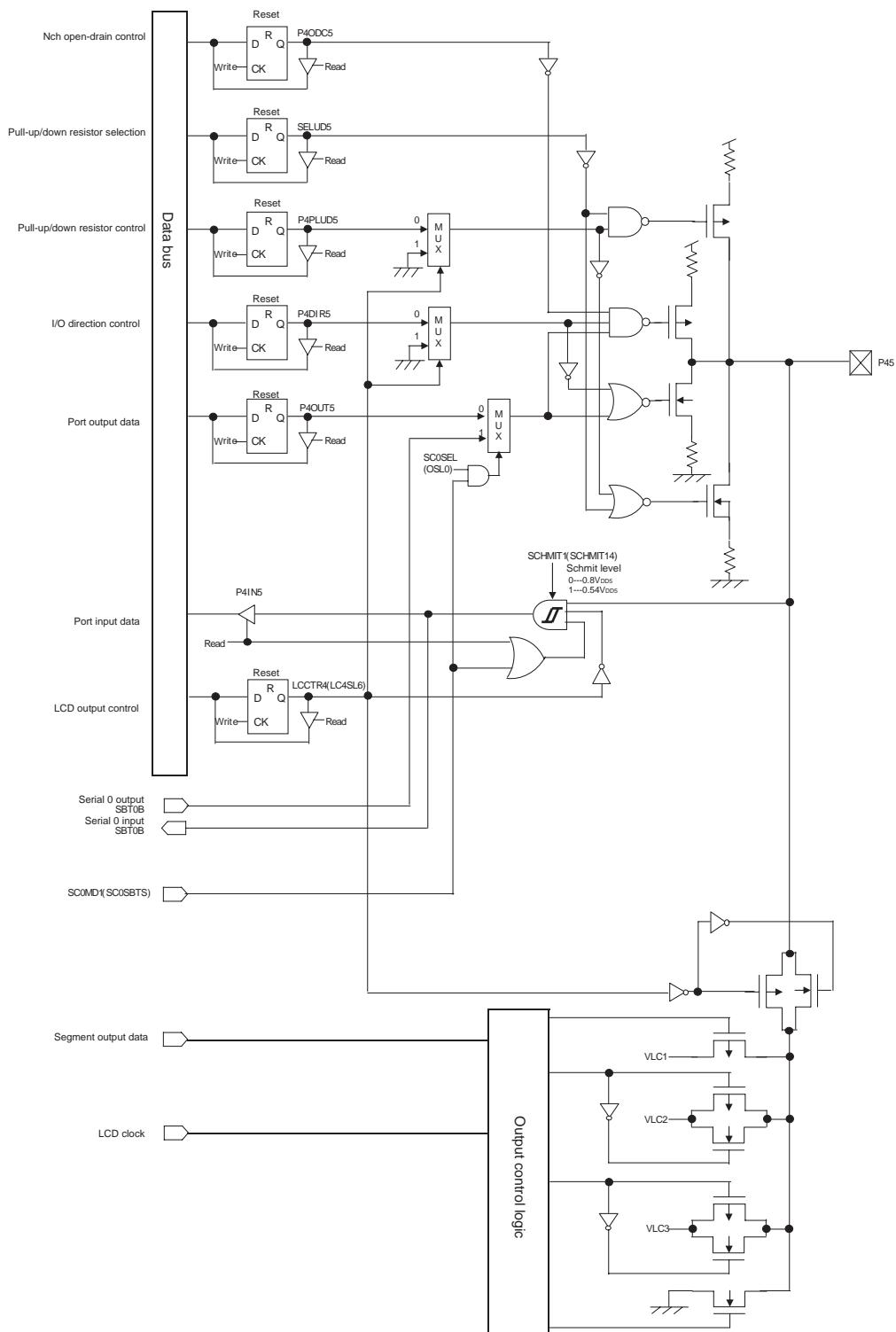


Figure:4.7.6 Block Diagram (P45)

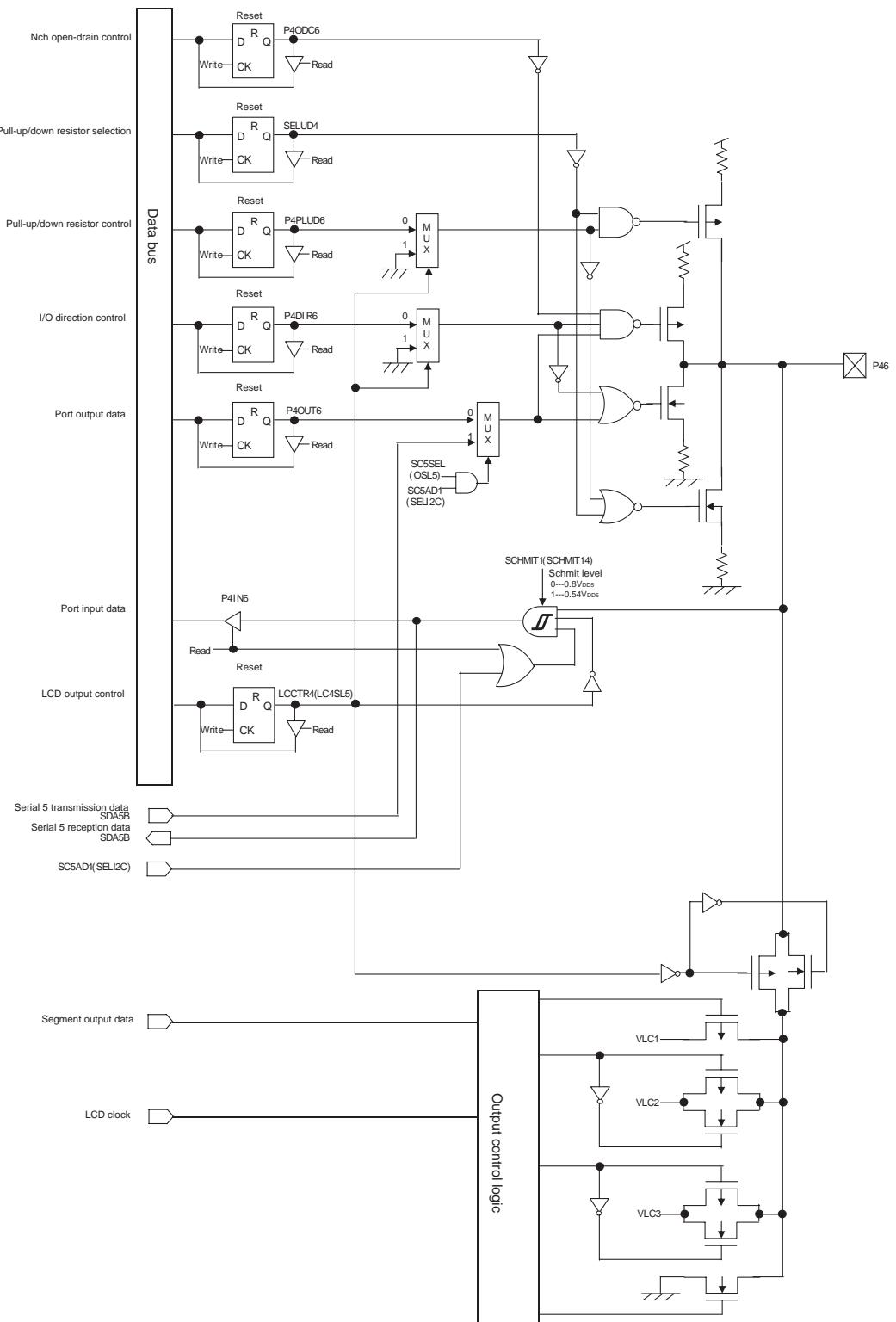


Figure:4.7.7 Block Diagram (P46)

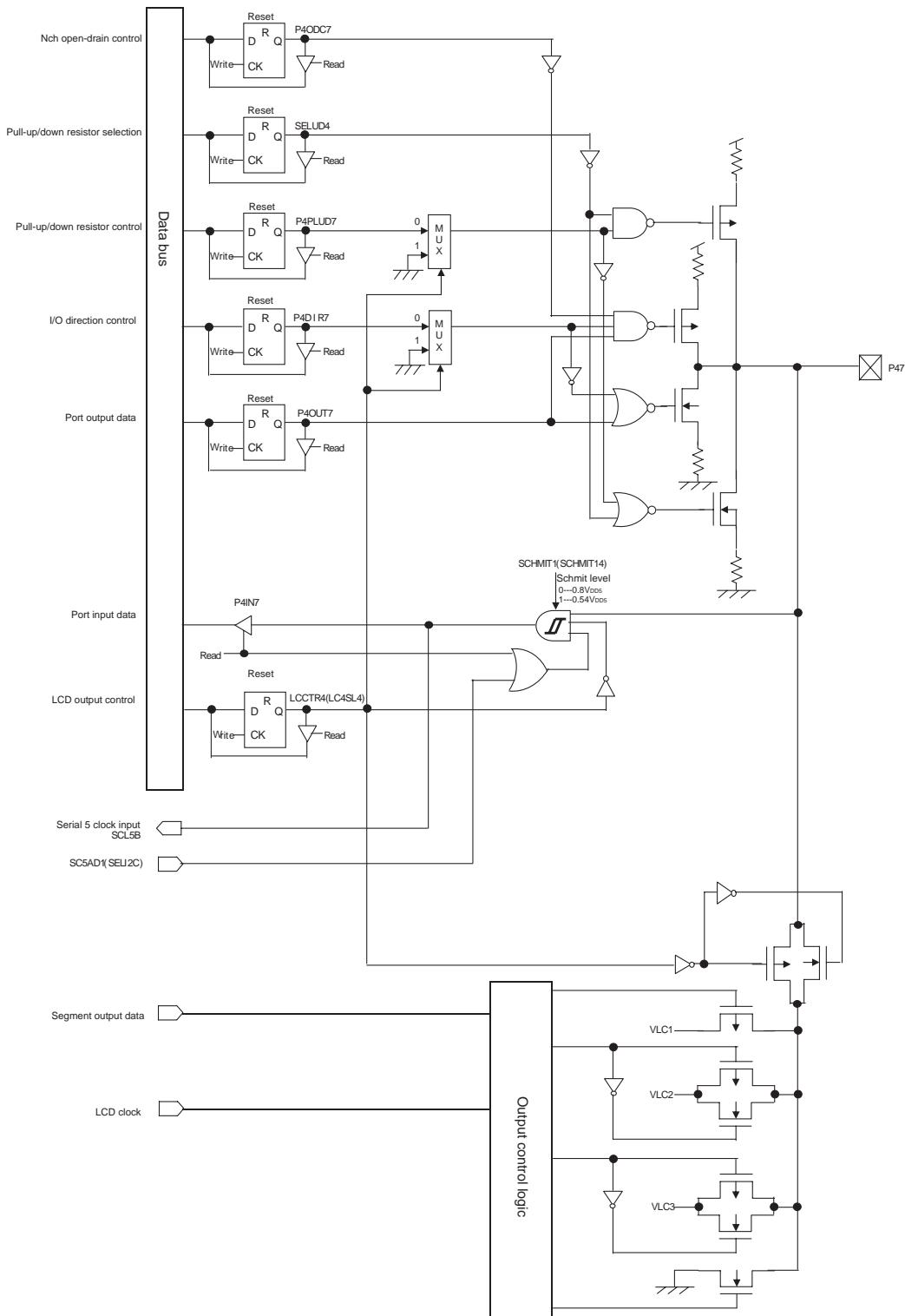


Figure:4.7.8 Block Diagram (P47)

4.8 Port 5

4.8.1 Description

■ General Port Setup

To output data to pins, set the control flag of the port 5 direction control register (P5DIR) to "1" and write the data to the port 5 output register (P5OUT).

To read input data of pins, set the control flag of the port 5 direction control register (P5DIR) to "0" and read the value of the port 5 input register (P5IN).

Each bit can be set individually as either an input or output by the port 5 I/O direction control register (P5DIR). The control flag of the port 5 direction control register (P5DIR) is set to "1" for output mode, and "0" for input mode.

Added/non-added of the pull-up resistor of each bit can be set by the port 5 pull-up or pull-down resistor control register (P5LUD). Set the control flag of the port 5 pull-up or pull-down resistor control register (P5PLUD) to "1" to add the pull-up or pull-down resistor.

Port 5 can be selected to add pull-up or pull-down resistor by bp5 of the pull-up/pull-down resistor selection register (SELUD).

For P50 and P52, each bit can be selected individually as Nch open-drain output by the port 5 Nch open-drain control register (P5ODC). The port 5 Nch open-drain control register (P5ODC) is set to "1" for Nch open-drain output, and "0" for push-pull output.

■ Special Function Pin Setup

P53 is also used as the I/O pin of buzzer A.

P54 is also used as the I/O pin of reverse buzzer A. Each bit can be set individually as either an input or output mode by the buzzer selection register (BUZSEL). The buzzer selection register (BUZSEL) is set to "1" to output buzzer/reverse buzzer, and "0" to be used as the general port.

P50 to P57 are also used as the input pin of KEY interrupt.

P50 to P57 are also used as LCD segment output pin. SEG 27 to 20 pins can be selected when the flag of the bp3 to 0 of the LCD output control register 4 (LCCTR4) and the flag of the bp7 to 4 of the LCD output control register 3 (LCCTR3). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P50 to P57 are the I/O pins of data with the external extension memory in the memory extension mode. In these mode, I/O control by registers is not available.

P50 is also used as the I/O pin of serial 0 transmission/reception data and the output pin of UART0 transmission data. When the SC0SBOS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P50 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 5 Nch open-drain control register (P5ODC).

P51 is also used as the input pin of the serial 0 reception data and UART0 reception data. When the SC0SBIS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P51 is the input pin of serial data.

P52 is also used as the I/O pin of serial 0 clock. When the SC0SBTS flag of the serial interface 0 mode register 1 (SC0MD1) is "1", P52 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 5 Nch open-drain control register (P5ODC).

4.8.2 Registers

Table:4.8.1 shows the registers that control the port 5.

Table:4.8.1 Port 5 Control Register

Registers	Address	R/W	Function	Page
P5OUT	0x03F15	R/W	Port 5 output register	IV-79
P5IN	0x03F25	R	Port 5 input register	IV-80
P5DIR	0x03F35	R/W	Port 5 direction control register	IV-80
P5PLUD	0x03F45	R/W	Port 5 pull-up/pull-down resistor control register	IV-80
P5ODC	0x03EF3	R/W	Port 5 Nch open-drain control register	IV-81
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-82
BUZSEL	0x03EE2	R/W	Buzzer output control register	IV-83
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-84

R/W:Readable/Writable

- Port 5 output register (P5OUT: 0x03F15)

bp	7	6	5	4	3	2	1	0
Flag	P5OUT7	P5OUT6	P5OUT5	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	P5OUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 5 Input Register (P5IN: 0x03F25)

bp	7	6	5	4	3	2	1	0
Flag	P5IN7	P5IN6	P5IN5	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	P5IN7-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 5 Direction Control Register (P5DIR: 0x03F35)

bp	7	6	5	4	3	2	1	0
Flag	P5DIR7	P5DIR6	P5DIR5	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P5DIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 5 Pull-up/Pull-down Resistor Control Register (P5PLUD: 0x03F45)

bp	7	6	5	4	3	2	1	0
Flag	P5PLUD7	P5PLUD6	P5PLUD5	P5PLUD4	P5PLUD3	P5PLUD2	P5PLUD1	P5PLUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P5PLUD7-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 5 Nch Open-drain Control Register (P5ODC:0x03EF3)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	P5ODC2	-	P5ODC0
At reset	-	-	-	-	-	0	-	0
Access	-	-	-	-	-	R/W	-	R/W

bp	Flag	Description
7-3	-	-
2	P5ODC2	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
1	-	-
0	P5ODC0	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Buzzer Output Control Register (BUZSEL: 0x03EE2)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	BUZSEL4	BUZSEL3	BUZSEL2	BUZSEL1	-
At reset	-	-	-	0	0	0	0	-
Access	-	-	-	R/W	R/W	R/W	R/W	-

bp	Flag	Description
7-5	-	-
4	BUZSEL4	Buzzer (Reverse) output selection 0:Port P54 1:NBUZZERA
3	BUZSEL3	Buzzer output selection 0:Port P53 1:BUZZERA
2	BUZSEL2	Control with P1OMD6 0:TM8IOC 1:NBUZZERB
1	BUZSEL1	Control with P1OMD5 0:TM7IOC 1:BUZZERB
0	-	-

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.8.3 Block Diagram

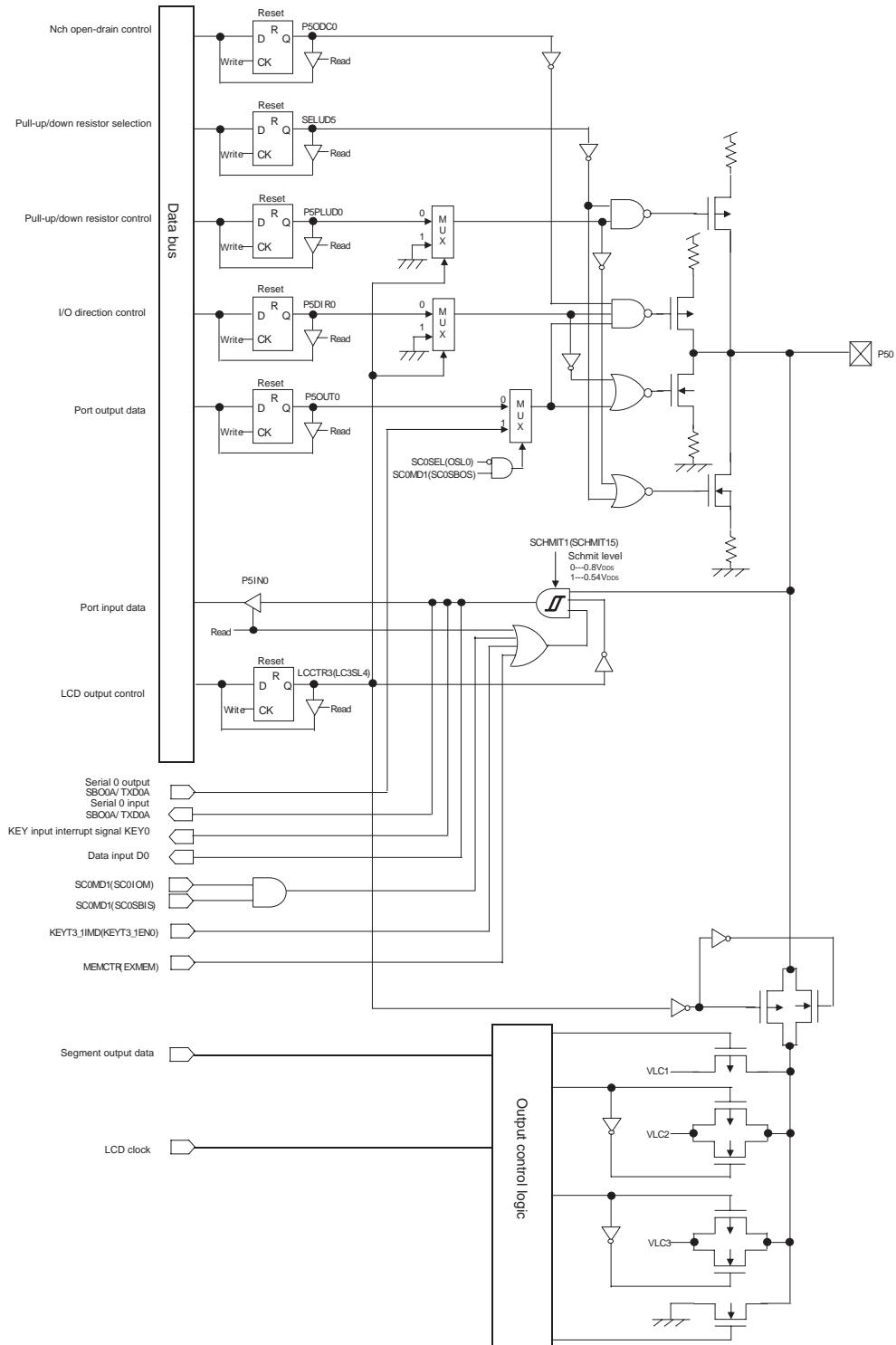


Figure:4.8.1 Block Diagram (P50)

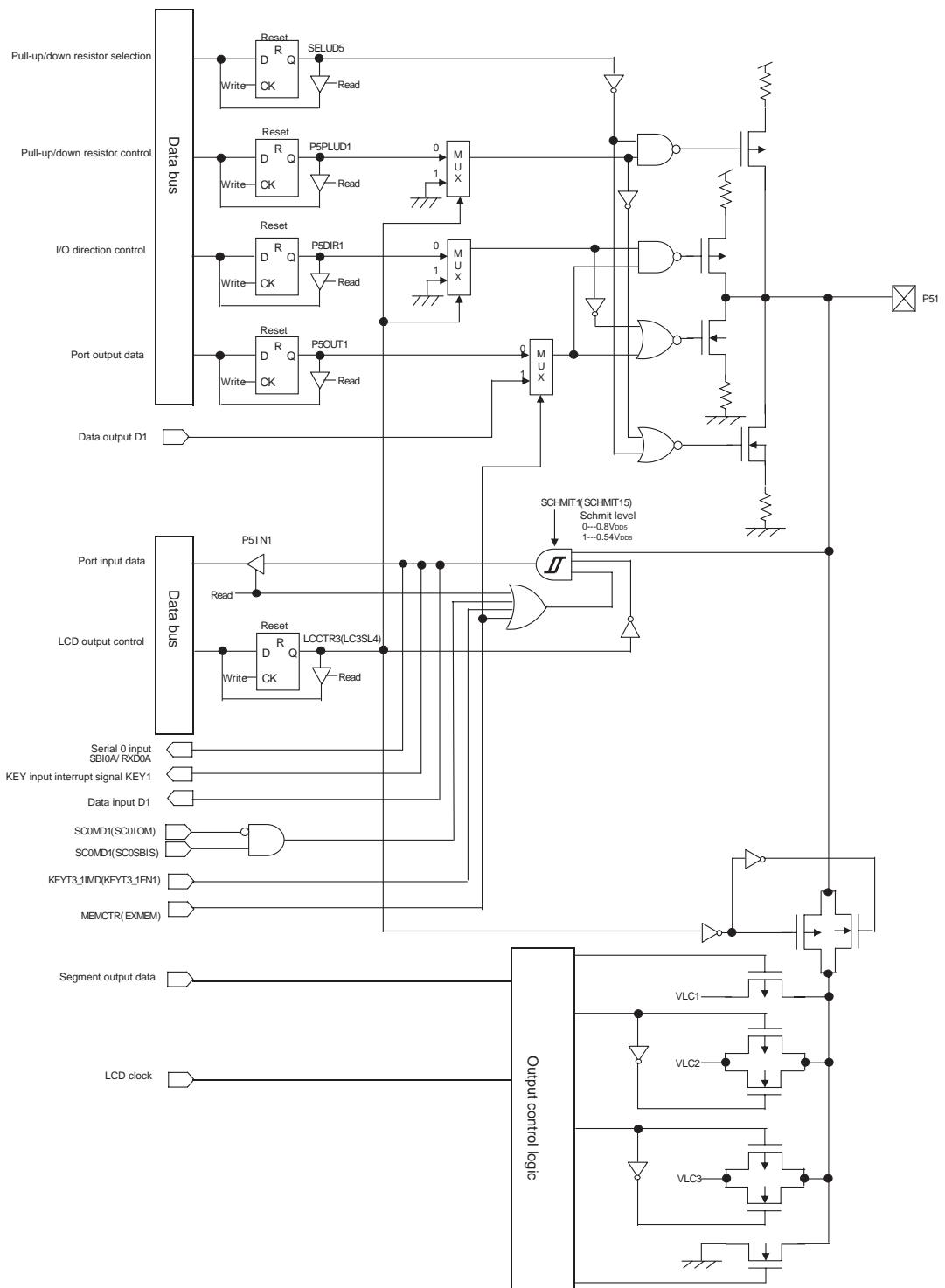


Figure:4.8.2 Block Diagram (P51)

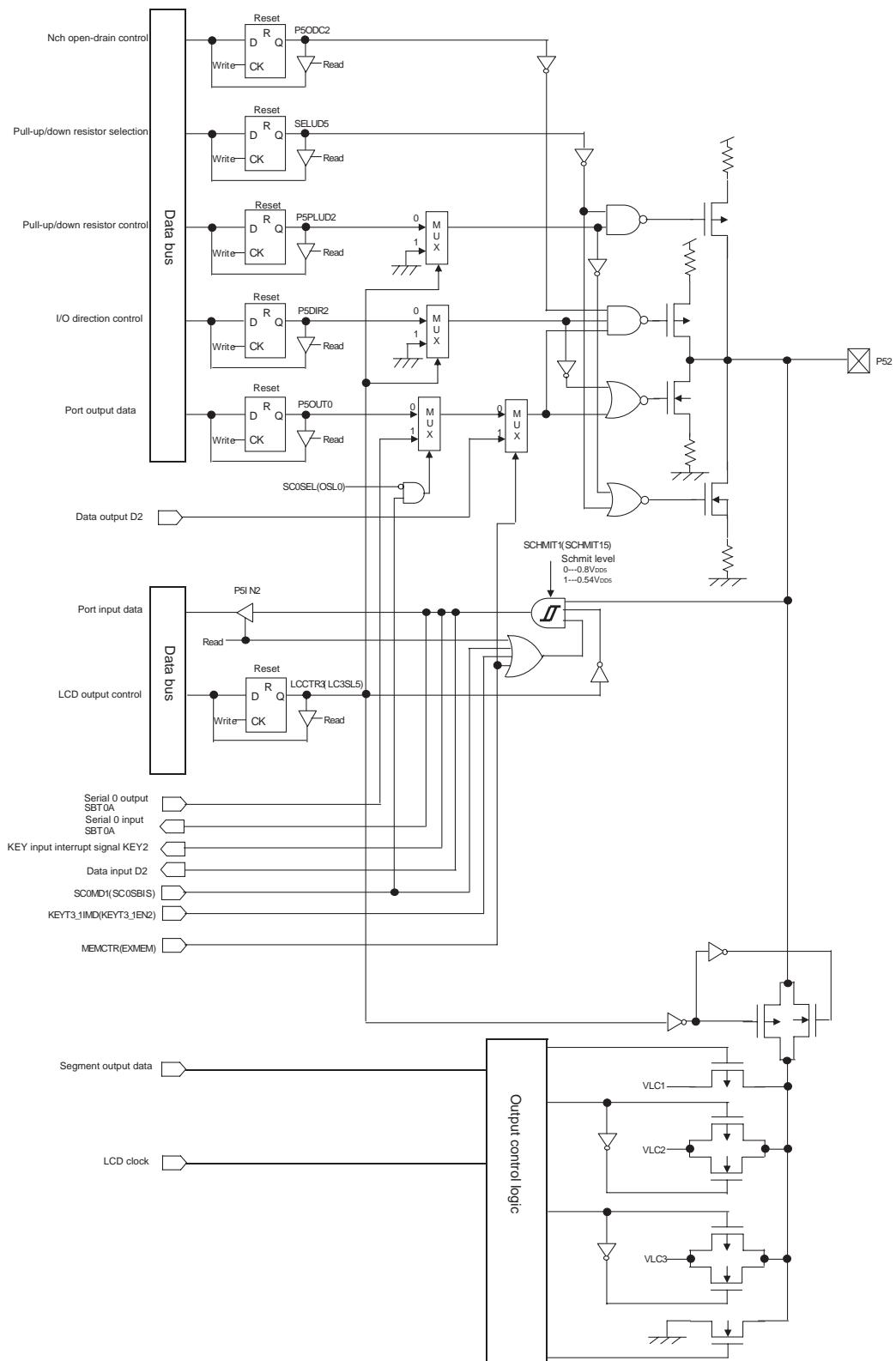


Figure:4.8.3 Block Diagram (P52)

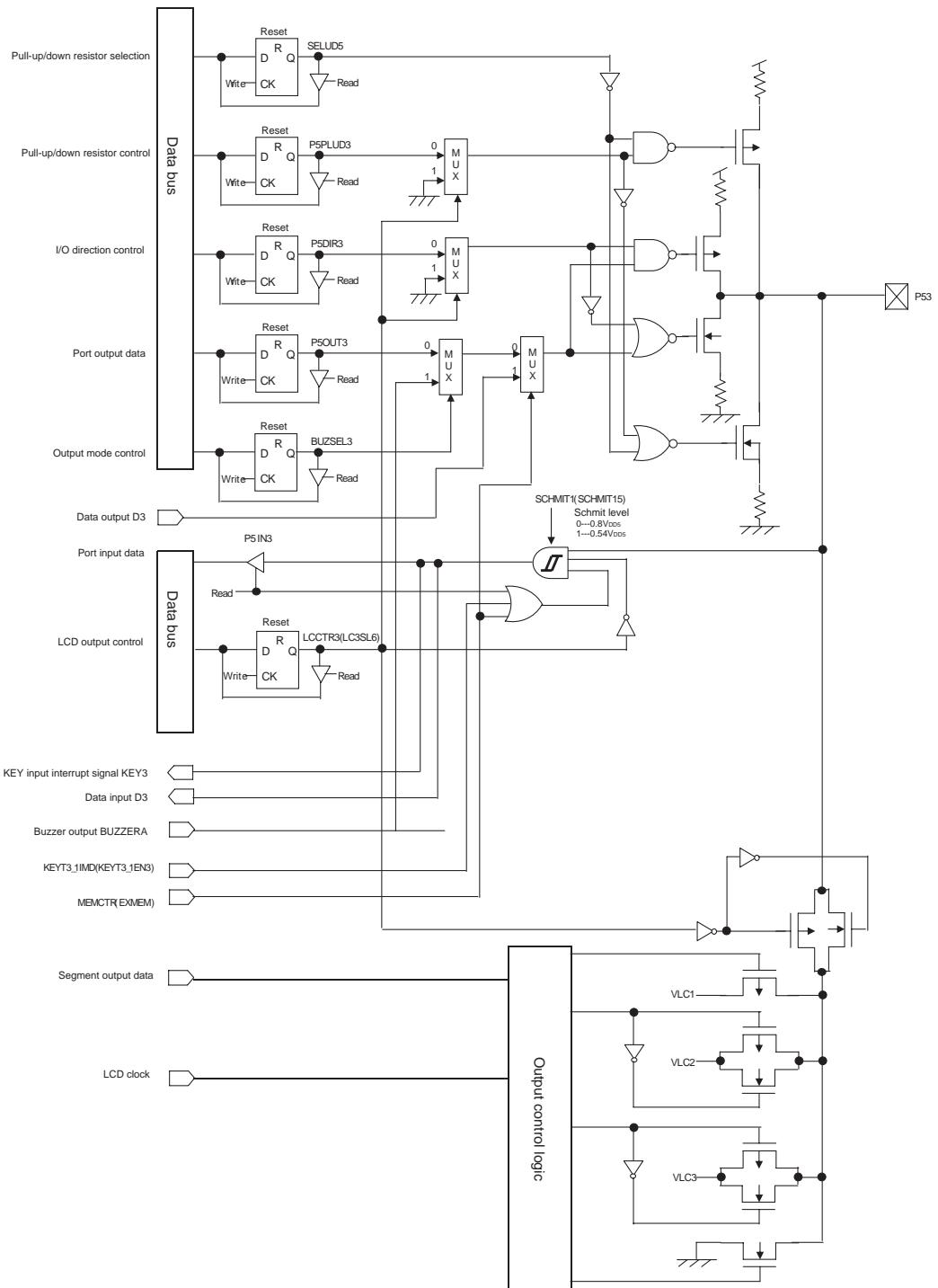


Figure:4.8.4 Block Diagram (P53)

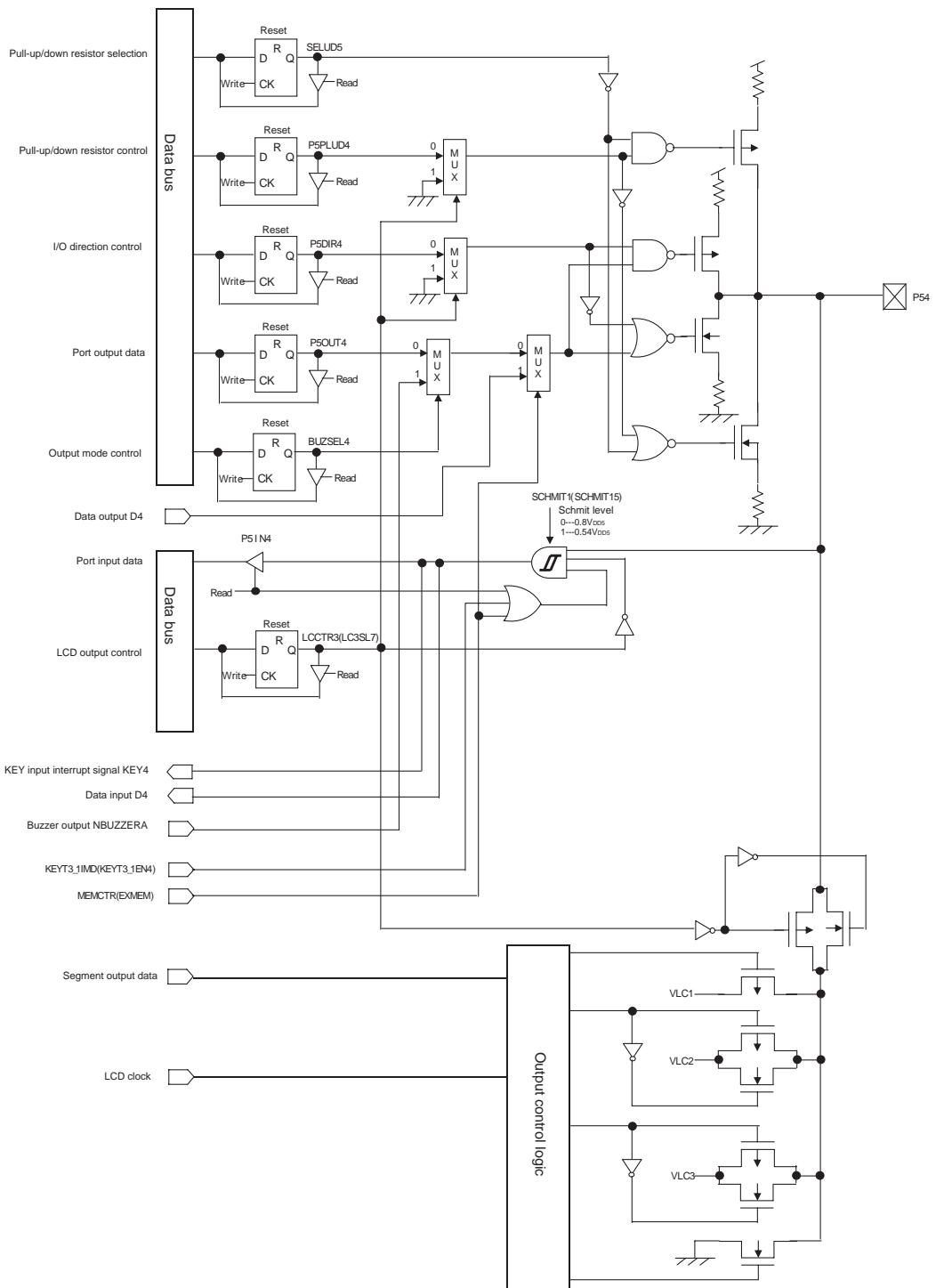


Figure:4.8.5 Block Diagram (P54)

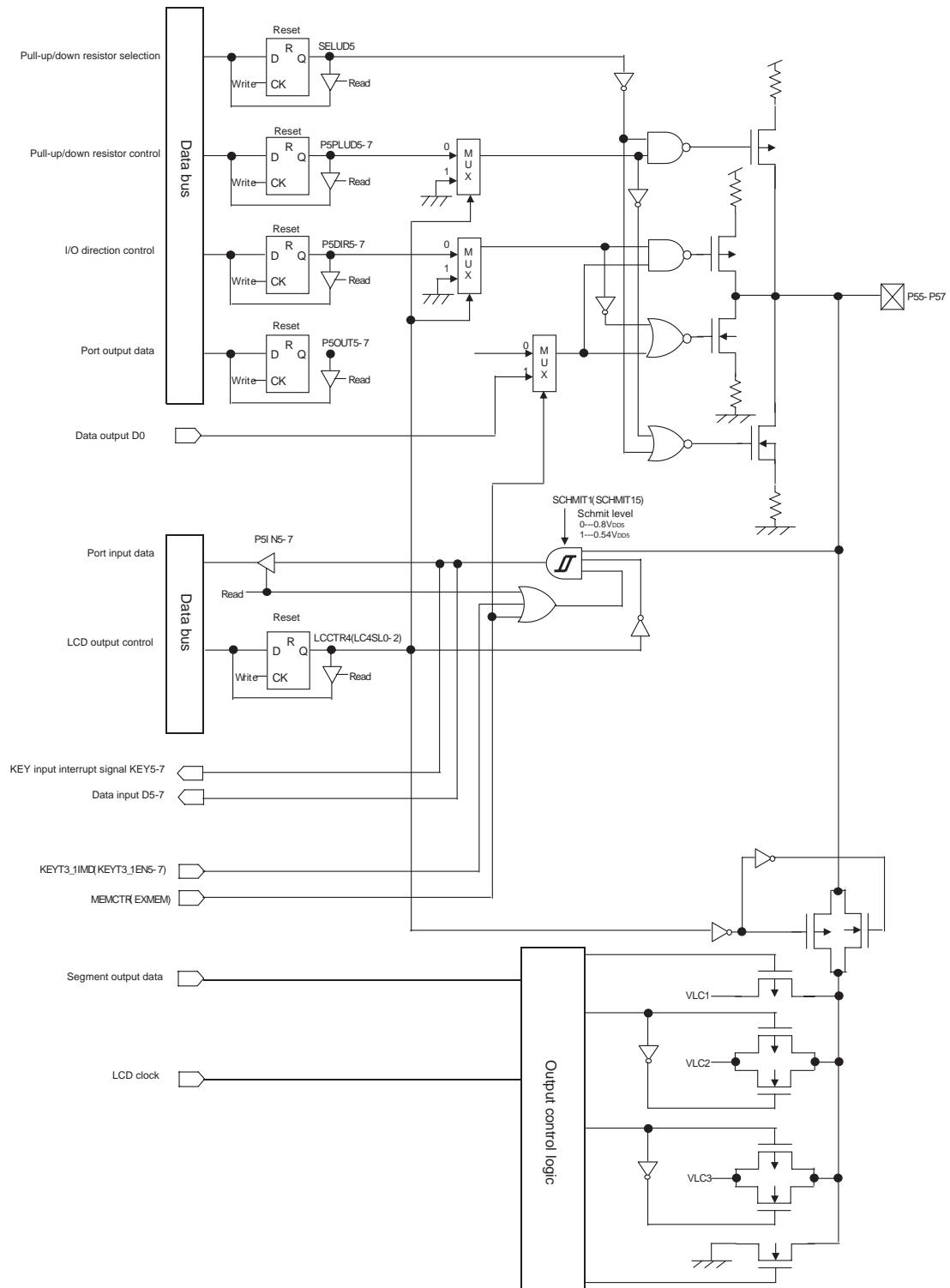


Figure:4.8.6 Block Diagram (P55 to P57)

4.9 Port 6

4.9.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 6 direction control register (P6DIR) to "1" and write data to the port 6 output register (P6OUT).

To read input data of pin, set the control flag of the port 6 direction control register (P6DIR) to "0" and read the value of the port 6 input register (P6IN).

Each bit can be set individually to either an input or output by the port 6 direction control register (P6DIR). The control flag of the port 6 direction control register (P6DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up (or pull-down) resistor is added or not by the port 6 pull-up/pull-down resistor control register (P6PLUD). Set the control flag of the port 6 pull-up resistor control register (P6PLUD) to "1" to add pull-up (or pull-down) resistor.

Port 6 can be selected to add pull-up or pull-down resistor by bp6 of the pull-up/pull-down resistor selection register (SELUD).

For P66 to P67, each bit can be selected individually as Nch open-drain output by the port 6 Nch open-drain control register (P6ODC). The port 6 Nch open-drain control register (P6ODC) is set to "1" for Nch open-drain output, and "0" for push-pull output.

■ Special Function Pin Setup

P60 to P67 are also used as LCD segment output pin. SEG 19 to 12 pins can be selected when the flag of the bp3 to 0 of the LCD output control register 3 (LCCTR3) and the flag of the bp7 to 4 of the LCD output control register 2 (LCCTR2). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P62 to P67 are the address output pins to the external extension memory in the memory extension memory extension mode. In these mode, the output mode is forcibly set.

P61 is also used as the analog B output.

P62 is also used as the I/O pin of timer 1.

P63 is also used as the I/O pin of timer 3.

P64 is also used as the I/O pin of timer 4. Each bit can be set individually as either an input or output mode by the port 6 output mode register (P6OMD). The port 6 output mode register (P6OMD) is set to "1" for I/O of special function data, and "0" to be used as the general port.

P65 is also used as the input pin of the serial 4 reception data. When the SC4SBIS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", P65 is the input pin of serial data.

P66 is also used as the I/O pin of serial 4 transmission/reception data and IIC4 transmission/reception data. When the SC4SBOS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", P66 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 6 Nch open-drain control register (P6ODC).

P67 is also used as the I/O pin of serial 4 clock and the output pin of IIC4 clock. When the SC4SBTS flag of the serial interface 4 mode register 1 (SC4MD1) is "1", P67 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 6 Nch open-drain control register (P6ODC).

4.9.2 Registers

Table:4.9.1 shows the registers that control the port 6.

Table:4.9.1 Port 6 Control Register

Registers	Address	R/W	Function	Page
P6OUT	0x03F16	R/W	Port 6 output register	IV-92
P6IN	0x03F26	R	Port 6 input register	IV-93
P6DIR	0x03F36	R/W	Port 6 direction control register	IV-93
P6PLUD	0x03F46	R/W	Port 6 pull-up/pull-down resistor control register	IV-93
P6OMD	0x03EE4	R/W	Port 6 output mode register	IV-94
P6ODC	0x03EF4	R/W	Port 6 Nch open-drain control register	IV-94
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-95
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-96

R/W:Readable/Writable

- Port 6 output register (P6OUT: 0x03F16)

bp	7	6	5	4	3	2	1	0
Flag	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	P6OUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 6 Input Register (P6IN: 0x03F26)

bp	7	6	5	4	3	2	1	0
Flag	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	P6IN7-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 6 Direction Control Register (P6DIR: 0x03F36)

bp	7	6	5	4	3	2	1	0
Flag	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P6DIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 6 Pull-up/Pull-down Resistor Control Register (P6PLUD: 0x03F46)

bp	7	6	5	4	3	2	1	0
Flag	P6PLUD7	P6PLUD6	P6PLUD5	P6PLUD4	P6PLUD3	P6PLUD2	P6PLUD1	P6PLUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P6PLUD7-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 6 Output Mode Register (P6OMD:0x03EE4)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	P6OMD4	P6OMD3	P6OMD2	-	-
At reset	-	-	-	0	0	0	-	-
Access	-	-	-	R/W	R/W	R/W	-	-

bp	Flag	Description
7-5	-	-
4	P6OMD4	I/O port, TM4IOB selection 0:Port P 64 1:TM4IOB
3	P6OMD3	I/O port, TM3IOB selection 0:Port P 63 1:TM3IOB
2	P6OMD2	I/O port, TM1IOB selection 0:Port P 62 1:TM1IOB
1-0	-	-

■ Port 6 Nch Open-drain Control Register (P6ODC:0x03EF4)

bp	7	6	5	4	3	2	1	0
Flag	P6ODC7	P6ODC6	-	-	-	-	-	-
At reset	0	0	-	-	-	-	-	-
Access	R/W	R/W	-	-	-	-	-	-

bp	Flag	Description
7-6	P6ODC7-6	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
5-0	-	-

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.9.3 Block Diagram

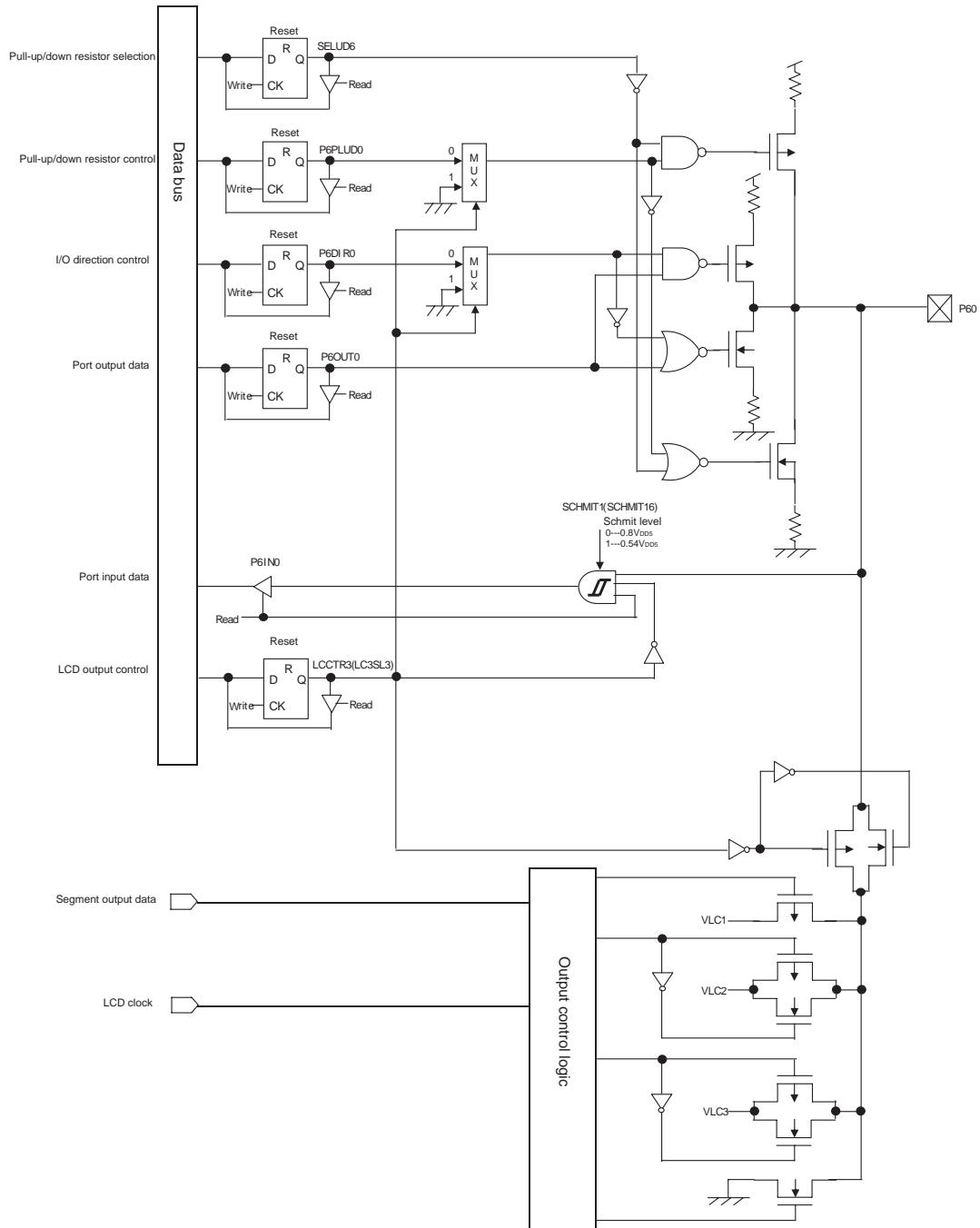


Figure:4.9.1 Block Diagram (P60)

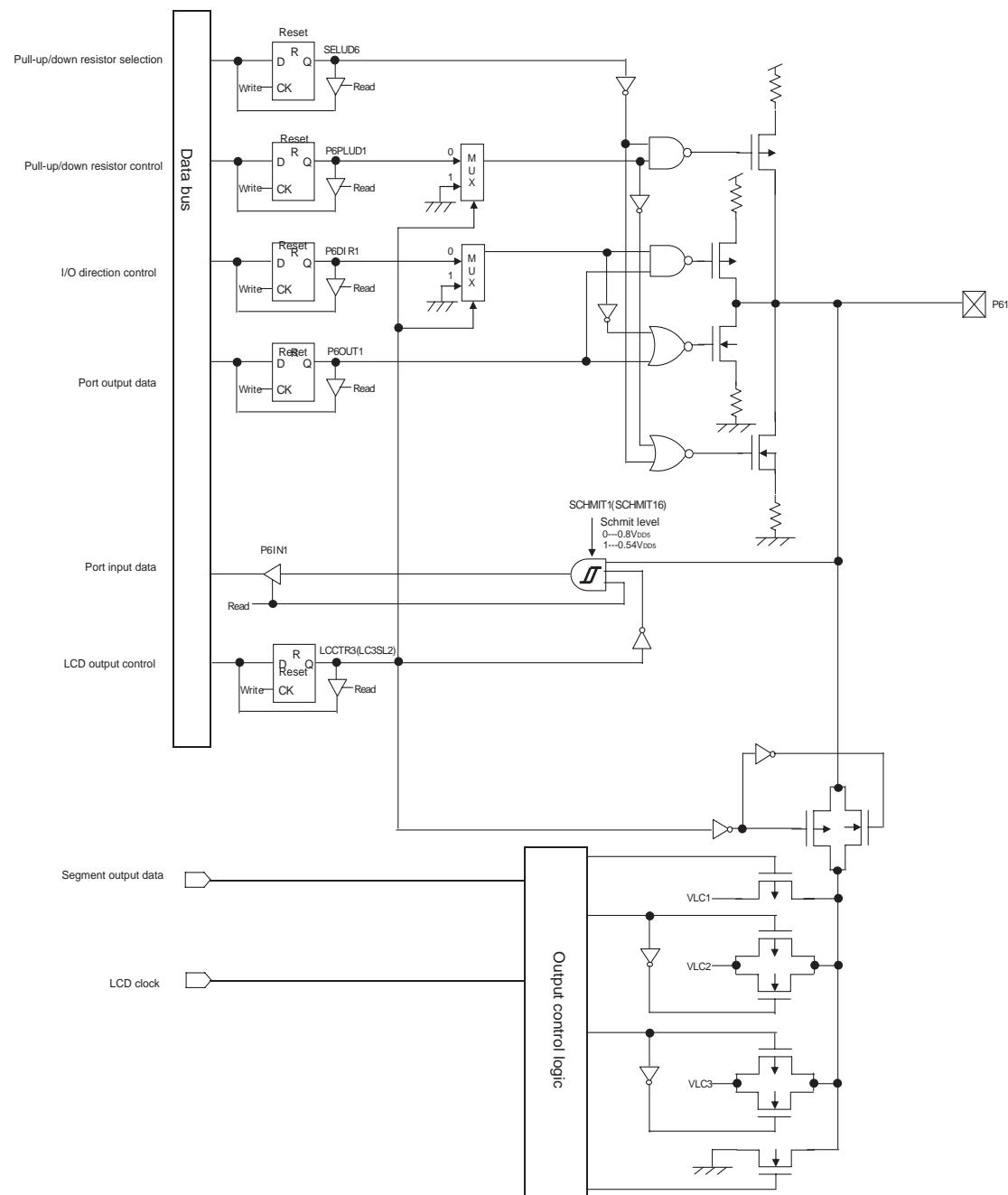


Figure:4.9.2 Block Diagram (P61)

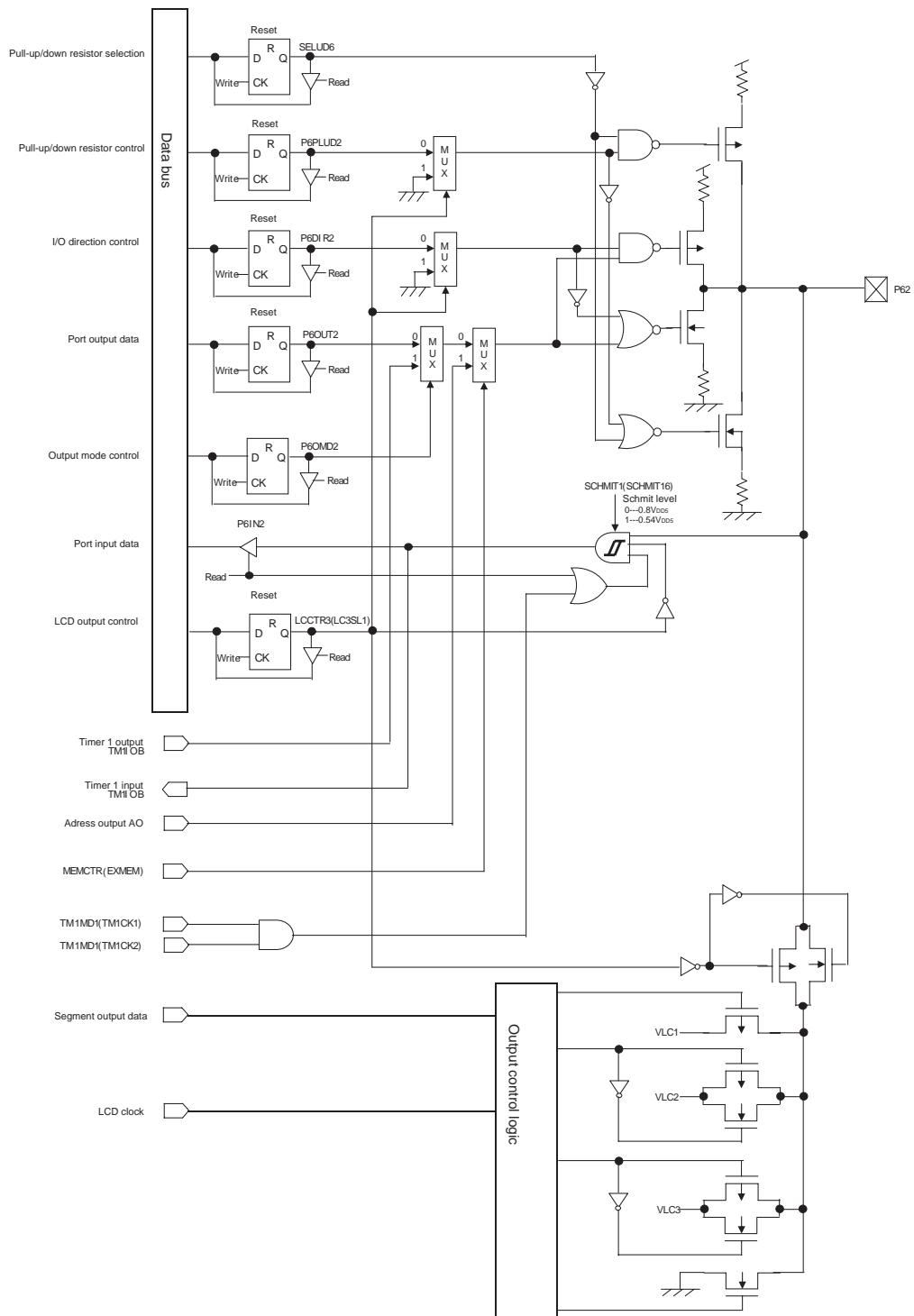


Figure 4.9.3 Block Diagram (P62)

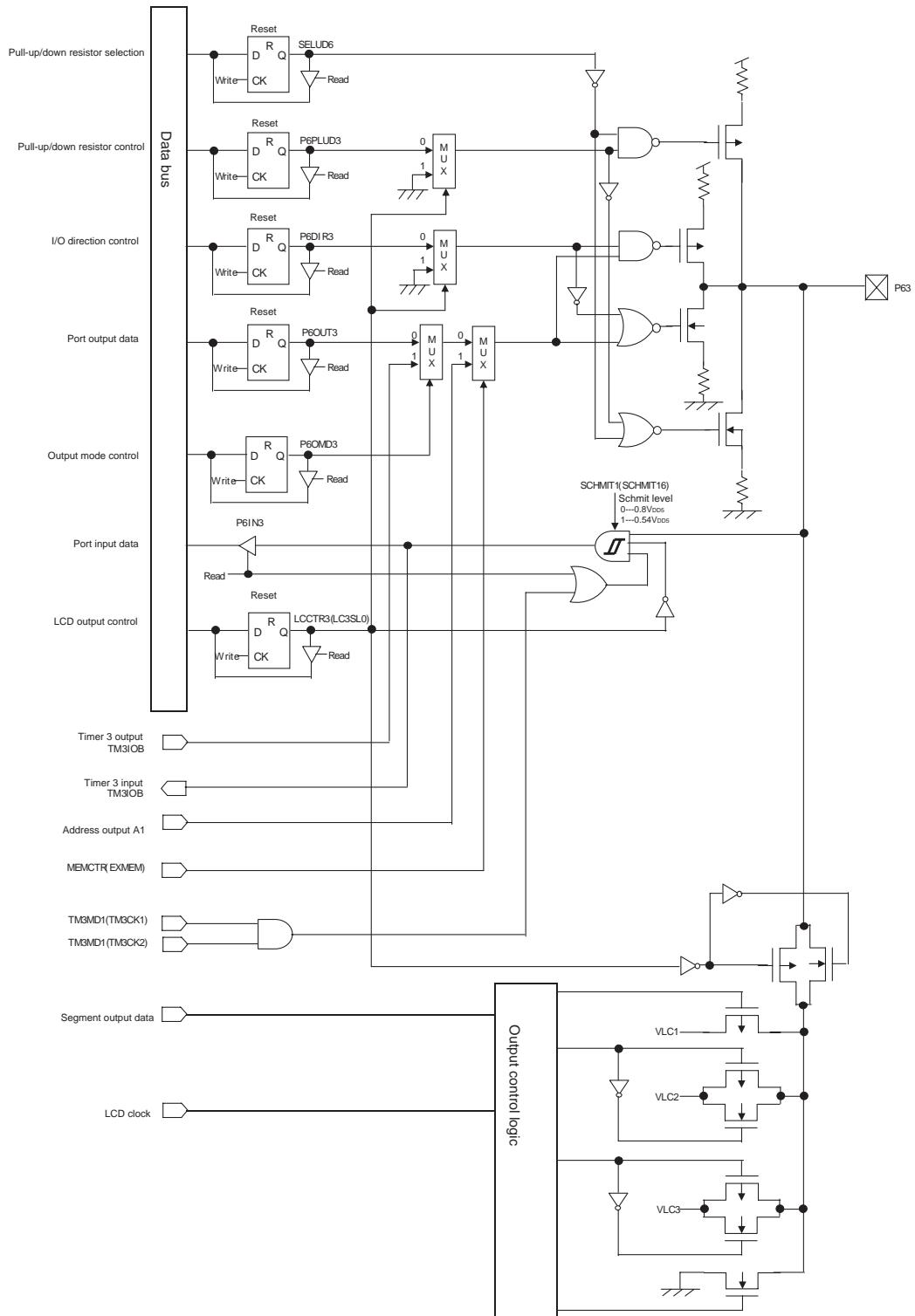


Figure:4.9.4 Block Diagram (P63)

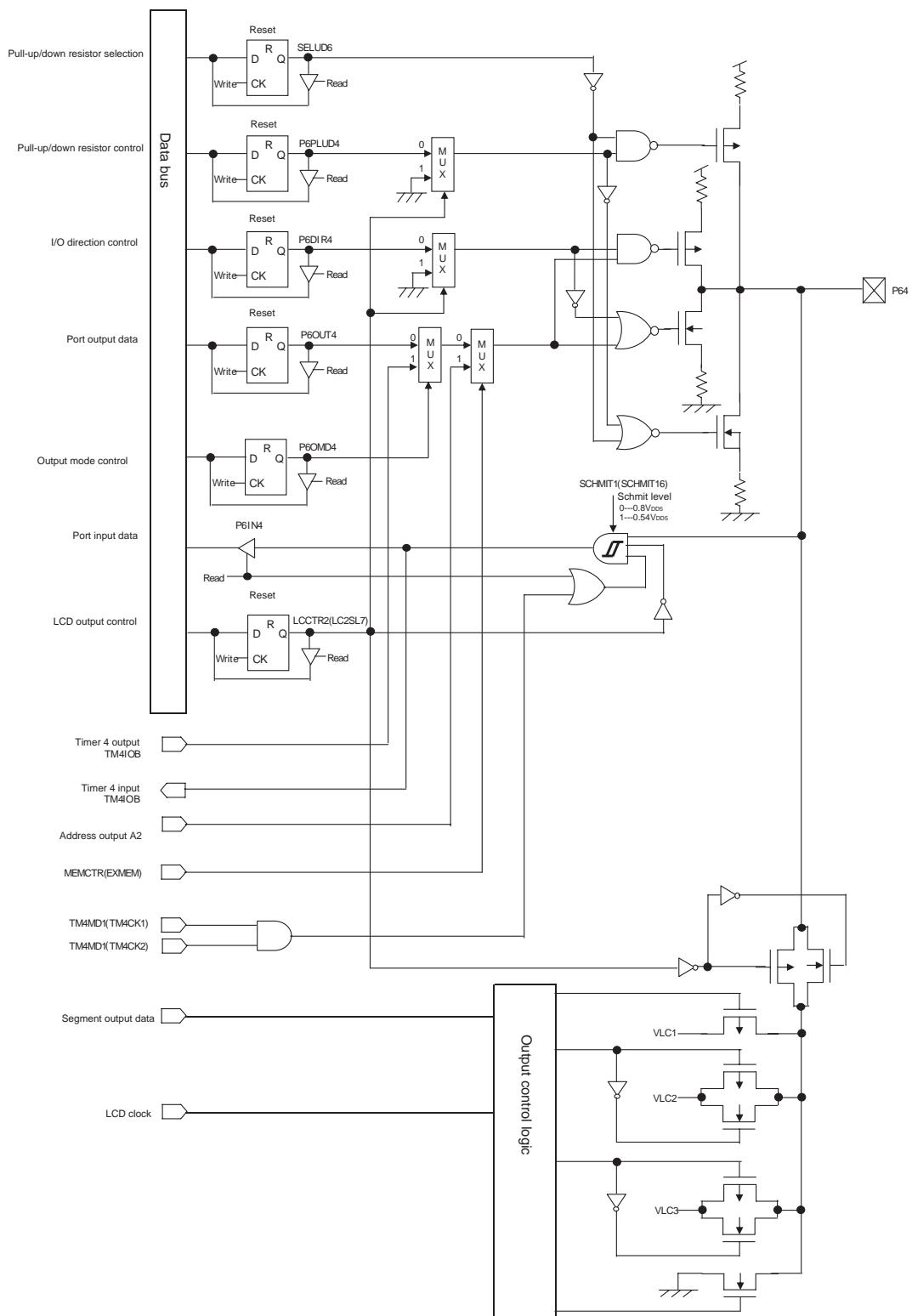


Figure:4.9.5 Block Diagram (P64)

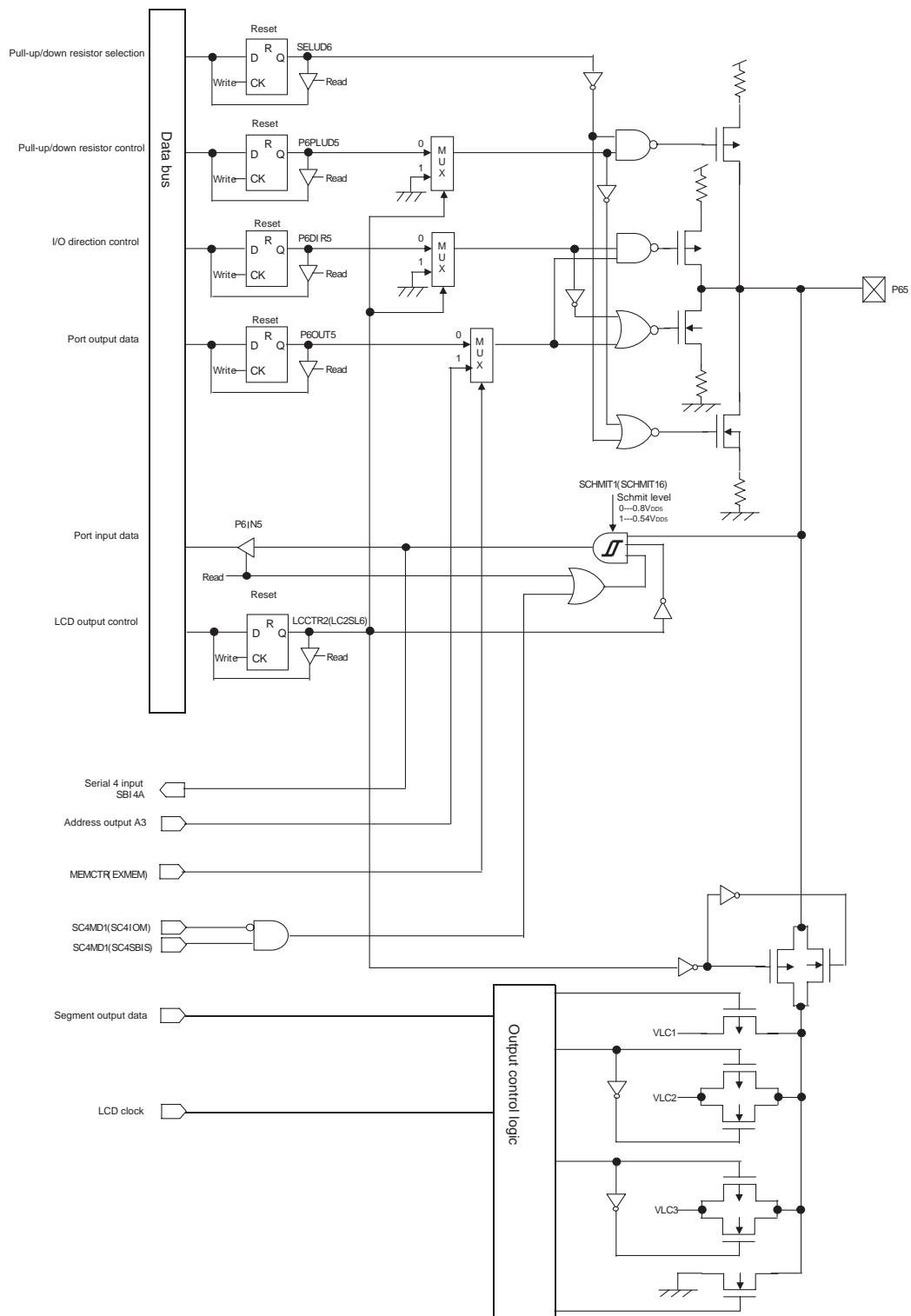


Figure:4.9.6 Block Diagram (P65)

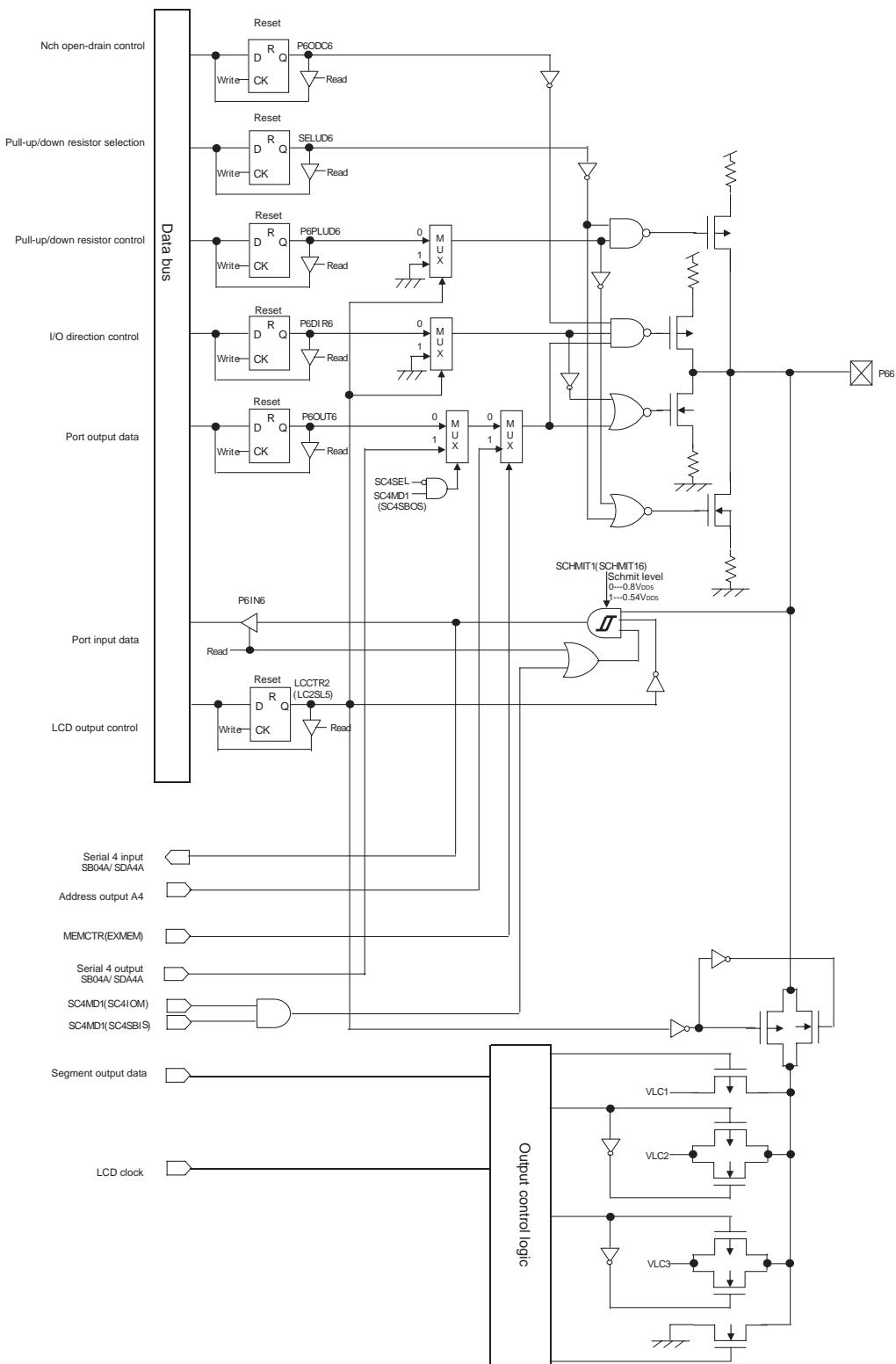


Figure:4.9.7 Block Diagram (P66)

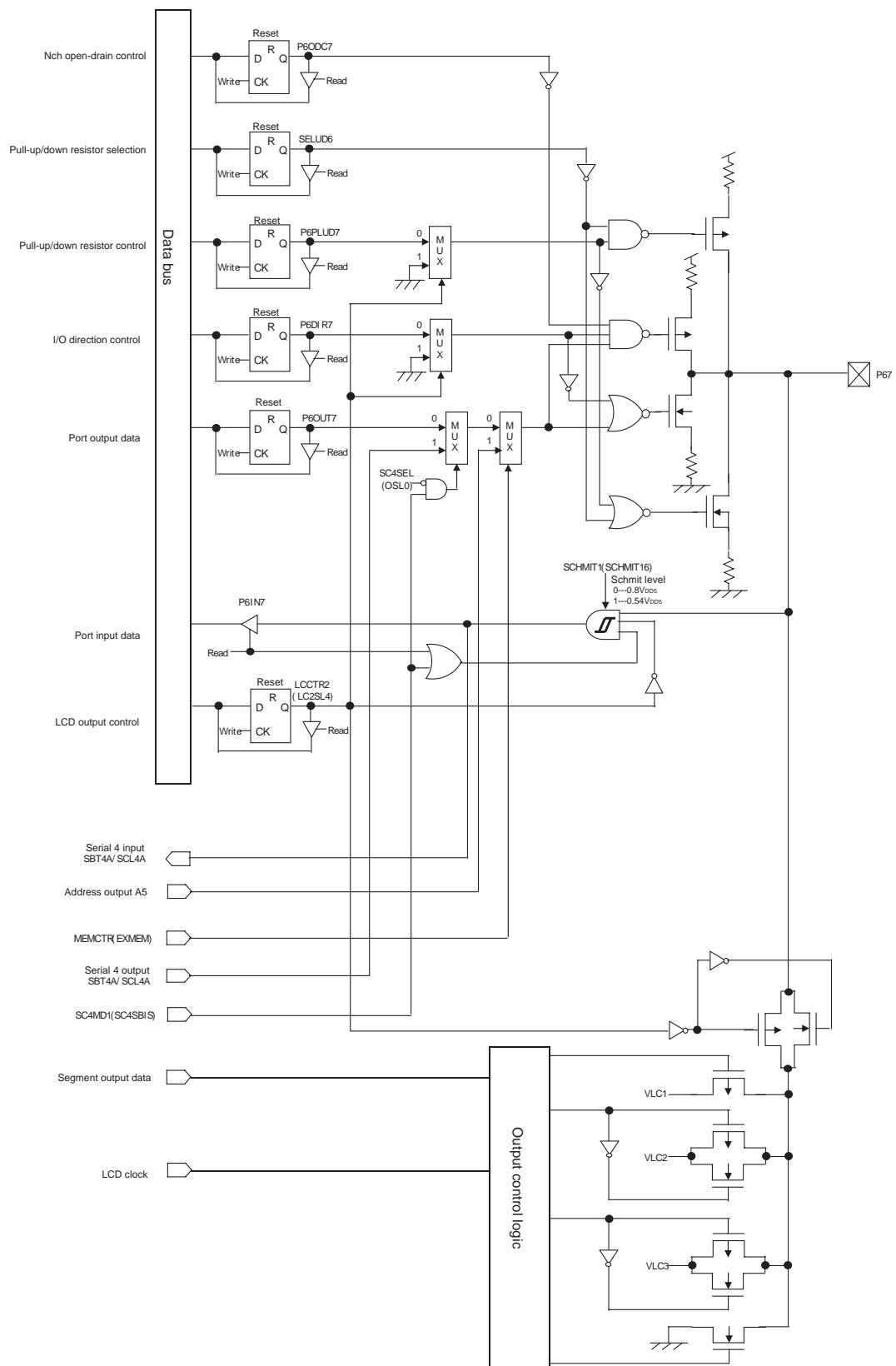


Figure:4.9.8 Block Diagram (P67)

4.10 Port 7

4.10.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 7 direction control register (P7DIR) to "1" and write data to the port 7 output register (P7OUT).

To read input data of pin, set the control flag of the port 7 direction control register (P7DIR) to "0" and read the value of the port 7 input register (P7IN).

Each bit can be set individually to either an input or output by the port 7 direction control register (P7DIR). The control flag of the port 7 direction control register (P7DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up (or pull-down) resistor is added or not, by the port 7 pull-up/pull-down resistor control register (P7PLUD). Set the control flag of the port 7 pull-up/pull-down resistor control register (P7PLUD) to "1" to add pull-up resistor.

Port 7 can be selected to add pull-up or pull-down resistor by bp7 of the pull-up/pull-down resistor selection register (SELUD).

For P70, P72 to P75 and P77, each bit can be selected individually as Nch open-drain output by the port 7 Nch open-drain control register (P7ODC). The port 7 Nch open-drain control register (P7ODC) is set to "1" for Nch open-drain output, and "0" for push-pull output.

■ Special Function Pin Setup

P70 to P77 are also used as LCD segment output pin. SEG 11 to 4 pins can be selected when the flag of the bp3 to 0 of the LCD output control register 2 (LCCTR2) and the flag of the bp7 to 4 of the LCD output control register 1 (LCCTR1). The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P70 to P71 are the address output pins to the external extension memory in the memory extension mode. In these mode, the output mode is forcibly set.

P72 to P74 are the output pins of write enable signal, read enable signal and chip selection signal in the memory extension mode. In these mode, the output mode is forcibly set.

P75 to P77 can be used as address output pin to the external extension memory in the memory extension mode. Set the bp5 of the address output control register (EXADV). Otherwise, this pin is used as a general port pin. Output mode is forcibly selected when the bp5 of the address output control register (EXADV) is "1" in the memory extension mode.

P70 is also used as the I/O pin of serial 2 transmission/reception data and the output pin of URAT2 transmission data. When the SC2SBOS flag of the serial interface 2 mode register 1 (SC2MD1) is "1", P70 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 7 Nch open-drain control register (P7ODC).

P71 is also used as the input pin of the serial 2 reception data and UART2 reception data. When the SC2SBIS flag of the serial interface 2 mode register 1 (SC2MD1) is "1", P71 is the input pin of serial data.

P72 is also used as the I/O pin of serial 2 clock. When the SC2SBTS flag of the serial interface 2 mode register 1 (SC2MD1) is "1", P72 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 7 Nch open-drain control register (P7ODC).

P73 is also used as the I/O pin of serial 5 transmission/reception data. When the SEL12C flag or I2CMON flag of the serial interface 5 address setting register (SC5AD1) is "1", P73 is the serial data I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 7 Nch open-drain control register (P7ODC).

P74 is also used as the input pin of serial 5 clock. When the SEL12C flag or I2CMON flag of the serial interface 5 address setting register (SC5AD1) is "1", P74 is the serial clock input pin. Push-pull output or Nch open-drain output can be selected by setting the Port 7 Nch open-drain control register (P7ODC).

P75 is also used as the I/O pin of serial 1 transmission/reception data and output pin of URAT1 transmission data. When the SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is "1", P75 is the I/O pin of the serial data. Push-pull output or Nch open-drain output can be selected by setting the Port 7 Nch open-drain control register (P7ODC).

P76 is also used as the input pin of serial 1 reception data and URAT1 reception data. When the SC1SBIS flag of the serial interface 1 mode register 1 (SC1MD1) is "1", P76 is the serial data input pin.

P77 is also used as the I/O pin of serial 1 clock. When the SC1SBTS flag of the serial interface 1 mode register 1 (SC1MD1) is "1", P77 is the serial clock I/O pin. Push-pull output or Nch open-drain output can be selected by setting the Port 7 Nch open-drain control register (P7ODC).

4.10.2 Registers

Table:4.10.1 shows the registers that control the port 7.

Table:4.10.1 Port 7 Control Register

Registers	Address	R/W	Function	Page
P7OUT	0x03F17	R/W	Port 7 output register	IV-107
P7IN	0x03F27	R	Port 7 input register	IV-107
P7DIR	0x03F37	R/W	Port 7 direction control register	IV-108
P7PLUD	0x03F47	R/W	Port 7 pull-up/pull-down resistor control register	IV-108
P7ODC	0x03EF5	R/W	Port 7 Nch open-drain control register	IV-109
SCHMIT1	0x03EEA	R/W	0.54 V _{DD5} input selection register 1	IV-110
SELUD	0x03F4C	R/W	Pull-up/pull-down resistor selection register	IV-111

R/W:Readable/Writable

- Port 7 output register (P7OUT: 0x03F17)

bp	7	6	5	4	3	2	1	0
Flag	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	P7OUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

- Port 7 Input Register (P7IN: 0x03F27)

bp	7	6	5	4	3	2	1	0
Flag	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	P7IN7-0	Input data 0:Pin is L(V _{SS} level) 1:Pin is H(V _{DD5} level)

■ Port 7 Direction Control Register (P7DIR: 0x03F37)

bp	7	6	5	4	3	2	1	0
Flag	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P7DIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 7 Pull-up/Pull-down Resistor Control Register (P7PLUD: 0x03F47)

bp	7	6	5	4	3	2	1	0
Flag	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P7PLUD7-0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 7 Nch Open-drain Control Register (P7ODC:0x03EF5)

bp	7	6	5	4	3	2	1	0
Flag	P7ODC7	-	P7ODC5	P7ODC4	P7ODC3	P7ODC2	-	P7ODC0
At reset	0	-	0	0	0	0	-	0
Access	R/W	-	R/W	R/W	R/W	R/W	-	R/W

bp	Flag	Description
7	P7ODC7	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
6	-	-
5-2	P7ODC5-2	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output
1	-	-
0	P7ODC0	Nch open-drain output selection 0:Push-pull output 1:Nch open-drain output

■ 0.54 V_{DD5} Input Control Register (SCHMIT1:0x03EEA)

The input level of P0(P00 to P07) to P7(P70 to P77) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	SCHMIT17	SCHMIT16	SCHMIT15	SCHMIT14	SCHMIT13	SCHMIT12	SCHMIT11	SCHMIT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SCHMIT17	Port 70 to Port 77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
6	SCHMIT16	Port 60 to Port 67 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
5	SCHMIT15	Port 50 to Port 57 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
4	SCHMIT14	Port 40 to Port 47 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
3	SCHMIT13	Port 30 to Port 36 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT12	Port 20 to Port 24 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT11	Port 10 to Port 16 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT10	Port 00 to Port 07 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

■ Pull-up/pull-down Resistor Selection Register (SELUD: 0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	SELUD7	SELUD6	SELUD5	SELUD4	SELUD3	SELUD2	SELUD1	SELUD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	SELUD7	Pull-up/pull-down selection (port7) 0:Pull-up 1:Pull-down
6	SELUD6	Pull-up/pull-down selection (port6) 0:Pull-up 1:Pull-down
5	SELUD5	Pull-up/pull-down selection (port5) 0:Pull-up 1:Pull-down
4	SELUD4	Pull-up/pull-down selection (port4) 0:Pull-up 1:Pull-down
3	SELUD3	Pull-up/pull-down selection (port3) 0:Pull-up 1:Pull-down
2	SELUD2	Pull-up/pull-down selection (port2) 0:Pull-up 1:Pull-down
1	SELUD1	Pull-up/pull-down selection (port1) 0:Pull-up 1:Pull-down
0	SELUD0	Pull-up/pull-down selection (port0) 0:Pull-up 1:Pull-down

4.10.3 Block Diagram

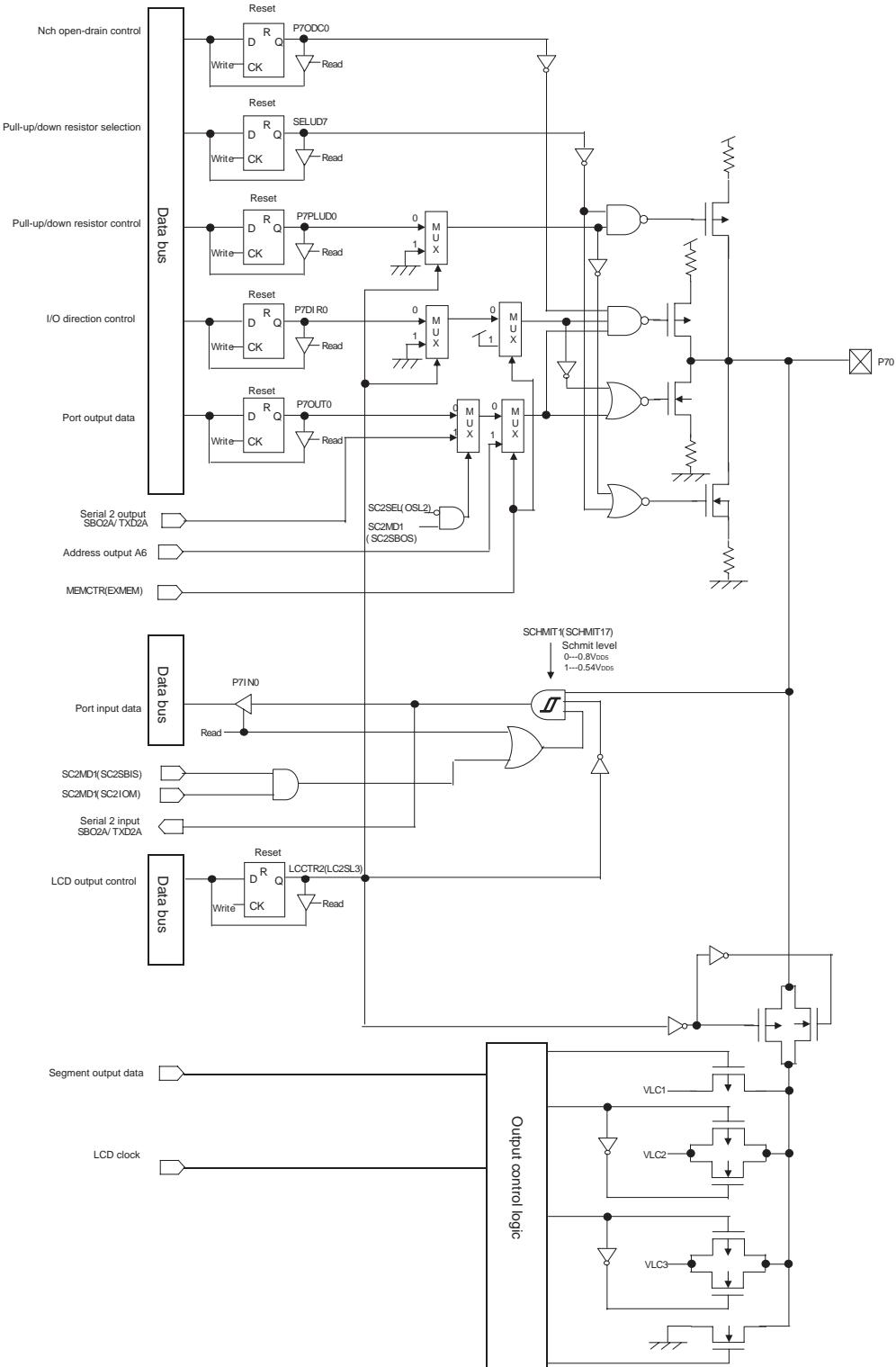


Figure:4.10.1 Block Diagram (P70)

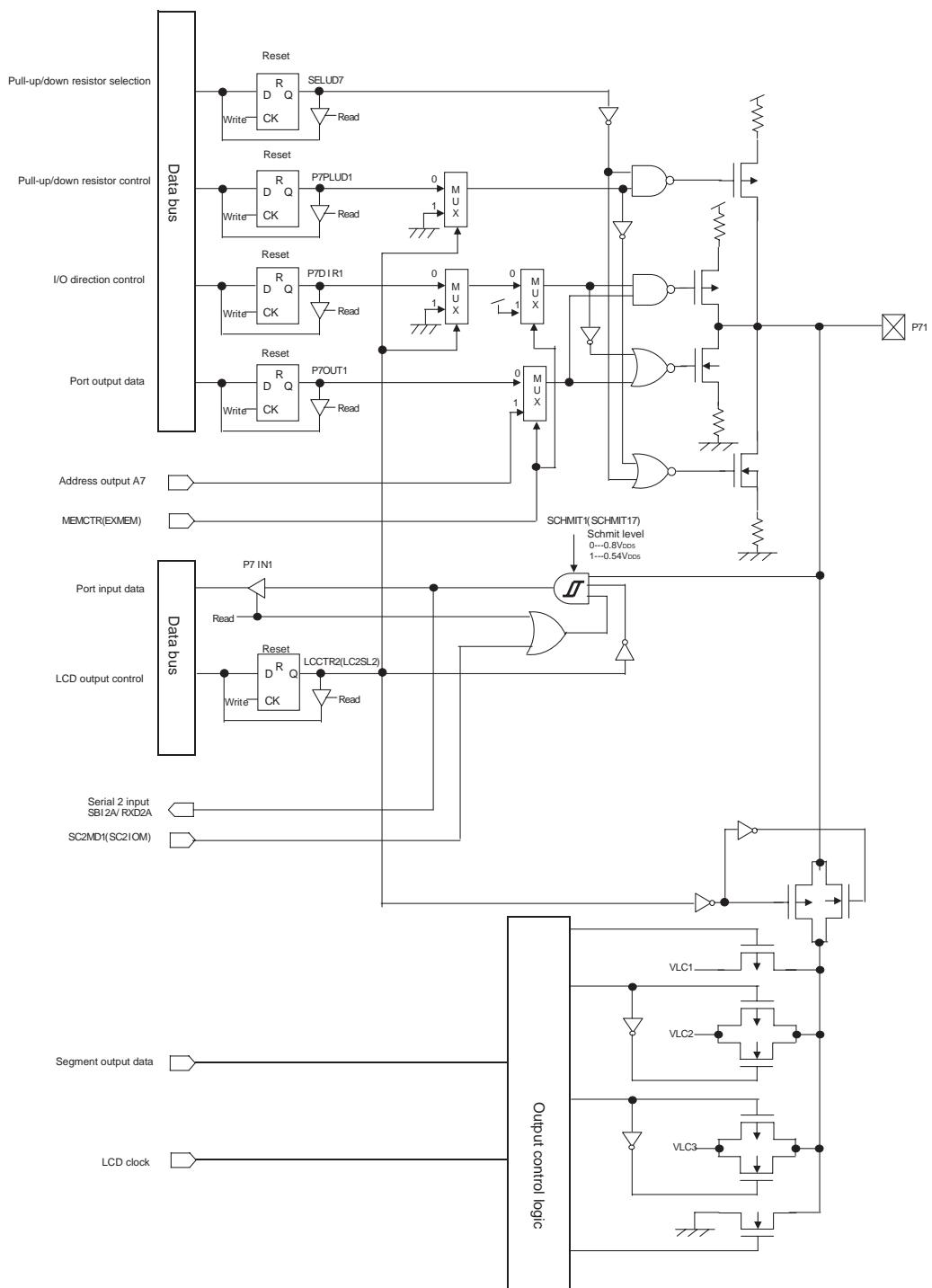


Figure:4.10.2 Block Diagram (P71)

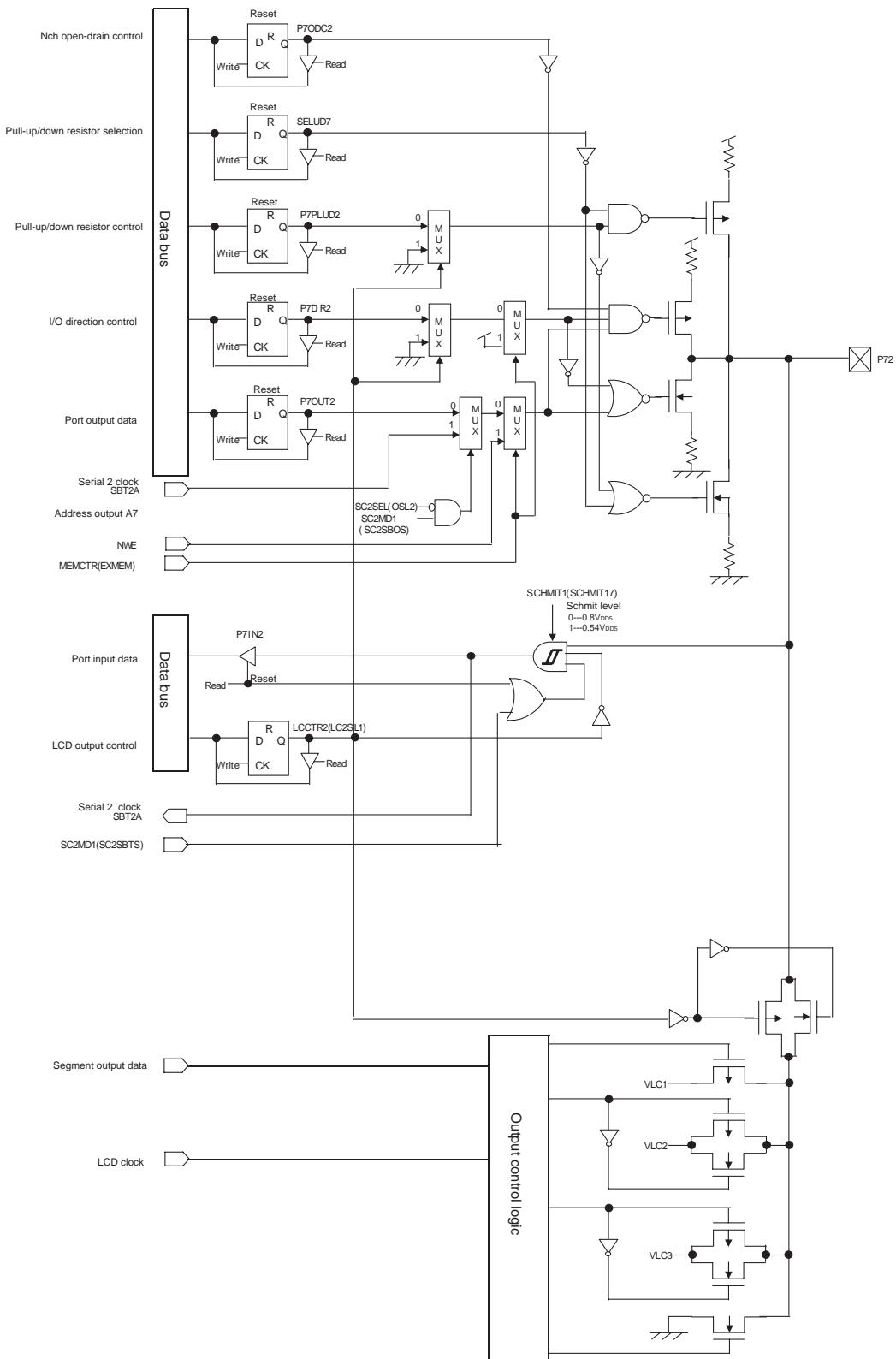


Figure:4.10.3 Block Diagram (P72)

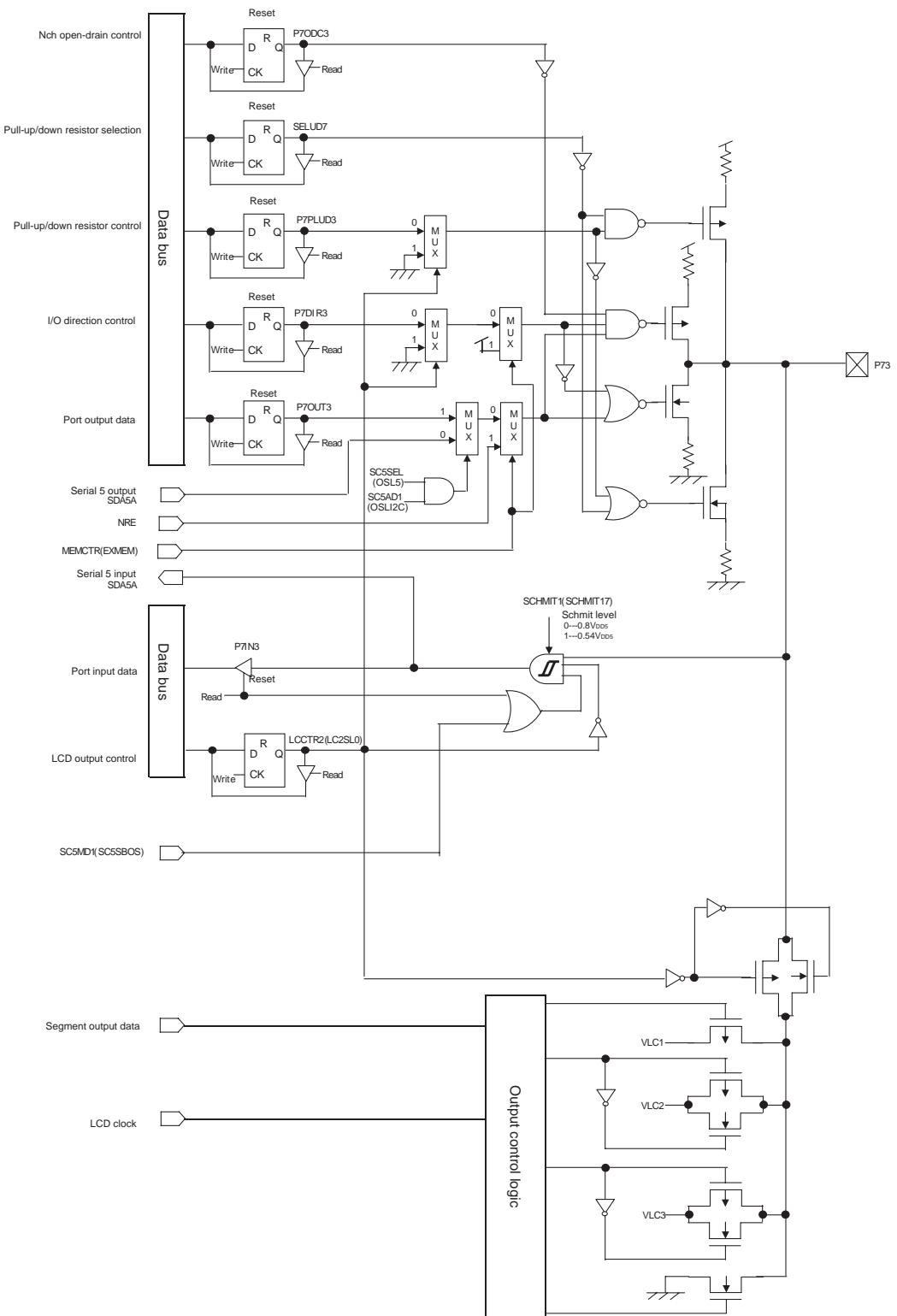


Figure 4.10.4 Block Diagram (P73)

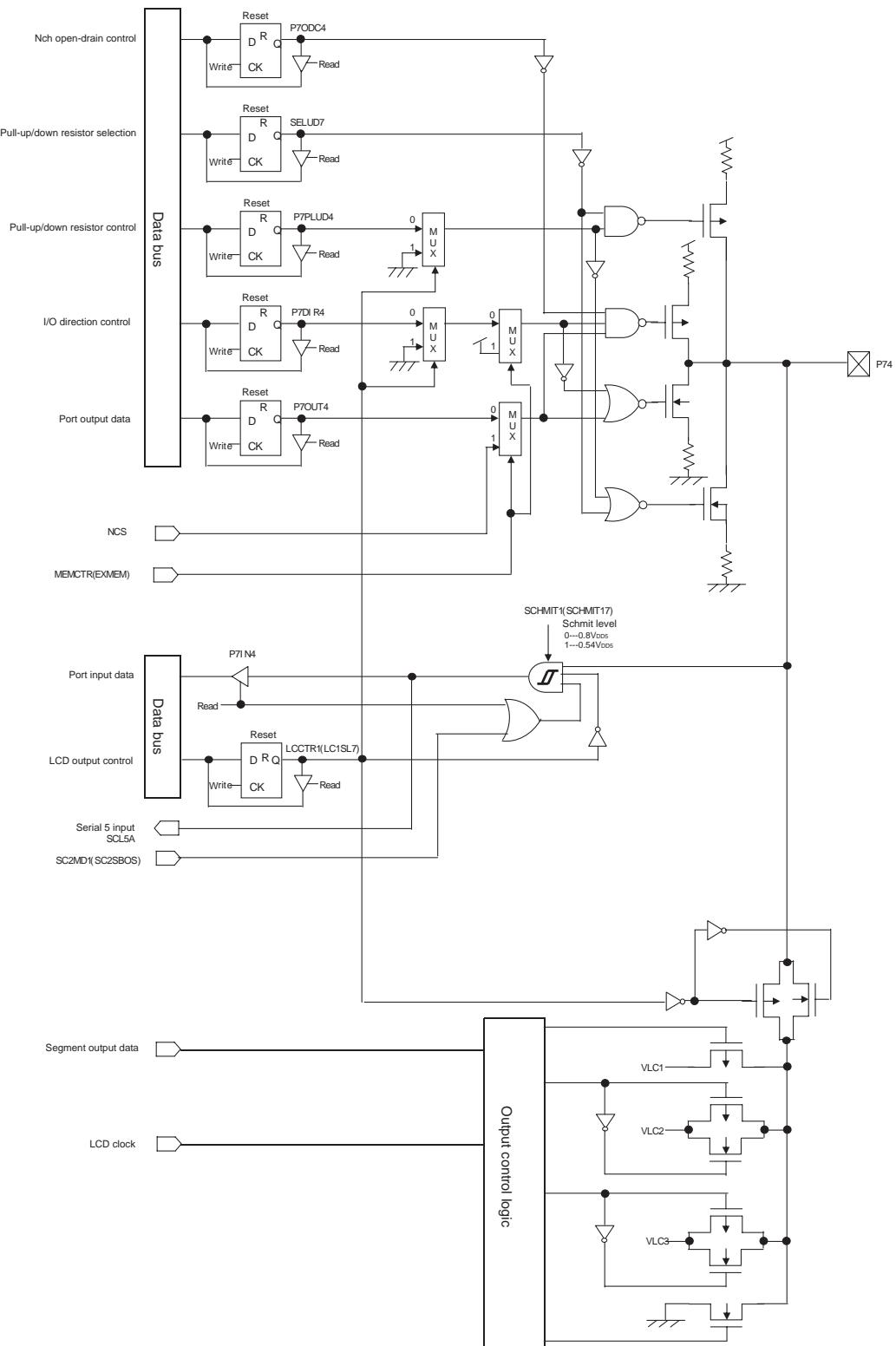


Figure:4.10.5 Block Diagram (P74)

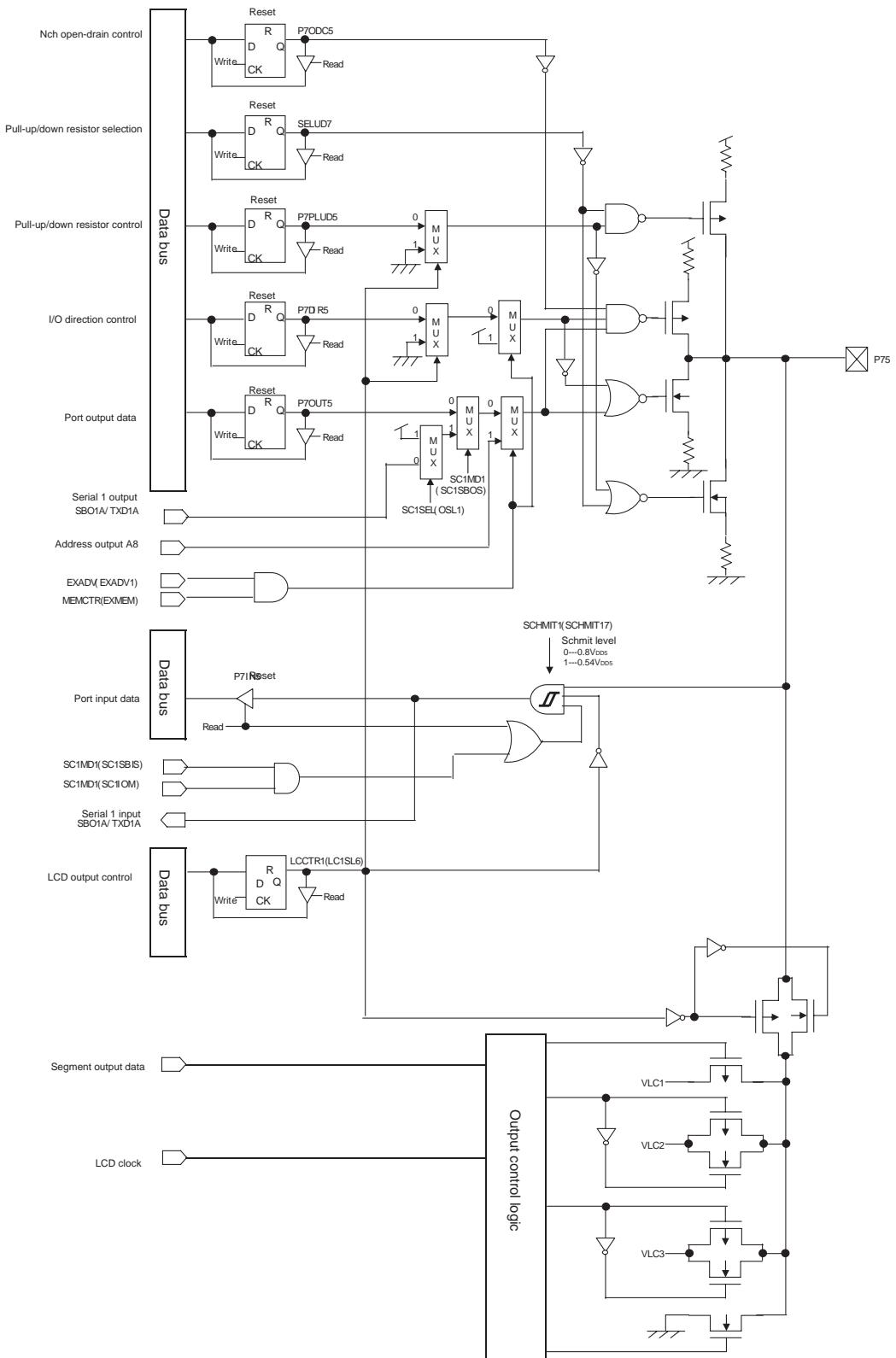


Figure:4.10.6 Block Diagram (P75)

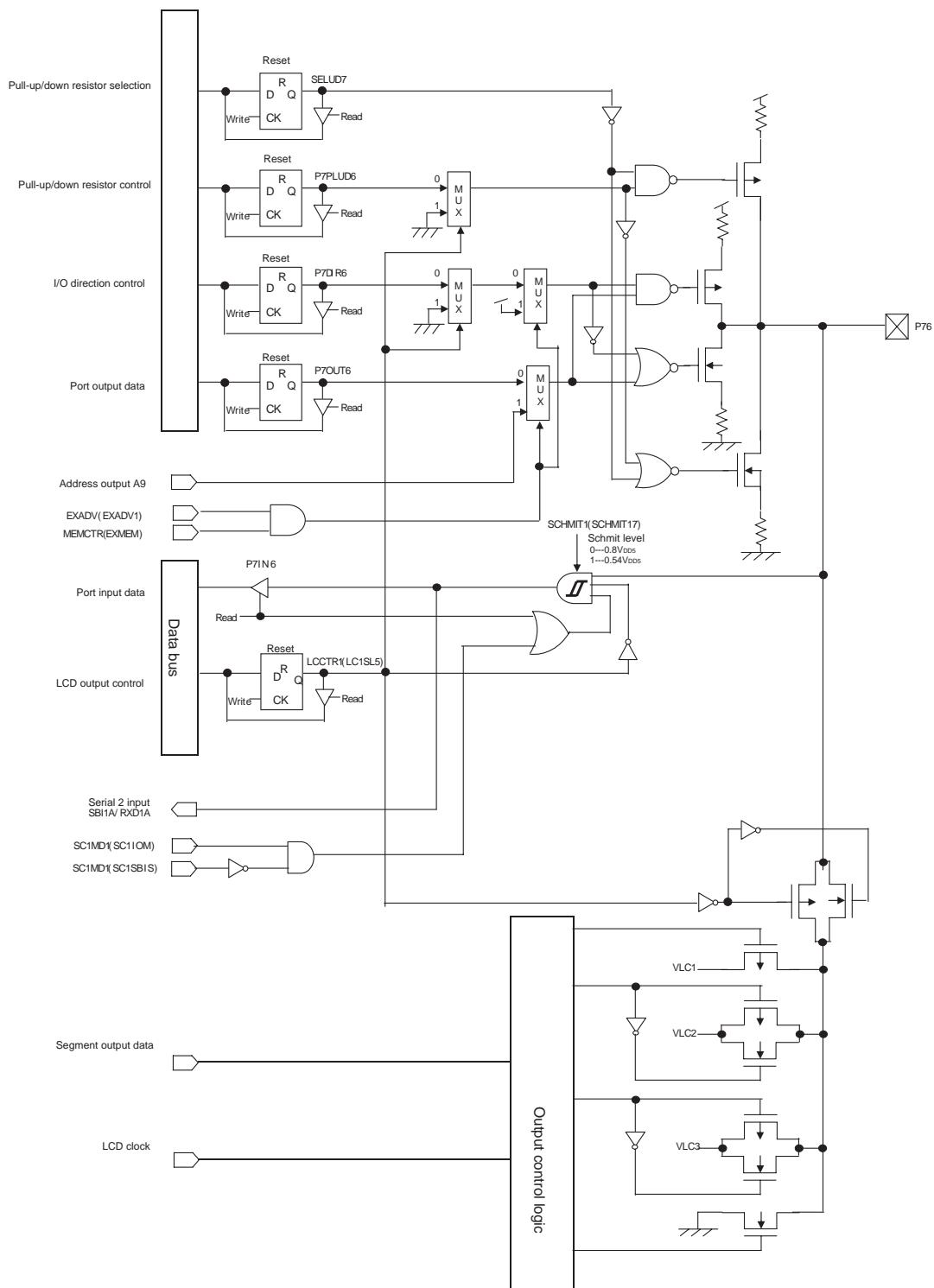


Figure:4.10.7 Block Diagram (P76)

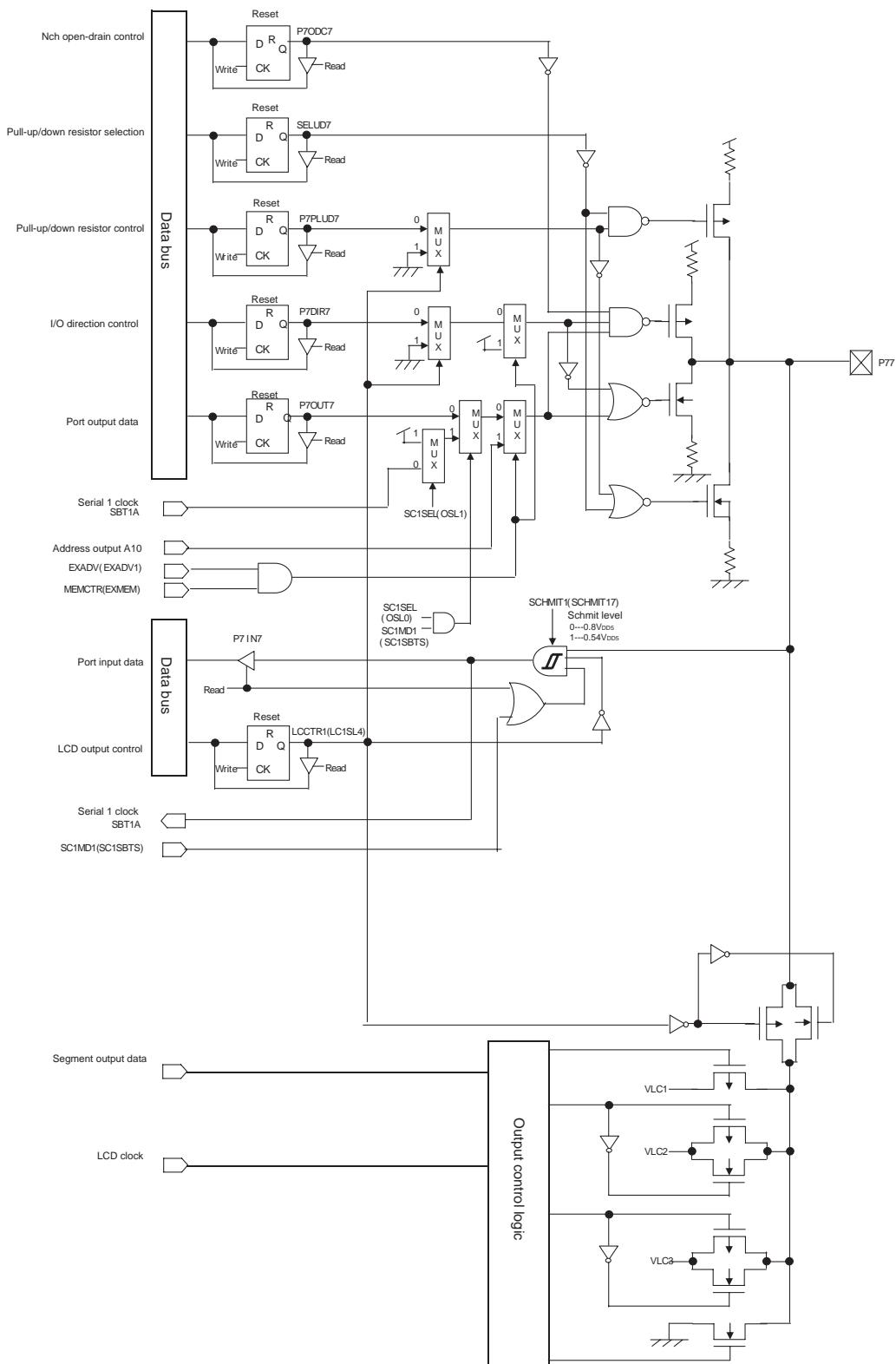


Figure:4.10.8 Block Diagram (P77)

4.11 Port 8

4.11.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 8 direction control register (P8DIR) to "1" and write data to the port 8 output register (P8OUT).

To read input data of pin, set the control flag of the port 8 direction control register (P8DIR) to "0" and read the value of the port 8 input register (P8IN).

Each bit can be set individually to either an input or output by the port 8 direction control register (P8DIR). The control flag of the port 8 direction control register (P8DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 8 pull-up resistor control register (P8PLU). Set the control flag of the port 8 pull-up resistor control register (P8PLU) to "1" to add pull-up resistor.

Each bit can be selected individually as synchronous mode by the port 8 synchronous output control register (P8SYO). The port 8 synchronous output control register (P8SYO) is set to "1" for synchronous output, and "0" for general port.

■ Special Function Pin Setup

P80 to P85 have the real time output control function and change the output pin to the follow 3 value ; "0", "1" and "high impedance (Hi-z)" by the event generate timing of the external interrupt 0 falling edge. The real time control is the function to change the output signal to the interrupt event without software.

P80 to P85 can be selected timer output or port output. Each bit for the I/O mode can be selected by the port 8 output mode register1 (P8OMD1). The port 8 output mode register1 (PAOMD1) is set to "1" for I/O of special function data, and "0" to be used as the general port.

P80 to P83 are also used as LCD segment output pin. SEG 3 to 0 pins can be selected when the flag of the bp3 to 0 of the LCD output control register 1 (LCCTR1) The switching of port and segment can be selected by each bit. When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P84 to P87 are also used as LCD common output pin COM0 to COM3. COM0 to COM3 pins can be selected when the flag of the bp4 to 7 of the LCD output control register 0 (LCCTR0). When the segment output is selected, the output mode is forcibly set and the pull-up resistor is disabled.

P80 to P87 can select synchronous output for each bit by the port 8 synchronous output control register (P8SYO). This port is used as synchronous output when the port 8 synchronous output control register (P8SYO) is "1", and as general port when the register is "0". The event for synchronous output is selected by the port 8 synchronous output event selection register (P8SEV). IRQ0 is selected when the bp1 and bp0 of the port 8 synchronous output event selection register (P8SEV) are 00. TM7IRQ is selected when they are 01, TM2IRQ is selected when they are 10, and TM1IRQ is selected when they are 11.

P80 can be used as address output pin to the external extension memory in the memory extension mode. Set the bp5 of the address output control register (EXADV). Otherwise, this pin is used as a general port pin. Output mode is forcibly selected when the bp5 of the address output control register (EXADV) is "1" in the memory extension mode.

P81 to P84 can be used as address output pin to the external extension memory in the memory extension mode. Set the bp6 of the address output control register (EXADV). Otherwise, this pin is used as a general port pin. Out-

put mode is forcibly selected when the bp6 of the address output control register (EXADV) is "1" in the memory extension mode.

P85 to P87 can be used as address output pin to the external extension memory in the memory extension mode. Set the bp7 of the address output control register (EXADV). Otherwise, this pin is used as a general port pin. Output mode is forcibly selected when the bp7 of the address output control register (EXADV) is "1" in the memory extension mode.

4.11.2 Registers

Table:4.11.1 shows the registers that control the port 8.

Table:4.11.1 Port 8 Control Register

Registers	Address	R/W	Function	Page
P8OUT	0x03F18	R/W	Port 8 output register	IV-122
P8IN	0x03F28	R	Port 8 input register	IV-123
P8DIR	0x03F38	R/W	Port 8 direction control register	IV-123
P8PLU	0x03F48	R/W	Port 8 pull-up resistor control register	IV-123
P8OMD1	0x03EE5	R/W	Port 8 output mode register1	IV-124
P8CNT1	0x03EFB	R/W	Port 8 output control register1	IV-125
P8CNT2	0x03EFC	R/W	Port 8 output control register2	IV-126
P8SYO	0x03EF7	R/W	Port 8 synchronous output control register	IV-126
P8SEV	0x03EF8	R/W	Port 8 synchronous output event selection register	IV-127
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection register 1	IV-127

R/W:Readable/Writable

- Port 8 output register (P8OUT: 0x03F18)

bp	7	6	5	4	3	2	1	0
Flag	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	P8OUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 8 Input Register (P8IN: 0x03F28)

bp	7	6	5	4	3	2	1	0
Flag	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	P8IN7-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 8 Direction Control Register (P8DIR: 0x03F38)

bp	7	6	5	4	3	2	1	0
Flag	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P8DIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 8 Pull-up Resistor Control Register (P8PLU: 0x03F48)

bp	7	6	5	4	3	2	1	0
Flag	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P8PLU7-0	Pull-up resistor selection 0:Not added 1:Added

■ Port 8 Output Mode Register1 (P8OMD1:0x03EE5)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P8OMD15	P8OMD14	P8OMD13	P8OMD12	P8OMD11	P8OMD10
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5	P8OMD15	I/O port, Timer output selection 0:Port P85 1:Timer output
4	P8OMD14	I/O port, Timer output selection 0:Port P84 1:Timer output
3	P8OMD13	I/O port, Timer output selection 0:Port P83 1:Timer output
2	P8OMD12	I/O port, Timer output selection 0:Port P82 1:Timer output
1	P8OMD11	I/O port, Timer output selection 0:Port P81 1:Timer output
0	P8OMD10	I/O port, Timer output selection 0:Port P80 1:Timer output

■ Port 8 Output Control Register1 (P8CNT1:0x03EFB)

bp	7	6	5	4	3	2	1	0
Flag	P8CNT17	P8CNT16	P8CNT15	P8CNT14	P8CNT13	P8CNT12	P8CNT11	P8CNT10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-6	P8CNT17-16	P83 Real time control (IRQ0 event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
5-4	P8CNT15-14	P82 Real time control (IRQ0 event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
3-2	P8CNT13-12	P81 Real time control (IRQ0 event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
1-0	P8CNT11-10	P80 Real time control (IRQ0 event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output

■ Port 8 Output Control Register2 (P8CNT2:0x03EFC)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	P8CNT23	P8CNT22	P8CNT21	P8CNT20
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3-2	P8CNT23-2	P85 Real time control (IRQO event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
1-0	P8CNT21-0	P84 Real time control (IRQO event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output

■ Port 8 Synchronous Output Control Register (P8SYO: 0x03EF7)

bp	7	6	5	4	3	2	1	0
Flag	P8SYO7	P8SYO6	P8SYO5	P8SYO4	P8SYO3	P8SYO2	P8SYO1	P88SYO0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	P8SYO7-0	Synchronous output selection 0:I/O port 1:Synchronous output

■ Port 8 Synchronous Output Event Selection Register (P8SEV: 0x03EF8)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	P8SEV1	P8SEV0
At reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R/W	R/W

bp	Flag	Description
-	-	-
1-0	P8SEV1-0	Synchronous output event selection 00: IRQ2 01: TM7IRQ 10: TM2IRQ 11: TM1IRQ

■ 0.54 V_{DD5} Input Control Register (SCHMIT2:0x03EFA)

The input level of P8 (P80 to P87) to PB (PB0 to PB7) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SCHMIT2B	SCHMIT2A	SCHMIT29	SCHMIT28
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3	SCHMIT2B	Port B0 to Prot B7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT2A	Port A0 to Prot A7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT29	Port 90 to Prot 96 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT28	Port 80 to Prot 87 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

4.11.3 Block Diagram

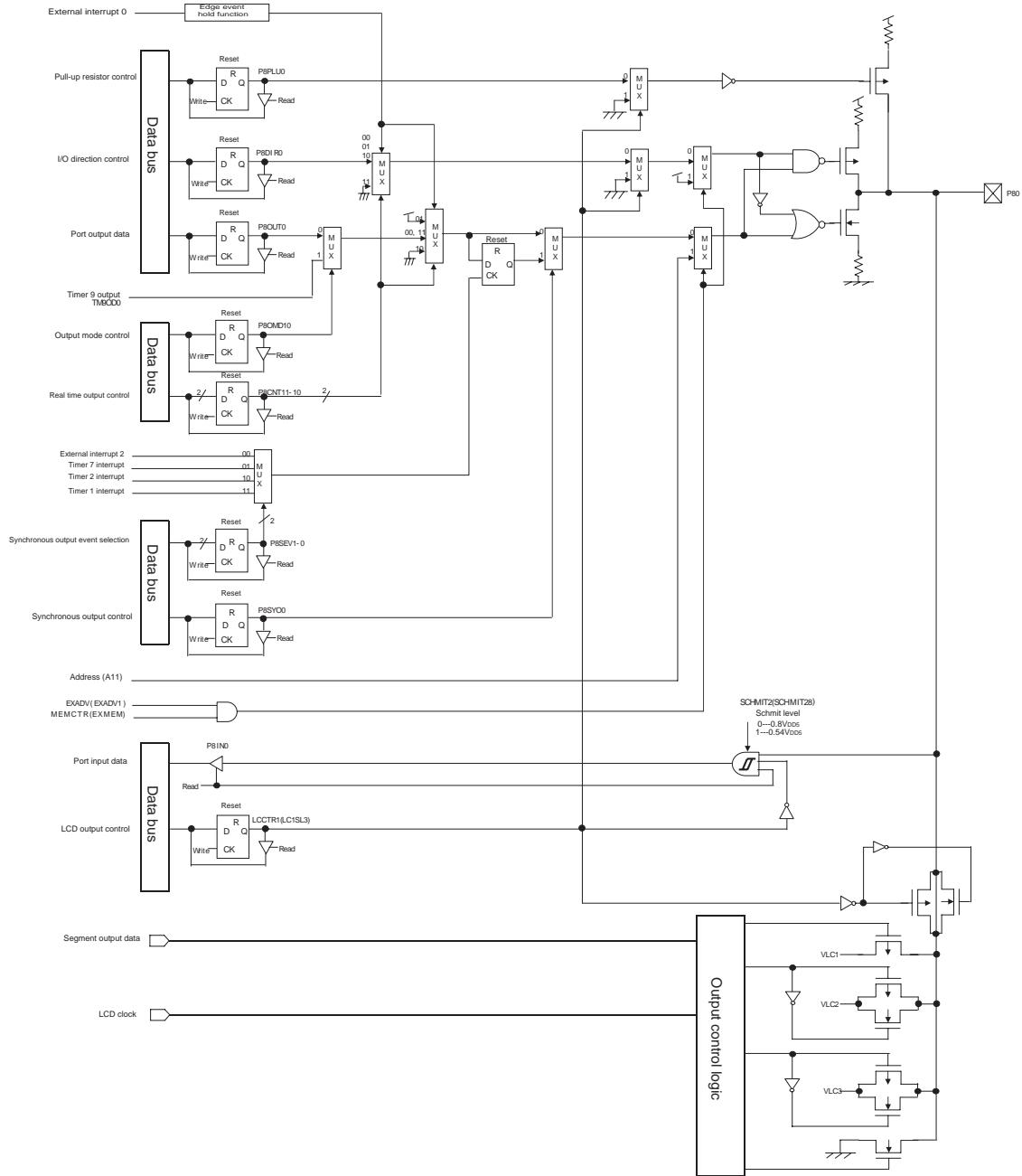


Figure 4.11.1 Block Diagram (P80)

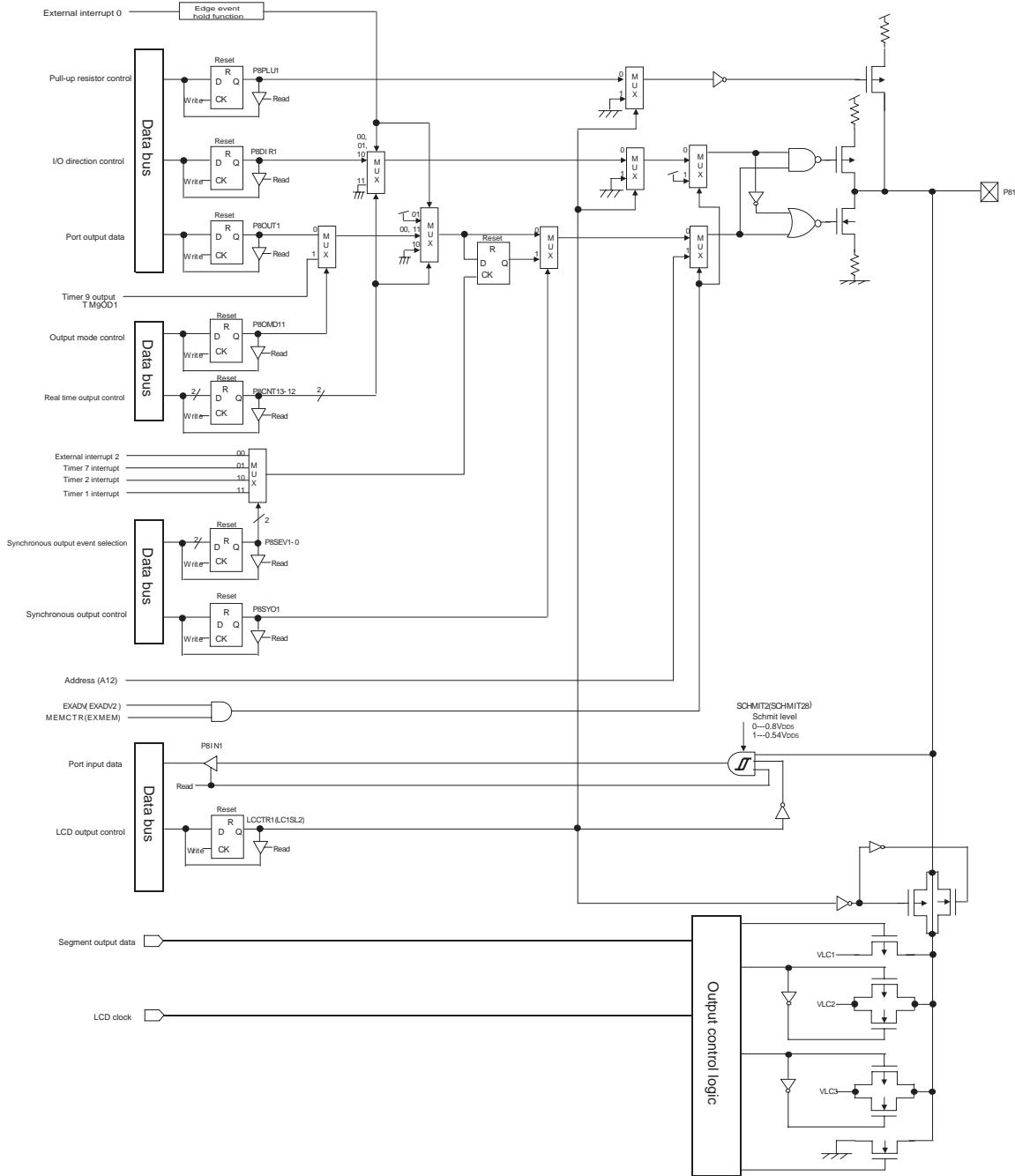


Figure:4.11.2 Block Diagram (P81)

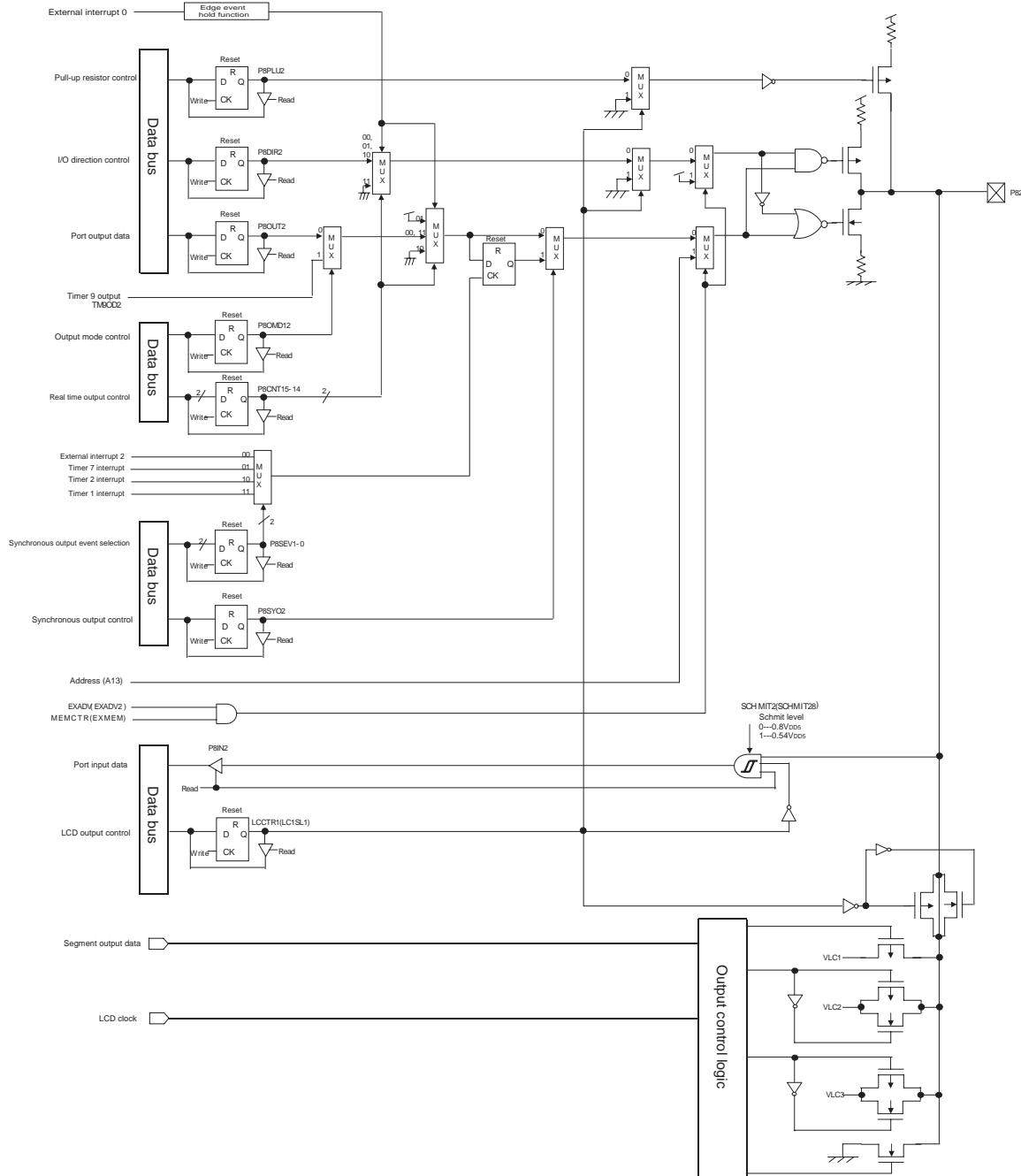


Figure:4.11.3 Block Diagram (P82)

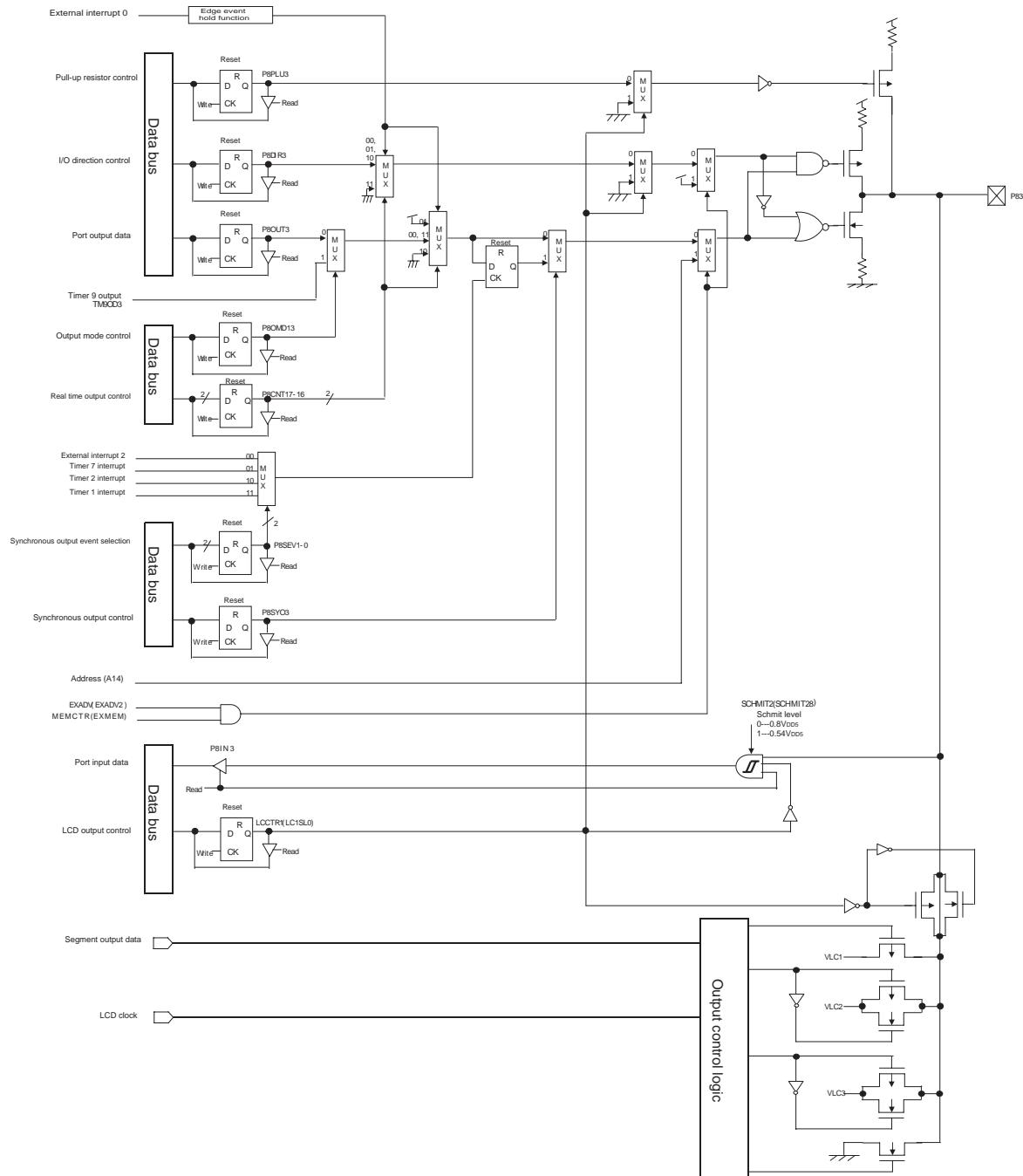


Figure:4.11.4 Block Diagram (P83)

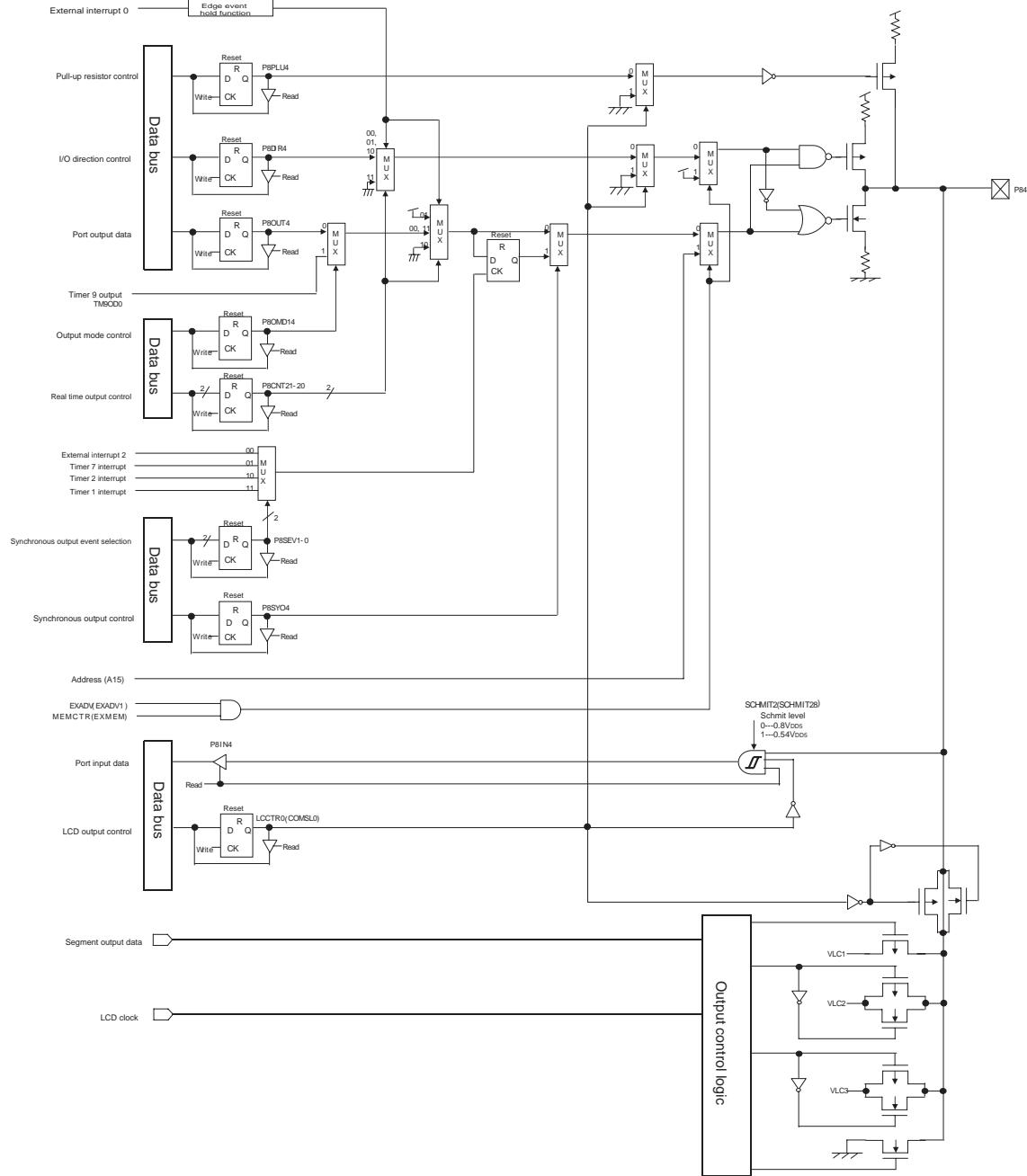


Figure:4.11.5 Block Diagram (P84)

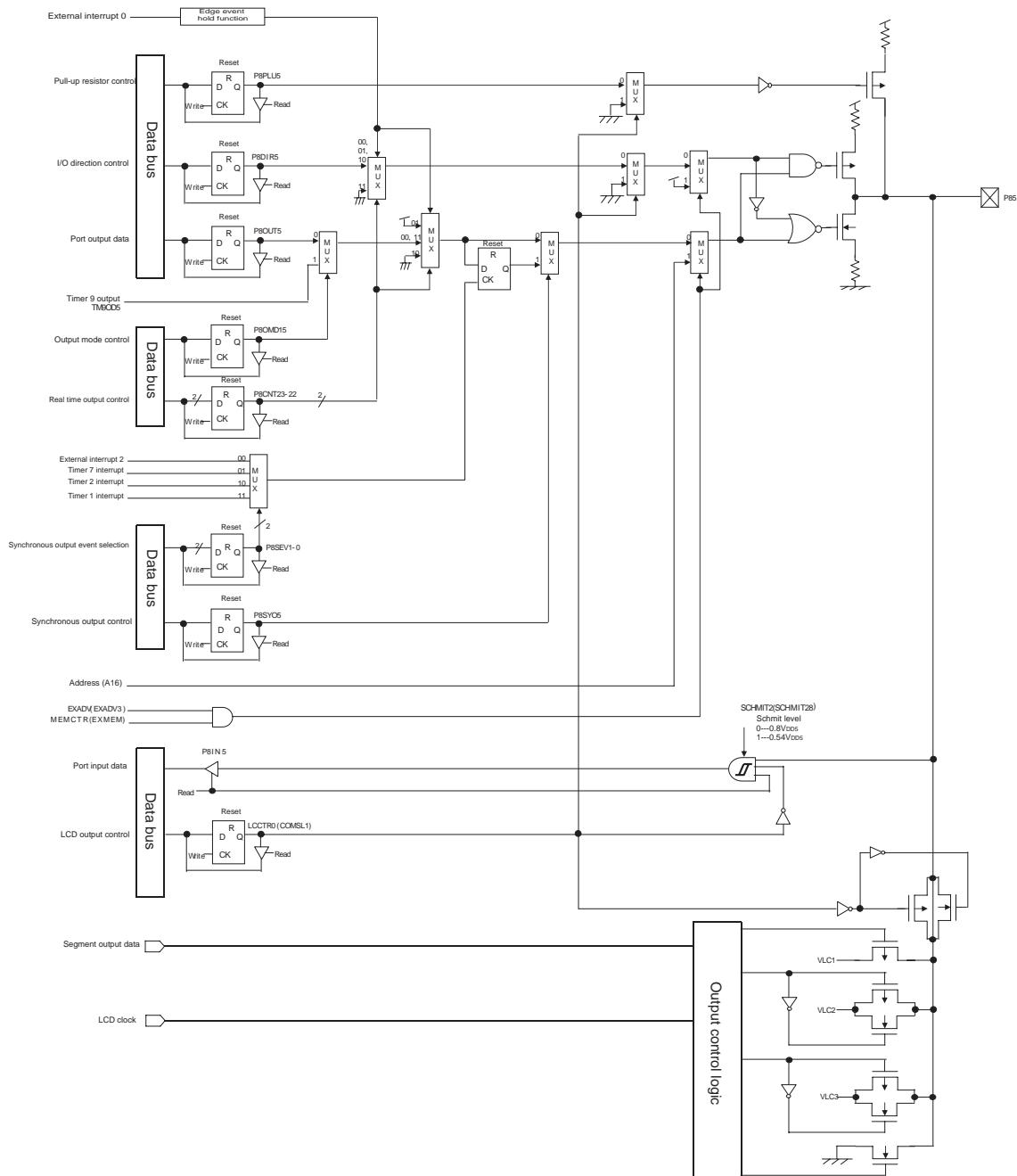


Figure:4.11.6 Block Diagram (P85)

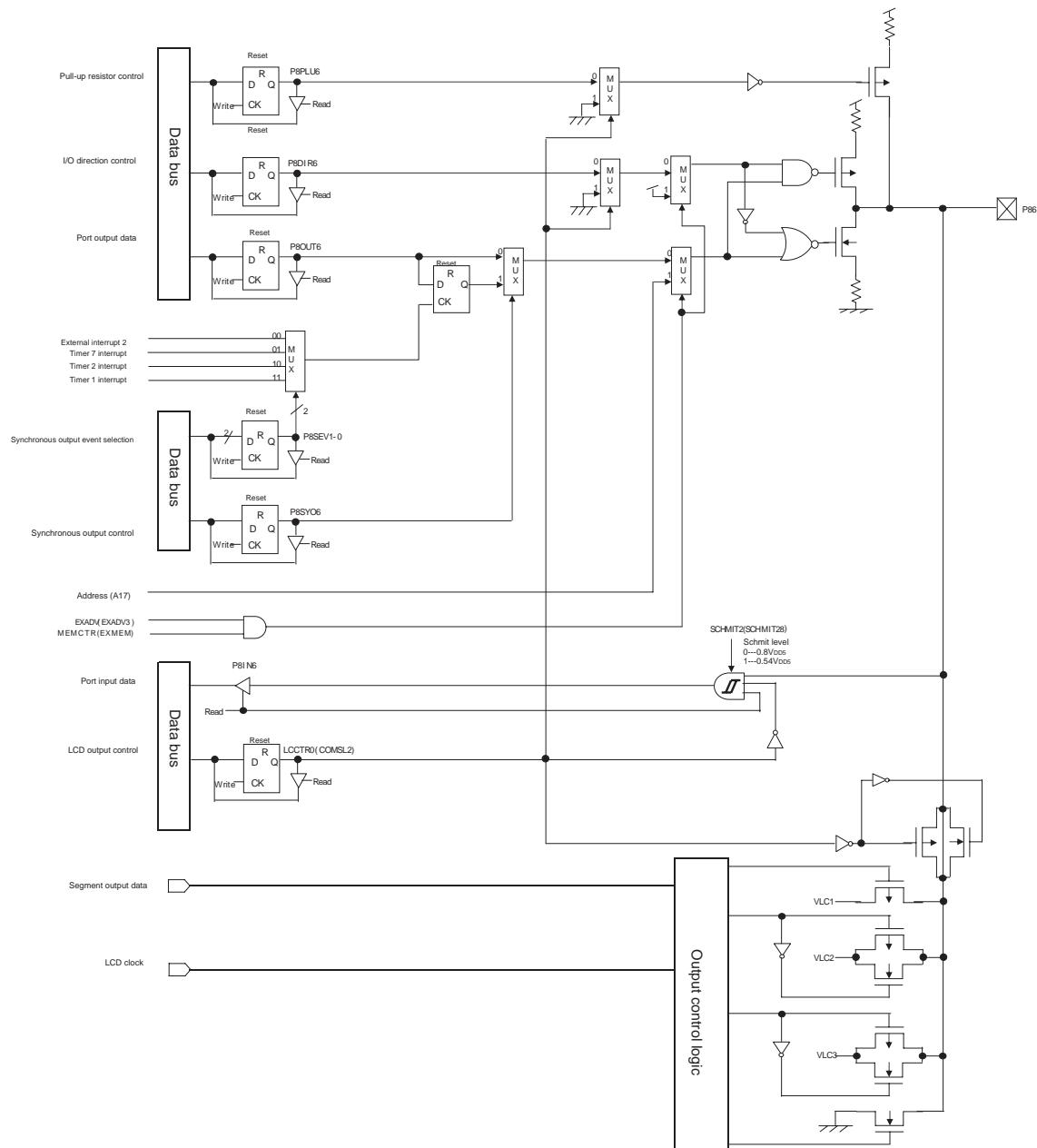


Figure:4.11.7 Block Diagram (P86)

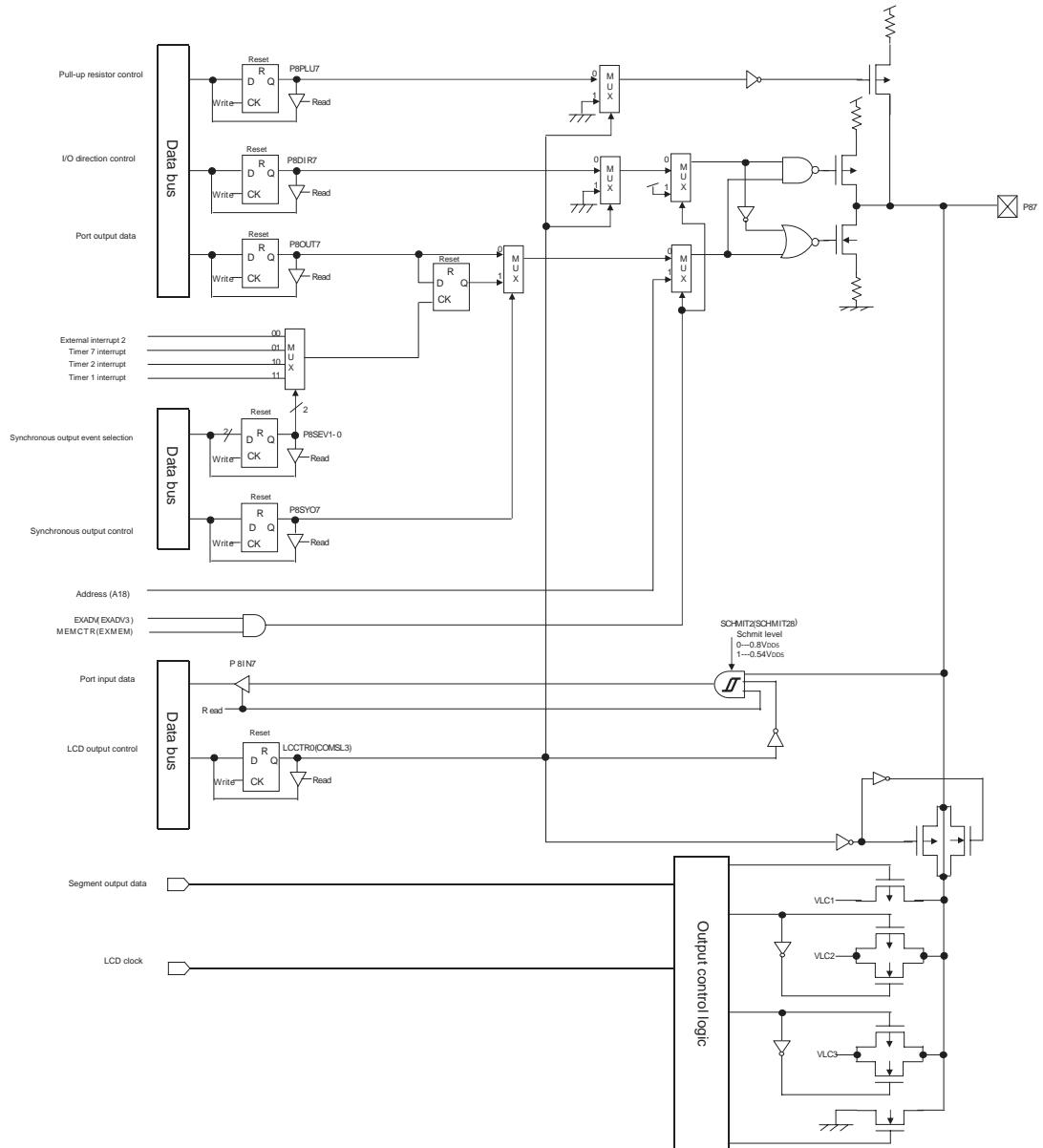


Figure:4.11.8 Block Diagram (P87)

4.12 Port 9

4.12.1 Description

■ General Port Setup

To output data to pin, set the control flag of the port 9 direction control register (P9DIR) to "1" and write data to the port 9 output register (P9OUT).

To read input data of pin, set the control flag of the port 9 direction control register (P9DIR) to "0" and read the value of the port 9 input register (P9IN).

Each bit can be set individually to either an input or output by the port 9 direction control register (P9DIR). The control flag of the port 9 direction control register (P9DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 9 pull-up resistor control register (P9PLU). Set the control flag of the port 9 pull-up resistor control register (P9PLU) to "1" to add pull-up resistor.

■ Special Function Pin Setup

P92 to P94 are also used as the power supply pin VLC3 to VLC1 of LCD drive circuit. VLC3 to VLC1 pins are selected by setting bp2 to 0 flag of LCD output control register 0 (LCCTR0) to "1". In selecting VLC3 to VLC1 pins, pull-up resistor is disabled.

P92 can be used as address output pin to the external extension memory in the memory extension mode. Set the bp5 of the address output control register (EXADV). Otherwise, this pin is used as a general port pin. Output mode is forcibly selected when the bp7 of the address output control register (EXADV) is "1" in the memory extension mode.

P93 is also used as input pin of data acknowledge signal in the memory extension mode. Output mode is forcibly selected in this mode.

P94 to P95 are also used as analog C, D.

P90 to P91 are also used as low-speed oscillator. These pins can be used as low-speed oscillator when XI/XO selection flag of low-speed oscillator selection register (XSEL).

4.12.2 Registers

Table:4.12.1 shows the registers that control the port 9.

Table:4.12.1 Port 9 Control Register

Registers	Address	R/W	Function	Page
P9OUT	0x03F19	R/W	Port 9 output register	IV-137
P9IN	0x03F29	R	Port 9 input register	IV-138
P9DIR	0x03F39	R/W	Port 9 direction control register	IV-138
P9PLU	0x03F49	R/W	Port 9 pull-up resistor control register	IV-138
P9OMD	0x03EE7	R/W	Port 9 output mode register	IV-139
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection register 1	IV-139

R/W:Readable/Writable

- Port 9 output register (P9OUT: 0x03F19)

bp	7	6	5	4	3	2	1	0
Flag	-	P9OUT6	P9OUT5	P9OUT4	P9OUT3	P9OUT2	P9OUT1	P9OUT0
At reset	-	x	x	x	x	x	x	x
Access	-	R/W						

bp	Flag	Flag
7	-	-
6-0	P9OUT6-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port 9 Input Register (P9IN: 0x03F29)

bp	7	6	5	4	3	2	1	0
Flag	-	P9IN6	P9IN5	P9IN4	P9IN3	P9IN2	P9IN1	P9IN0
At reset	-	x	x	x	x	x	x	x
Access	-	R	R	R	R	R	R	R

bp	Flag	Description
7	-	-
6-0	P9IN6-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port 9 Direction Control Register (P9DIR: 0x03F39)

bp	7	6	5	4	3	2	1	0
Flag	-	P9DIR6	P9DIR5	P9DIR4	P9DIR3	P9DIR2	P9DIR1	P9DIR0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P9DIR6-0	I/O mode selection 0:Input mode 1:Output mode

■ Port 9 Pull-up Resistor Control Register (P9PLU: 0x03F49)

bp	7	6	5	4	3	2	1	0
Flag	-	P9PLU6	P9PLU5	P9PLU4	P9PLU3	P9PLU2	P9PLU1	P9PLU0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W						

bp	Flag	Description
7	-	-
6-0	P9PLU6-0	Pull-up resistor selection 0:Not added 1:Added

■ Port 9 Output Mode Register (P9OMD:0x03EE7)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	Reserved	-	-	-	-
At reset	-	-	-	0	-	-	-	-
Access	-	-	-	R/W	-	-	-	-

bp	Flag	Description
7-5	-	-
4	Reserved	Always set to "0".
3-0	-	-

■ 0.54 V_{DD5} Input Control Register (SCHMIT2:0x03EFA)

The input level of P 8(P80 to P87) to PB (PB0 to PB7) recognized "H" can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SCHMIT2B	SCHMIT2A	SCHMIT29	SCHMIT28
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3	SCHMIT2B	Port B0 to Prot B7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT2A	Port A0 to Prot A7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT29	Port 90 to Prot 96 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT28	Port 80 to Prot77 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

4.12.3 Block Diagram

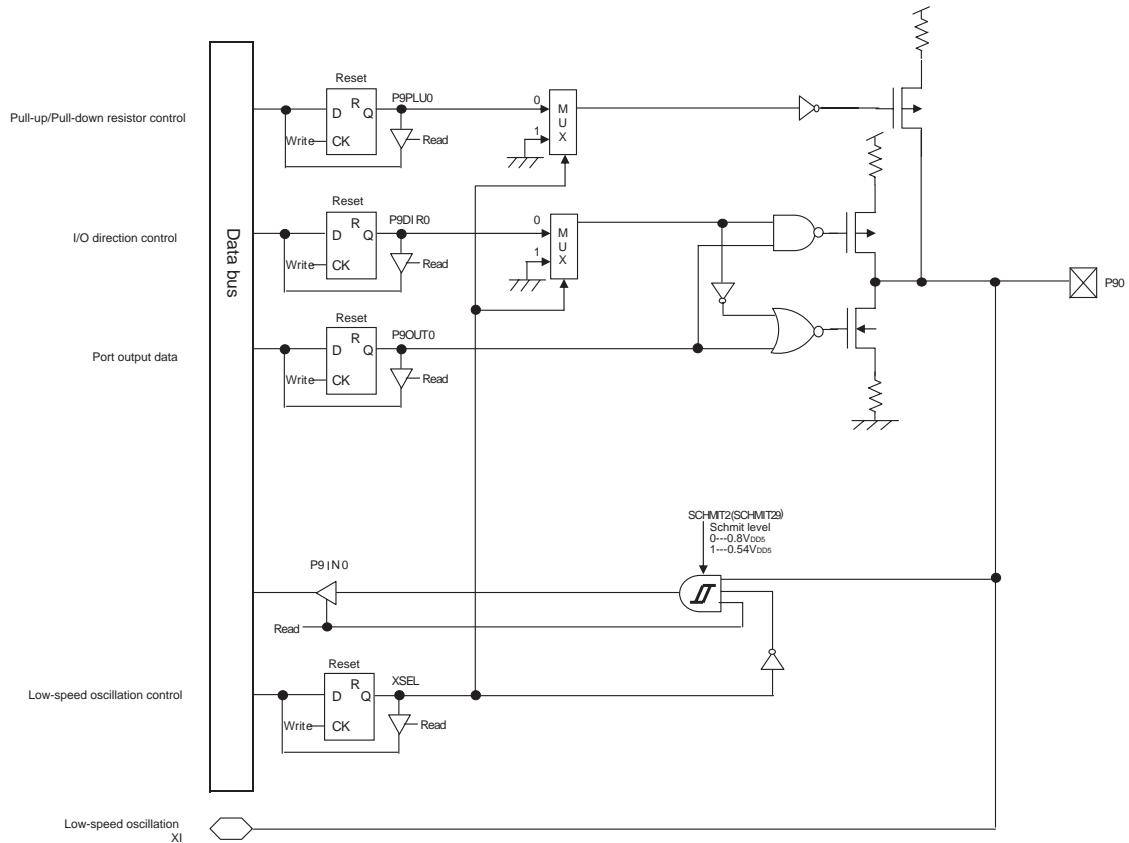


Figure 4.12.1 Block Diagram (P90)

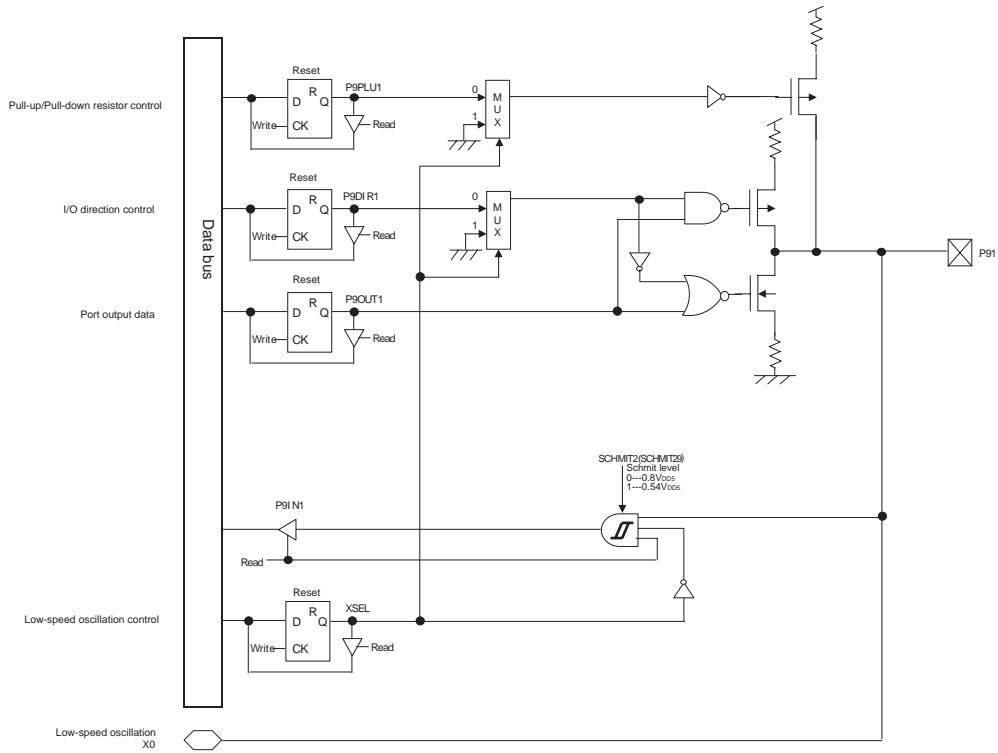


Figure:4.12.2 Block Diagram (P91)

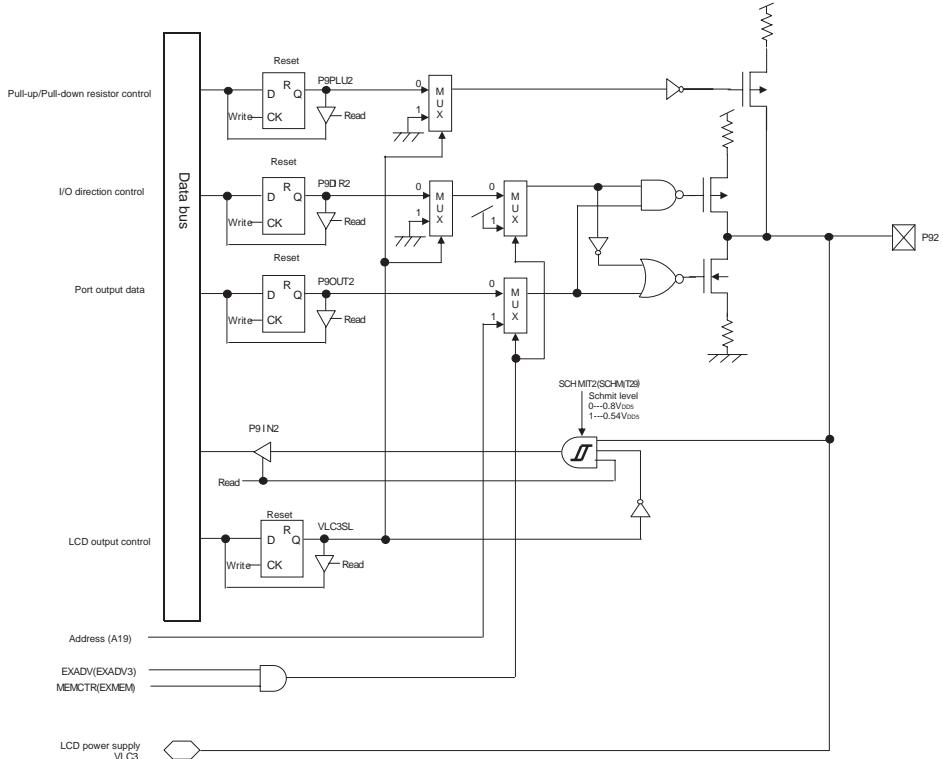


Figure:4.12.3 Block Diagram (P92)

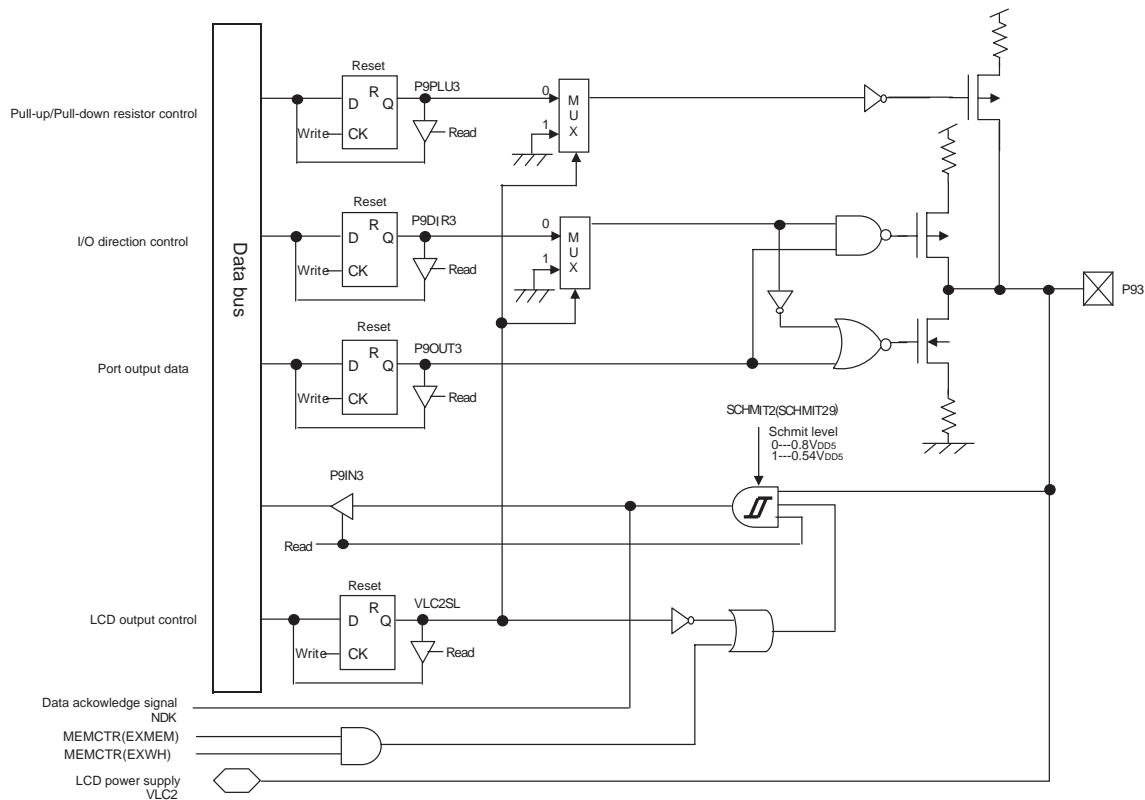


Figure:4.12.4 Block Diagram (P93)

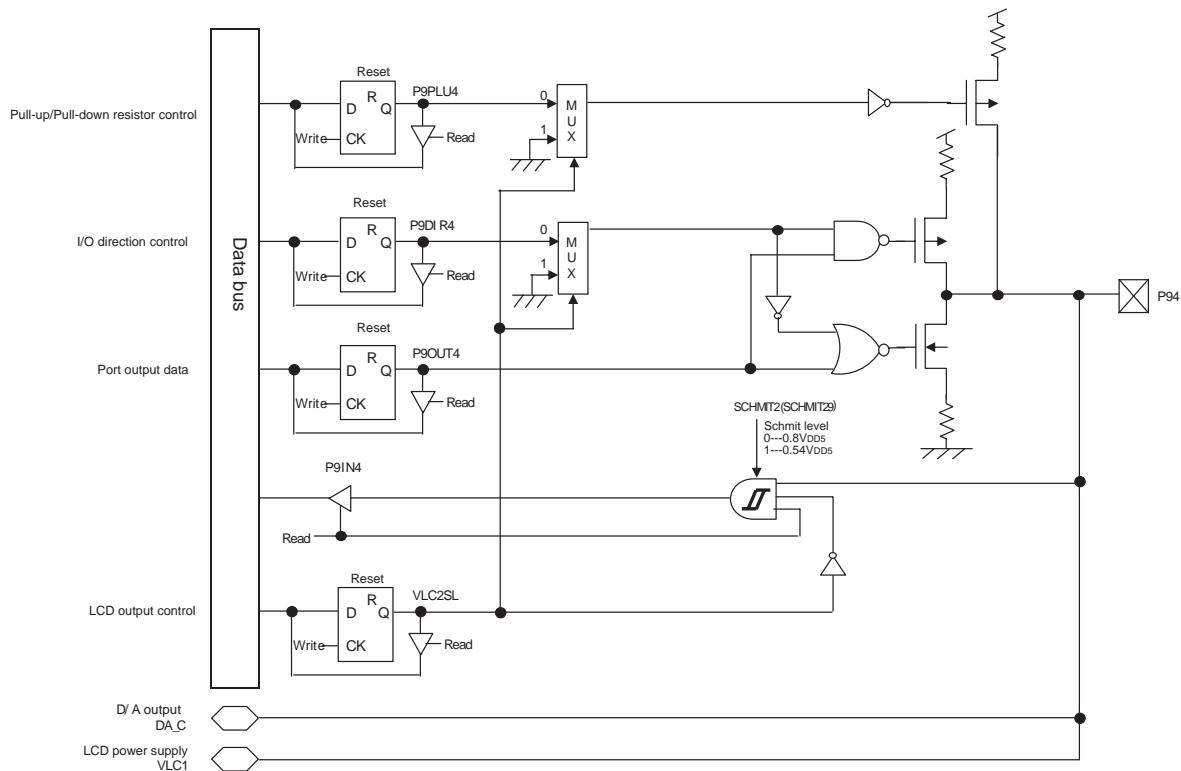


Figure:4.12.5 Block Diagram (P94)

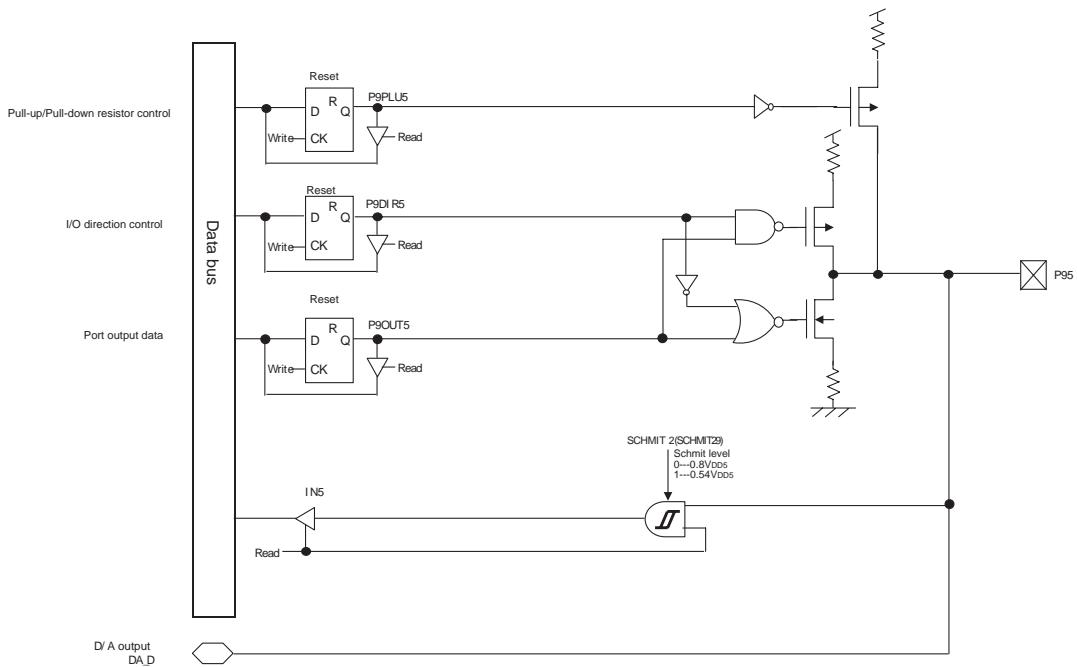


Figure:4.12.6 Block Diagram (P95)

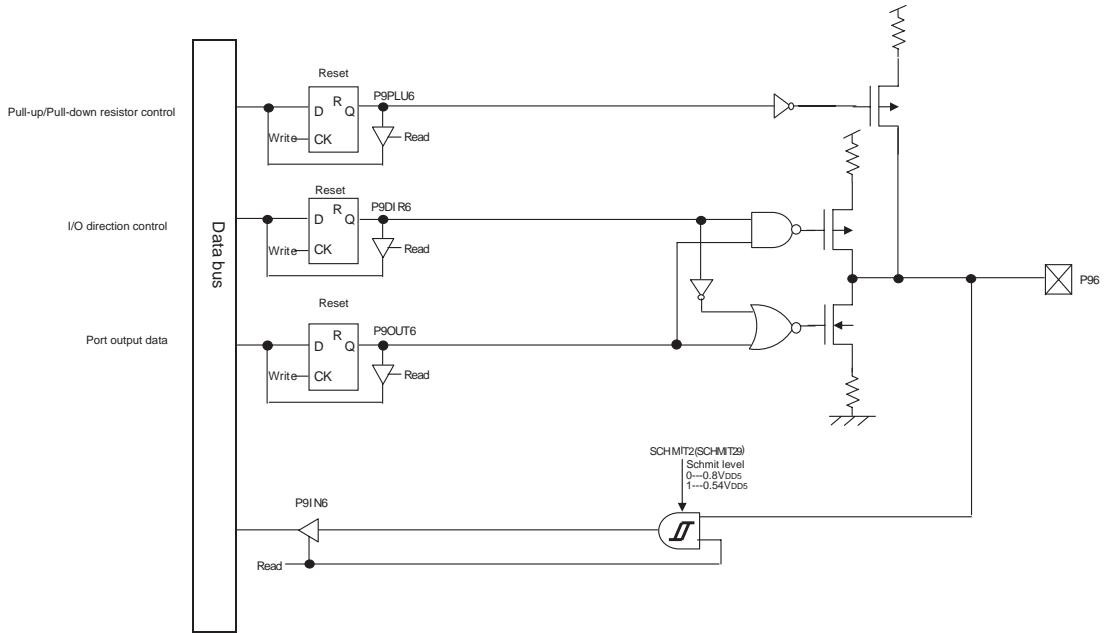


Figure:4.12.7 Block Diagram (P96)

4.13 Port A

4.13.1 Description

■ General Pin Setup

To output data to pin, set the control flag of the port A direction control register (PADIR) to "1" and write data to the port A output register (PAOUT).

To read input data of pin, set the control flag of the port A direction control register (PADIR) to "0" and read the value of the port A input register (PAIN).

Each bit can be set individually to either an input or output by the port A direction control register (PADIR). The control flag of the port A direction control register (PADIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port A pull-up resistor control register (PAPLU). Set the control flag of the port A pull-up resistor control register (PAPLU) to "1" to add pull-up/pull-down resistor.

Each bit can be selected individually as input mode by the port A input mode register (PAIMD). The control flag of the port A input mode register (PAIMD) is set to "1" to input the special function data and 1 is read out from the port A input register (PAIN), and "0" to use as the general port.

■ Special Function Pin Setup

PA0, PA2 and PA5 have the real time output control function and change the output pin to the follow 3 value ; "0", "1" and "high impedance (Hi-z)" by the event generate timing of the external interrupt 0 falling edge. The real time control is the function to change the output signal to the interrupt event without software.

PA0 to PA7 are also used as analog input pin. Input mode for each bit can be selected by the port A input mode register (PAIMD). When PA0 is used as analog input pin, the value of the port A input register is read to be "0".

PA0 is also used as timer 0 I/O pin, remote control carrier output pin. Each bit for the output mode can be selected by bp0 of the port A output mode register (PAOMD). The port A output mode register (PAOMD) is set to "1" to output the special function data, and "0" to use as the general port.

The bp3 of the remote control carrier output control register (RMCTR) is set to "0" to timer output, and "1" for remote control carrier output.

PA1 is also used as timer 1 I/O pin.

PA2 is also used as timer 2 I/O pin.

PA3 is also used as timer 3 I/O pin.

PA4 is also used as timer 4 I/O pin.

PA5 is also used as timer 7 I/O pin.

PA6 is also used as timer 8 I/O pin.

PA7 is also used as timer 9 I/O pin. Each bit for the I/O mode can be selected by the port A output mode register (PAOMD). The port A output mode register (PAOMD) is set to "1" to in/output the special function data, and "0" to use as the general port.

4.13.2 Registers

Table:4.13.1 shows the registers that control the port A.

Table:4.13.1 Port A Output Control Register

Registers	Address	R/W	Function	Page
PAOUT	0x03F1A	R/W	Port A output register	IV-145
PAIN	0x03F2A	R	Port A input register	IV-146
PADIR	0x03F3A	R/W	Port A direction control register	IV-146
PAPLU	0x03F4A	R/W	Port A pull-up resistor control register	IV-146
PAOMD	0x03EE6	R/W	Port A output mode register	IV-147
PAIMD	0x03EE8	R/W	Port A input control register1	IV-148
PACNT	0x03EF6	R/W	Port A output control register	IV-149
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection register 1	IV-150

R/W:Readable/Writable

- Port A output register (PAOUT: 0x03F1A)

bp	7	6	5	4	3	2	1	0
Flag	PAOUT7	PAOUT6	PAOUT5	PAOUT4	PAOUT3	PAOUT2	PAOUT1	PAOUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Flag
7-0	PAOUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

■ Port A Input Register (PAIN: 0x03F2A)

bp	7	6	5	4	3	2	1	0
Flag	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	PAIN7-0	Input data 0:Pin is L(V_{SS} level) 1:Pin is H(V_{DD5} level)

■ Port A Direction Control Register (PADIR: 0x03F3A)

bp	7	6	5	4	3	2	1	0
Flag	PADIR7	PADIR6	PADIR5	PADIR4	PADIR3	PADIR2	PADIR1	PADIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Flag
7-0	PADIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port A Pull-up Resistor Control Register (PAPLU: 0x03F4A)

bp	7	6	5	4	3	2	1	0
Flag	PAPLU7	PAPLU6	PAPLU5	PAPLU4	PAPLU3	PAPLU2	PAPLU1	PAPLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	PAPLU7-0	Pull-up resistor selection 0:Not added 1:Added

■ Port A Output Mode Register (P9OMD:0x03EE6)

bp	7	6	5	4	3	2	1	0
Flag	PAOMD7	PAOMD6	PAOMD5	PAOMD4	PAOMD3	PAOMD2	PAOMD1	PAOMD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	PAOMD7	I/O port, TM9IOA selection 0:Port PA7 1:TM9IOA
6	PAOMD6	I/O port, TM8IOA selection 0:Port PA6 1:TM8IOA
5	PAOMD5	I/O port, TM7IOA selection 0:Port PA5 1:TM7IOA
4	PAOMD4	I/O port, TM4IOA selection 0:Port PA4 1:TM4IOA
3	PAOMD3	I/O port, TM3IOA selection 0:Port PA3 1:TM3IOA
2	PAOMD2	I/O port, TM2IOA selection 0:Port PA2 1:TM2IOA
1	PAOMD1	I/O port, TM1IOA selection 0:Port PA1 1:TM1IOA
0	PAOMD0	I/O port, TM0IOA/RMOUTA selection 0:Port PA0 1:TM0IOA/RMOUTA

■ Port A Input Mode Register (PAIMD: 0x03EE8)

bp	7	6	5	4	3	2	1	0
Flag	PAIMD7	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Flag
7	PAIMD7	I/O port, AN7 Analog input selection 0:Port PA7 1:AN7 analog input
6	PAIMD6	I/O port, AN6 Analog input selection 0:Port PA6 1:AN6 analog input
5	PAIMD5	I/O port, AN5 Analog input selection 0:Port PA5 1:AN5 analog input
4	PAIMD4	I/O port, AN4 Analog input selection 0:Port PA4 1:AN4 analog input
3	PAIMD3	I/O port, AN3 Analog input selection 0:Port PA3 1:AN3 analog input
2	PAIMD2	I/O port, AN2 Analog input selection 0:Port PA2 1:AN2 analog input
1	PAIMD1	I/O port, AN1 Analog input selection 0:Port PA1 1:AN1 analog input
0	PAIMD0	I/O port, AN0 Analog input selection 0:Port PA0 1:AN0 analog input

■ Port A Output Control Register (PACNT:0x03EF6)

bp	7	6	5	4	3	2	1	0
Flag	-	-	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5-4	PACNT5-4	PA5 Real time control (IRQO event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
3-2	PACNT3-2	PA2 Real time control (IRQO event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
1-0	PACNT1-0	PA0 Real time control (IRQO event) 00:I/O port (Real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output

■ 0.54 V_{DD5} Input Control Register (SCHMIT2:0x03EFA)

The input level of P8 (P80 to P87) to PB (PB0 to PB7) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SCHMIT2B	SCHMIT2A	SCHMIT29	SCHMIT28
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3	SCHMIT2B	Port B0 to Prot B7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT2A	Port A0 to Prot A7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT29	Port 90 to Prot 96 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT28	Port 80 to Prot 87 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

4.13.3 Block Diagram

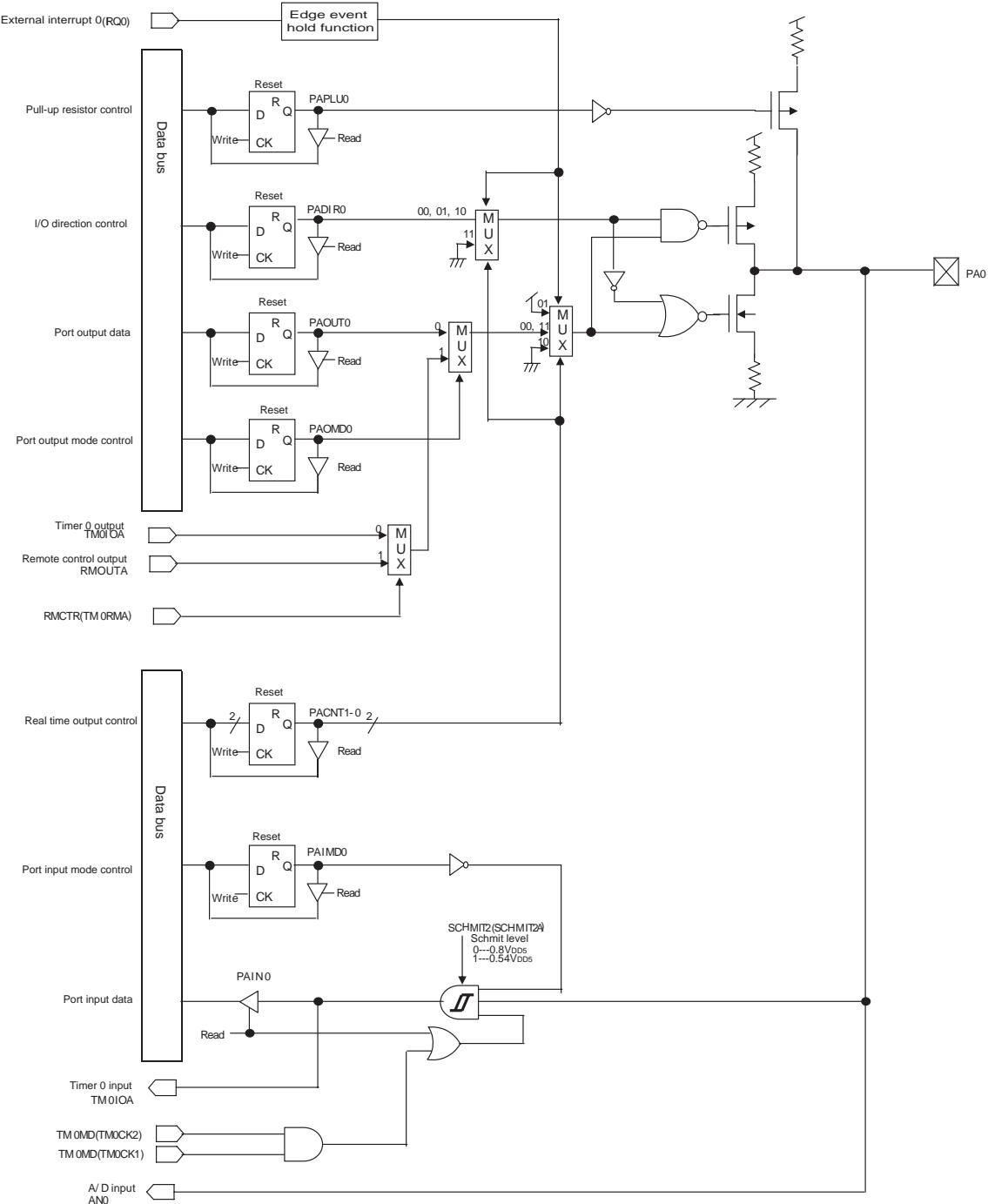


Figure:4.13.1 Block Diagram (PA0)

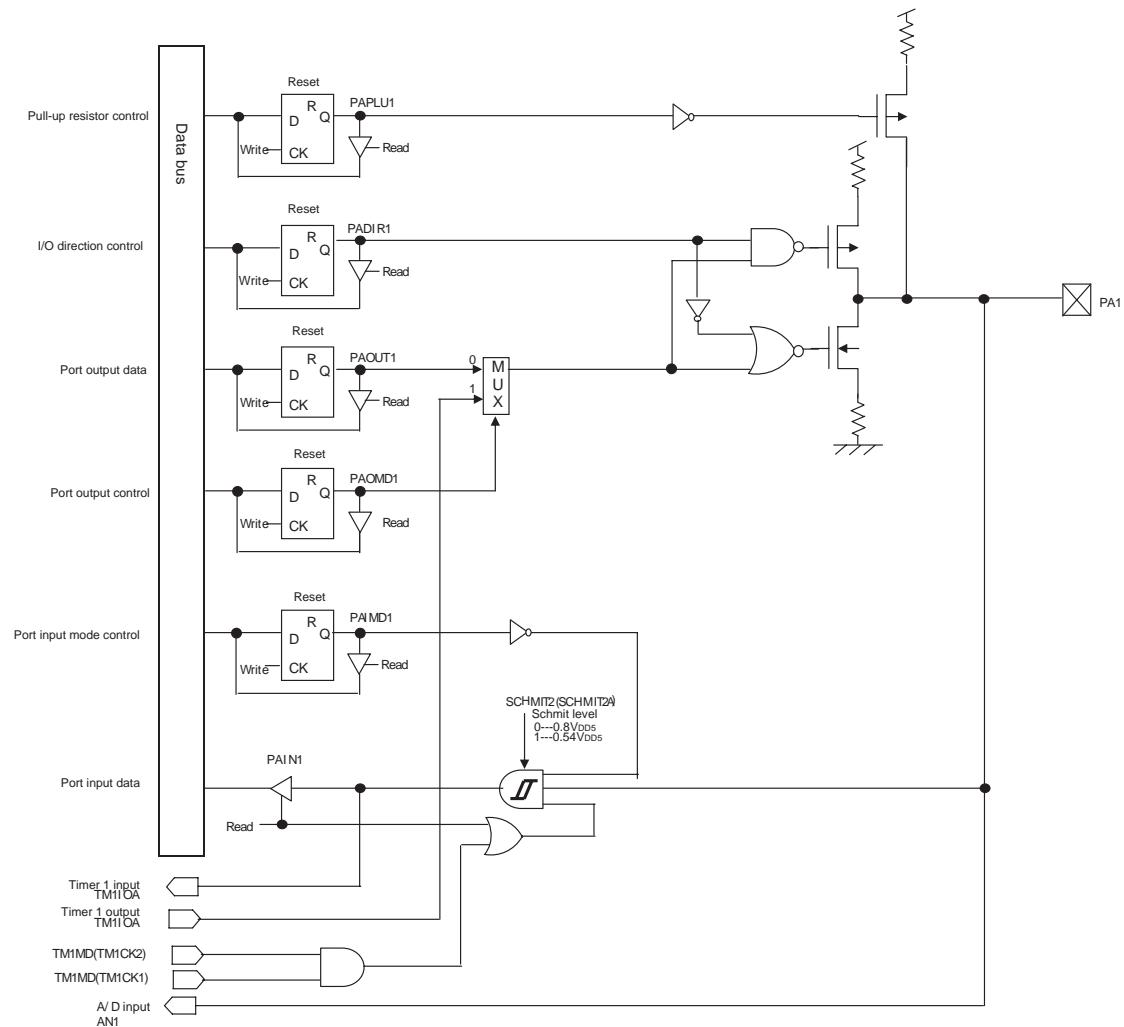


Figure:4.13.2 Block Diagram (PA1)

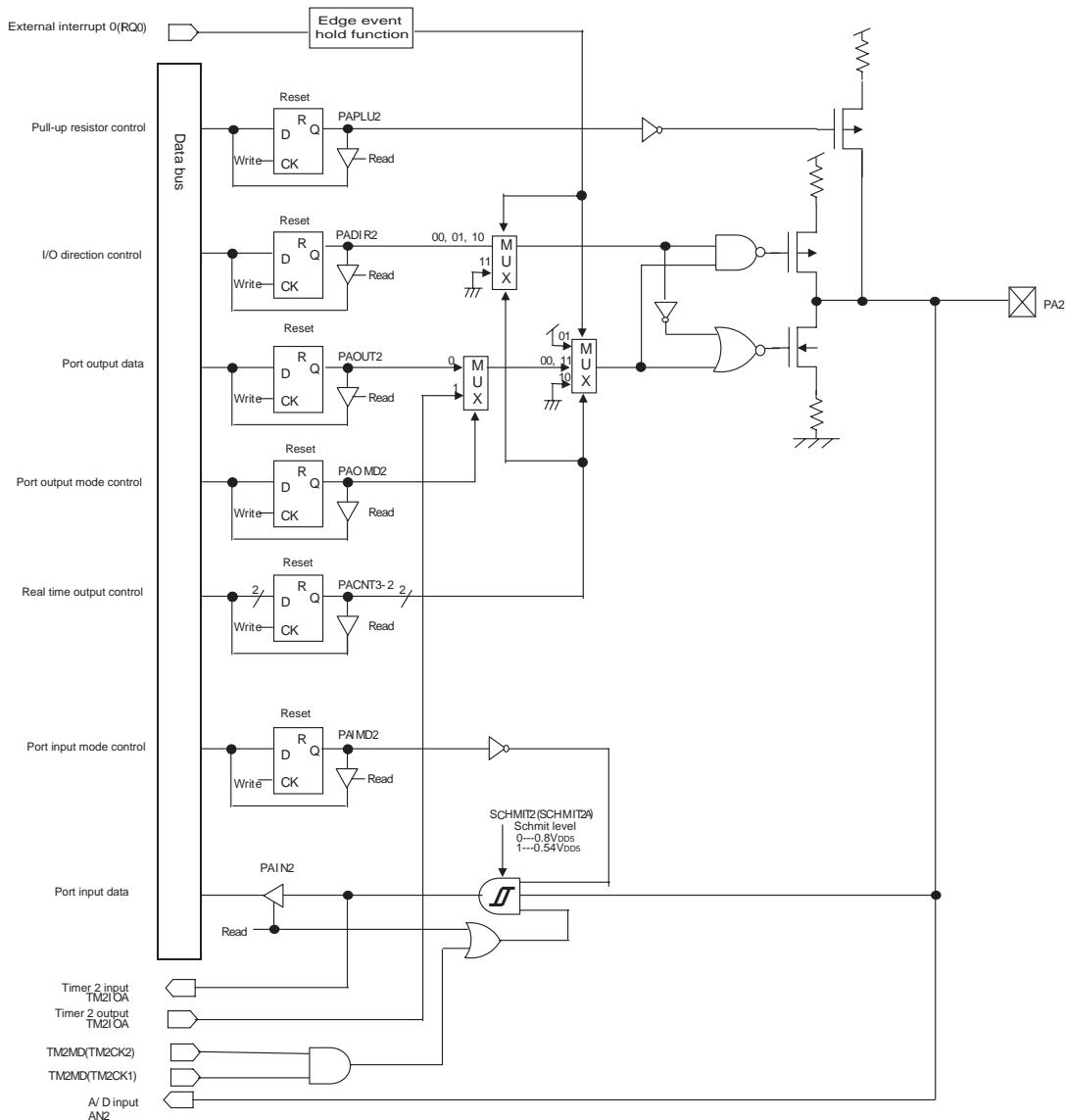


Figure:4.13.3 Block Diagram (PA2)

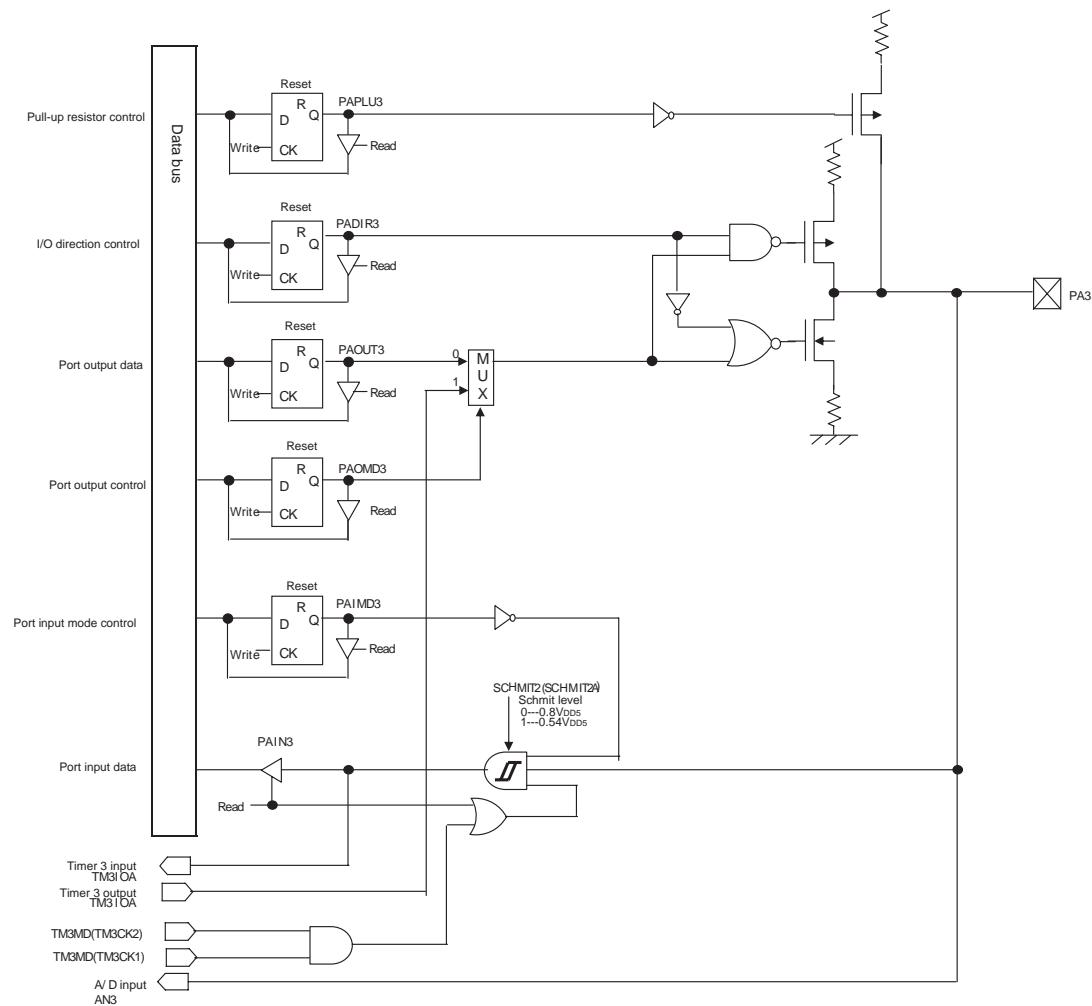


Figure:4.13.4 Block Diagram (PA3)

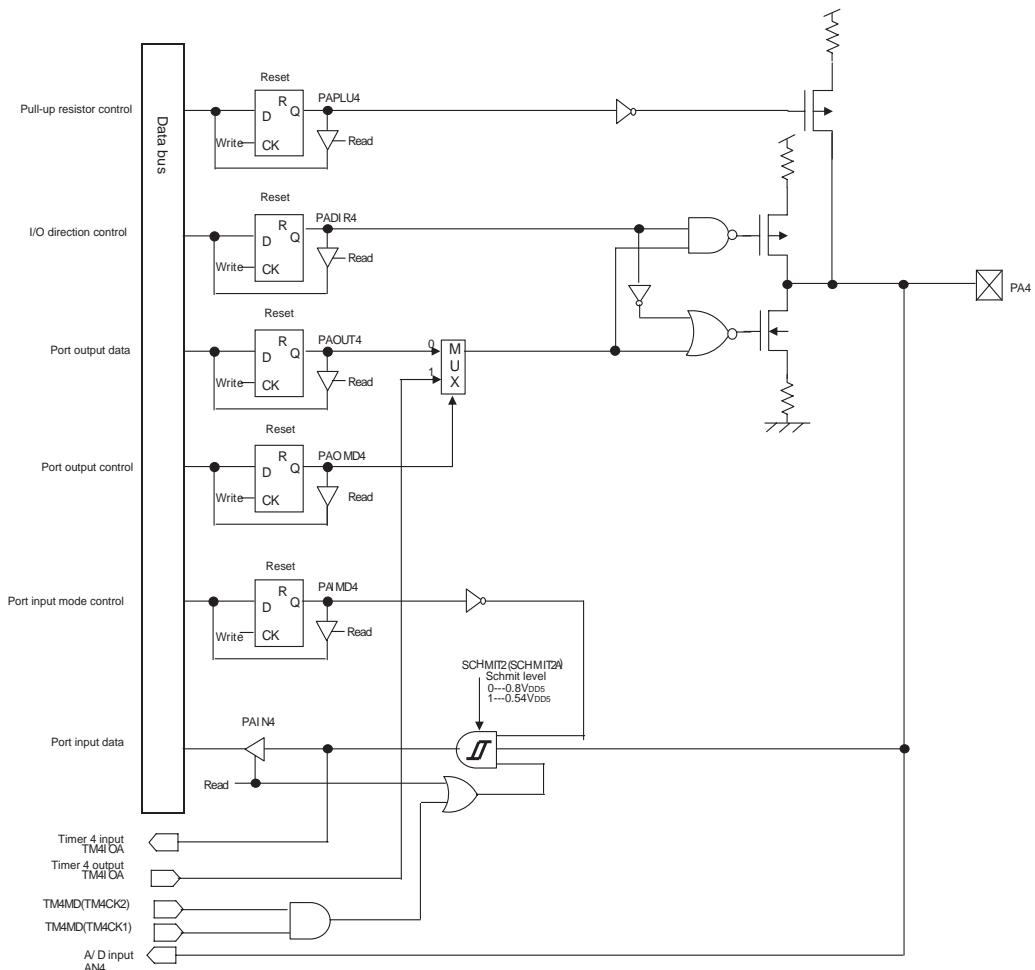


Figure:4.13.5 Block Diagram (PA4)

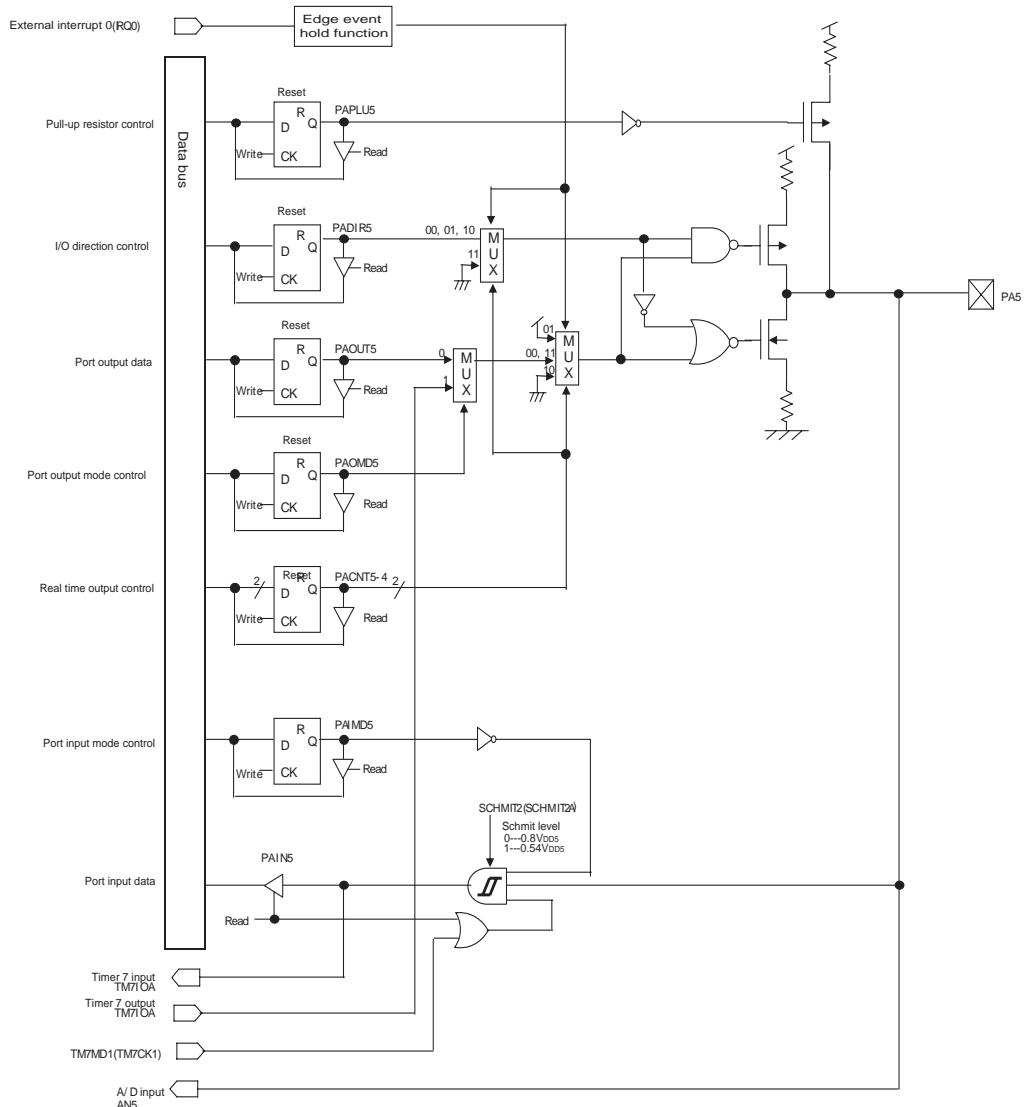


Figure:4.13.6 Block Diagram (PA5)

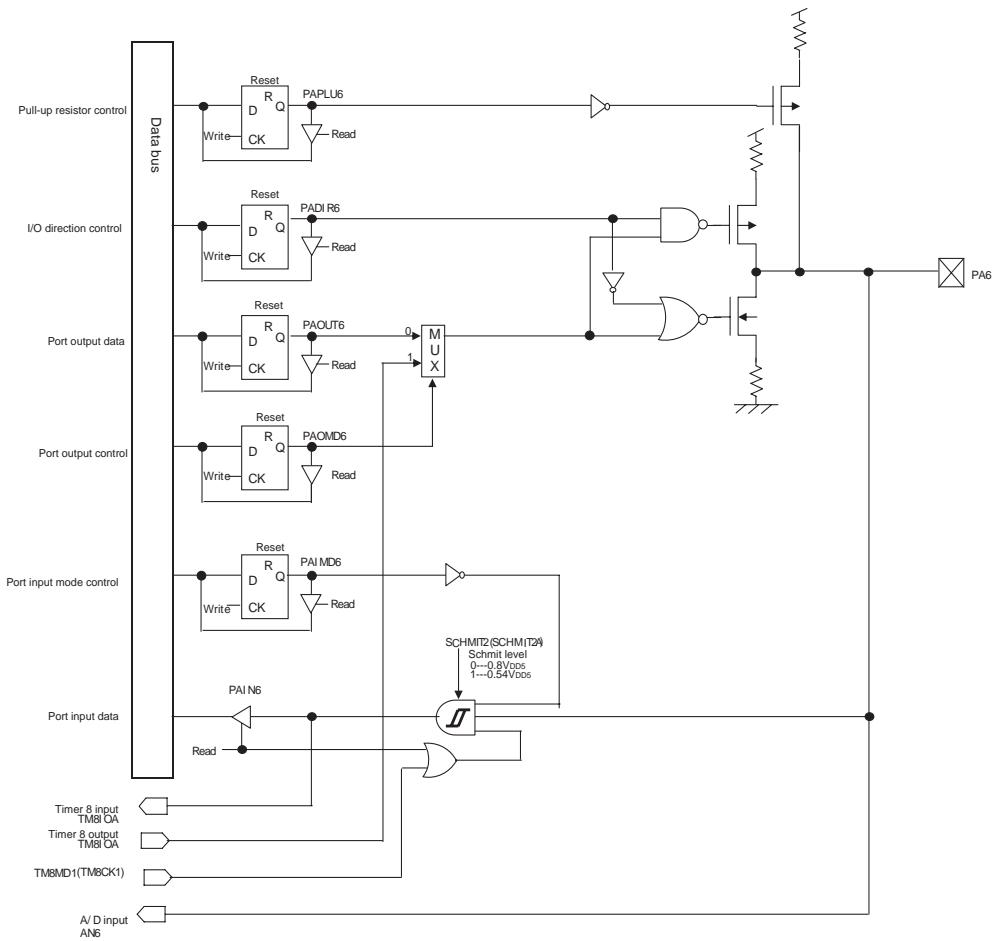


Figure:4.13.7 Block Diagram (PA6)

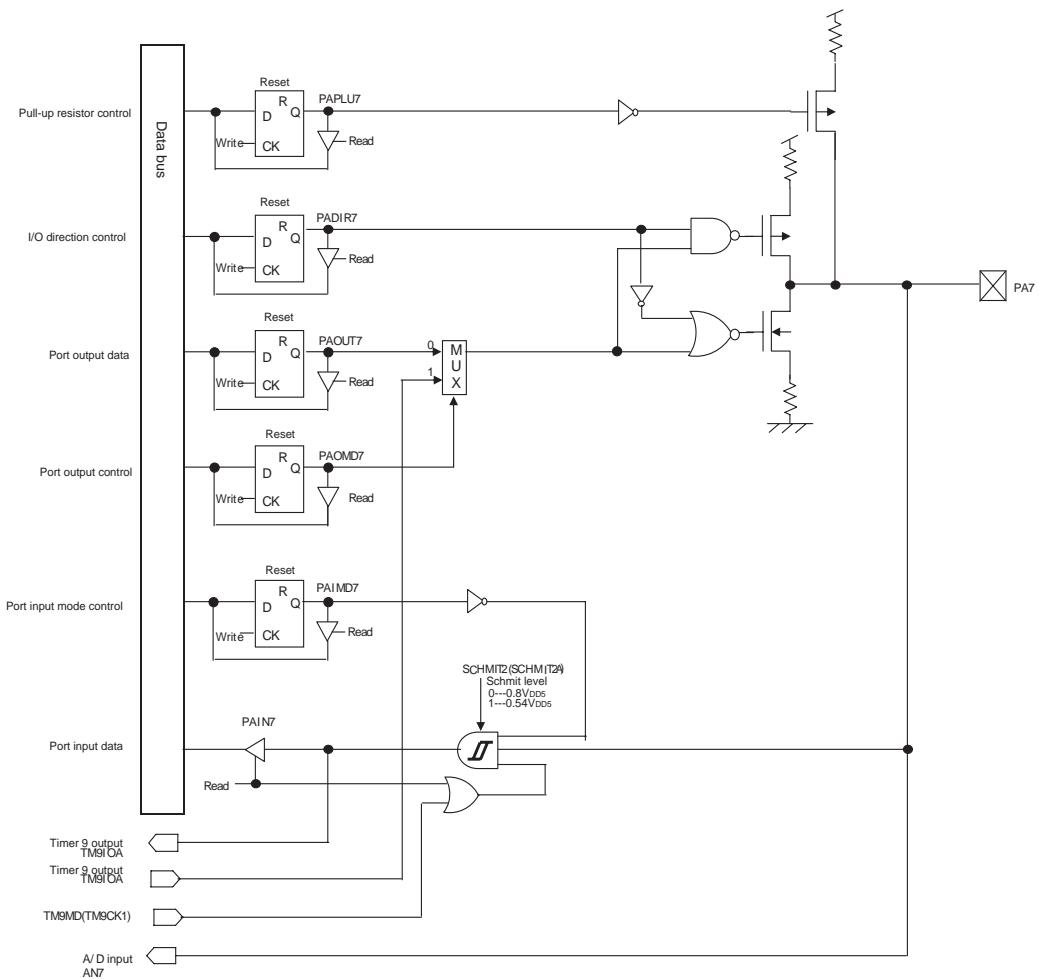


Figure:4.13.8 Block Diagram (PA7)

4.14 Port B

4.14.1 Description

■ General Pin Setup

To output data to pin, set the control flag of the port B direction control register (PBDIR) to "1" and write data to the port B output register (PBOUT).

To read input data of pin, set the control flag of the port B direction control register (PBDIR) to "0" and read the value of the port B input register (PBIN).

Each bit can be set individually to either an input or output by the port B direction control register (PBDIR). The control flag of the port B direction control register (PBDIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port B pull-up resistor control register (PBPLU). Set the control flag of the port B pull-up resistor control register (PBPLU) to "1" to add pull-up resistor.

Each bit can be selected individually as input mode by the port B input mode register (PBIMD). The control flag of the port B input mode register (PBIMD) is set to "1" to input the special function data and 1 is read out from the port B input register (PBIN), and "0" to use as the general port.

■ General Pin Setup

PB0 to PB7 are also used as analog input pin. Input mode for each bit can be selected by the port B input mode register (PBIMD). When these pins are used as analog input pin, the value of the port B input register is read to be "0".

4.14.2 Registers

Table:4.14.1 shows the registers that control the port B.

Table:4.14.1 Port B Output Control Register

Registers	Address	R/W	Function	Page
PBOUT	0x03F1B	R/W	Port B output register	IV-160
PBIN	0x03F2B	R	Port B input register	IV-160
PBDIR	0x03F3B	R/W	Port B direction control register	IV-161
PBPLU	0x03F4B	R/W	Port B pull-up resistor control register	IV-161
PBIMD	0x03EE9	R/W	Port B input register	IV-162
SCHMIT2	0x03EFA	R/W	0.54 V _{DD5} input selection register 1	IV-163

R/W:Readable/Writable

- Port B output register (PBOUT: 0x03F1B)

bp	7	6	5	4	3	2	1	0
Flag	PBOUT7	PBOUT6	PBOUT5	PBOUT4	PBOUT3	PBOUT2	PBOUT1	PBOUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W							

bp	Flag	Description
7-0	PBOUT7-0	Output data 0:Output L(V _{SS} level) 1:Output H(V _{DD5} level)

- Port B Input Register (PBIN: 0x03F2B)

bp	7	6	5	4	3	2	1	0
Flag	PBIN7	PBIN6	PBIN5	PBIN4	PBIN3	PBIN2	PBIN1	PBIN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7-0	PBIN7-0	Input data 0:Pin is L(V _{SS} level) 1:Pin is H(V _{DD5} level)

■ Port B Direction Control Register (PBDIR: 0x03F3B)

bp	7	6	5	4	3	2	1	0
Flag	PBDIR7	PBDIR6	PBDIR5	PBDIR4	PBDIR3	PBDIR2	PBDIR1	PBDIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	PBDIR7-0	I/O mode selection 0:Input mode 1:Output mode

■ Port B Pull-up Resistor Control Register (PBPLU: 0x03F4B)

bp	7	6	5	4	3	2	1	0
Flag	PBPLU7	PBPLU6	PBPLU5	PBPLU4	PBPLU3	PBPLU2	PBPLU1	PBPLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-0	PBPLU7-0	Pull-up resistor selection 0:Not added 1:Added

■ Port B Input Mode Register (PBIMD: 0x03EE9)

bp	7	6	5	4	3	2	1	0
Flag	PBIMD7	PBIMD6	PBIMD5	PBIMD4	PBIMD3	PBIMD2	PBIMD1	PBIMD0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	PBIMD7	I/O port, AN15 Analog input selection 0:Port PB7 1:AN15 Analog input
6	PBIMD6	I/O port, AN14 Analog input selection 0:Port PB6 1:AN14 Analog input
5	PBIMD5	I/O port, AN13 Analog input selection 0:Port PB5 1:AN13 Analog input
4	PBIMD4	I/O port, AN12 Analog input selection 0:Port PB4 1:AN12 Analog input
3	PBIMD3	I/O port, AN11 Analog input selection 0:Port PB3 1:AN11 Analog input
2	PBIMD2	I/O port, AN10 Analog input selection 0:Port PB2 1:AN10 Analog input
1	PBIMD1	I/O port, AN9 Analog input selection 0:Port PB1 1:AN9 Analog input
0	PBIMD0	I/O port, AN8 Analog input selection 0:Port PB0 1:AN8 Analog input

■ 0.54 V_{DD5} Input Control Register (SCHMIT2:0x03EFA)

The input level of P8 (P80 to P87) to PB (PB0 to PB7) recognized “H” can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SCHMIT2B	SCHMIT2A	SCHMIT29	SCHMIT28
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3	SCHMIT2B	Port B0 to Prot B7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
2	SCHMIT2A	Port A0 to Prot A7 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
1	SCHMIT29	Port 90 to Prot 96 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}
0	SCHMIT28	Port 80 to Prot 87 Schmit level switching 0:0.8 V _{DD5} 1:0.54 V _{DD5}

4.14.3 Block Diagram

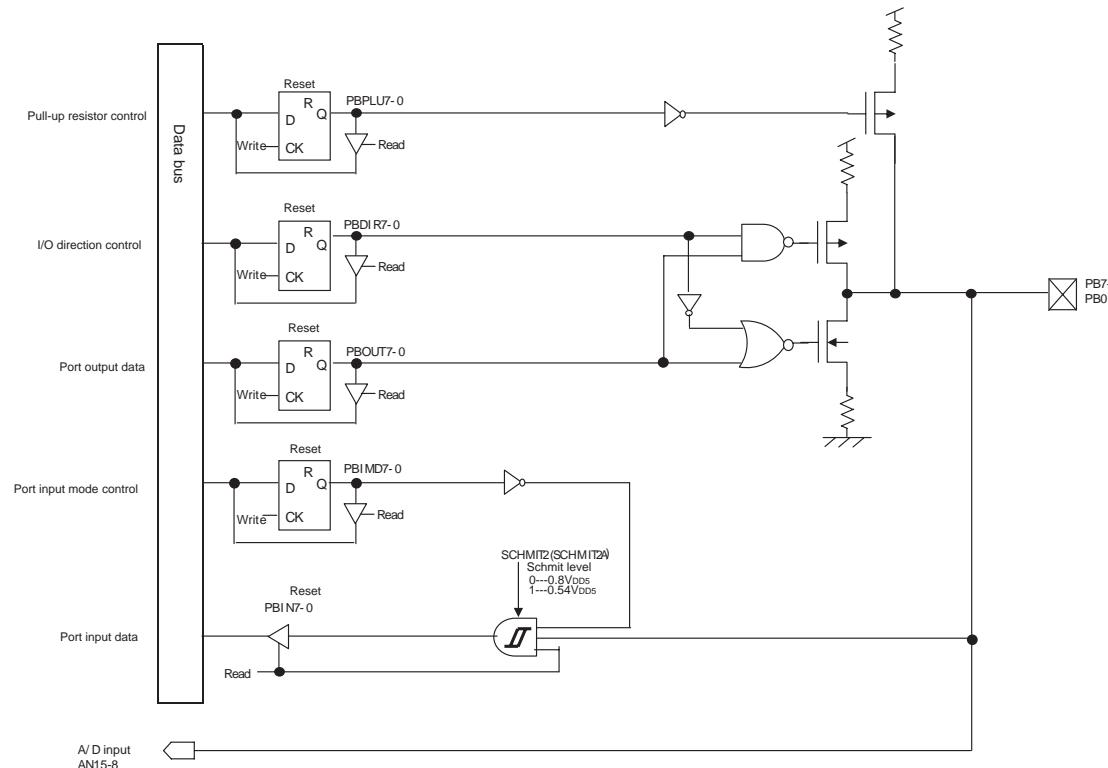


Figure:4.14.1 Block Diagram (PA7 to PA0)

4.15 Real Time Output Control

P80 to P85, PA0, PA2, PA5 have the real time output function that can switch pin output at the falling edge event of the external interrupt 0 pin (P20/IRQ0).

The real time control can change the timer output signal (PWM output, timer pulse output, remote control career output) by synchronizing the external event without interposition. Switchable output values at the event generation are "0", "1", and "High-impedance (Hi-z)".

4.15.1 Registers

Table:4.15.1 shows the real time output control registers of port 1.

Table:4.15.1 Real Time Output Control Registers

	Register	Address	R/W	Function	Page
Port1	P8OUT	0x03F18	R/W	Port 8 output register	IV-122
	P8DIR	0x03F38	R/W	Port 8 direction control register	IV-123
	P8PLU	0x03F48	R/W	Port 8 pull-up resistor control register	IV-123
	P8OMD1	0x03EE5	R/W	Port 8 output mode register 1	IV-124
	P8CNT1	0x03EFB	R/W	Port 8 output control register 1	IV-125
	P8CNT2	0x03EFC	R/W	Port 8 output control register 2	IV-126
PortA	PAOUT	0x03F1A	R/W	Port A output register	IV-145
	PADIR	0x03F3A	R/W	Port A direction control register	IV-146
	PAPLU	0x03F4A	R/W	Port A pull-up resistor control register	IV-146
	PAOMD	0x03EE6	R/W	Port A output mode register	IV-147
	PACNT	0x03EF6	R/W	Port A output control register	IV-149

4.15.2 Operation

■ Real Time Output Pin Setup

The real time output pin is set at the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT). Selectable pins are P80 to P85, PA0, PA2, PA5, and the pin can be specified by each bit. Output mode should be selected with the port 8 direction control register (P8DIR), the port A direction control register (PADIR). The pin output that is switched at the falling edge event of the external interrupt 0 pin (P20/IRQ0) is "0", "1", and "High-impedance". Port is input mode at the hi-impedance.

The real time control changes the timer output signal (PWM output, timer pulse output remote control career output) by synchronizing with the external event. It is also available to normal port output.

When I/O port (real time control disabled) is selected at the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT), the value is not be changed even if switching event is generated. Set to this mode to use this pin as a general port.

■ Real Time Output Control Operation

After setting the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT), the functions selected at the port 8 output mode register (PA8MD), the port A output mode register (PAOMD) are output to the pin until the falling edge is generated at the external interrupt 0 pin (P20/IRQ0).

When the falling edge of the external interrupt 0 is generated, pin output is switched to the set value. The falling edge event is taken in the edge event hold function that is shown below and the setup value of the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT) is held until the information is cleared.

■ Real Time Output Release (Clearance of edge event hold function)

After the event generation, when the write operation to the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT) is done, the information of the edge event hold function is cleared and all output pins are reset to the output data before the event generation.

When the event is generated again, the data is switched to the setup value of the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT) again. To cancel the real time control, set the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT) to I/O port (real time control disabled).



Regardless of the setup at the external interrupt 0 control register (IRQ0ICR), valid edge of IRQ0 is only the falling edge.



When the real time output control function is used, writing operation should be done to the port 8 output control register 1 (P8CNT1), the port 8 output control register 2 (P8CNT2), the port A output control register (PACNT) in advance and clear the information of the edge event hold function.



When real time output release (the write operation to P8CNT1, P8CNT2 and PACNT) and the event generation is executed at the same time, the event generation is given to priority and setting value of P8CNT1, P8CNT2 and PACNT is given to priority.

■ Timing of Real Time Output Control (Port A)

PACNT set value:"0" (Low) output

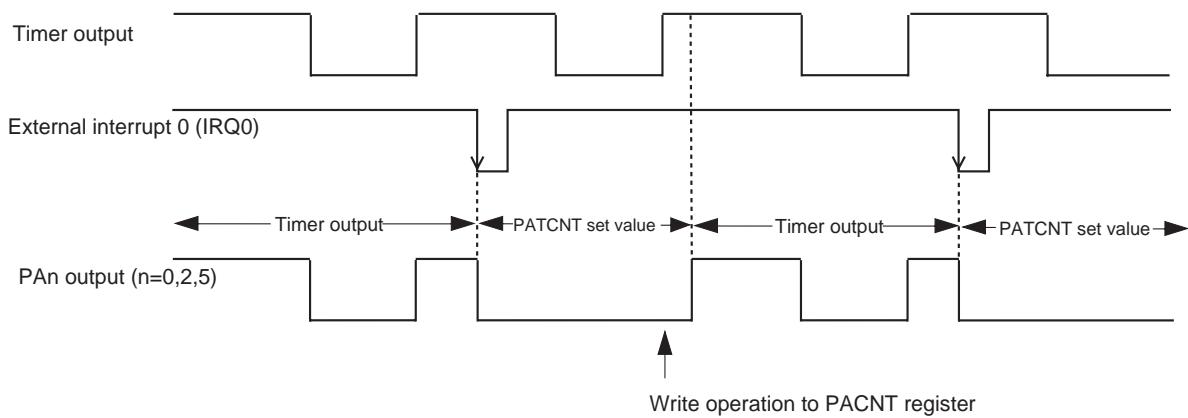


Figure:4.15.1 Timing of Real Time Output Control

4.16 Synchronous Output

Port 8 has the synchronous output function that outputs any set data to pins without software at the timing of the specified event generation. Synchronous event is selected from the external interrupt 0 (P22/IRQ2), timer 1 interrupt, timer 2 interrupt, and timer 7 interrupt signal.

4.16.1 Registers

Table:4.16.1 shows the port 8 synchronous output control registers.

Table:4.16.1 Synchronous Output Control Register

	Register	Address	R/W	Function	Page
Port 8	P8OUT	0x03F18	R/W	Port 8 output register	IV-122
	P8DIR	0x03F38	R/W	Port 8 direction control register	IV-123
	P8PLU	0x03F48	R/W	Port 8 pull-up resistor control register	IV-123
	P8SYO	0x03EF7	R/W	Port 8 synchronous output control register	IV-126
	P8SEV	0x03EF8	R/W	Port 8 synchronous output event selection register	IV-127

4.16.2 Operation

■ Synchronous Output Setup

Port 8 synchronous output pin for each bit is set with the synchronous output control register (P8SYO). The synchronous output event is selected by the synchronous output event selection register (P8SEV).

When the external interrupt 2 (IRQ2) is selected, data is synchronized with the falling regardless of IRQ2ICR edge specification.

■ Synchronous output Operation

When the synchronous output control register (P8SYO) is set to disable the synchronous output (I/O port), the port 8 is functioned as a general port. When the port 8 is set to disable the synchronous output, the synchronous output value store register always loads the same value as the port 8 output register (P8OUT).

After the output mode is selected with the port 8 direction control register (P8DIR), when the synchronous output is enabled with the synchronous output control register (P8SYO), the value of the synchronous output value store register is output. The synchronous output value store register holds the value at which the synchronous output is enabled until the synchronous output event which is set with the synchronous output event selection register (P8SEV).

Port 8 output register (P8OUT) stores the value which should be output from pin after the synchronous output event is generated. When the synchronous output event that is set with the synchronous output event selection register (P8SEV) is generated, the data of the synchronous output store register is switched to the data of the port 8 output register (P8OUT), and the output value from pin changes.



Set the initial value of the synchronous output to the port 8 output register (P8OUT) before the synchronous output is enabled with the synchronous output control register (P8SY0).

■ Port 8 Synchronous Output (External interrupt 2 IRQ2)

Figure:4.16.1 shows the synchronous output timing when the synchronous output event is set to the external interrupt 0. The value of the port 8 output register is output by synchronizing with the IRQ2 falling edge.

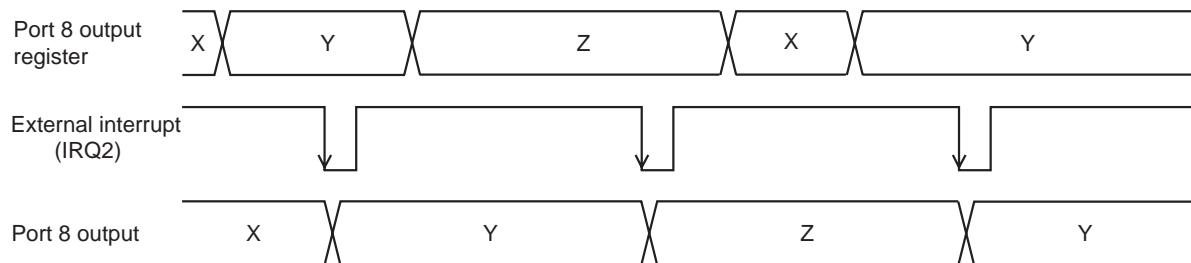


Figure:4.16.1 Synchronous Output Timing by Event Generation (IRQ2)

■ Port 8 Synchronous Output (Timer 1, 2 and 7)

The timer interrupt flag TMnIRQ is generated when the value of the binary counter matches with the compare register. The port 8 output latched data is output from the port 8 at the timing of the TMnIRQ flag rising.

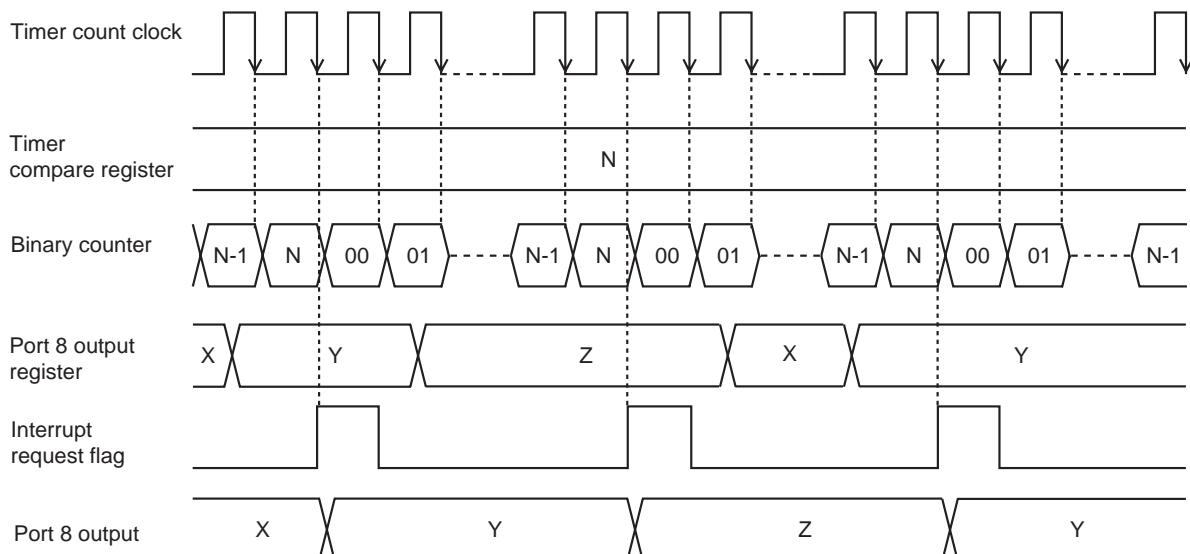


Figure:4.16.2 Synchronous Output Timing by Event Generation (Timer 1, 2, and 7)

5

Chapter 5 8-bit Timers

5.1 Overview

This LSI contains and five 8-bit timers (Timers 0, 1, 2, 3 and 4) combined baud rate timers. Timers 0 and 1 or Timers 2 and 3 can be used as 16-bit timer with cascade connection. In a cascade connection, Timers 0, 2 and 4 form the "timer 0", or the lower 8 bits of 16-bit counter, and Timers 1 and 3 form the "timer 1", or the upper 8 bits. In addition, cascading timers 0 through 2 forms a 24-bit counter; cascading timers 0 through 3, a 32-bit counter.

8-bit timer contains two prescalers which can use at the same time. Each prescaler counts fpll, fs as the base clock. Configurations of hardware are shown below.

Prescaler 0 (fpll base) 7 bits Prescaler

Prescaler 1 (fs base) 3 bits Prescaler

Prescaler 0 outputs fpll/4, fpll/16, fpll/32, fpll/64, fpll/128.

Prescaler 1 outputs fs/2, fs/4, fs/8.

fpll or fs can be selected as the clock source for each timer by using the prescaler output.

Pins can be switched to TMnIOA/TMnIOB/TMnIOC.

TM0IOA (PA0)
TM0IOB (P03)
TM0IOC (P10)
TM1IOA (PA1)
TM1IOB (P62)
TM1IOC (P12)
TM2IOA (PA2)
TM2IOB (P03)
TM2IOC (P11)
TM3IOA (PA3)
TM3IOB (P63)
TM3IOC (P13)
TM4IOA (PA4)
TM4IOB (P64)
TM4IOC (P14)



On the text, if there is not much functional difference in pins A, B and C, "A", "B" and "C" of the pin names are omitted.

5.1.1 Functions

Table:5.1.1 shows functions that can be used with each timer.

Table:5.1.1 Timer Functions

	Timer 0 (8-bit)	Timer 1 (8-bit)	Timer 2 (8-bit)	Timer 3 (8-bit)	Timer 4 (8-bit)
Interrupt source	TM0IRQ	TM1IRQ	TM2IRQ	TM3IRQ	TM4IRQ
Timer operation	O	O	O	O	O
Event count	TM0IOA input/ TM0IOB input/ TM0IOC input	TM1IOA input/ TM1IOB input/ TM1IOC input	TM2IOA input/ TM2IOB input/ TM2IOC input	TM3IOA input/ TM3IOB input/ TM3IOC input	TM4IOA input/ TM4IOB input/ TM4IOC input
Timer pulse output	TM0IOA output/ TM0IOB output/ TM0IOC output	TM1IOA output/ TM1IOB output/ TM1IOC output	TM2IOA output/ TM2IOB output/ TM2IOC output	TM3IOA output/ TM3IOB output/ TM3IOC output	TM4IOA output/ TM4IOB output/ TM4IOC output
PWM output	TM0IOA output/ TM0IOB output/ TM0IOC output	-	TM2IOA output/ TM2IOB output/ TM2IOC output	-	TM4IOA output/ TM4IOB output/ TM4IOC output
PWM Output with Additional Pulses	O	-	O	-	O
Synchronous output	-	Port 8	Port 8	-	-
Serial transfer clock output	Serial 0, 1, 2, 3, 4				
Pulse width measurement	External interrupt 0 (P20/IRQ0)	-	External interrupt 2 (P22/IRQ2)	-	External interrupt 4 (P24/IRQ4)
Cascade Connection	O	O	O	-	-
	O		-	-	-
	O			-	-
Clock source	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM0IO input Synchronous fx Synchronous TM0IO input Simple timer A input	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM1IO input Synchronous fx Synchronous TM1IO input Simple timer A input	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM2IO input Synchronous fx Synchronous TM2IO input Simple timer A input	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM3IO input Synchronous fx Synchronous TM3IO input Simple timer A input	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM4IO input Synchronous fx Synchronous TM4IO input Simple timer A input
fpll:Machine clock (High frequency oscillation) fx:Machine clock (Low frequency oscillation) fs:System clock [Chapter 2 2.6 Clock Switching]					

5.1.2 Block Diagram

■ Prescaler Block Diagram

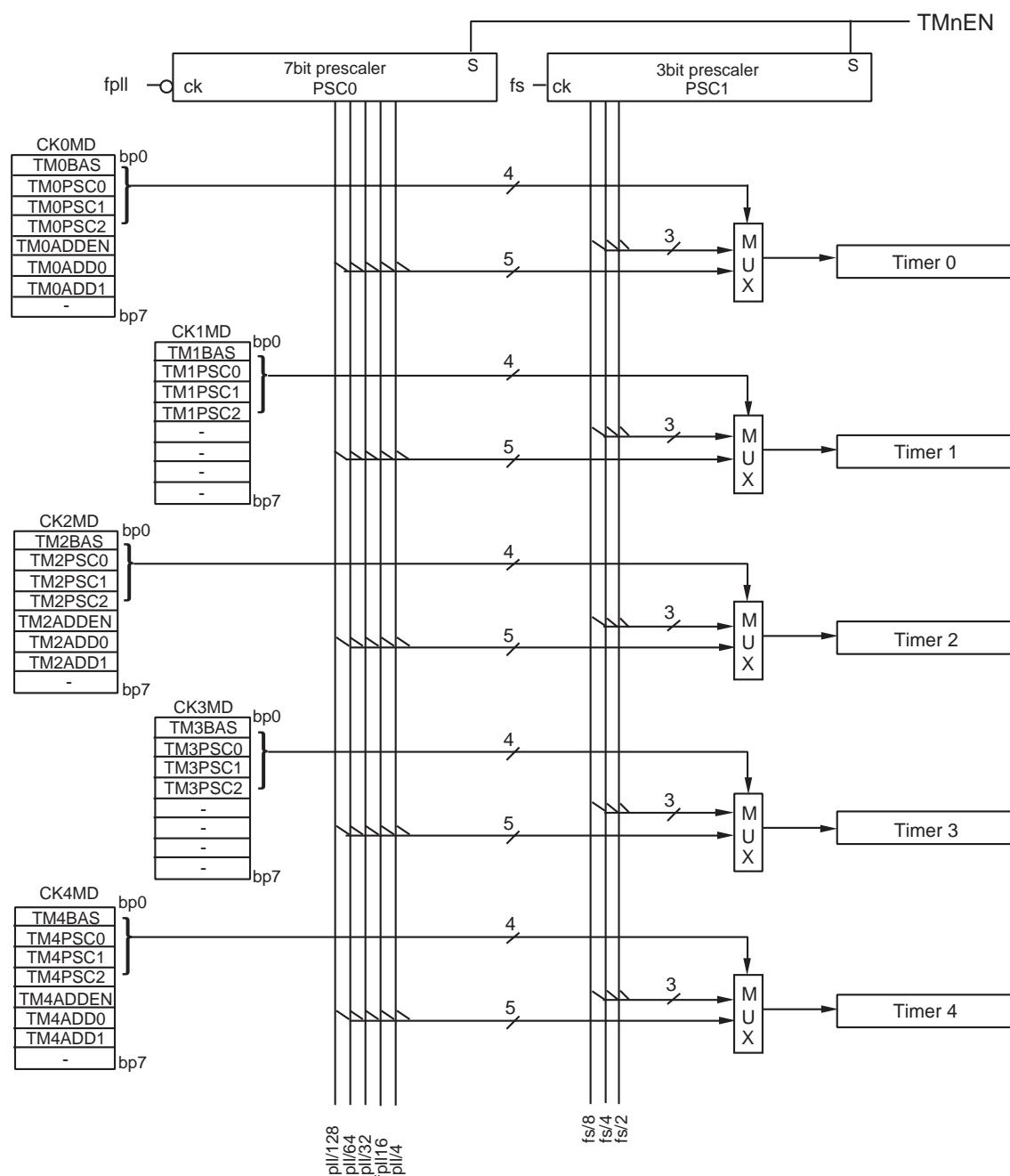


Figure:5.1.1 Prescaler Block Diagram

■ Timers 0 and 1 Block Diagram

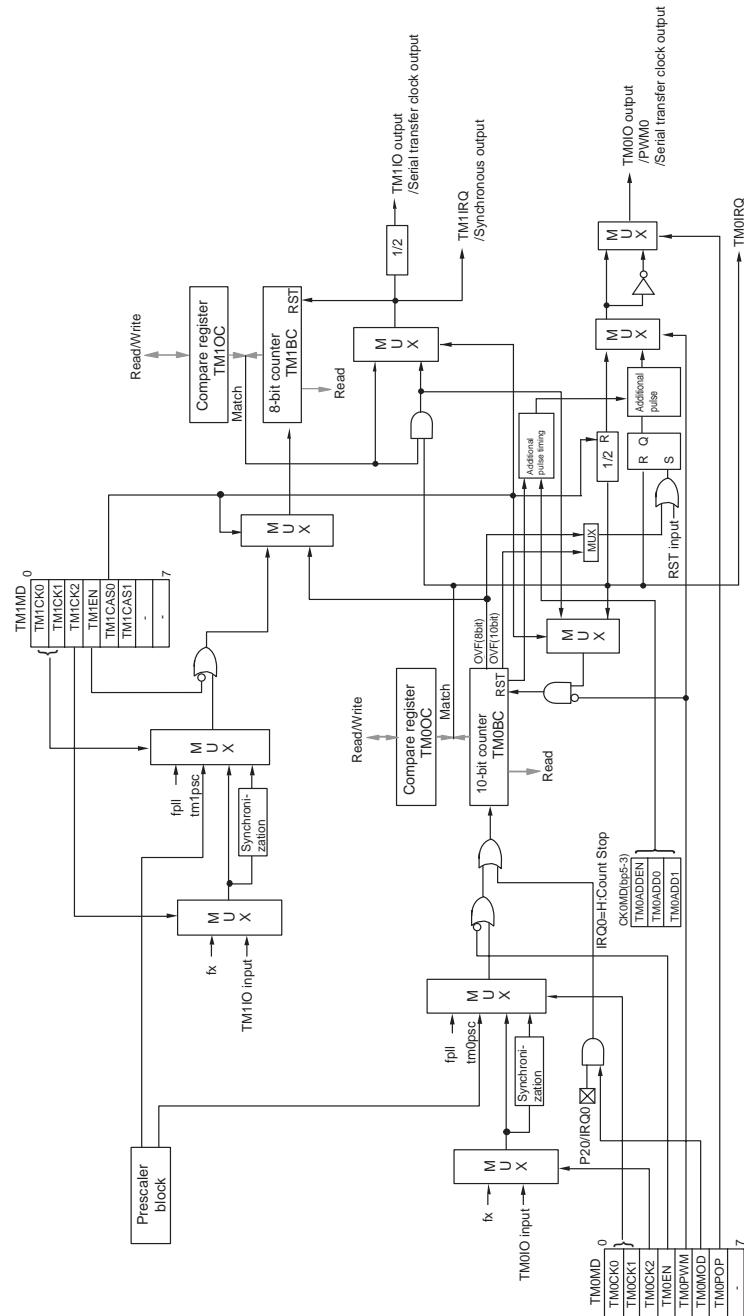


Figure:5.1.2 Timers 0 and 1 Block Diagram

■ Timers 2 and 3 Block Diagram

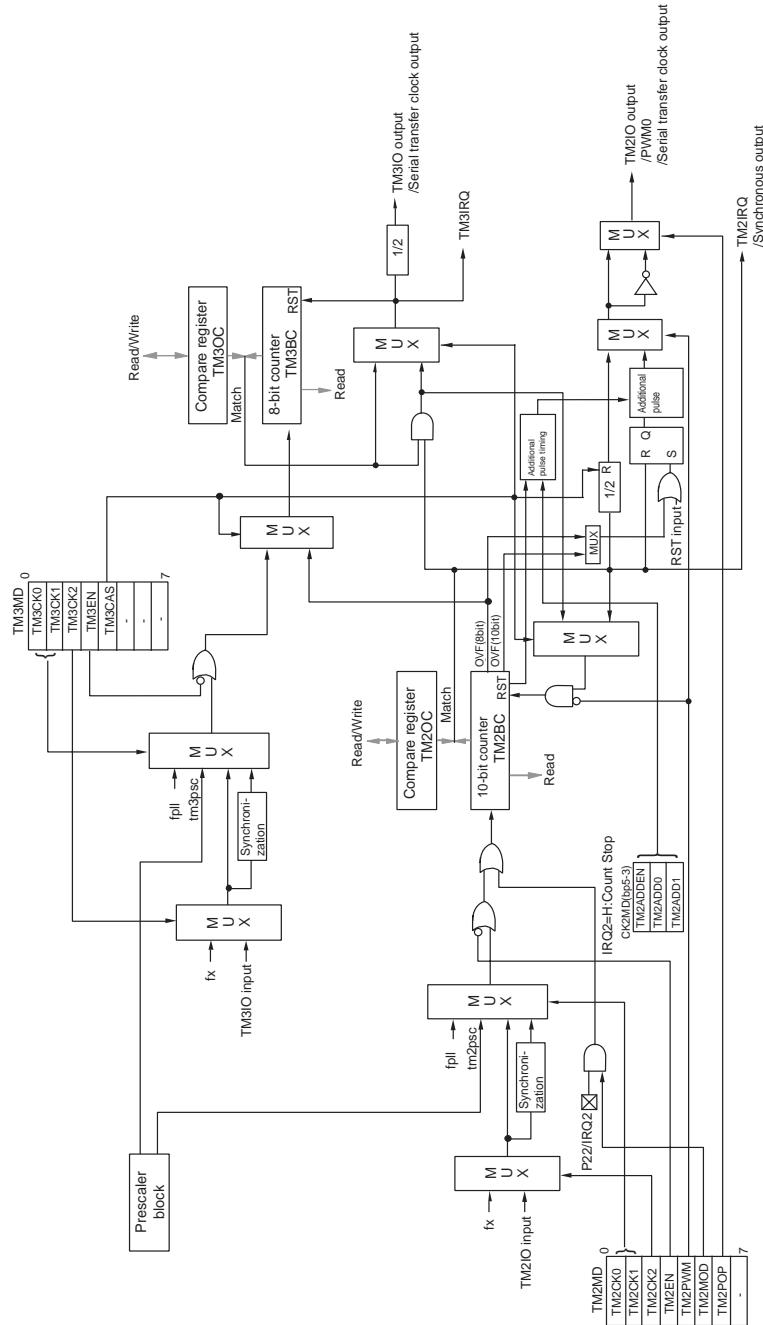


Figure:5.1.3 Timers 2 and 3 Block Diagram

■ Timer 4 Block Diagram

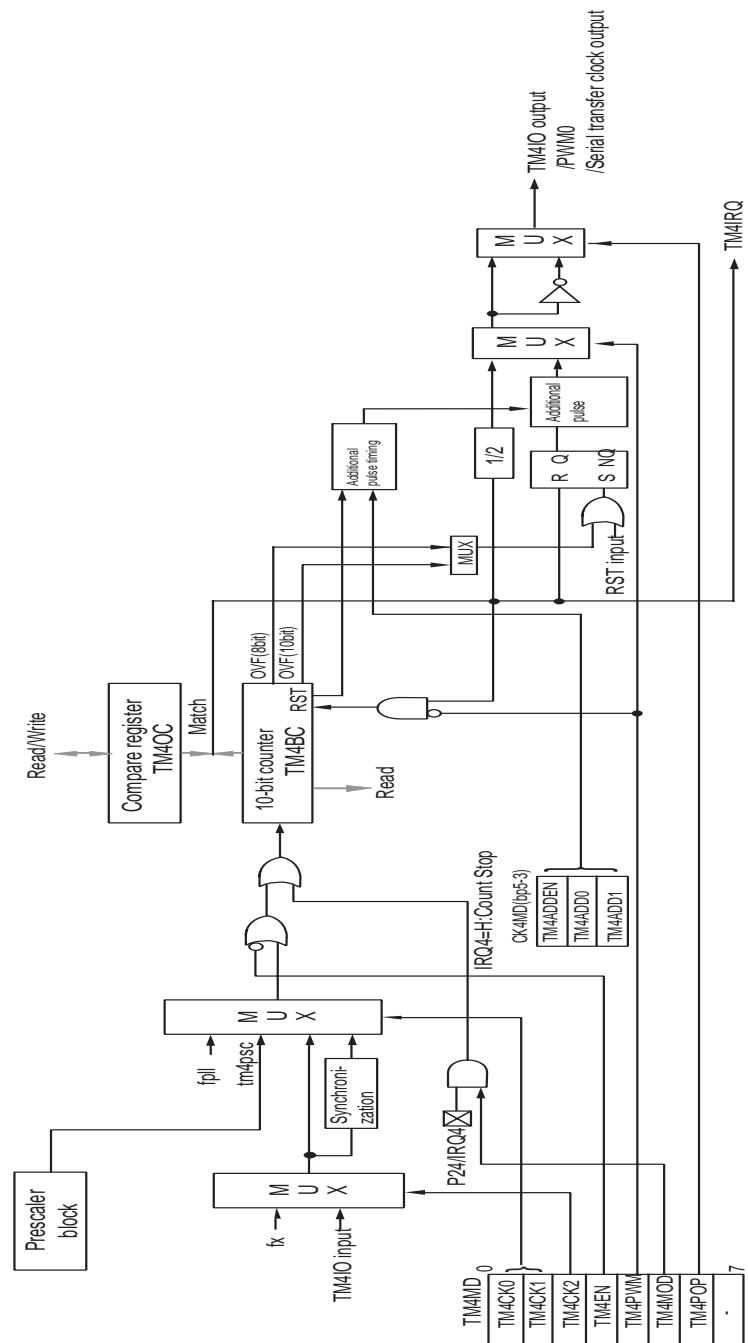


Figure:5.1.4 Timer 4 Block Diagram

5.2 Control Registers

Timers 0 to 4 consist of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD).

When the prescaler output is selected as the count clock source of timers 0 to 4, they should be controlled by the prescaler selection register (CKnMD).

5.2.1 Registers

Table:5.2.1 shows registers that control timers 0 to 4.

Table:5.2.1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 0	TM0BC	0x03F50	R	Timer 0 binary counter	V-15
	TM0OC	0x03F52	R/W	Timer 0 compare register	V-13
	TM0MD	0x03F54	R/W	Timer 0 mode register	V-16
	CK0MD	0x03F56	R/W	Timer 0 prescaler selection register	V-10
	TM0ICR	0x03FE8	R/W	Timer 0 interrupt control register	III-26
Timer 1	TM1BC	0x03F51	R	Timer 1 binary counter	V-15
	TM1OC	0x03F53	R/W	Timer 1 compare register	V-13
	TM1MD	0x03F55	R/W	Timer 1 mode register	V-17
	CK1MD	0x03F57	R/W	Timer 1 prescaler selection register	V-11
	TM1ICR	0x03FE9	R/W	Timer 1 interrupt control register	III-26
Timer 2	TM2BC	0x03F58	R	Timer 2 binary counter	V-15
	TM2OC	0x03F5A	R/W	Timer 2 compare register	V-13
	TM2MD	0x03F5C	R/W	Timer 2 mode register	V-18
	CK2MD	0x03F5E	R/W	Timer 2 prescaler selection register	V-11
	TM2ICR	0x03FEA	R/W	Timer 2 interrupt control register	III-26
Timer 3	TM3BC	0x03F59	R	Timer 3 binary counter	V-15
	TM3OC	0x03F5B	R/W	Timer 3 compare register	V-13
	TM3MD	0x03F5D	R/W	Timer 3 mode register	V-19
	CK3MD	0x03F5F	R/W	Timer 3 prescaler selection register	V-12
	TM3ICR	0x03FEB	R/W	Timer 3 interrupt control register	III-26
Timer 4	TM4BC	0x03F60	R	Timer 4 binary counter	V-15
	TM4OC	0x03F62	R/W	Timer 4 compare register	V-14
	TM4MD	0x03F64	R/W	Timer 4 mode register	V-20
	CK4MD	0x03F66	R/W	Timer 4 prescaler selection register	V-12
	TM4ICR	0x03FEC	R/W	Timer 4 interrupt control register	III-26
	TMCKSEL1	0x03E42	R/W	Timer clock selection register 1	V-21
	TMCKSEL2	0x03E43	R/W	Timer clock selection register 2	VII-31
	TMINSEL1	0x03E44	R/W	Timer input selection register 1	V-22
	TMINSEL2	0x03E45	R/W	Timer input selection register 2	V-23

R/W: Readable / Writable

R: Readable only

5.2.2 Timer Prescaler Registers

Timer prescaler selection register selects the count clock for 8-bit timer.

The register which selects prescaler output is consisted by the timer prescaler selection register (CKnMD).

- Timer 0 Prescaler Selection Register (CK0MD:0x03F56)

bp	7	6	5	4	3	2	1	0
Flag	-	TM0ADD1	TM0ADD0	TM0ADDEN	TM0PSC2	TM0PSC1	TM0PSC0	TM0BAS
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6-5	TM0ADD1-0	Positions of Additional pulses (within 4 cycles of PWM basic waveform) 00:No pulse 01:At second cycle 10:At first and third cycles 11:At first, second, and third cycles
4	TM0ADDEN	Additional pulses PWM output control 0:Prohibited (8-bit PWM output) 1:Permitted
3-0	TM0PSC2-0, TM0BAS	Select the clock source 0000:fpll/4 0010:fpll/16 0100:fpll/32 0110:fpll/64 1XX0:fpll/128 0X01:fs/2 0X11:fs/4 1XX1:fs/8

■ Timer 1 Prescaler Selection Register (CK1MD:0x03F57)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	TM1PSC2	TM1PSC1	TM1PSC0	TM1BAS
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3-0	TM1PSC2-0, TM1BAS	Select the clock source 0000:fpll/4 0010:fpll/16 0100:fpll/32 0110:fpll/64 1XX0:fpll/128 0X01:fs/2 0X11:fs/8 1XX1:fs/4

■ Timer 2 Prescaler Selection Register (CK2MD:0x03F5E)

bp	7	6	5	4	3	2	1	0
Flag	-	TM2ADD1	TM2ADD0	TM2ADDEN	TM2PSC2	TM2PSC1	TM2PSC0	TM2BAS
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6-5	TM2ADD1-0	Positions of Additional pulses (within 4 cycles of PWM basic waveform) 00:No pulse 01:At second cycle 10:At first and third cycles 11:At first, second, and third cycles
4	TM2ADDEN	Additional pulses PWM output control 0:Prohibited (8-bit PWM output) 1:Permitted
3-0	TM2PSC2-0, TM2BAS	Select the clock source 0000:fpll/4 0010:fpll/16 0100:fpll/32 0110:fpll/64 1XX0:fpll/128 0X01:fs/2 0X11:fs/4 1XX1:fs/8

■ Timer 3 Prescaler Selection Register (CK3MD:0x03F5F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	TM3PSC2	TM3PSC1	TM3PSC0	TM3BAS
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-4	-	-
3-0	TM3PSC2-0, TM3BAS	Select the clock source 0000:fpll/4 0010:fpll/16 0100:fpll/32 0110:fpll/64 1XX0:fpll/128 0X01:fs/2 0X11:fs/8 1XX1:fs/4

■ Timer 4 prescaler selection register (CK4MD:0x03F66)

bp	7	6	5	4	3	2	1	0
Flag	-	TM4ADD1	TM4ADD0	TM4ADDEN	TM4PSC2	TM4PSC1	TM4PSC0	TM4BAS
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6-5	TM4ADD1-0	Positions of Additional pulses (within 4 cycles of PWM basic waveform) 00:No pulse 01:At second cycle 10:At first and third cycles 11:At first, second, and third cycles
4	TM4ADDEN	Additional pulses PWM output control 0:Prohibited (8-bit PWM output) 1:Permitted
3-0	TM4PSC2-0, TM4BAS	Select the clock source 0000:fpll/4 0010:fpll/16 0100:fpll/32 0110:fpll/64 1XX0:fpll/128 0X01:fs/2 0X11:fs/4 1XX1:fs/8

5.2.3 Programmable Timer Registers

Each of timers 0 to 4 has 8-bit programmable timer registers.

Programmable timer register consists of compare register and binary counter.

Compare register is 8-bit register which stores the value to be compared to binary counter are stocked.

- Timer 0 Compare Register (TM0OC:0x03F52)

bp	7	6	5	4	3	2	1	0
Flag	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

- Timer 1 Compare Register (TM1OC:0x03F53)

bp	7	6	5	4	3	2	1	0
Flag	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

- Timer 2 Compare Register (TM2OC:0x03F5A)

bp	7	6	5	4	3	2	1	0
Flag	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

- Timer 3 Compare Register (TM3OC:0x03F5B)

bp	7	6	5	4	3	2	1	0
Flag	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 4 Compare Register (TM4OC:0x03F62)

bp	7	6	5	4	3	2	1	0
Flag	TM4OC7	TM4OC6	TM4OC5	TM4OC4	TM4OC3	TM4OC2	TM4OC1	TM4OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

Binary counter is 8-bit up counter. If any data is written to compare register the counting is stopped and binary counter is cleared to 0x00.

■ Timer 0 Binary Counter (TM0BC:0x03F50)

bp	7	6	5	4	3	2	1	0
Flag	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 1 Binary Counter (TM1BC:0x03F51)

bp	7	6	5	4	3	2	1	0
Flag	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 2 Binary Counter (TM2BC:0x03F58)

bp	7	6	5	4	3	2	1	0
Flag	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 3 Binary Counter (TM3BC:0x03F59)

bp	7	6	5	4	3	2	1	0
Flag	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 4 Binary Counter (TM4BC:0x03F60)

bp	7	6	5	4	3	2	1	0
Flag	TM4BC7	TM4BC6	TM4BC5	TM4BC4	TM4BC3	TM4BC2	TM4BC1	TM4BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

5.2.4 Timer Mode Registers

Timer mode register is readable/writable register that controls timers 0 to 4.

- Timer 0 Mode Register (TM0MD:0x03F54)

bp	7	6	5	4	3	2	1	0
Flag	-	TM0POP	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	TM0POP	Start polarity selection of output signal 0:Timer output L→H, PWM H→L 0:Timer output H→L, PWM L→H
5	TM0MOD	Pulse width measurement control 0:Normal timer operation 1:P20 pulse width measurement
4	TM0PWM	Select timer 0 operation mode 0:Normal timer operation 1:PWM operation
3	TM0EN	Timer 0 count control 0:Halt the count 1:Operate the count
2-0	TM0CK2-0	Select the clock source X00:fpll X01:TM0PSC (prescaler output) 010:fx 011:Synchronous fx 110:TM0IO input 111:Synchronous TM0IO output

■ Timer 1 Mode Register (TM1MD:0x03F55)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	TM1CAS1	TM1CAS0	TM1EN	TM1CK2	TM1CK1	TM1CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	Reserved	Always set to "0". *
5-4	TM1CAS1-0	Select operation mode of timer 1 0:Normal operation 01:16-bit cascade connection 10:24-bit cascade connection 11:32-bit cascade connection
3	TM1EN	Timer 1 count control 0:Halt the count 1:Operate the count
2-0	TM1CK2-0	Select the clock source X00:fpll X01:TM1PSC (prescaler output) 010:fx 011:Synchronous fx 110:TM1IO input 111:Synchronous TM0IO input



Always set "0" to the bp denoted by *.

■ Timer 2 Mode Register (TM2MD:0x03F5C)

bp	7	6	5	4	3	2	1	0
Flag	-	TM2POP	TM2MOD	TM2PWM	TM2EN	TM2CK2	TM2CK1	TM2CK0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	TM2POP	Select start compulsion of output signal 0:Timer output L→H, PWM H→L 0:Timer output H→L, PWM L→H
5	TM2MOD	Pulse width measurement control 0:Normal timer operation 1:P22 pulse width measurement
4	TM2PWM	Select timer 2 operation mode 0:Normal timer operation 1:PWM operation
3	TM2EN	Timer 2 count control 0:Halt the count 1:Operate the count
2-0	TM2CK2-0	Select the clock source X00:fpll X01:TM2PSC (prescaler output) 010:fx 011:Synchronous fx 110:TM2IO input 111:Synchronous TM2IO output

■ Timer 3 Mode Register (TM3MD:0x03F5D)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	TM3CAS	TM3EN	TM3CK2	TM3CK1	TM3CK0
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	TM3CAS	Select timer 3 operation mode 0:Normal timer operation 1:Cascade connection
3	TM3EN	Timer 3 count control 0:Halt the count 1:Operate the count
2-0	TM3CK2-0	Select clock source X00:fpll X01:TM3PSC (prescaler output) 010:fx 011:Synchronous fx 110:TM3IO input 111:Synchronous TM3IO input

■ Timer 4 Mode Register (TM4MD:0x03F64)

bp	7	6	5	4	3	2	1	0
Flag	-	TM4POP	TM4MOD	TM4PWM	TM4EN	TM4CK2	TM4CK1	TM4CK0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	TM4POP	Select start compulsion of output signal 0:Timer output L→H, PWM H→L 0:Timer output H→L, PWM L→H
5	TM4MOD	Pulse width measurement control 0:Normal timer operation 1:P24 pulse width measurement
4	TM4PWM	Select timer 4 operation mode 0:Normal timer operation 1:PWM operation
3	TM4EN	Timer 4 count control 0:Halt the count 1:Operate the count
2-0	TM4CK2-0	Select the clock source X00:fpll X01:TM4PSC (prescaler output) 010:fx 011:Synchronous fx 110:TM4IO input 111:Synchronous TM4IO output

■ Timer Clock Selection Register 1 (TMCKSEL1:0x03E42)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	TM4IOSEL	TM3IOSEL	TM2IOSEL	TM1IOSEL	TM0IOSEL
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	TM4IOSEL	Timer 4 input selection 0:Port 1:Simple timer
3	TM3IOSEL	Timer 3 input selection 0:Port 1:Simple timer
2	TM2IOSEL	Timer 2 input selection 0:Port 1:Simple timer
1	TM1IOSEL	Timer 1 input selection 0:Port 1:Simple timer
0	TM0IOSEL	Timer 0 input selection 0:Port 1:Simple timer

■ Timer Input Selection Register 1 (TMINSEL1:0x03E44)

bp	7	6	5	4	3	2	1	0
Flag	TMINSEL17	TMINSEL16	TMINSEL15	TMINSEL14	TMINSEL13	TMINSEL12	TMINSEL11	TMINSEL10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-6	TMINSEL17-16	Timer 3 input selection (at port selection) 00:TM3IOA(PA3) 01:TM3IOB(P63) 10:TM3IOC(P13) 11:1 input to timer
5-4	TMINSEL15-14	Timer 2 input selection (at port selection) 00:TM2IOA(PA2) 01:TM2IOB(P03) 10:TM2IOC(P11) 11:Remote control career input (from the inside)
3-2	TMINSEL13-12	Timer 1 input selection (at port selection) 00:TM1IOA(PA1) 01:TM1IOB(P62) 10:TM1IOC(P12) 11:Remote control career input (from the inside)
1-0	TMINSEL11-10	Timer 0 input selection (at port selection) 00:TM0IOA(PA0) 01:TM0IOB(P03) 10:TM0IOC(P10) 11:1 input to timer

■ Timer Input Selection Register 2 (TMINSEL2:0x03E45)

bp	7	6	5	4	3	2	1	0
Flag	TMINSEL27	TMINSEL26	TMINSEL25	TMINSEL24	TMINSEL23	TMINSEL22	TMINSEL21	TMINSEL20
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-6	TMINSEL27-26	Timer 9 input selection (at port selection) 00:TM9IOA(PA7) 01:TM9IOB(P02) 10:1 input to timer 11:1 input to timer
5-4	TMINSEL25-24	Timer 8 input selection (at port selection) 00:TM8IOA(PA6) 01:TM8IOB(P01) 10:TM8IOC(P16) 11:1 input to timer
3-2	TMINSEL23-22	Timer 7 input selection (at port selection) 00:TM7IOA(PA5) 01:TM7IOB(P00) 10:TM7IOC(P15) 11:1 input to timer
1-0	TMINSEL21-20	Timer 4 input selection (at port selection) 00:TM4IOA(PA4) 01:TM4IOB(P64) 10:TM4IOC(P14) 11:Remote control career input (from the inside)

5.3 Prescaler

5.3.1 Prescaler Operation

■ Prescaler Operation (Prescaler 0 to 1)

Prescaler 0, prescaler 1 are each free-run counter of 7 bits, 3 bits and output the dividing clock of the reference clock. This count up operation starts automatically when any TMnEN flags of 8-bit timer are set to "1" and operate the timer n counting. Also, it stops automatically when all TMnEN flags of 8-bit timer are set to "0" and stop all timer counting.

■ Count Timing of Prescaler Operation (Prescaler 0 to 1)

Prescaler 0 counts up at the rising edge of fpll.

Prescaler 1 counts up at the rising edge of fs.

■ Peripheral Functions

Peripheral functions which can use the prescaler output dividing clock, or registers which control the dividing clock selections are shown below.

Timer 0 Count Clock	CK0MD
Timer 1 Count Clock	CK1MD
Timer 2 Count Clock	CK2MD
Timer 3 Count Clock	CK3MD
Timer 4 Count Clock	CK4MD



Start the timer operation after the prescaler setup. Also, at the timer, the prescaler output should be set up by the timer mode register. The prescaler starts counting at the start of the timer operation.

5.3.2 Setup Example

■ Prescaler Operation Setup Example

fs/2 clock which is output from the prescaler 1 is selected to the count clock of the timer 0.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(1) Select fs/2 to the prescaler output by the TM0PSC 1 to 0, TM0BAS flag of the timer 0 prescaler selection register.

At the timer, prescaler output selection should be set up by the timer mode register.

5.4 8-bit Timer Count

5.4.1 8-bit Timer Operation

Timer operation can constantly generates interrupts.

■ 8-bit Timer Operation (Timers 0,1,2,3, and 4)

The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from 0x00.

Table shows clock source that can be selected by timer.

Clock source	per Count	Timer 0 (8-bit)	Timer 1 (8-bit)	Timer 2 (8-bit)	Timer 3 (8-bit)	Timer 4 (8-bit)
fpll	100 ns	O	O	O	O	O
fpll/4	400 ns	O	O	O	O	O
fpll/16	1.6 μ s	O	O	O	O	O
fpll/32	3.2 μ s	O	O	O	O	O
fpll/64	6.4 μ s	O	O	O	O	O
fpll/128	12.8 μ s	O	O	O	O	O
fs/2	400 ns	O	O	O	O	O
fs/4	800 ns	O	O	O	O	O
fs/8	1.6 μ s	O	O	O	O	O
fx	30.5 μ s	O	O	O	O	O

fpll=fosc=10 MHz fx=32.768 kHz
fs=fpll/2=5 MHz



When fx is used as clock source, they are counted at the rising of the count clock and when others are used, they are counted at the falling of the count clock.

■ Count Timing of Timer Operation (Timers 0,1,2,3, and 4)

Binary counter counts up with selected clock source as a count clock. The basic operation of the whole function of 8-bit timer is as follows:

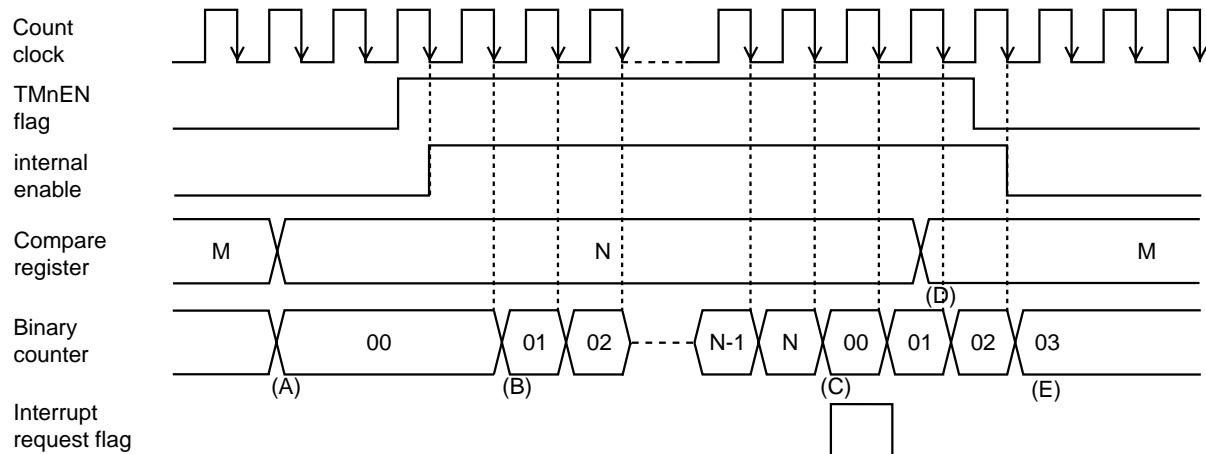


Figure:5.4.1 Count Timing of Timer Operation (Timers 0,1,2,3, and 4)

- (A) If the value is written to the compare register during the TMnEN flag is stopped ("0"), the binary counter is cleared to 0x00.
- (B) When the TMnEN flag starts to operate ("1"), the Internal Enable will be turned on at the next Count Clock. Then the binary counter begins counting up.
- (C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to 0x00 and the counting is restarted.
- (D) Even if the compare register is rewritten during the TMnEN flag is enabled ("1"), the binary counter is not changed.
- (E) When the TMnEN flag stops operating ("0"), the Internal Enable will be turned off at the next Count Clock. As a result, the binary counter stops counting.



Switch the count clock after the timer operation is stopped, as the counting is not generated correctly during the timer operation.



TMnEN flag of the TMnMD and other bits should not be changed at the same time to operate correctly.



When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So set the compare register as:

Compare register setting = (count till the interrupt request -1)

However, the interrupt generation cycle when the compare register is set to "00" is the same as it is set to "01".



If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.



If the timer interrupt request flag may have already been set before timer is started, the timer interrupt request flag should be cleared before timer is started.



The binary counter of the 8-bit timer is controlled by signals generated by sampling values of the TMnEN flag with the Count Clock. If the low-speed clock (fx) is selected as a Count Clock source, it is important to remember the followings.

After the timer halts, read the binary counter as follows:

Wait until another count clock passes, then read the value. In other words, the value is one count less than the actual value if you don't wait. Another options is that read more than once to obtain accurate value by an appropriate program.

In case of modify the timer settings (selecting clocks or functions, for example) while the timer is suspended, let the Count Clock count one more after the flag has been turned off. Otherwise the results will not be guaranteed.



If CPU operation mode is changed (from NORMAL to SLOW) when the high-frequency oscillation clock (fpll) or the prescaler output (TMnPSC) is selected as clock source, the timer operation should be stopped before operation mode transition and should be reset to start the timer after operation mode transition.

In the SLOW/HALT1 mode, as timer clock source, do not select fpll or the clock (TMnPSC) generated from fpll.



If the low-speed clock (fx) is selected as a Count Clock source, the delay produced by the binary counter may give a wrong value.

Never write values into the compare register (TMnOC) during counting. Selecting the synchronous low-speed clock (fx) as a Count Clock source solves those problems; getting correct values and allowing to write into the register during counting.



After the timer interrupt request flag is generated, maximum 3 system clock is required until the next interrupt request flag is generated. During this period, the interrupt request flag is not generated even if the binary counter reaches the set value of the compare register.



When the compare register (TMnOC) is set to '00', clear the binary counter before starting the operation.

5.4.2 Setup Example

■ Timer Operation Setup Example (Timers 0,1,2,3, and 4)

Timer function can be set by using timer 0 that generates the constant interrupt. Interrupt is generated every 250 cycles (200 µs) by selecting fs/2 (at fs=2.5 MHz operation) as a clock source.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the counting of the timer 0.
(2) Disable the interrupt TM0ICR(0x03FE8) bp1 :TM0IE =0	(2) Set the TM0IE flag of the TM0ICR register to "0" to disable the interrupt.
(3) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(3) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(5) Select fs/2 to the prescaler output by the TM0PSC 2 to 0 flag and TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(6) Set the cycle of the interrupt generation TM0OC (0x03F52) =0xF9	(6) Set the value of the interrupt generation cycle to the timer 0 compare register (TM0OC). The cycle is 250, so that the setting value is set to 249 (0xF9). At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(7) Set the interrupt level TM0ICR(0x03FE8) bp7-6 :TM0LV1-0 =10	(7) Set the interrupt level by the TM0LV1 to 0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, clear the request flag. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(8) Enable the interrupt TM0ICR (0x03FE8) bp1 :TM0IE =1	(8) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(9) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(9) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

The TM0BC starts to count up from 0x00. When the TM0BC reaches the setting value of the TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of the TM0BC becomes 0x00 and restart to count up.

5.5 8-bit Event Count

5.5.1 Operation

Event count operation has 2 types; TMnIO input and synchronous TMnIO input, according to the clock source selection.

■ 8-bit Event Count Operation (Timers 0,1,2,3, and 4)

Event count operation means that the binary counter (TMnBC) counts the input signal from external to the TMnIO pin. If the value of the binary counter reaches the setting value of the compare register (TMnOC), interrupts can be generated at the next count clock.

Table:5.5.1 Event Count Input Clock

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4
Event input	TM0IOA input/ TM0IOB input/ TM0IOC input	TM1IOA input/ TM1IOB input/ TM1IOC input	TM2IOA input/ TM2IOB input/ TM2IOC input	TM3IOA input/ TM3IOB input/ TM3IOC input	TM4IOA input/ TM4IOB input/ TM4IOC input
	Synchronous TM0IO input	Synchronous TM1IO input	Synchronous TM2IO input	Synchronous TM3IO input	Synchronous TM4IO input

■ Count Timing of TMnIO Input (Timers 0,1,2,3, and 4)

When TMnIO input is selected, TMnIO is input to the count clock of the timer n.

The binary counter is started to count up at the falling edge of the TMnIO input signal.

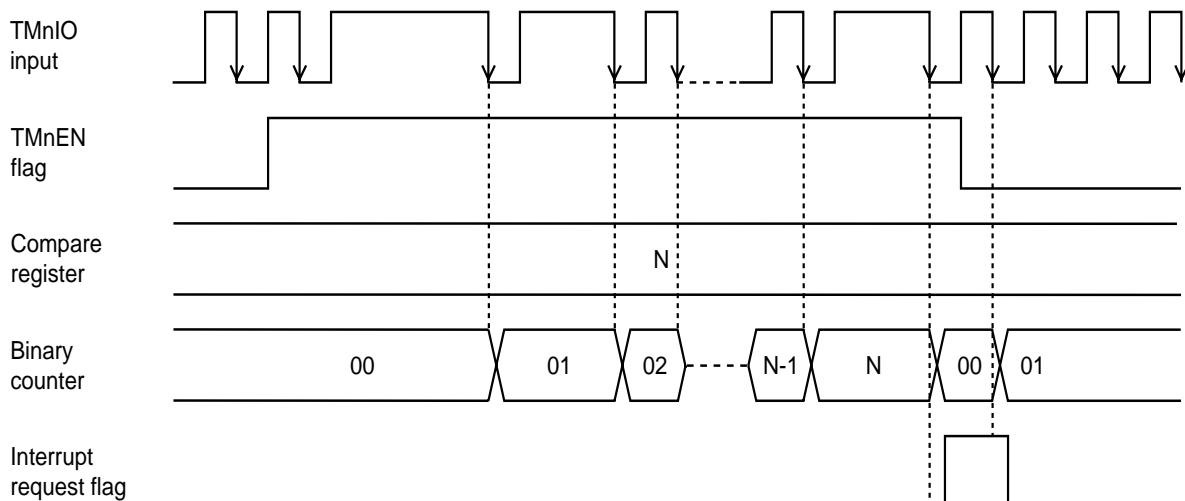


Figure:5.5.1 Count Timing of TMnIO Input (Timers 0,1,2,3, and 4)



If the TMnIO Input is selected as a Count Clock source, the delay produced by the binary counter may give a wrong value.

Never write values into the compare register (TMnOC) during counting. Selecting the event count of the synchronous TMnIO Input as a Count Clock source solves those problems; getting correct values and allowing to write into the register during counting.



The binary counter of the 8-bit timer is controlled by signals generated by sampling values of the TMnEN flag with the Count Clock. If the TMnIO Input is selected as a Count Clock source, it is important to remember the followings.

After the timer halts, read the binary counter as follows:

Wait until another count clock passes, then read the value. In other words, the value is one count less than the actual value if you don't wait. Another options is that read more than once to obtain accurate value by an appropriate program.

In case of modify the timer settings (selecting clocks or functions, for example) while the timer is suspended, let the Count Clock count one more after the flag has been turned off. Otherwise the results will not be guaranteed.

■ Count Timing of Synchronous TMnIO Input (Timers 0,1,2,3, and 4)

If the synchronous TMnIO input is selected, fs is input to the timer n count clock. The count enable signal is synchronized with the falling edge of the system clock.

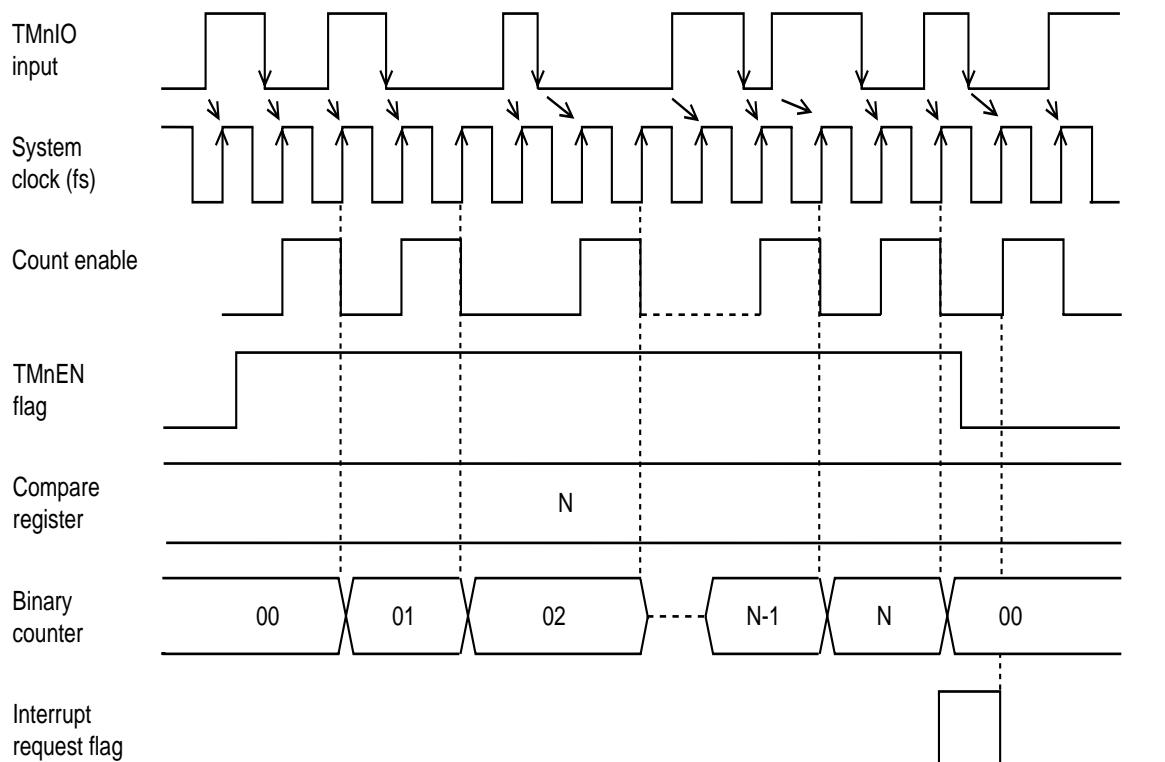


Figure:5.5.2 Count Timing of Synchronous TMnIO Input (Timers 0,1,2,3, and 4)



When the synchronous TMnIO input is selected as the count clock source, the timer n counter counts up in synchronization with system clock, therefore the correct value is always read out.



Input from TMnIO should be used to a waveform, which has 2 times and over cycles of system clock (fs). If less than the above waveforms are input, it may not be counted correctly.

5.5.2 Setup Example

■ Event Count Setup Example (Timers 0,1,2,3, and 4)

If the falling edge of the TM0IO input pin signal is detected 5 times, an interrupt is generated.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register to "0" to stop timer 0 counting.
(2) Disable the interrupt TM0ICR(0x03FE8) bp1 :TM0IE =0	(2) Set the TM0IE flag of the TM0ICR register to "0" to disable the interrupt.
(3) Set the special function pin to input PADIR(0x03F3A) bp0 :PADIR0 =0 TMINSEL1(0x03E44) bp1-0 :TMINSEL11-10 =00 TMCKSEL1(0x03E42) bp0 :TM0IOSEL =0	(3) Set the PADIRO flag of the port A direction control register (PADIR) to "0", TMINSEL11 to 10 flag of TMINSEL1 register to "00" and TM0IOSEL of TMCKSEL1 register to "0" in order to set PA0 pin to input mode. [Chapter 4. I/O Ports]
(4) Set the interrupt generation cycle TM0OC (0x03F52) =0x04	(4) Set the interrupt generation cycle to the timer 0 compare register (TM0OC). Counting is 5, so the setting value should be 4. At the time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(5) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(5) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(6) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =110	(6) Select the TM0IO input to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(7) Set the interrupt level TM0ICR(0x03FE8) bp7-6 :TM0LV1-0 =10	(7) Set the interrupt level by the TM0LV1 to 0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, clear the request flag. [Chapter 3. 3.1.4. Maskable Interrupt Control Register Setup]
(8) Enable the interrupt TM0ICR(0x03FE8) bp1 :TM0IE =1	(8) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.

Setup Procedure	Description
(9) Start the event count TM0MD(0x03F54) bp3 :TM0EN =1	(9) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

Every time TM0BC detects the falling edge of TM0IO input, TM0BC counts up from 0x00. When TM0BC reaches the setting value of TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of TM0BC becomes 0x00 and counting up is restarted.

5.6 8-bit Timer Pulse Output

5.6.1 Operation

The TMnIO pin can output a pulse signal at any frequency.

■ Operation of Timer Pulse Output (Timers 0,1,2,3, and 4)

The timers can output signals of $2 \times$ cycle of the setup value in the compare register (TMnOC). Output pins are as follows;

Table:5.6.1 Timer Pulse Output Pin

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4
Pulse output pin	TM0IOA output/ TM0IOB output/ TM0IOC output	TM1IOA output/ TM1IOB output/ TM1IOC output	TM2IOA output/ TM2IOB output/ TM2IOC output	TM3IOA output/ TM3IOB output/ TM3IOC output	TM4IOA output/ TM4IOB output/ TM4IOC output

■ Count Timing of Timer Pulse Output (Timers 0,1,2,3, and 4)

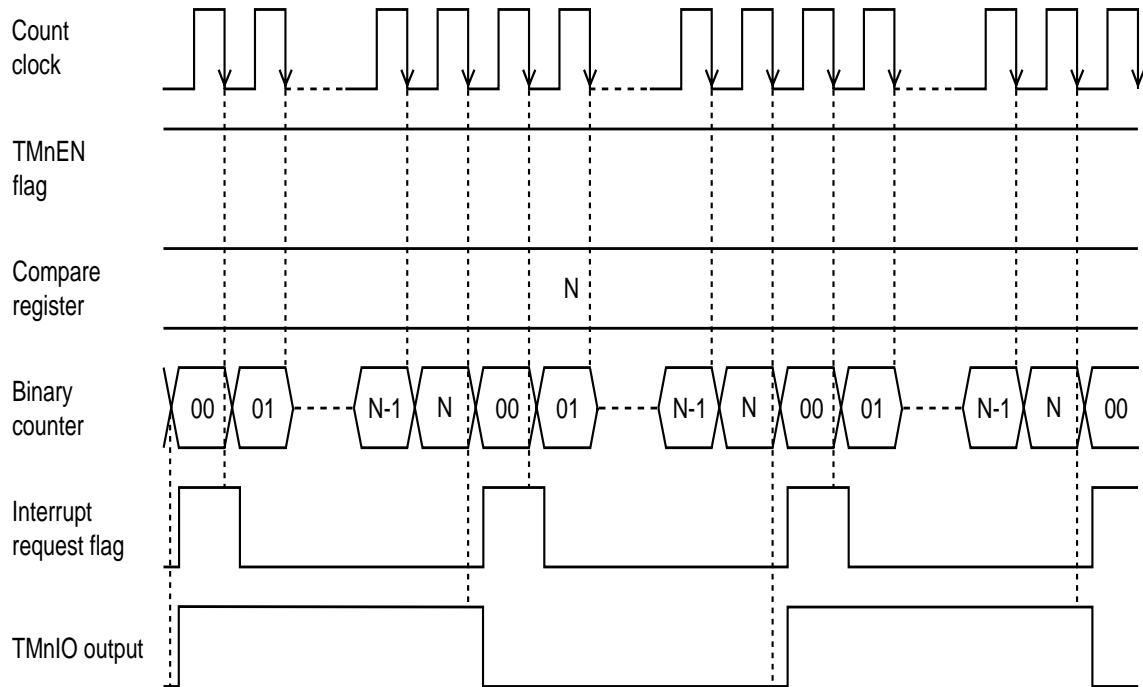


Figure:5.6.1 Count Timing of Timer Pulse Output (Timers 0,1,2,3, and 4)

- The TMnIO pin outputs signals of $2 \times$ cycle of the setup value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to 0x00, TMnIO output (timer output) is inverted.

5.6.2 Setup Example

■ Timer Pulse Output Setup Example (Timers 0,1,2,3, and 4)

TM0IO pin outputs 50 kHz pulse by using timer 0. For this, select fs/2 for clock source, and set a 1/2 cycle (100 kHz) for the timer 0 compare register (at fs = 10 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to the output mode PAOMD(0x03F09) bp0 :PAOMD0 =1 PADIR (0x03F3A) bp0 :PADIR0 =1	(2) Set the PAOMD0 flag of the port A output mode register (PAOMD) to "1" to set PA0 pin to the special function pin. Set the TM0MOD flag of the port A direction control register (PADIR) to "1" to set the output mode. [Chapter 4. I/O Ports]
(3) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(3) Set the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(5) Select fs/2 to the prescaler output by the TM0PSC 2 to 0 flags and TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(6) Set the timer pulse output cycle TM0OC (0x03F52) =0x31	(6) Set the timer 0 compare register (TM0OC) to the 1/2 of the timer pulse output cycle. The setting value should be 50-1=49 (0x31), for 100 kHz to be divided by 5 MHz. At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(7) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(7) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

TM0BC counts up from 0x00. If TM0BC reaches the setting value of the TM0OC register, then TM0BC is cleared to 0x00, TM0IO output signal is inverted and TM0BC restarts to count up from 0x00.

If any data is written to compare register when the binary counter is stopped, timer output is reset to "L".



If any data is written to compare register when the binary counter is stopped, timer output is "L".



[Compare register] Compare register=Timer pulse output / (Selection clock cycle × 2)-1

5.7 8-bit PWM Output

The TMnIO pin outputs the PWM waveform, which is determined by the match timing for the compare register and the overflow timing of the binary counter.

5.7.1 Operation

■ Operation of 8-bit PWM Output (Timers 0, 2 and 4)

The PWM waveform with an arbitrary duty cycle is generated by setting the duty cycle of PWM period to the compare register (TMnOC). The cycle is the period from the full count to the overflow of the 8-bit timer.

Table:5.7.1 shows PWM output pins;

Table:5.7.1 Output Pins of PWM Output

	Timer 0	Timer 2	Timer 4
PWM output pin	TM0IOA output/ TM0IOB output/ TM0IOC output	TM2IOA output/ TM2IOB output/ TM2IOC output	TM4IOA output/ TM4IOB output/ TM4IOC output

■ Count Timing of PWM Output (at Normal) (Timers 0, 2 and 4)

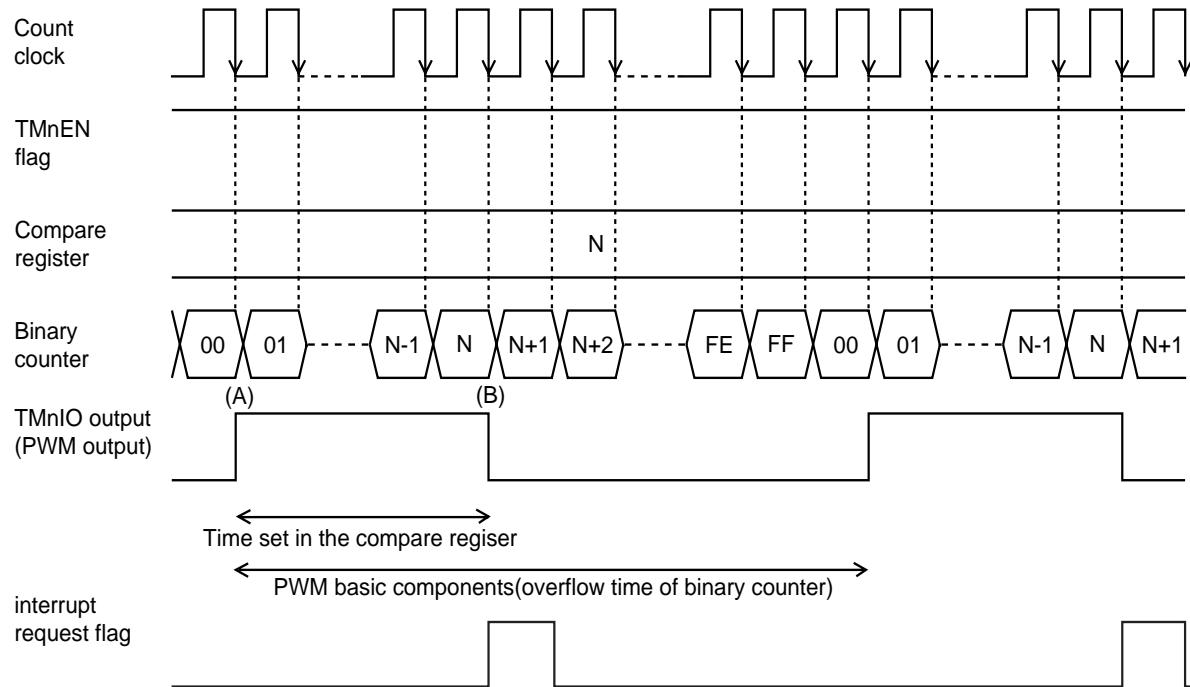


Figure:5.7.1 Count Timing of PWM Output (at Normal) (Timers 0, 2 and 4)

When TMnPOP flag is "0", PWM output waveform

- (A) TMnIO output is "H" while the value of binary counter count up from 0x01 to the value stored in the compare register.
- (B) TMnIO output is "L" after the value of binary counter match to the value in the compare register, then the binary counter continues counting up till the overflow.



The initial setting of PWM output is changed from "L" output to "H" output at the selection of PWM operation by the TMnPWM flag of the TMnMD register (when TMnPOP flag= 0).

■ Count Timing of PWM Output (when the compare register is 0x00) (Timers 0, 2 and 4)

Here is the count timing when the compare register is set to 0x00.

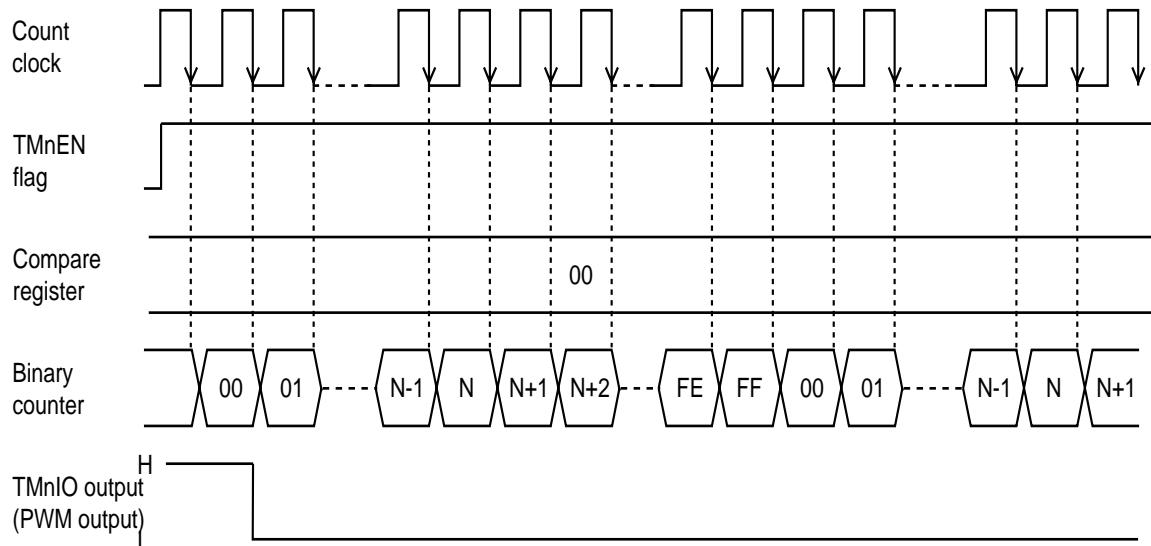


Figure:5.7.2 Count Timing of PWM Output (when the compare register is 0x00) (Timers 0, 2 and 4)

When TMnEN flag is stopped ("0"), PWM output is "H".

■ Count Timing of PWM Output (when the compare register is 0xFF) (Timers 0, 2 and 4)

Here is the count timing when the compare register is set to 0xFF.

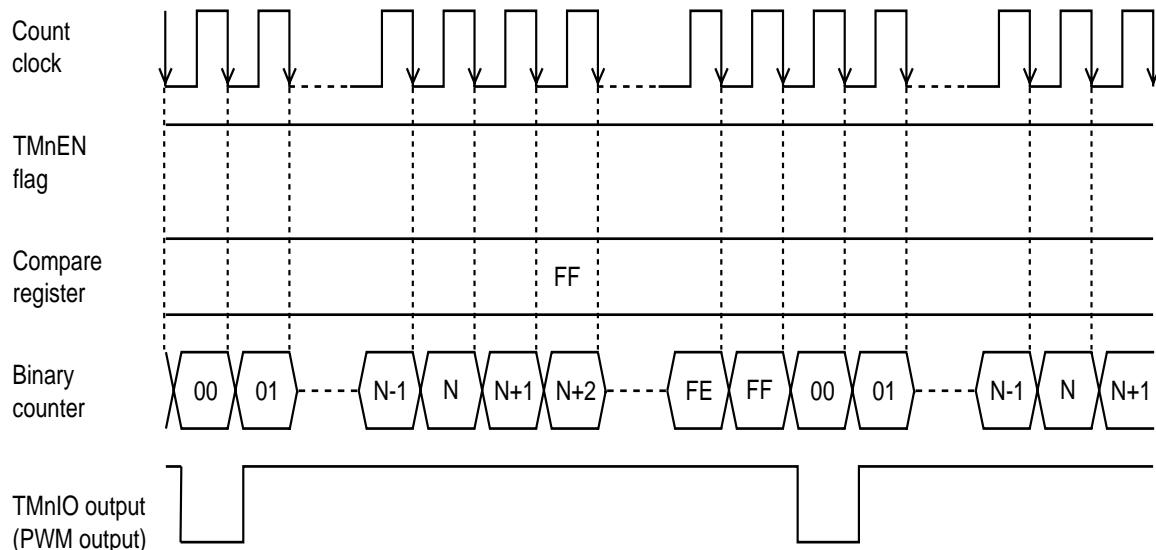


Figure:5.7.3 Count Timing of PWM Output (when the compare register is 0xFF) (Timers 0, 2 and 4)

5.7.2 PWM Outputs With Additional Pulses

■ PWM Output with Additional Pulses Method (Timers 0, 2, and 4)

This method allows the user to add one bit of pulse at a time into a PWM waveform. Up to 3 bits can be added in 4 cycles of the basic waveform.

To determine where to place, or not to place additional bits in the cycles is controlled by the timer 0 prescaler selection register (bits 5 and 6 of CK0MD), the timer 2 prescaler selection register (bits 5 and 6 of CK2MD), or the timer 4 prescaler selection register (bits 5 and 6 of CK4MD).

■ How to add pulses

The timer 0 prescaler selection register (bits 5 and 6 of CK0MD), the timer 2 prescaler selection register (bits 5 and 6 of CK2MD), or the timer 4 prescaler selection register (bits 5 and 6 of CK4MD) controls positions of pulses. For example, if "00" is specified for the CK0MD, CK2MD, or CK4MD register, not a single pulse will be added to the PWM. However, if "11" is specified, total of 3 bits will be added in the 4 cycles of the PWM.

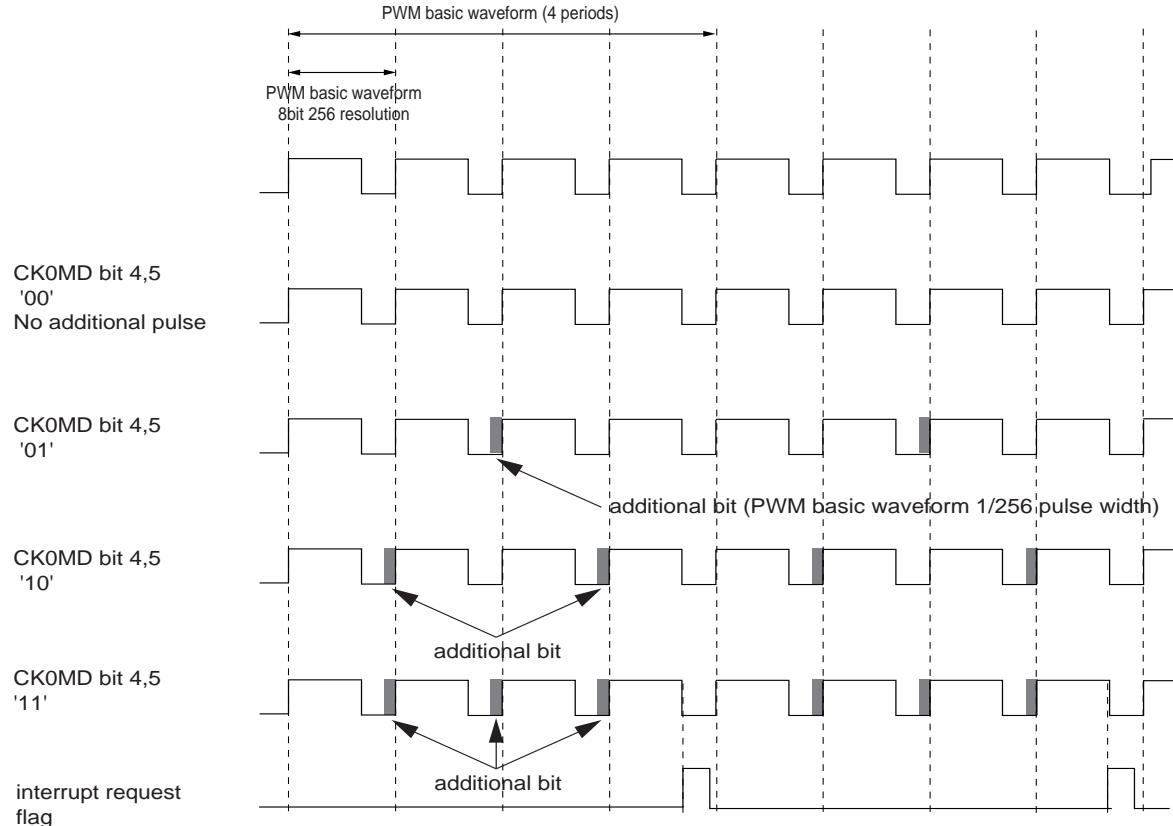
Table:5.7.2 shows the positions of pulses with the values of the CK0MD/CK2MD/CK4MD register;Figure:5.7.4 the positions of pulses with the values of the CK0MD/CK2MD/CK4MD register.

Table:5.7.2 Additional pulses settings

CKnMD Register		Locations of additional pulses (Within the four cycles of the basic waveform)
bit6	bit5	
0	0	No pulse
0	1	At second cycle
1	0	At first and third cycles
1	1	At first, second and third cycles



An interrupt occurs at the 4th cycle.



During 4 cycles of the PWM basic waveform, additional pulses(1/256 pulse width of PWM basic waveform) can be added in any of the periods 0 to 3.

Figure:5.7.4 Additional pulses and the PWM waveform



Do not change the setting of Timer n prescaler selection register (CKnMD) during timer operation.

5.7.3 Setup Example

■ PWM Output Setup Example (Timers 0, 2 and 4)

The 1/4 duty cycle PWM output waveform is output from the TM0IO output pin at 19.53 Hz by using the timer 0. $F_s/2$ oscillates at 5 MHz. Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register.

An example setup procedure, with a description of each step is shown below.

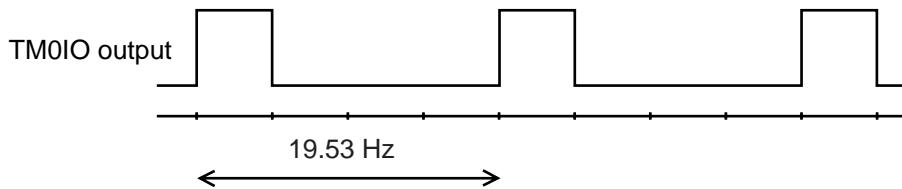


Figure 5.7.5 Output Waveform of TM0IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the special function pin to the output mode PAOMD(0x03F09) bp0 :PAOMD0 =1 PADIR (0x03F3A) bp0 :PADIR0 =1	(2) Set the PAOMD0 flag of the port A output mode register (PAOMD) to "1" to set PA0 pin to the special function pin. Set the TM0MOD flag of the port A direction control register (PADIR) to "1" to set the output mode. [Chapter 4. I/O Ports]
(3) Select the PWM operation TM0MD(0x03F54) bp4 :TM0PWM =1 bp5 :TM0MOD =0 bp6 :TM0POP =0	(3) Set the TM0PWM flag of the TM0MD register to "1", the TM0MOD flag to "0" and the TM0POP flag to "0" to select the PWM operation.
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(5) Select $fs/2$ to the prescaler output by the TM0PSC2 to 0 and TM0BAS flags of the timer 0 prescaler selection register.

Setup Procedure	Description
(6) Set the period of PWM "H" output TM0OC (0x03F52) =0x40	(6) Set the "H" period of PWM output to the timer 0 compare register (TM0OC). The setting value is set to $256/4=64$ (0x40), because it should be the 1/4 duty of the full count (256). At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(7) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(7) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

5.8 Synchronous Output

5.8.1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latch data is output from port 8 at the next count clock.

■ Synchronous Output Operation by 8-bit Timer (Timers 1 and 2)

The value of the port 8 output register (0x03F18) is output from the output pin in synchronization with the interrupt request generation by the match of the binary counter and the compare register.

Only port 8 can perform synchronous output operation, and individual bits can be set. 8-bit timers that have synchronous output operation are timers 1 and 2.

Table:5.8.1 Synchronous Output Port (Timers 1 and 2)

	Timer 1	Timer 2
Synchronous output port	Port 8	Port 8

■ Timing of Synchronous Output (Timers 1 and 2)

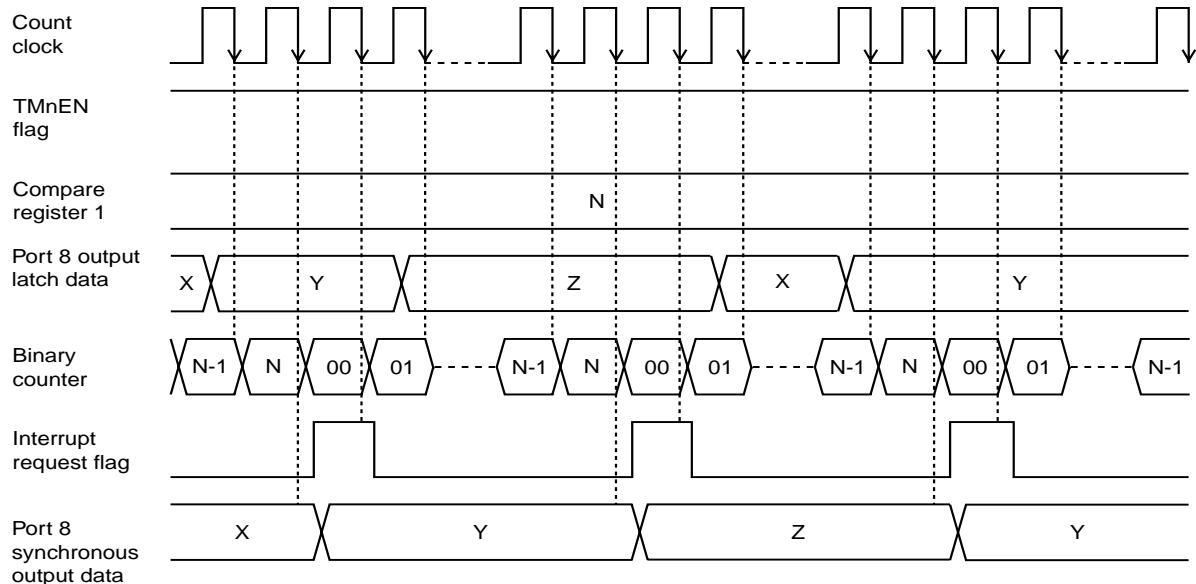


Figure:5.8.1 Timing of Synchronous Output (Timers 1 and 2)

- The value of the port 8 output register is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

5.8.2 Setup Example

■ Synchronous Output Setup Example (Timers 1 and 2)

Setup example that the value of the port 8 output register is output constantly (100 µs) by using the timer 1 from the synchronous output pin is shown below. The clock source of the timer 1 is selected fs/2 (fs=2 MHz at operation).

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM1MD(0x03F55) bp3 :TM1EN =0	(1) Set the TM1EN flag of the timer 1 mode register (TM1MD) to "0" to stop the timer 1 counting.
(2) Select the synchronous output event P8SEV(0x03F08) bp1-0 :P8SEV1-0 =11	(2) Set the P8SEV1 to 0 flag of the pin control register (P8SEV) to "11" to set the synchronous output event to the timer 1 interrupt.
(3) Set the synchronous output pin P8SYO(0x03F07) =0xFF P8DIR(0x03F38) =0xFF	(3) Set the port 8 synchronous output control register (P8SYO) to 0xFF to set the synchronous output pin. Set the port 8 direction control register (P8DIR) to 0xFF to set port 8 to output mode. [Chapter 4. I/O Ports]
(4) Select the normal timer operation TM1MD(0x03F55) bp4 :TM1CAS =0	(4) Set the TM1CAS flag of the TM1MD register to "0" to select the normal timer operation.
(5) Select the count clock source TM1MD(0x03F55) bp2-0 :TM1CK2-0 =X01	(5) Select the prescaler output to the clock source by the TM1CK2 to 0 flag of the TM1MD register.
(6) Select and enable the prescaler output CK1MD(0x03F57) bp3-1 :TM1PSC2-0 =0X0 bp0 :TM1BAS =1	(6) Select fs/2 to the prescaler output by the TM1PSC2 to 0 and TM1BAS flags of the timer 1 prescaler selection register (CK1MD).
(7) Set the synchronous output event TM1OC (0x03F53) =0x63	(7) Set the synchronous output generation cycle to the timer 1 compare register (TM1OC). The setting value is set to 100-1=99 (0x63), because 1 MHz is divided by 10 kHz. At that time, the timer 1 binary counter (TM1BC) is initialized to 0x00.
(8) Start the timer operation TM1MD(0x03F55) bp3 :TM1EN =1	(8) Set the TM1EN flag of the TM1MD register to "1" to operate the timer 1.

- TM1BC counts up from 0x00. If any data is written to the port 8 output register (P8OUT), the value of the port 8 output register is output from the synchronous output pin in every time an interrupt request is generated by the match of TM1MC and the set value of the TM1OC register.

5.9 Serial Transfer Clock Output

5.9.1 Operation

Serial transfer clock can be created by using the timer output signal.

Serial transfer clock operation by 8-bit timer (Timers 0, 1, 2, 3 and 4)

- Timer 0: Serial interface 0, 1, 2, 3, 4
 - Timer 1: Serial interface 0, 1, 2, 3, 4
 - Timer 2: Serial interface 0, 1, 2, 3, 4
 - Timer 3: Serial interface 0, 1, 2, 3, 4
 - Timer 4: Serial interface 0, 1, 2, 3, 4
- Timing of Serial Transfer Clock (Timers 0, 1, 2, 3 and 4)

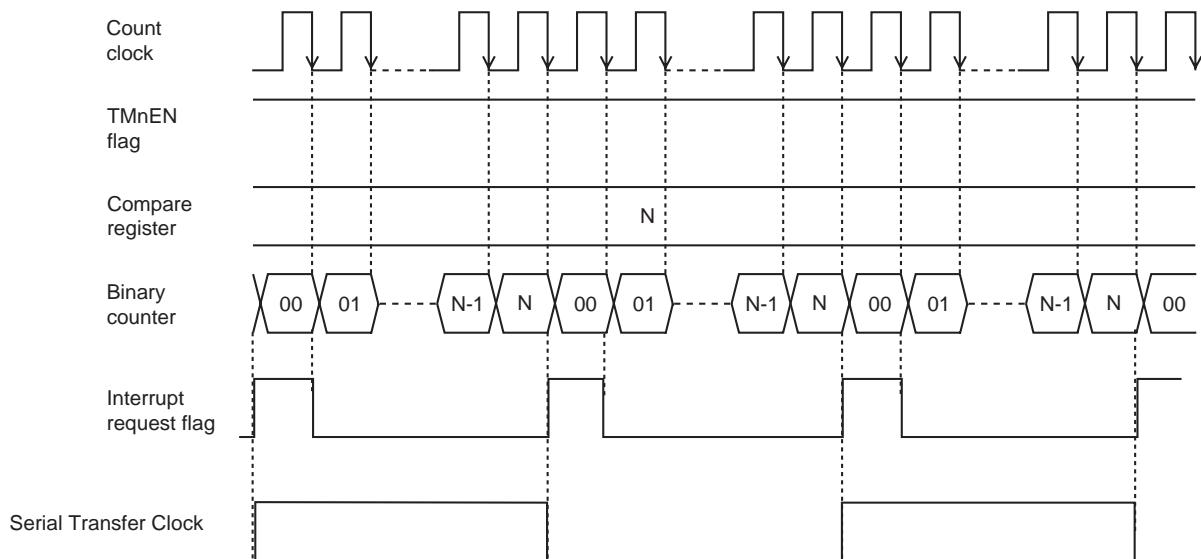


Figure:5.9.1 Timing of Serial Transfer Clock (Timers 0, 1, 2, 3 and 4)

- The timer frequency is 1/2 of the set frequency set by the compare register.
- For the baud rate calculation and the serial interface setup, refer to Serial Interface.

5.9.2 Setup Example

■ Serial Transfer Clock Setup Example (Timer 0)

How to create a transfer clock for half duplex UART (Serial 0) using with the timer 0 is shown below. The baud rate is selected to be 300 bps, the source clock of timer 0 is selected to be $fs/2$ (at $fs=2$ MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(2) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(3) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(3) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(4) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(4) Select $fs/2$ to the prescaler output by the TM0PSC2 to 0 flags and the TM0BAS flag of the timer 0 prescaler selection register.
(5) Set the baud rate TM0OC (0x03F52) =0xCF	(5) Set the timer 0 compare register (TM0OC) such a value that the baud rate comes to 300 bps. At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(6) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(6) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

- TM0BC counts up from 0x00. Timer 0 output is the clock of the serial interface 0 at transmission and reception.
- Refer to Serial Interface for the compare register set value and serial operation setup.

5.10 Simple Pulse Width Measurement

5.10.1 Operation

Timer measures the "L" duration of the pulse signal input from the external interrupt pin.

■ Simple Pulse Width Measurement Operation by 8-bit Timer (Timers 0, 2 and 4)

Sample input signals of the external interrupt pins, which is used to measure the simple pulse width, at the Count Clock. The binary counter will count while the signals are LOW. Pulse width "L" period can be measured by reading the count of timer. 8-bit timers that have the simple pulse width measurement function are the Timers 0, 2 and 4.

Table:5.10.1 Simple Pulse Width Measurement Able Pins

	Timer 0	Timer 2	Timer 4
Simple pulse width measurement enable pin	External interrupt 0 (P20/IRQ0)	External interrupt 2 (P22/IRQ2)	External interrupt 4 (P22/IRQ4)

■ Count Timing of Simple Pulse Width Measurement (Timers 0, 2 and 4)

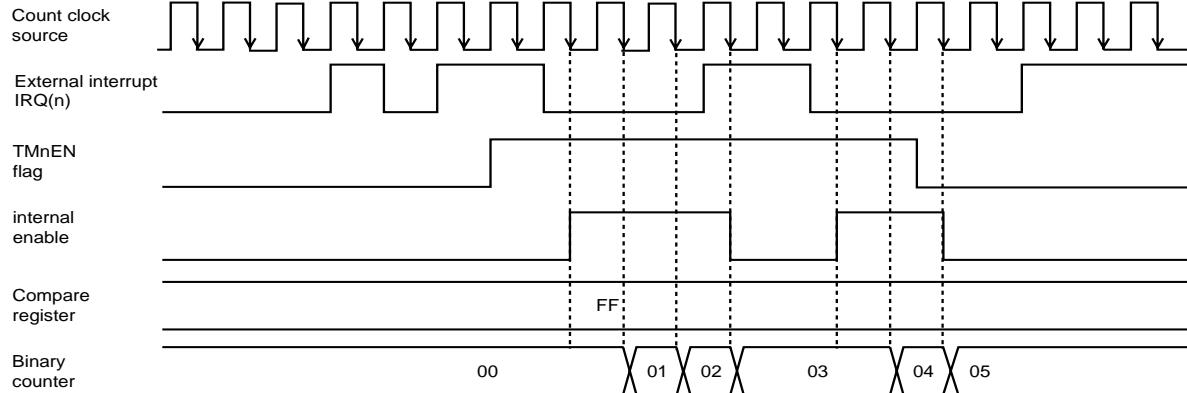


Figure:5.10.1 Count Timing of Simple Pulse Width Measurement (Timers 0, 2 and 4)

- Internal enable signal is generated when the count clock executes samplings of the condition while the TMnEN flag is operated ("1") and the input signal of external interrupt pins for simple pulse width measurement is "L". While the internal enable is "H", timer counts up.

5.10.2 Setup Example

■ Setup Example of Simple Width Measurement by 8-bit Timer (Timers 0, 2 and 4)

The pulse width of "L" period of the external interrupt 0 (IRQ0) input signal is measured by the timer 0. The clock source of the timer 0 is selected to fs/2.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the pulse width measurement operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =1	(2) Set the TM0PWM flag of the TM0MD register to "0" and TM0MOD flag to "1" to enable the timer operation during "L" period to be measured.
(3) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(3) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(4) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(4) Select fs/2 to the prescaler output by the TM0PSC1 to 0 flag and the TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(5) Set the compare register TM0OC (0x03F52) =0xFF	(5) Set the timer 0 compare register (TM0OC) to the bigger value than the cycle of fs/2 / "L" period of measured pulse width. At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(6) Set the interrupt level IRQ0ICR(0x03FE2) bp7-6 :IRQ0LV1-0 ="XX"	(6) Set the interrupt level by the IRQ0LV1 to 0 flag of the external interrupt 0 control register (IRQ0ICR). If the interrupt request flag is already set, clear all interrupt request flags. [Chapter 3. 3.1.4. Maskable Interrupt Control Register Setup]
(7) Set the interrupt valid edge IRQ0ICR(0x03FE2) bp5 :REDG0 =1	(7) Set the REDG0 flag of the IRQ0ICR register to "1" to specify the interrupt valid edge to the rising edge.
(8) Enable the interrupt IRQ0ICR(0x03FE2) bp1 :IRQ0IE =1	(8) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
(9) Enable the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(9) Set the TM0EN flag of the TM0MD register to "1" to enable the timer 0 operation.

- At sampling the negative edge of the external interrupt 0 (IRQ0) input with the count clock, the internal enable is set. And after the setting, the next count clock makes TM0BC start to count up from 0x00. Timer 0 continues to count up during "L" period of IRQ0 input, then stop the counting with positive edge of IRQ0 input as a trigger. At the same time, reading the value of TM0BC by interrupt handling can detects "L" period of IRQ0 input.

5.11 Cascade Connection

5.11.1 16-bit Cascade Connection Operation

Cascading Timers 0 and 1 or Timers 2 and 3 forms a 16-bit timer.

■ Operation (Timer 0 + Timer 1, Timer 2 + Timer 3)

Timers 0 and 1 or Timers 2 and 3 are combined to be a 16-bit timer. Cascading timer is operated at the clock source of Timers 0 or 2 which are lower 8 bits.

Table:5.11.1 Timer Functions at 16-bit Cascade Connection

	Timer 0+Timer1 (16-bit)	Timer 2+Timer 3 (16-bit)
Interrupt source	TM1IRQ	TM3IRQ
Timer operation	O	O
Event count	O TM0IO input	O TM2IO input
PWM output	-	-
Synchronous output	O	-
Pulse width measurement	O	O
Clock source	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM0IO input Synchronous fx Synchronous TM0IO input Simple timer A input	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM2IO input Synchronous fx Synchronous TM2IO input Simple timer A input
<p>fpll:Machine clock (High frequency oscillation) fx:Machine clock (Low frequency oscillation) fs:System clock [Chapter 2. 2.6 Clock Switching]</p>		

- At cascade connection, the binary counter and the compare register are operated as a 16-bit register. At operation, set the TMnEN flag of the lower 8-bit timers to "1" to be operated.

The upper 8-bit timer outputs waveforms of the timer pulse output and interrupt request flags. Also, select the clock source by the lower 8-bit timer.

Other setup and count timing is the same to the 8-bit timer at independently operation.



When timer 0 and timer 1 are used in cascade connection, timer 1 is used as an interrupt request flag. Timer pulse output of timer 0 is "L" fixed output.
An interrupt request of timer 0 is not generated, but the timer 0 interrupt should be disabled.



When timer 2 and timer 3 are used in cascade connection, timer 3 is used as an interrupt request flag. Timer pulse output of timer 2 is "L" fixed output.
An interrupt request of timer 2 is not generated, but the timer 2 interrupt should be disabled.



At 16-bit cascade connection, when the clear of the binary counter is needed by rewriting the compare register, set the TMnEM flag of both the upper 8-bit timer and the lower 8-bit timer to "0" to stop counting.



Use a 16-bit access instruction to set the (TM1OC + TM0OC) register, (TM3OC + TM2OC) register.



During cascade connection, PWM output function cannot be used. When connecting cascade, always set TMPWM flag of timer mode register to "0".



Stop the timer in order to read out the value of timer connected in cascade.

5.11.2 24-bit Cascade Connection Operation

Timers 0, 1 and 2 can be cascaded to form one 24-bit timer in the 24-bit cascade mode.

■ Operation (Timer 0 + Timer 1 + Timer 2)

Timers 0, 1 and 2 can be cascaded to form a 24-bit timer. Then, the timer runs by clock sources of the timer 0 for the lower 8-bit timer.

Table:5.11.2 Timer Functions in 24-bit Cascade Mode

	Timer 0 + Timer 1 + Timer 2 (24-bit)
Interrupt source	TM2IRQ
Timer operation	O
Event count	O TM0IO input
PWM output	-
Synchronous output	O
Pulse width measurement	O
Clock sources	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM0IO input Synchronous fx Synchronous TM0IO input
fpll: Machine clock (High frequency oscillation) fx: Machine clock (Low frequency oscillation) fs: System clock [Chapter 2 2.6 Clock Switching]	

- At cascade connection, the binary counter and compare register are operated as 24-bit registers. At operation, set the TM0EN flag of the timer 0 to "1".

The timer 2 outputs waveforms of the timer pulse output and interrupt request flags. Also, select the clock source by the timer 0.

Other setup and count timing are the same as the settings of 8-bit timer at independently operation.



When the timers 0, 1 and 2 are cascaded, the timer 2 is used for a timer pulse output and an interrupt request flag. Timer pulse output of the timers 0 and 1 is "L" fixed output. Although an interrupt request would not occur at the timer 0 or timer 1, interrupts should be disabled for the both timers.



At 24-bit cascade connection, when the binary counter needs to be cleared because of rewriting the compare registers, set the TM0EM flag of the timer 0 to "0" to stop counting. Then start rewriting all compare registers for the timers 0 through 2.



During cascade connection, PWM output function cannot be used. When connecting cascade, always set TMPWM flag of timer mode register to "0".



During 24-bit cascade connection, always set the TM3CAS flag of the timer 3 mode register (TM3MD) to "0".



Stop the timer in order to read out the value of timer connected in cascade.

5.11.3 32-bit Cascade Connection Operation

Timers 0, 1, 2 and 3 can be cascaded to form one 32-bit timer in the 32-bit cascade mode.

■ Operation (Timer 0 + Timer 1 + Timer 2 + Timer 3)

Timers 0, 1, 2 and 3 can be cascaded to form a 32-bit timer. Then, the timer runs by clock sources of the timer 0 for the lower 8-bit timer.

Table:5.11.3 Timer Functions in 32-bit Cascade Mode

	Timer 0 + Timer 1 + Timer 2 + Timer 3 (32-bit)
Interrupt source	TM3IRQ
Timer operation	O
Event count	O TM0IO input
PWM output	-
Synchronous output	O
Pulse width measurement	O
Clock sources	fpll fpll/4 fpll/16 fpll/32 fpll/64 fpll/128 fs/2 fs/4 fs/8 fx TM0IO input Synchronous fx Synchronous TM0IO input
fpll: Machine clock (High frequency oscillation) fx: Machine clock (Low frequency oscillation) fs: System clock [Chapter 2 2.6 Clock Switching]	

- At cascade connection, the binary counter and compare register are operated as 32-bit registers. At operation, set the TM0EN flag of the timer 0 to "1".

The timer 3 outputs waveforms of the timer pulse output and interrupt request flags. Also, select the clock source by the timer 0.

Other setup and count timing are the same as the settings of 8-bit timer at independently operation.



When the timers 0, 1, 2 and 3 are cascaded, the timer 3 is used for a timer pulse output and an interrupt request flag. Timer pulse output of the timers 0, 1 and 2 is "L" fixed output. Although an interrupt request would not occur at the timer 0, timer 1 or timer 2, interrupts should be disabled for the three timers.



At 32-bit cascade connection, when the binary counter needs to be cleared because of rewriting the compare registers, set the TM0EM flag of the timer 0 to "0" to stop counting. Then start rewriting all compare registers for the timers 0 through 3.



During cascade connection, PWM output function cannot be used. When connecting cascade, always set TMPWM flag of timer mode register to "0".



During 32-bit cascade connection, always set the TM3CAS flag of the timer 3 mode register (TM3MD) to "0".



Stop the timer in order to read out the value of timer connected in cascade.

5.11.4 Setup Example

■ 16-bit Cascade Connection Timer Setup Example (Timer 0 + Timer 1)

Setting example of timer function that an interrupt is constantly generated by cascade connection of the timer 0 and the timer 1, as a 16-bit timer is shown. An interrupt is generated 2500 times every 1 ms by selecting source clock fs/2 (fs=5 MHz at operation).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0 TM1MD(0x03F55) bp3 :TM1EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0", the TM1EN flag of the timer 1 mode register (TM1MD) to "0" to stop the timer 0 and the timer 1 counting.
(2) Disable the timer interrupt TM0ICR(0x03FE8) bp1 :TM0IE =0 TM1ICR(0x03FE9) bp1 :TM1IE =0	(2) Set the TM0IE flag of the timer 0 interrupt control register (TM0ICR) to "0" to disable the interrupt. Set the TM1IE flag of the timer 1 interrupt control register (TM1ICR) to "0" to disable the interrupt.
(3) Select the normal lower timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(3) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer 0 operation.
(4) Set the cascade connection TM1MD(0x03F55) bp4 :TM1CAS =1	(4) Set the TM1CAS flag of the TM1MD register to "0" to connect the timer 1 and the timer 0 to the cascade.
(5) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(5) Select the prescaler to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(6) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(6) Select fs/2 to the prescaler output by the TM0PSC2 to 0 flags and the TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(7) Set the interrupt generation cycle TM1OC,TM0OC (0x03F53,0x03F52) = 0x09C3	(7) Set the timer 1 compare register + timer 0 compare register (TM1OC + TM0OC) to the interrupt generation cycle (0x09C3:2500 cycles -1). At that time, timer 1 binary counter + timer 0 binary counter (TM1BC + TM0BC) are initialized to 0x0000.
(8) Set the level of the upper timer interrupt TM1ICR(0x03FE9) bp7-6 :TM1LV1-0 =10	(8) Set the interrupt level by the TM1LV1 to 0 flag of the timer 1 interrupt control register (TM1ICR). If any interrupt request flag may be already set, clear all request flags. [Chapter 3. 3.1.4. Maskable Interrupt Control Register Setup]

Setup Procedure	Description
(9) Enable the lower timer interrupt TM1ICR(0x03FE9) bp1 :TM1IE =1	(9) Set the TM1IE flag of the TM1ICR register to "1" to enable the interrupt.
(10) Start the lower timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(10) Set the TM0EN flag of the TM0MD register to "1" to operate the 16-bit cascade connection.

- TM1BC + TM0BC counts up from 0x0000 as a 16-bit timer.

When TM1BC + TM0BC reaches the set value of TM1BC + TM0BC register, the timer 1 interrupt request flag is set at the next count clock, and the value of TM1BC + TM0BC becomes 0x0000 and restarts count up.

6

Chapter 6 8-bit Simple-Timers

6.1 Overview

This timer is a 8-bit simple timer that can be used as a serial transfer clock, LCD clock or 8-bit/16-bit timer count.

8-bit simple timer contains two prescalers. Each prescaler counts fpll, fs as the base clock. Configurations of hardware are shown below.

Prescaler 0 (fpll base) 5 bits Prescaler

Prescaler 1 (fs base) 2 bits Prescaler

Prescaler 0 outputs fpll/2, fpll/4, fpll/8, fpll/16, fpll/32.

Prescaler 1 outputs fs/2, fs/4.

The TMAMD1 register can select a clock source for timer from fpll and fs by using the internal prescaler output.

6.1.1 Functions

Table:6.1.1 shows clock sources of 8-bit simple timer.

Table:6.1.1 Timer Functions

	Timer A (8-bit)
Clock source	fpll fpll/2 fpll/4 fpll/8 fpll/16 fpll/32 fs/2 fs/4
fpll:Machine clock (High frequency oscillation) fs:System clock	

6.1.2 Block Diagram

■ Timer A Block Diagram

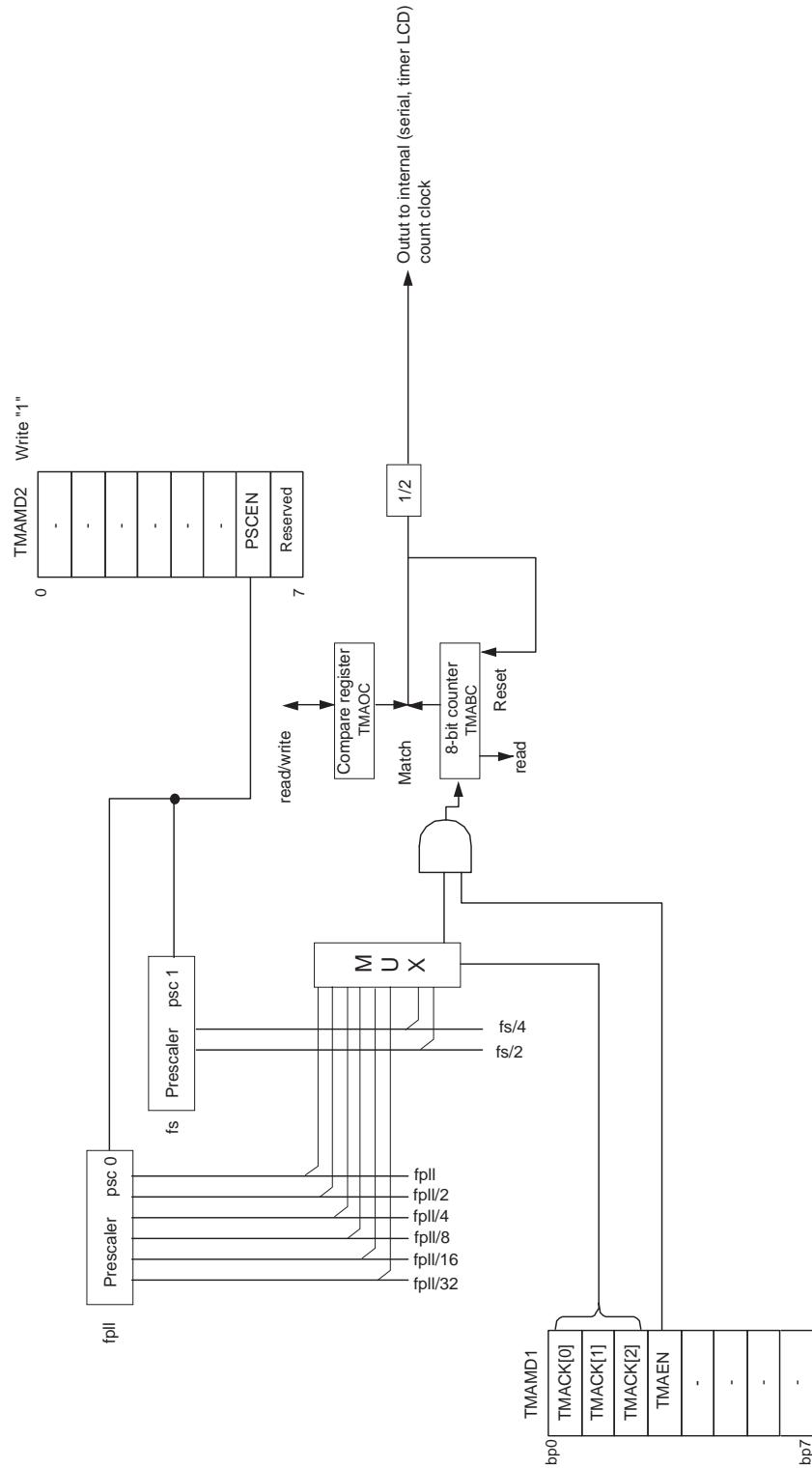


Figure:6.1.1 Timer A Block Diagram

6.2 Control Registers

Timer A consists of the binary counter (TMABC) and the compare register (TMAOC). It is controlled by the mode register (TMAMD).

6.2.1 Registers

Table:6.2.1 shows registers that control timer A.

Table:6.2.1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer A	TMABC	0x03F61	R	Timer A binary counter	VI-5
	TMAOC	0x03F63	R/W	Timer A compare register	VI-5
	TMAMD1	0x03F65	R/W	Timer A mode register 1	VI-6
	TMAMD2	0x03F67	R/W	Timer A mode register 2	VI-7

R/W: Readable / Writable

R: Readable only

6.2.2 Programmable Timer Registers

Timer A has 8-bit programmable timer registers.

Programmable timer registers consist of a compare register and a binary counter.

The compare register is a 8-bit register which stores the value to be compared to the binary counter.

- **Timer A Compare Register (TMAOC:0x03F63)**

bp	7	6	5	4	3	2	1	0
Flag	TMAOC7	TMAOC6	TMAOC5	TMAOC4	TMAOC3	TMAOC2	TMAOC1	TMAOC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

Binary counter is 8-bit up counter. The binary counter to stop the count operation is cleared to 0x00.

- **Timer A Binary Counter (TMABC:0x03F61)**

bp	7	6	5	4	3	2	1	0
Flag	TMABC7	TMABC6	TMABC5	TMABC4	TMABC3	TMABC2	TMABC1	TMABC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

6.2.3 Timer Mode Registers

Timer mode registers are readable/writable registers that control timer A.

■ Timer A Mode Register 1 (TMAMD1:0x03F65)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	Reserved	TMAEN	TMACK2	TMACK1	TMACK0
At reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	Reserved	Always set to "0". *
3	TMAEN	Timer A count control 0:Halt the count 1:Operate the count
2-0	TMACK2-0	Select the clock source 000:fpll 001:fpll/2 010:fpll/4 011:fpll/8 100:fpll/16 101:fpll/32 110:fs/2 111:fs/4



Always set "0" to the bp denoted by *.

■ Timer A Mode Register 2 (TMAMD2:0x03F67)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	PSCEN	-	-	-	-	-	-
At reset	0	0	-	-	-	-	-	-
Access	R/W	R/W	-	-	-	-	-	-

bp	Flag	Description
7	Reserved	Always set to "0". *
6	PSCEN	Prescaler operation control 0:Deactivate Prescaler 1:Operate Prescaler
5-0	-	-



Always set "0" to the bp denoted by *.

6.3 8-bit Simple Timer Count

6.3.1 8-bit Simple Timer Operation

8-bit simple timer in this LSI contains one timer as only a basic function of “Chapter 5 8-bit Timers”.

■ 8-bit Simple Timer Operation (Timer A)

The fundamental cycle of timer count is set by the clock source selection and the setting value of the compare register (TMAOC), in advance. If the binary counter (TMABC) reaches the setting value of the compare register, binary counter is cleared at the next count clock and counting is restarted from 0x00. There is, however, no interrupt function.

The following table shows clock source that can be selected by timer.

Clock source	per Count	Timer A (8-bit)
fpll	50 ns	O
fpll/2	100 ns	O
fpll/4	200 ns	O
fpll/8	400 ns	O
fpll/16	0.8 μ s	O
fpll/32	1.6 μ s	O
fs/2	200 ns	O
fs/4	400 ns	O
fpll=20 MHz fx=32.768 kHz fs=fpll/2=10 MHz		



When fpll is selected the clock source, prescaler operation control frag (PSCEN flag of TMAMD2 register) is set necessary before set TMAEN flag.

■ Count Timing of Timer Operation (Timer A)

Binary counter counts up with selected clock source as a count clock. The basic operation of the whole function of 8-bit timer is as follows:

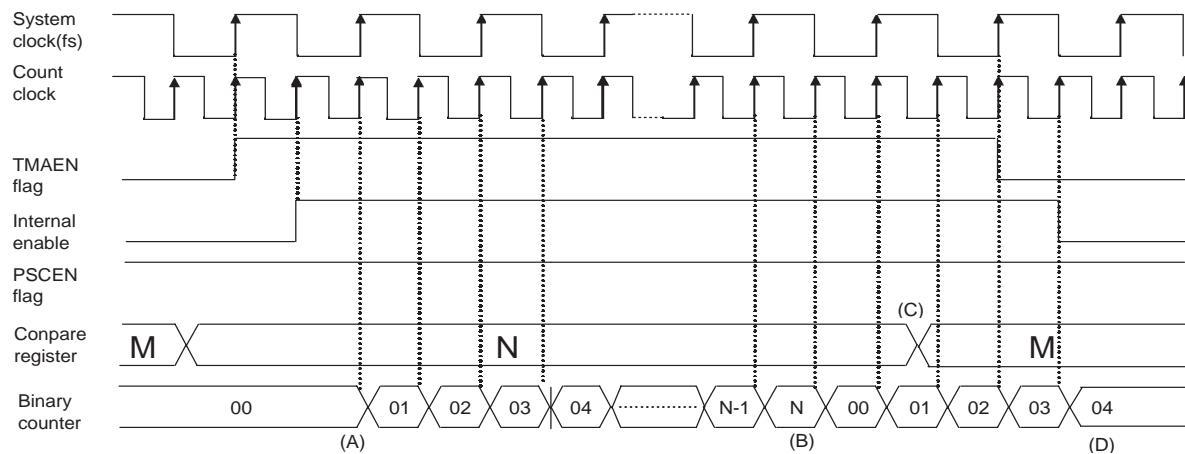


Figure:6.3.1 Count Timing of Timer Operation (Timer A)

- (A) When the TMAEN flag, the PSCEN flag start to operate ("1"), the Internal Enable will be turned on at the next Count Clock. Then the binary counter begins counting up.
- (B) If the binary counter reaches the value of the compare register, the binary counter is cleared to 0x00 at the next count clock and the counting is restarted.
- (C) Even if the compare register is rewritten during the TMAEN flag is enabled ("1"), the binary counter is not changed.
- (D) When the TMAEN flag stops operating ("0"), the binary counter stops counting and cleared to 0x00.



Switch the count clock after the timer operation is stopped, as the counting is not generated correctly during the timer operation.



TMAEN flag of the TMAMD and other bits should not be changed at the same time to operate correctly.



When the binary counter reaches the value in the compare register, the value of the internal count clock is inverted at the next count clock. So set the compare register as:

Compare register setting = (count till the compare match -1)



If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

6.4 Serial Transfer Clock Output

6.4.1 Operation

Serial transfer clock can be created by using the timer output signal.

Serial transfer clock operation by 8-bit timer (Timer A)

- Timer A: Serial interfaces 0 to 4
- Timing of Serial Transfer Clock (Timer A)

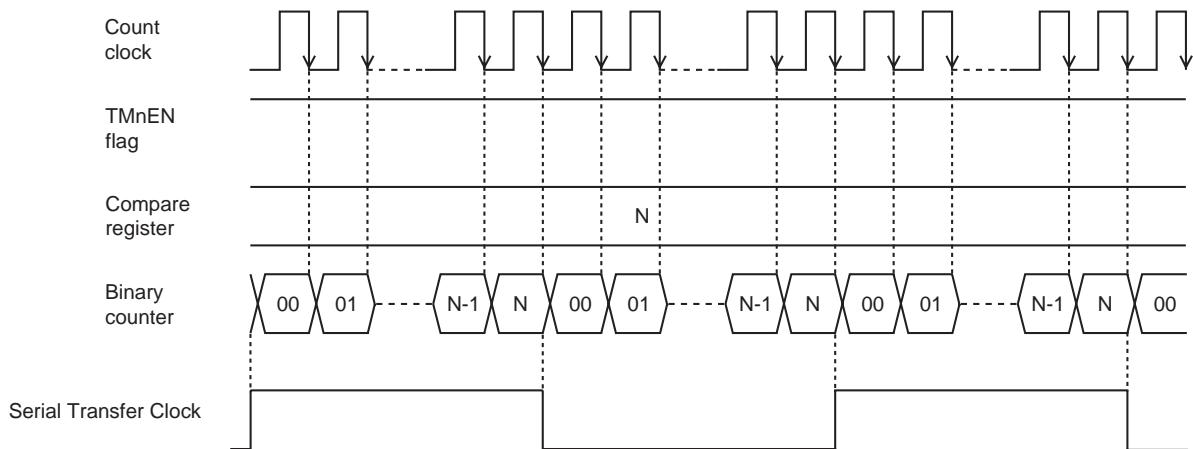


Figure:6.4.1 Timing of Serial Transfer Clock (Timer A)

- The timer frequency is 1/2 of the set frequency set by the compare register.
- For the baud rate calculation and the serial interface setup, refer to [Serial Interface](#).



The output signal of this timer can be used as the clock source of 8-bit timer/16-bit timer as well as above-mentioned the serial transfer clock.

6.4.2 Setup Example

■ Serial Transfer Clock Setup Example (Timer A)

How to create a transfer clock for half duplex UART (Serial 0) using with the timer A is shown below. The baud rate is selected to be 300 bps, the source clock of timerA is selected to be $fs/2$ (at $fs=2$ MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TMAMD1(0x03F65) bp3 :TMAEN =0	(1) Set the TMAEN flag of the timer A mode register 1 (TMAMD1) to "0" to stop the timer A counting.
(2) Select the count clock source TMAMD1(0x03F65) bp2-0 :TMACK2-0 =110	(2) Select the prescaler output to the clock source by the TMACK2 to 0 flags of the TMAMD1 register.
(3) Set the baud rate TMAOC (0x03F63) =0xCF	(3) Set the timer A compare register (TMAOC) such a value that the baud rate comes to 300 bps.
(4) Start the timer operation TMAMD2(0x03F67) bp6 :PSCEN =1	(4) Set the PSCEN flag of the timer A mode register 2 (TMAMD2) to "1" to operate the timer counting.
(5) Start the timer operation TMAMD1(0x03F65) bp3 :TMAEN =1	<ul style="list-style-type: none"> • Set the TMAEN flag of the TMAMD1 register to "1" to operate the timer A.

- TMABC counts up from 0x00. Timer A output is the clock of the serial interface 0 at transmission and reception.
- For the baud rate calculation and the serial interface setup, refer to [Serial Interface](#).

7

Chapter 7 16-bit Timers

7.1 Overview

This LSI contains three general-purpose 16-bit timers (timer 7, timer 8 and timer 9). The 16-bit timer has compare register with double buffer and single buffer. The buffer can be selected.

Timer n (high precision 16-bit timer) contains 2 sets of compare registers with double buffering and 2 sets of independent interrupt functions such as timer n interrupt and timer n compare register 2-match interrupt.

Pins can be switched to TMnIOA/TMnIOB/TMnIOC.

TM7IOA (PA5)
TM7IOB (P00)
TM7IOC (P15)
TM8IOA (PA6)
TM8IOB (P01)
TM8IOC (P16)
TM9IOA (PA7)
TM9IOB (P02)



On the text, if there is not much functional difference in pins A , B and C, “A”, “B” and “C” of the pin names are omitted.

7.1.1 Functions

Table:7.1.1 shows the functions of each timer.

Table:7.1.1 16-bit Timer Functions

	Timer 7 (High precision 16-bit timer)	Timer 8 (High precision 16-bit timer)	Timer 9 (High precision 16-bit timer)
Input source	TM7IRQ TM7OC2IRQ	TM8IRQ TM8OC2IRQ	TM9IRQ TM9OC2IRQ
Timer operation	O	O	O
Event count	OTM7IOA input/TM7IOB input/TM7IOC input	OTM8IOA input/TM8IOB input/TM8IOC input	OTM9IOA input/TM9IOB input/TM9IOC input
Timer pulse output	OTM7IOA output/TM7IOB output/TM7IOC output	OTM8IOA output/TM8IOB output/TM8IOC output	OTM9IOA output/TM9IOB output
PWM output (duty is changeable)	OTM7IOA output/TM7IOB output/TM7IOC output	OTM8IOA output/TM8IOB output/TM8IOC output	OTM9IOA output/TM9IOB output
High precision PWM output (duty/cycle are changeable)	OTM7IOA output/TM7IOB output/TM7IOC output	OTM8IOA output/TM8IOB output/TM8IOC output	OTM9IOA output/TM9IOB output
IGBT output (duty is changeable)	OTM7IOA output/TM7IOB output/TM7IOC output, TM8IOA output/TM8IOB output/TM8IOC output	x	x
High precision IGBT output (duty/cycle are changeable)	OTM7IOA output/TM7IOB output/TM7IOC output, TM8IOA output/TM8IOB output/TM8IOC output	x	x
Synchronous output	O	x	x
Capture function	O	O	O
Pulse width measurement	O	O	O
32-bit cascade connection Timer operation, PWM output, High precision PWM output	O	x	x
Clock source	fpll fpll/2 fpll/4 fpll/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16 Synchronous TM7IO input Synchronous TM7IO/2 input Synchronous TM7IO/4 input Synchronous TM7IO/16 input Timer A output Timer A output/2 Timer A output/4 Timer A output/16	fpll fpll/2 fpll/4 fpll/16 fs fs/2 fs/4 fs/16 TM8IO input TM8IO input/2 TM8IO input/4 TM8IO input/16 Synchronous TM8IO input Synchronous TM8IO/2 input Synchronous TM8IO/4 input Synchronous TM8IO/16 input Timer A output Timer A output/2 Timer A output/4 Timer A output/16	fpll fpll/2 fpll/4 fpll/16 fs fs/2 fs/4 fs/16 TM9IO input TM9IO input/2 TM9IO input/4 TM9IO input/16 Synchronous TM9IO input Synchronous TM9IO/2 input Synchronous TM9IO/4 input Synchronous TM9IO/16 input Timer A output Timer A output/2 Timer A output/4 Timer A output/16
fpll:Machine clock (High frequency oscillation) fs:System clock [Chapter 2.6.Clock Switching]			

7.1.2 Block Diagram

■ Timer 7 Block Diagram

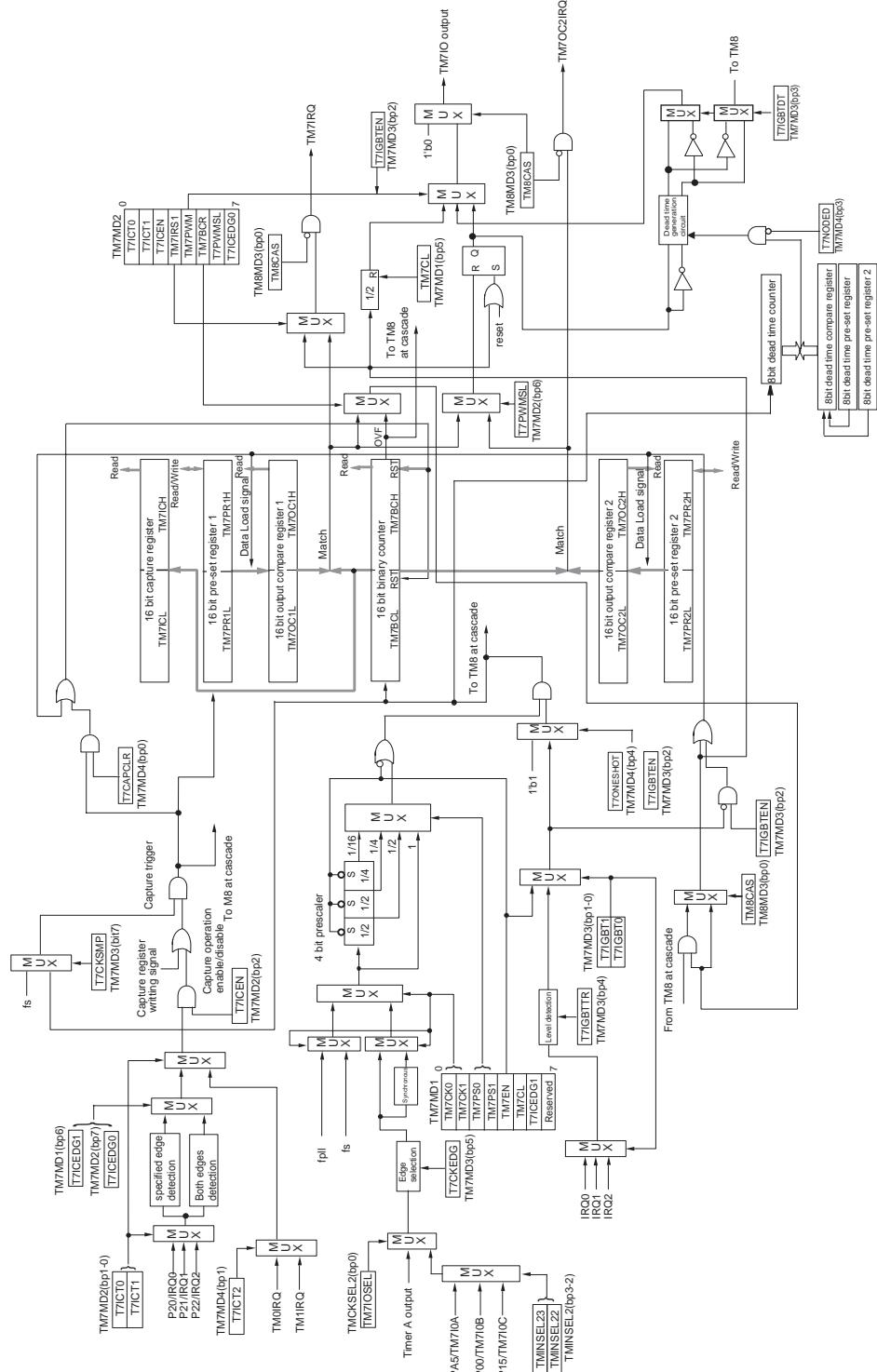


Figure 7.1.1 Timer 7 Block Diagram

■ Timer 8 Block Diagram

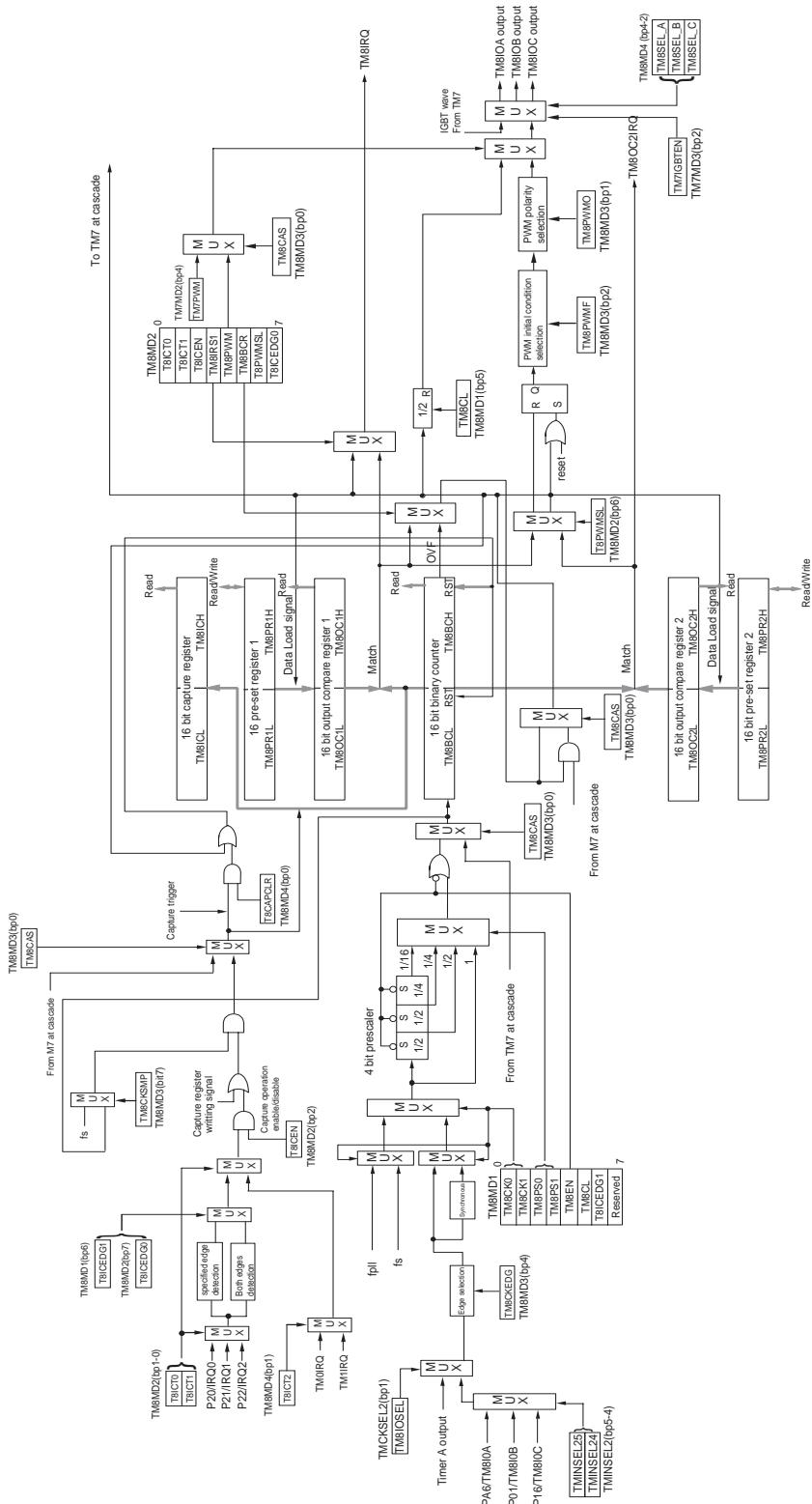


Figure:7.1.2 Timer 8 Block Diagram

■ Timer 9 Block Diagram

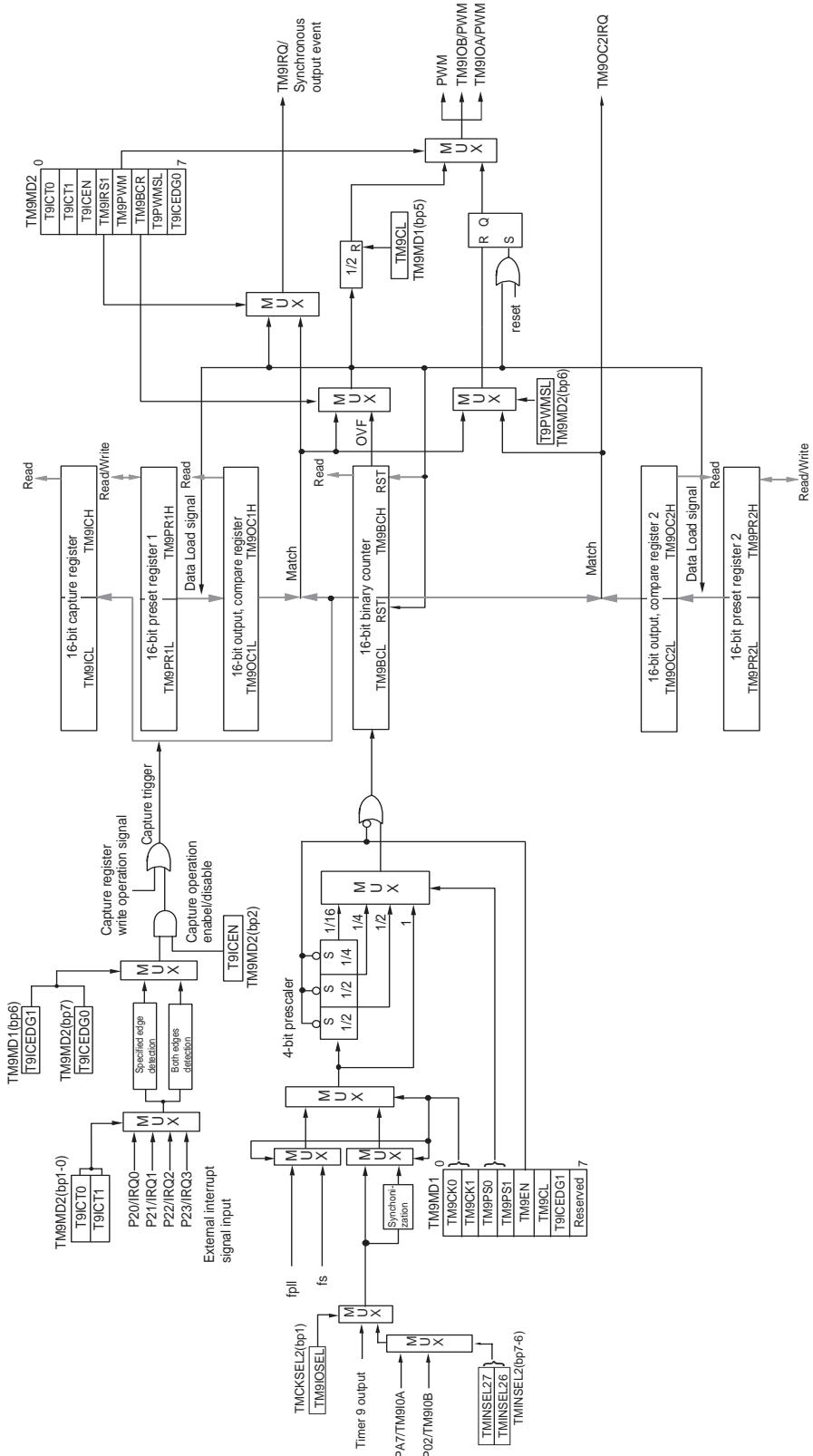


Figure:7.1.3 Timer 9 Block Diagram

7.2 Control Registers

Timer 7 contains the binary counter (TM7BC), the compare register 1 (TM7OC1) with its double buffer preset register 1 (TM7PR1), the compare register 2 (TM7OC2) with its double buffer preset register 2 (TM7PR2), the capture register (TM7IC), the dead time preset register 1 (TM7DPR1) and the dead time preset register 2 (TM7DPR2). Timer 7 is controlled by the mode register 1 (TM7MD1), the mode register 2 (TM7MD2), the mode register 3 (TM7MD3), and the mode register 4 (TM7MD4).

Timer 8 contains the binary counter (TM8BC), the compare register 1 (TM8OC1) with its double buffer preset register 1 (TM8PR1), the compare register 2 (TM8OC2) with its double buffer preset register 2 (TM8PR2) and the capture register (TM8IC). Timer 8 is controlled by the mode register 1 (TM8MD1), the mode register 2 (TM8MD2), the mode register 3 (TM8MD3) and and the mode register 4 (TM8MD4).

Timer 9 contains the binary counter (TM9BC), the compare register 1 (TM9OC1), and its double buffer present register (TM9PR1), the compare register 2 (TM9OC2) and its double buffer preset register 2 (TM9PR2) , the capture register (TM9IC). The mode register 1 (TM9MD1) and mode register 2 (TM9MD2) controls timer 7.

7.2.1 Registers

Table:7.2.1 shows the registers that control timers 7 to 9.

Table:7.2.1 16-bit Timer Control Registers (1/2)

	Register	Address	R/W	Function	Page
Timer 7	TM7BCL	0x03F70	R	Timer 7 binary counter (lower 8 bits)	VII-12
	TM7BCH	0x03F71	R	Timer 7 binary counter (upper 8 bits)	VII-12
	TM7OC1L	0x03F72	R	Timer 7 compare register 1 (lower 8 bits)	VII-10
	TM7OC1H	0x03F73	R	Timer 7 compare register 1 (upper 8 bits)	VII-10
	TM7PR1L	0x03F74	R/W	Timer 7 preset register 1 (lower 8 bits)	VII-11
	TM7PR1H	0x03F75	R/W	Timer 7 preset register 1 (upper 8 bits)	VII-11
	TM7ICL	0x03F76	R	Timer 7 input capture register (lower 8 bits)	VII-12
	TM7ICH	0x03F77	R	Timer 7 input capture register (upper 8 bits)	VII-12
	TM7MD1	0x03F78	R/W	Timer 7 mode register 1	VII-20
	TM7MD2	0x03F79	R/W	Timer 7 mode register 2	VII-21
	TM7OC2L	0x03F7A	R	Timer 7 compare register 2 (lower 8 bits)	VII-10
	TM7OC2H	0x03F7B	R	Timer 7 compare register 2 (upper 8 bits)	VII-10
	TM7PR2L	0x03F7C	R/W	Timer 7 preset register 2 (lower 8 bits)	VII-11
	TM7PR2H	0x03F7D	R/W	Timer 7 preset register 2 (upper 8 bits)	VII-11
	TM7MD3	0x03F8E	R/W	Timer 7 mode register 3	VII-22
	TM7MD4	0x03F6E	R/W	Timer 7 mode register 4	VII-23
Timer 8	TM8BCL	0x03F80	R	Timer 8 binary counter (lower 8 bits)	VII-16
	TM8BCH	0x03F81	R	Timer 8 binary counter (upper 8 bits)	VII-16
	TM8OC1L	0x03F82	R	Timer 8 compare register 1 (lower 8 bits)	VII-14
	TM8OC1H	0x03F83	R	Timer 8 compare register 1 (upper 8 bits)	VII-14
	TM8PR1L	0x03F84	R/W	Timer 8 preset register 1 (lower 8 bits)	VII-15
	TM8PR1H	0x03F85	R/W	Timer 8 preset register 1 (upper 8 bits)	VII-15
	TM8ICL	0x03F86	R	Timer 8 input capture register (lower 8 bits)	VII-16
	TM8ICH	0x03F87	R	Timer 8 input capture register (upper 8 bits)	VII-16
	TM8MD1	0x03F88	R/W	Timer 8 mode register 1	VII-24
	TM8MD2	0x03F89	R/W	Timer 8 mode register 2	VII-25
	TM8OC2L	0x03F8A	R	Timer 8 compare register 2 (lower 8 bits)	VII-14
	TM8OC2H	0x03F8B	R	Timer 8 compare register 2 (upper 8 bits)	VII-14
	TM8PR2L	0x03F8C	R/W	Timer 8 preset register 2 (lower 8 bits)	VII-15
	TM8PR2H	0x03F8D	R/W	Timer 8 preset register 2 (upper 8 bits)	VII-15
	TM8MD3	0x03F8F	R/W	Timer 8 mode register 3	VII-26
	TM8MD4	0x03F6F	R/W	Timer 8 mode register 4	VII-27

	Register	Address	R/W	Function	Page
Timer 9	TM9BCL	0x03E30	R	Timer 9 binary counter (lower 8 bits)	VII-19
	TM9BCH	0x03E31	R	Timer 9 binary counter (upper 8 bits)	VII-19
	TM9OC1L	0x03E32	R	Timer 9 compare register 1 (lower 8 bits)	VII-17
	TM9OC1H	0x03E33	R	Timer 9 compare register 1 (upper 8 bits)	VII-17
	TM9PR1L	0x03E34	R/W	Timer 9 preset register 1 (lower 8 bits)	VII-18
	TM9PR1H	0x03E35	R/W	Timer 9 preset register 1 (upper 8 bits)	VII-18
	TM9ICL	0x03E36	R	Timer 9 input capture register (lower 8 bits)	VII-19
	TM9ICH	0x03E37	R	Timer 9 input capture register (upper 8 bits)	VII-19
	TM9MD1	0x03E38	R/W	Timer 9 mode register 1	VII-28
	TM9MD2	0x03E39	R/W	Timer 9 mode register 2	VII-29
	TM9OC2L	0x03E3A	R	Timer 9 compare register 2 (lower 8 bits)	VII-17
	TM9OC2H	0x03E3B	R	Timer 9 compare register 2 (upper 8 bits)	VII-17
	TM9PR2L	0x03E3C	R/W	Timer 9 preset register 2 (lower 8 bits)	VII-18
	TM9PR2H	0x03E3D	R/W	Timer 9 preset register 2 (upper 8 bits)	VII-18
	TM9MD3	0x03F3E	R/W	Timer 9 mode register 3	VII-30
	TMCKSEL2	0x03E43	R/W	Timer clock selection register 2	VII-31
	TMINSEL2	0x03E45	R/W	Timer input selection register 2	VII-32

7.2.2 Programmable Timer Registers

Timer 7 has a set of 16-bit programmable timer registers, which contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate these registers by 16-bit access.

A compare register is a 16-bit register which stores comparative value of the compare register and the binary counter.

- Timer 7 Compare Register 1 Lower 8 bits (TM7OC1L:0x03F72)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

- Timer 7 Compare Register 1 Upper 8 bits (TM7OC1H:0x03F73)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

- Timer 7 Compare Register 2 Lower 8 bits (TM7OC2L:0x03F7A)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

- Timer 7 Compare Register 2 Upper 8 bits (TM7OC2H:0x03F7B)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Timer 7 preset register 1 and 2 are buffer registers of the compare registers 1, 2 of timer 7. If the set value is written to the timer 7 preset registers 1, 2 when the counting is stopped, the same set value is loaded to the timer 7 compare register. If set value is written to the timer 7 preset registers 1, 2 during counting, the set value of the timer 7 preset registers 1, 2 is loaded to the timer 7 compare registers 1, 2 at the timing that the timer 7 binary counter is cleared. Also, If the set value is written to the timer 7 preset register 1 and 2 during IGBT operation, the set value of the timer 7 preset register is loaded to the timer 7 compare register at the timing that the IGBT is disabled.

■ Timer 7 Preset Register 1 Lower 8 bits (TM7PR1L:0x03F74)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 7 Preset Register 1 Upper 8 bits (TM7PR1H:0x03F75)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 7 Preset Register 2 Lower 8 bits (TM7PR2L:0x03F7C)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 7 Preset Register 2 Upper 8 bits (TM7PR2H:0x03F7D)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

Binary counter is a 16-bit up counter. If any data is written to a preset register 1 when the counting is stopped, the binary counter is cleared to 0x0000. At IGBT setting, when IGBT operation is stopped, the binary counter is cleared to 0x0000. Also, by setting the register, the binary counter is cleared to 0x0000 at capture.

■ Timer 7 Binary Counter Lower 8 bits (TM7BCL:0x03F70)

bp	7	6	5	4	3	2	1	0
Flag	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Binary Counter Upper 8 bits (TM7BCH:0x03F71)

bp	7	6	5	4	3	2	1	0
Flag	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Input capture register is a register that holds the value loaded from a binary counter by a capture trigger. A capture trigger is generated by an input signal from an external interrupt pin, the timer 0 interrupt, the timer 1 interrupt and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disabled.).

■ Timer 7 Input Capture Register Lower 8 bits (TM7ICL;0x03F76)

bp	7	6	5	4	3	2	1	0
Flag	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Input Capture Register Upper 8 bits (TM7ICH;0x03F77)

bp	7	6	5	4	3	2	1	0
Flag	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Dead Time Preset Register 1 (TM7DPR1:0x03F7E)

bp	7	6	5	4	3	2	1	0
Flag	TM7DPR17	TM7DPR16	TM7DPR15	TM7DPR14	TM7DPR13	TM7DPR12	TM7DPR11	TM7DPR10
At reset	0	0	0	0	0	0	0	0
Access	R/W							

■ Timer 7 Dead Time Preset Register 2 (TM7DPR2:0x03F7F)

bp	7	6	5	4	3	2	1	0
Flag	TM7IDPR27	TM7IDPR26	TM7IDPR25	TM7IDPR24	TM7IDPR23	TM7IDPR22	TM7IDPR21	TM7IDPR20
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Timer 8 has a set of 16-bit programmable timer registers, which contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate these registers by 16-bit access.

A compare register is a 16-bit register which stores comparative value of the compare register and the binary counter.

■ Timer 8 Compare register 1 Lower 8 bits (TM8OC1L:0x03F82)

bp	7	6	5	4	3	2	1	0
Flag	TM8OC1L7	TM8OC1L6	TM8OC1L5	TM8OC1L4	TM8OC1L3	TM8OC1L2	TM8OC1L1	TM8OC1L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 8 Compare register 1 Upper 8 bits (TM8OC1H:0x03F83)

bp	7	6	5	4	3	2	1	0
Flag	TM8OC1H7	TM8OC1H6	TM8OC1H5	TM8OC1H4	TM8OC1H3	TM8OC1H2	TM8OC1H1	TM8OC1H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 8 Compare Register 2 Lower 8 bits (TM8OC2L:0x03F8A)

bp	7	6	5	4	3	2	1	0
Flag	TM8OC2L7	TM8OC2L6	TM8OC2L5	TM8OC2L4	TM8OC2L3	TM8OC2L2	TM8OC2L1	TM8OC2L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 8 Compare Register 2 Upper 8 bits (TM8OC2H:0x03F8B)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Timer 8 preset register 1 and 2 are buffer registers of the compare registers 1, 2 of timer 8. If the set value is written to the timer 8 preset registers 1, 2 when the counting is stopped, the same set value is loaded to the timer 7 compare register. If set value is written to the timer 8 preset registers 1, 2 during counting, the set value of the timer 8 preset registers 1, 2 is loaded to the timer 8 compare registers 1, 2 at the timing that the timer 8 binary counter is cleared.

■ Timer 8 Preset Register 1 Lower 8 bits (TM8PR1L:0x03F84)

bp	7	6	5	4	3	2	1	0
Flag	TM8PR1L7	TM8PR1L6	TM8PR1L5	TM8PR1L4	TM8PR1L3	TM8PR1L2	TM8PR1L1	TM8PR1L0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 8 Preset Register 1 Upper 8 bits (TM8PR1H:0x03F85)

bp	7	6	5	4	3	2	1	0
Flag	TM8PR1H7	TM8PR1H6	TM8PR1H5	TM8PR1H4	TM8PR1H3	TM8PR1H2	TM8PR1H1	TM8PR1H0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 8 Preset Register 2 Lower 8 bits (TM8PR2L:0x03F8C)

bp	7	6	5	4	3	2	1	0
Flag	TM8PR2L7	TM8PR2L6	TM8PR2L5	TM8PR2L4	TM8PR2L3	TM8PR2L2	TM8PR2L1	TM8PR2L0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 8 Preset Register 2 Upper 8 bits (TM8PR2H:0x03F8D)

bp	7	6	5	4	3	2	1	0
Flag	TM8PR2H7	TM8PR2H6	TM8PR2H5	TM8PR2H4	TM8PR2H3	TM8PR2H2	TM8PR2H1	TM8PR2H0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

Binary counter is a 16-bit up counter. If any data is written to a preset register 1 when the counting is stopped, the binary counter is cleared to 0x0000. During the timer counting, the binary counter is cleared to 0x0000 at capture by setting the register.

■ Timer 8 Binary Counter Lower 8 bits (TM8BCL:0x03F80)

bp	7	6	5	4	3	2	1	0
Flag	TM8BCL7	TM8BCL6	TM8BCL5	TM8BCL4	TM8BCL3	TM8BCL2	TM8BCL1	TM8BCL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 8 Binary Counter Upper 8 bits (TM8BCH:0x03F81)

bp	7	6	5	4	3	2	1	0
Flag	TM8BCH7	TM8BCH6	TM8BCH5	TM8BCH4	TM8BCH3	TM8BCH2	TM8BCH1	TM8BCH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Input capture register is a register that holds the value loaded from a binary counter by a capture trigger. A capture trigger is generated by an input signal from an external interrupt pin, the timer 0 interrupt, the timer 1 interrupt and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disabled.).

■ Timer 8 Input Capture Register Lower 8 bits (TM8ICL:0x03F86)

bp	7	6	5	4	3	2	1	0
Flag	TM8ICL7	TM8ICL6	TM8ICL5	TM8ICL4	TM8ICL3	TM8ICL2	TM8ICL1	TM8ICL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 8 Input Capture Register Upper 8 bits (TM8ICH:0x03F87)

bp	7	6	5	4	3	2	1	0
Flag	TM8ICH7	TM8ICH6	TM8ICH5	TM8ICH4	TM8ICH3	TM8ICH2	TM8ICH1	TM8ICH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Timer 9 has a set of 16-bit programmable timer registers, which contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate these registers by 16-bit access.

A compare register is a 16-bit register which stores comparative value of the compare register and the binary counter.

■ Timer 9 Compare Register 1 Lower 8 bits (TM9OC1L:0x03E32)

bp	7	6	5	4	3	2	1	0
Flag	TM9OC1L7	TM9OC1L6	TM9OC1L5	TM9OC1L4	TM9OC1L3	TM9OC1L2	TM9OC1L1	TM9OC1L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 9 Compare Register 1 Upper 8 bits (TM9OC1H:0x03E33)

bp	7	6	5	4	3	2	1	0
Flag	TM9OC1H7	TM9OC1H6	TM9OC1H5	TM9OC1H4	TM9OC1H3	TM9OC1H2	TM9OC1H1	TM9OC1H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 9 Compare Register 2 Lower 8 bits (TM9OC2L:0x03E3A)

bp	7	6	5	4	3	2	1	0
Flag	TM9OC2L7	TM9OC2L6	TM9OC2L5	TM9OC2L4	TM9OC2L3	TM9OC2L2	TM9OC2L1	TM9OC2L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 9 Compare Register 2 Upper 8 bits (TM9OC2H:0x03E3B)

bp	7	6	5	4	3	2	1	0
Flag	TM9OC2H7	TM9OC2H6	TM9OC2H5	TM9OC2H4	TM9OC2H3	TM9OC2H2	TM9OC2H1	TM9OC2H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Timer 9 preset registers 1 and 2 are buffer registers of the compare registers 1 and 2 of timer 9. If the set values are written to the timer 9 preset registers 1 and 2 when the counting is stopped, the same set values are loaded to the timer 9 compare register. If the set values are written to the timer 9 preset registers 1 and 2 during counting, the set values of the timer 9 preset registers 1 and 2 are loaded to the timer 9 compare registers 1 and 2 at the timing that the timer 9 binary counter is cleared.

■ Timer 9 Preset Register 1 Lower 8 bits (TM9PR1L:0x03E34)

bp	7	6	5	4	3	2	1	0
Flag	TM9PR1L7	TM9PR1L6	TM9PR1L5	TM9PR1L4	TM9PR1L3	TM9PR1L2	TM9PR1L1	TM9PR1L0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 9 Preset Register 1 Upper 8 bits (TM9PR1H:0x03E35)

bp	7	6	5	4	3	2	1	0
Flag	TM9PR1H7	TM9PR1H6	TM9PR1H5	TM9PR1H4	TM9PR1H3	TM9PR1H2	TM9PR1H1	TM9PR1H0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 9 Preset Register 2 Lower 8 bits (TM9PR2L:0x03E3C)

bp	7	6	5	4	3	2	1	0
Flag	TM9PR2L7	TM9PR2L6	TM9PR2L5	TM9PR2L4	TM9PR2L3	TM9PR2L2	TM9PR2L1	TM9PR2L0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

■ Timer 9 Preset Register 2 Upper 8 bits (TM9PR2H:0x03E3D)

bp	7	6	5	4	3	2	1	0
Flag	TM9PR2H7	TM9PR2H6	TM9PR2H5	TM9PR2H4	TM9PR2H3	TM9PR2H2	TM9PR2H1	TM9PR2H0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

Binary counter is a 16-bit up counter. If any data is written to a preset register 1 when the counting is stopped, the binary counter is cleared to 0x0000.

■ Timer 9 Binary Counter Lower 8 bits (TM9BCL:0x03E30)

bp	7	6	5	4	3	2	1	0
Flag	TM9BCL7	TM9BCL6	TM9BCL5	TM9BCL4	TM9BCL3	TM9BCL2	TM9BCL1	TM9BCL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 9 Binary Counter Upper 8 bits (TM9BCH:0x03E31)

bp	7	6	5	4	3	2	1	0
Flag	TM9BCH7	TM9BCH6	TM9BCH5	TM9BCH4	TM9BCH3	TM9BCH2	TM9BCH1	TM9BCH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Input capture register is a register that holds the value loaded from a binary counter by a capture trigger. A capture trigger is generated by an input signal from an external interrupt pin, and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disabled.).

■ Timer 9 Input Capture Register Lower 8 bits (TM9ICL:0x03E36)

bp	7	6	5	4	3	2	1	0
Flag	TM9ICL7	TM9ICL6	TM9ICL5	TM9ICL4	TM9ICL3	TM9ICL2	TM9ICL1	TM9ICL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 9 Input Capture Register Upper 8 bits (TM9ICH:0x03E37)

bp	7	6	5	4	3	2	1	0
Flag	TM9ICH7	TM9ICH6	TM9ICH5	TM9ICH4	TM9ICH3	TM9ICH2	TM9ICH1	TM9ICH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

7.2.3 Timer Mode Registers

This is a readable/writable register that controls timer 7.

■ Timer 7 Mode Register 1 (TM7MD1:0x03F78)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	T7ICEDG1	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0
At reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0". *
6	T7ICEDG1	Capture trigger edge selection 0:Falling edge 1:Rising edge
5	TM7CL	Timer output reset signal 0:Operate timer output 1:Disable timer output (reset)
4	TM7EN	Timer count control 0:Halt the count 1:Operate the count
3-2	TM7PS1-0	Count clock selection 00:1/1 of clock 01:1/2 of clock 10:1/4 of clock 11:1/16 of clock
1-0	TM7CK1-0	Clock source selection 00:fpll 01:fs 10:TMIO input 11:Synchronous TMIO input



Always set "0" to the bp denoted by *.

■ Timer 7 Mode Register 2 (TM7MD2:0x03F79)

bp	7	6	5	4	3	2	1	0
Flag	T7ICEDG0	T7PWMSL	TM7BCR	TM7PWM	TM7IRS1	T7ICEN	T7ICT1	T7ICT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	T7ICEDG0	Capture trigger edge selection 0:Select the both edges 1:Select the specified edge
6	T7PWMSL	PWM mode selection 0:Set duty by OC1 1:Set duty by OC2
5	TM7BCR	Timer 7 count clear factor selection 0:Full count OVF 1:Match of BC and OC1
4	TM7PWM	Timer output waveform selection 0:Output timer 1:Output PWM
3	TM7IRS1	Timer 7 interrupt factor selection 0:Counter clear 1:Match of BC and OC1
2	T7ICEN	Input capture operation enable select flag 0:Disable capture operation 1:Enable capture operation
1-0	T7ICT1-0	Capture trigger selection 00:External interrupt 0 input signal 01:External interrupt 1 input signal 10:External interrupt 2 input signal 11:Timer interrupt

■ Timer 7 Mode Register 3 (TM7MD3:0x03F8E)

bp	7	6	5	4	3	2	1	0
Flag	TM7CKSMP	TM7BUFSEL	TM7CKEDG	T7IGBTTR	T7IGBDT	T7IGBTEN	T7IGBT1	T7IGBT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	TM7CKSMP	Capture sampling selection 0:Count clock 1:fs
6	TM7BUFSEL	TM7OC1,2 buffer selection 0:Double buffer 1:Single buffer
5	TM7CKEDG	TM7IO count edge selection 0:Falling edge 1:Both edges
4	T7IGBTTR	IGBT trigger level selection 0:H 1:L
3	T7IGBDT	IGBT dead time insert timing 0:Falling edge standard 1:Rising edge standard
2	T7IGBTEN	IGBT operation enable 0:Disable 1:Enable
1-0	T7IGBT1-0	IGBT/timer startup factor selection 00:Timer 7 count operation 01:External interrupt 0 input signal 10:External interrupt 1 input signal 11:External interrupt 2 input signal



When IGBT is not selected, set as
T7IGBTEN=0
T7IGBT1-0=00

■ Timer 7 Mode Register 4 (TM7MD4:0x03F6E)

bp	7	6	5	4	3	2	1	0
Flag	T7TRGACT	T7IGBTSFT	T7IGBTCNT	T7ONESHOT	T7NODED	-	T7ICT2	T7CAPCLR
At reset	0	0	0	0	0	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W

bp	Flag	Description
7	T7TRGACT	Trigger reception flag of IGBT active outputting 0:Enable 1:Disable
6	T7IGBTSFT	IGBT software startup flag 0:Halt 1:Enable
5	T7IGBTCNT	BC operation when disable IGBT is invalid 0:Halt 1:Operated
4	T7ONESHOT	One shot pulse selection 0:Continuous pulse 1:One shot pulse
3	T7NODED	Dead time selection 0:With dead time 1:Without dead time
2	-	-
1	T7ICT2	Capture trigger selection 0:Timer 0 interrupt 1:Timer 1 interrupt
0	T7CAPCLR	BC clearance at capture 0:Unclear 1:Clear



T7CAPCLR flag is effective when timer is operating. The binary counter is uncleared when capturing at timer stop.

This is a readable/writable register that controls timer 8.

■ Timer 8 Mode Register 1 (TM8MD1:0x03F88)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	T8ICEDG1	TM8CL	TM8EN	TM8PS1	TM8PS0	TM8CK1	TM8CK0
At reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0" *
6	T8ICEDG1	Capture trigger edge selection 0:Falling edge 1:Rising edge
5	TM8CL	Timer output reset signal 0:Operate timer output 1:Disable timer output (reset)
4	TM8EN	Timer count control 0:Halt the count 1:Operate the count
3-2	TM8PS1-0	Count clock selection 00:1/1 of clock 01:1/2 of clock 10:1/4 of clock 11:1/16 of clock
1-0	TM8CK1-0	Clock source selection 00:fpll 01:fs 10:TMIO input 11:Synchronous TMIO input



Always set "0" to the bp denoted by *.

■ Timer 8 Mode Register 2 (TM8MD2:0x03F89)

bp	7	6	5	4	3	2	1	0
Flag	T8ICEDG0	TM8PWMSL	TM8BCR	TM8PWM	TM8IRS1	TM8ICEN	T8ICT1	T8ICT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	T8ICEDG0	Capture trigger edge selection 0:Select the both edges 1:Select the specified edge
6	TM8PWMSL	PWM mode selection 0:Set duty by OC1 1:Set duty by OC2
5	TM8BCR	Timer 8 count clear factor selection 0:Full count OVF 1:Match of BC and OC1
4	TM8PWM	Timer output waveform selection 0:Output timer 1:Output PWM
3	TM8IRS1	Timer 8 interrupt factor selection 0:Counter clear 1:Match of BC and OC1
2	T8ICEN	Input capture operation enable select flag 0:Disable capture operation 1:Enable capture operation
1-0	T8ICT1-0	Capture trigger selection 00:External interrupt 0 input signal 01:External interrupt 1 input signal 10:External interrupt 2 input signal 11:Timer interrupt

■ Timer 8 Mode Register 3 (TM8MD3:0x03F8F)

bp	7	6	5	4	3	2	1	0
Flag	TM8CKSMP	TM8BUFSEL	-	TM8CKEDG	-	TM8PWMF	TM8PWMO	TM8CAS
At reset	0	0	-	0	-	0	0	0
Access	R/W	R/W	-	R/W	-	R/W	R/W	R/W

bp	Flag	Description
7	TM8CKSMP	Capture sampling selection 0:Count clock 1:fs
6	TM8BUFSEL	TM8OC1, 2 buffer selection 0:Double buffer 1:Single buffer
5	-	-
4	TM8CKEDG	Timer 8 count edge selection 0:Falling edge 1:Both edges
3	-	-
2	TM8PWMF	PWM output selection at timer 8 stopped 0:L 1:H
1	TM8PWMO	Timer 8 PWM output polarity selection 0:Normal turn 1:Reverse turn
0	TM8CAS	Cascade selection 0:Timer 7, timer 8 independence 1:Timer 7, timer 8 cascade

■ Timer 8 Mode Register 4 (TM8MD4:0x03F6F)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	Reserved	Reserved	TM8SEL_C	TM8SEL_B	TM8SEL_A	T8ICT2	T8CAPCLR
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	Reserved	Always set to "0".
4	TM8SEL_C	Port C selection 0:Timer 8 output 1:IGBT output
3	TM8SEL_B	Port B selection 0:Timer 8 output 1:IGBT output
2	TM8SEL_A	Port A selection 0:Timer 8 output 1:IGBT output
1	T8ICT2	Capture trigger selection 0:Timer 0 interrupt 1:Timer 1 interrupt
0	T8CAPCLR	BC clearance at capture 0:Unclear 1:Clear



T8CAPCLR flag is effective when timer is operating. The binary counter is uncleared when capturing at timer stop.



Always set "0" to the bp denoted by *.

This is a readable/writable register that controls timer 9.

■ Timer 9 Mode Register 1 (TM9MD1:0x03E38)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	T9ICEDG1	TM9CL	TM9EN	TM9PS1	TM9PS0	TM9CK1	TM9CK0
At reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Always set to "0". *
6	T9ICEDG1	Capture trigger edge selection 0:Falling edge 1:Rising edge
5	TM9CL	Timer output reset signal 0:Operate timer output 1:Disable timer output (reset)
4	TM9EN	Timer count control 0:Halt the count 1:Operate the count
3-2	TM9PS1-0	Count clock selection 00:1/1 of clock 01:1/2 of clock 10:1/4 of clock 11:1/16 of clock
1-0	TM9CK1-0	Clock source selection 00:fpll 01:fs 10:TMIO input 11:Synchronous TMIO input



Always set "0" to the bp denoted by *.

■ Timer 9 Mode Register 2 (TM8MD2:0x03E39)

bp	7	6	5	4	3	2	1	0
Flag	T9ICEDG0	T9PWMSL	TM9BCR	TM9PWM	TM9IRS1	T9ICEN	T9ICT1	T9ICT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	T9ICEDG0	Capture trigger edge selection 0:Select the both edges 1:Select the specified edge
6	TM9PWMSL	PWM mode selection 0:Set duty by OC1 1:Set duty by OC2
5	TM9BCR	Timer count clear factor selection 0:Full count OVF 1:Match of BC and OC1
4	TM9PWM	Timer output waveform selection 0:Output timer 1:Output PWM
3	TM9IRS1	Timer interrupt factor selection 0:Counter clear 1:Match of BC and OC1
2	T9ICEN	Input capture operation enable selection 0:Disable capture operation 1:Enable capture operation
1-0	T9ICT1-0	Capture trigger selection 00:External interrupt 0 input signal 01:External interrupt 1 input signal 10:External interrupt 2 input signal 11:External interrupt 3 input signal

■ Timer 9 Mode Register 3 (TM9MD3:0x03E3E)

bp	7	6	5	4	3	2	1	0
Flag	TM9CKSMP	-	-	-	-	-	-	-
At reset	0	-	-	-	-	-	-	-
Access	R/W	-	-	-	-	-	-	-

bp	Flag	Description
7	TM9CKSMP	Input capture sampling selection 0:Count clock 1:fs
6-0	-	-

■ Timer Clock Selection Register 2 (TMCKSEL2: 0x03E43)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM9IOSEL	TM8IOSEL	TM7IOSEL
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2	TM9IOSEL	Timer 9 input selection 0: External input 1: Timer A output
1	TM8IOSEL	Timer 8 input selection 0: External input 1: Timer A output
0	TM7IOSEL	Timer 7 input selection 0: External input 1: Timer A output

■ Timer Input Selection Register 2 (TMINSEL2: 0x03E45)

bp	7	6	5	4	3	2	1	0
Flag	TMINSEL27	TMINSEL26	TMINSEL25	TMINSEL24	TMINSEL23	TMINSEL22	TMINSEL21	TMINSEL20
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7-6	TMINSEL27-6	Timer 9 input selection (at port selection) 00:TM9IOA(PA7) 01:TM9IOB(P02) 10:Prohibited 11:Prohibited
5-4	TMINSEL25-4	Timer 8 input selection (at port selection) 00:TM8IOA(PA6) 01:TM8IOB(P01) 10:TM8IOC(P16) 11:Prohibited
3-2	TMINSEL23-2	Timer 7 input selection (at port selection) 00:TM7IOA(PA5) 01:TM7IOB(P00) 10:TM7IOC(P15) 11:Prohibited
1-0	TMINSEL21-0	Timer 4 input selection (at port selection) 00:TM4IOA(PA4) 01:TM4IOB(P64) 10:TM4IOC(P14) 11:Remote control career input (from the inside)

7.3 Operation

7.3.1 Operation

The timer operation can constantly generate interrupts.

■ 16-bit Timer Operation (Timers 7, 8 and 9)

The generation cycle of an timer interrupt is set by the clock source selection and the set value of the compare register 1 (TMnOC1), in advance. When the binary counter (TMnBC) reaches the set value of the compare register 1, an interrupt is generated at the next count clock. There are 2 sources to be selected to clear the binary counter; the TMnOC1 compare match and the full count overflow. After the binary counter is cleared, the counting up is restarted from 0x0000.

Table:7.3.1 16-bit Timer Interrupt Source and Binary Counter Clear Source (Timers 7, 8 and 9)

TM7MD2 register		Interrupt source	Binary counter clear source
TM7IRS1 flag	TM7BCR flag		
1	1	TM7OC1 compare match	TM7OC1 compare match
0	1	TM7OC1 compare match	TM7OC1 compare match
1	0	TM7OC1 compare match	Full count overflow
0	0	Full count overflow	Full count overflow
TM8MD2 register		Interrupt source	Binary counter clear source
TM8IRS1 flag	TM8BCR flag		
1	1	TM8OC1 compare match	TM8OC1 compare match
0	1	TM8OC1 compare match	TM8OC1 compare match
1	0	TM8OC1 compare match	Full count overflow
0	0	Full count overflow	Full count overflow
TM9MD2 register		Interrupt source	Binary counter clear source
TM9IRS1 flag	TM9BCR flag		
1	1	TM9OC1 compare match	TM9OC1 compare match
0	1	TM9OC1 compare match	TM9OC1 compare match
1	0	TM9OC1 compare match	Full count overflow
0	0	Full count overflow	Full count overflow

Timer n can generate another set of an independent interrupt (timer n compare register 2 match interrupt) by the set value of the timer n compare register 2 (TMnOC2). At the time of the interrupt, the binary counter is cleared as the above setup.

The compare register is double buffer type. So, when the value of the preset registers is changed during the counting, the changed value is stored to the compare register when the binary counter is cleared. This function can change the compare register value constantly, without disturbing the cycle during timer operation (Reload function).



When the CPU reads the 16-bit binary counter (TMnBC), the read data is handled in 8-bits units even if it is a 16-bit MOVW instruction. As a result, it will read the data incorrectly if a carry from the lower 8 bits to the upper 8 bits occurs during counting operation.

To read the correct value of the 16-bit counting (TMnBC), use the writing program function to the input capture register (TMnIC). By writing to the TMnIC, the counting data of TMnBC can be stored to TMnIC to read out the correct counting value during timer operation.

[Chapter 7.9.1. Operation]



To count properly, do not switch the count clock on the timer operation. To switch the count clock, stop the timer operation.



Set the timer n mode register when the TMnEN flag of the TMnMD1 register is set to "0" to stop counting.



When changing CPU operation mode (NORMAL mode to SLOW mode) at selecting the high oscillation clock (fpll) for the clock source, stop the timer operation before the transition to the operation mode, set it again after the transition to the mode to operate the timer.

And in SLOW/HALT1 mode, do not select the high oscillation clock (fpll) for the clock source.

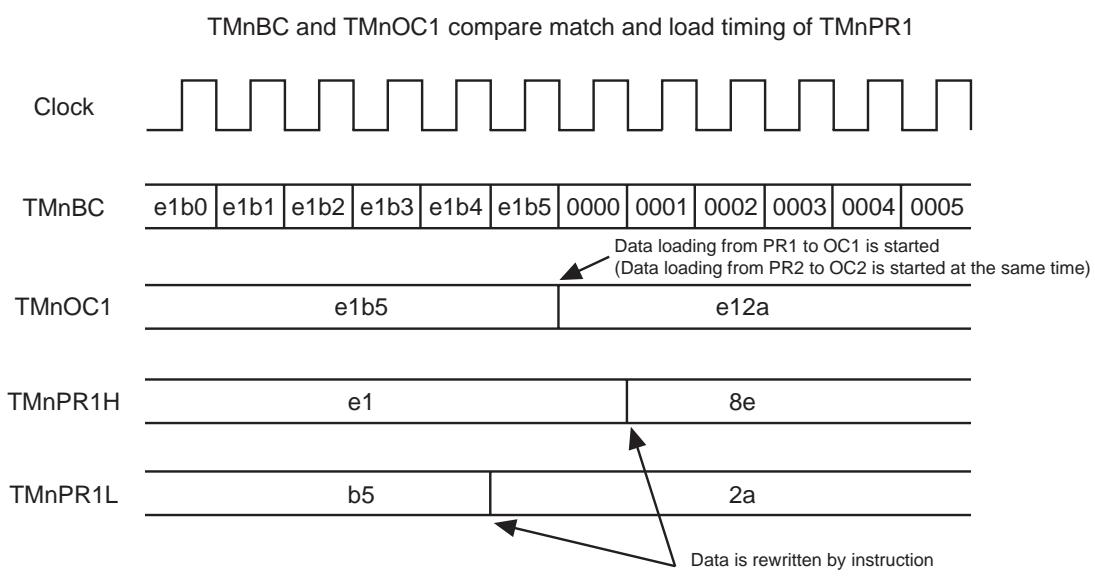


When a data is written to 16-bit timer preset register (TMnPR1, TMnPR2), it is recognized as a 8-bit unit data inside LSI even if it is a 16-bit access MOVW instruction.

After lower 8 bits of preset register is written, if data loading from preset register to compare register (TMnOC1, TMnOC2) is started before the upper 8bits is written, data which is not written is loaded to the upper 8bits and rewritten data is loaded to the lower 8bits.

Therefore, writing data to the preset register (TMnPR1, TMnPR2) need to be completed before data loading from the preset register to the compare register is started.

The following chart is the timing of rewriting and loading of TMnPR1 and TMnOC1. Moreover, when it writes in TMnPR2, it may load the incorrect data to TMnOC2 in the same way.



Data e12a is loaded to OC1 as PR1 writing ($e1b5 \rightarrow 8e2a$) and loading to OC1 are operated at the same time.

Table:7.3.2shows the clock source that can be selected.

Table:7.3.2 Clock Source at Timer Operation (Timers 7, 8 and 9)

Clock source	1 count time
fpll	100 ns
fpll/2	200 ns
fpll/4	400 ns
fpll/16	1.6 μ s
fs	200 ns
fs/2	400 ns
fs/4	800 ns
fs/16	3.2 μ s
fpll=10 MHz (PLL not used) fs=fpll/2=5 MHz	

■ Count Timing of Timer Operation (Timers 7, 8 and 9)

The binary counter counts up with the selected clock source as the count clock. The basic operation of whole 16-bit timer functions is as below.

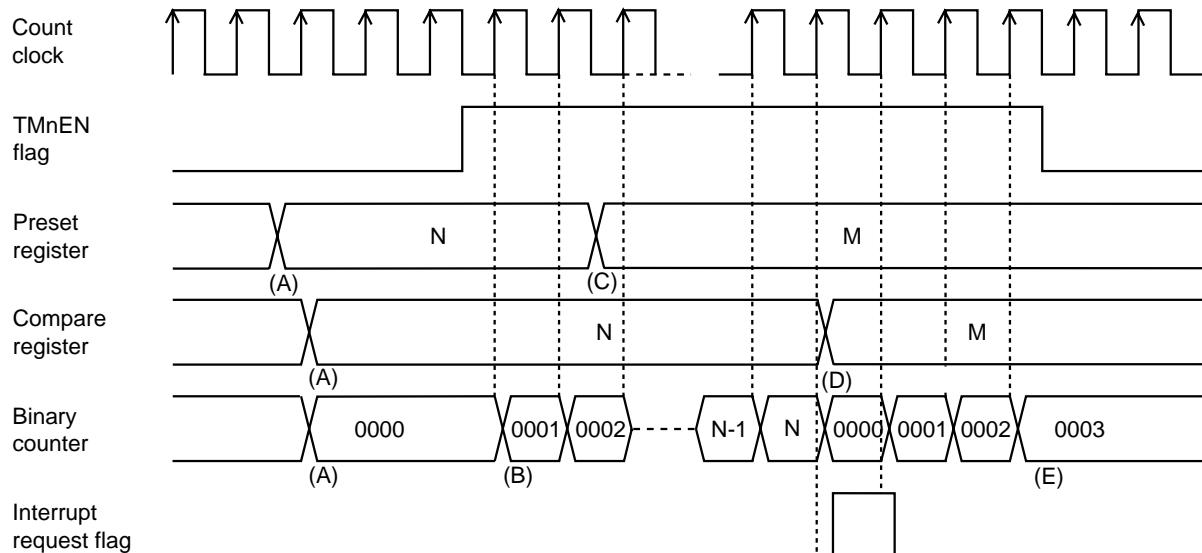


Figure:7.3.1 Count Timing of Timer Operation (Timers 7, 8 and 9)

(A)When a data is written to the preset register while the TMnEN flag is stopped (“0”), the same value is loaded during the writing cycle and the binary counter is cleared to 0x0000.

(B)When TMnEN flag is (“1”), the binary counter starts counting. The counting starts at the rising edge of the count clock.

(C)Even if the preset register is rewritten when the TMnEN flag is (“1”), the binary counter is not changed.

(D)When the binary counter reaches value of compare register 1, the set value of the preset register is loaded to the compare register at the next count clock. And the interrupt request flag is set at the next count clock, and the binary counter is cleared to 0x0000 to restart counting up.

(E)When the TMnEN flag is (“0”), the binary counter is stopped.



When the binary counter reaches the value of the compare register, the interrupt request flag is set to the next count clock, and the binary counter is cleared. So, set the compare register as:

(the set value of the compare register) = (the counts till the interrupt generation-1)
However, if "00" is specified for the compare register, an interrupt timing is the same as if you set it to "01".



Up to 3 system clock is needed till the next interrupt request flag generated. During the period, an interrupt request flag is not generated at compare match.



When the timer n compare register 2 match interrupt is generated and TMnOC1 compare match is selected as a binary counter clear source, the set value of the compare register 2 should be smaller than the set value of the compare register 1.



There is a possibility that the timer interrupt request flag has already been set before the timer is started, clear the timer interrupt request flag.



When the binary counter is used as a free-counter that counts 0x0000 to 0xFFFF, set 0xFFFF to the compare register 1 or set the TMnBCR flag of the TMnMD2 register to "0".



The TMnEN flag of the TMnMD register is not changed with other bits. There a possibility of malfunctioning.



Set up 16-bit timer counter clock should be done when the timer interrupt is disabled.



When the binary counter is read out on the timer operation, it is regarded as the data by 8 bits unit in LSI. So, when the digit is raised from lower 8 bits to upper 8 bits, correct value cannot be read out.

Stop the timer to read out the correct value.

7.3.2 Setup Example

■ Timer Operation Setup Example

Timer 7 generates an interrupt constantly for timer function. fpll/2 (fpll=10 MHz at operation) is selected as a clock source to generate an interrupt every 1000 cycles (200 µs).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to “0” to stop the timer 7 counting.
(2) Disable the interrupt TM7ICR(0x03FEF) bp1:TM7IE =0	(2) Set the TM7IE flag of the TM7ICR register to “0” to disable the interrupt.
(3) Select the timer clear source TM7MD2(0x03F79) bp5:TM7BCR =1	(3) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to “1” to select the compare match to the binary counter clear source.
(4) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =01	(4) Select fpll to the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Besides, select 1/2 fpll to the count clock source by the TM7PS1 to 0 flag.
(5) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0=00	(5) Set IGBT/timer startup factor to timer 7 count operation.
(6) Set the interrupt generation cycle TM7PR1(0x03F75,0x03F74) =0x03E7	(6) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The cycle is 1000. The set value should be 1000-1=999 (0x03E7). At the time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(7) Set the interrupt level TM7ICR(0x03FEF) bp7-6:TM7LV1-0 =10	(7) Set the interrupt level by the TM7LV1 to 0 flag of the timer 7 interrupt control register (TM7ICR). If the interrupt request flag is already set, clear the request flag. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(8) Enable the interrupt TM7ICR (0x03FEF) bp1:TM7IE =1	(8) Set the TM7IE flag of the TM7ICR register to “1” to enable the interrupt.
(9) Start the timer operation TM7MD1 (0x03F78) bp4:TM7EN =1	(9) Set the TM7EN flag of the TM7MD1 register to “1” to operate the timer 7.

TM7BC counts up from 0x0000. When TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock and the TM7BC becomes 0x0000 and counts up again.

7.4 16-bit Event Count

7.4.1 Operation

Event count operation has 2 types; TMnIO input and synchronous TMnIO input. These can be selected as the count clock. Each type can select 1/1, 1/2, 1/4, or 1/16 as a count clock source. Also, it is possible to select the count edge. (the falling edge and the both edge at the normal operation are selectable)

■ 16-bit Event Count Operation (Timers 7, 8 and 9)

The binary counter (TMnBC) counts the external signal input to the TMnIO pin. If the binary counter reaches the set value of the compare register (TMnOC), an interrupt can be generated at the next count clock.

Table:7.4.1

	Timer 7	Timer 8	Timer 9
Event input	TM7IOA input/ TM7IOB input/ TM7IOC input	TM8IOA input/ TM8IOB input/ TM8IOC input	TM9IOA input/ TM9IOB input
	Synchronous TM7IO input	Synchronous TM8IO input	Synchronous TM9IO input

■ Count Timing of TMnIO Input (Timers 7, 8 and 9)

When TMnIO input is selected, TMnIO input signal is input to the timer n count clock. The binary counter counts up at the falling edge of the TMnIO input signal or TMnIO input signal that passed the divider.

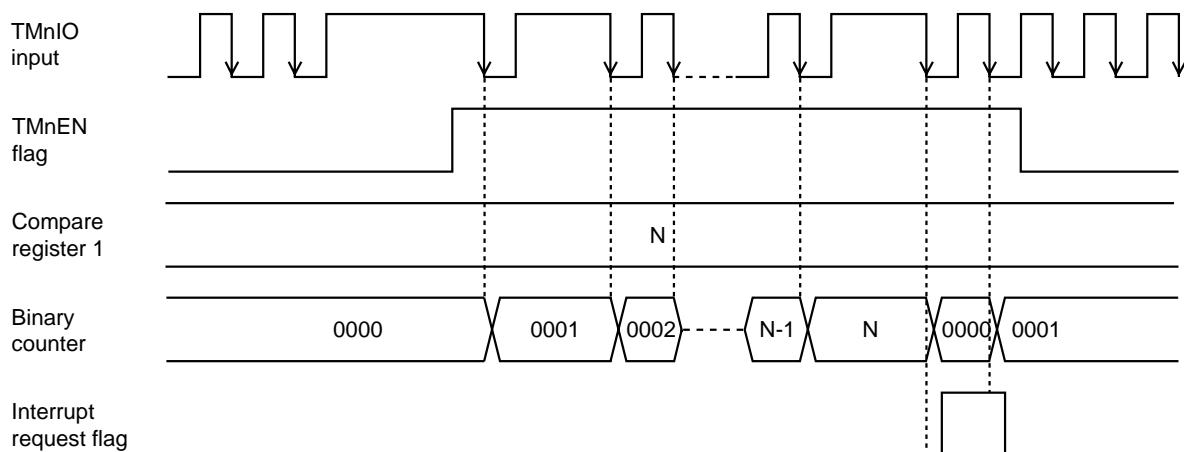


Figure:7.4.1 Count Timing TMnIO Input (Timers 7, 8 and 9)



If the event input (TMnIO input) is selected by count clock source, don't read out the value of timer n binary counter. If read out the value of timer n binary counter, use the event count by the synchronous TMnIO input / the synchronous IRQ2 input / the synchronous IRQ3 input, which is shown in the following page.



When using TMnIO input, after selecting fs as the count clock first, then set each mode register and preset register. After that, operate the timer on selecting TMnIO input. Do not write any data to the preset register on the operation. Only TMnIO input can recover from STOP mode in 16-bit timer.



When using the event input (TMnIO input), clear the binary counter before starting the timer operation. Also, when setting 0x0000 to the compare register, use the event count by TMnIO input which is shown below.



When the event input (TMnIO input) is selected as the count clock source, even if the set value is written to the preset register at the timer stop, the same set value may not be loaded to the compare register. To prevent this, select the system clock (fs) for the count clock source once, write the set value to the preset register, then select the event input (TMnIO) as the clock source to start the timer operation.



When the event input (TMnIO) input is selected as the count clock source, all pins from TMnIOA to TMnIOC are input mode. Therefore the procedure such as pull-up is required in order not to input midpoint potential to unused pins.

■ Count Timing of Synchronous TMnIO Input (Timers 7, 8 and 9)

If the synchronous TMnIO input is selected, the synchronizing circuit output signal is input to the timer n count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TMnIO input signal is changed. The binary counter counts up at the rising edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the division circuit.

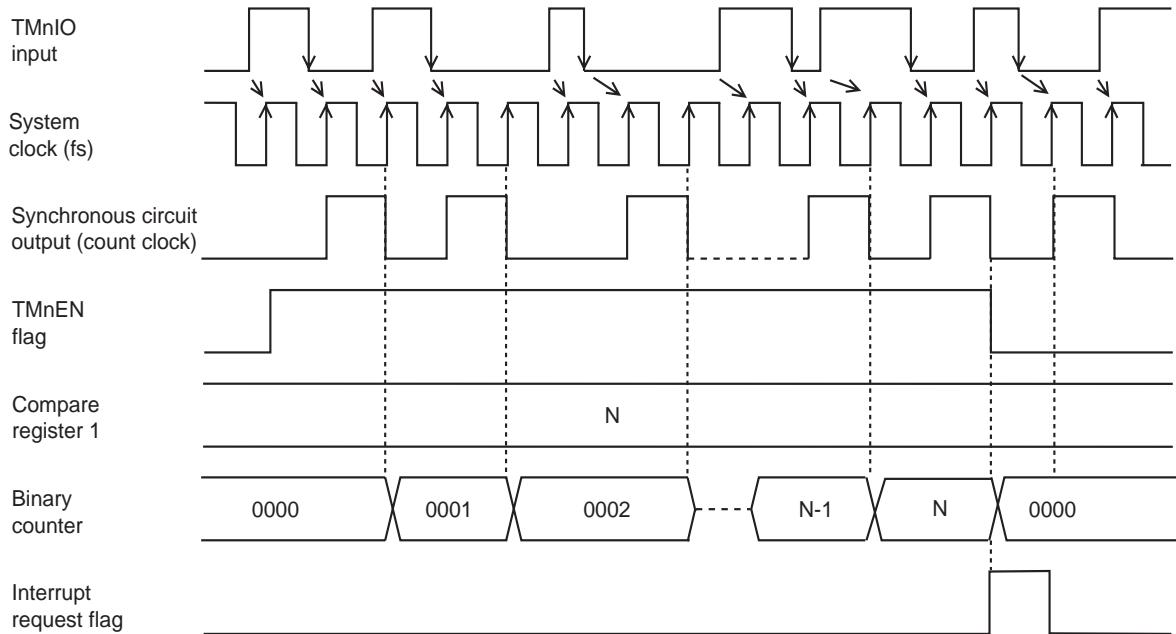


Figure:7.4.2 Count Timing of Synchronous TMnIO Input (Timers 7, 8 and 9)



The timer n binary counter counts up the binary counter at the signal in synchronization with the system clock so that correct value is read out from the timer n binary counter.



Input from TMnIO should be used to a waveform, which has 2 times and over cycles of system clock (fs). If less than the above waveforms are input, it may not be counted correctly.

■ Count Timing of TMnIO Input (Both edges selected)

When TMnIO input is selected, TMnIO input signal is input to the timer n count clock. The binary counter counts up at the falling edge of the TMnIO input signal or TMnIO input signal that passed the divider.

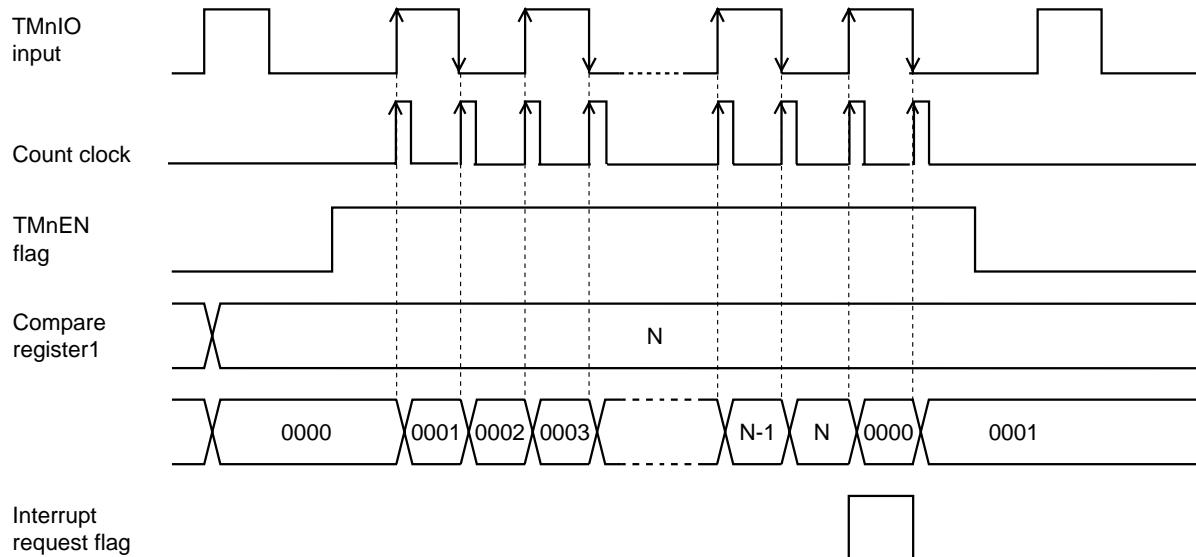


Figure:7.4.3 Count Timing TMnIO Input (Timers 7, 8 and 9)



When both edges are selected, they are counted only at the normal operation (high-speed oscillation). Input from TMnIO should be done the waveform which has more than 2 times cycle than fpll (when duty ratio is 50%). If the waveform which has less cycle is input, it may not be counted correctly.

7.4.2 Setup Example

■ Event Count Setup Example

When the falling edge of the TM7IO input pin signal is detected 5 times using timer 7, an interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM7MD1 (0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop the timer 7 counting.
(2) Disable the interrupt TM7ICR(0x03FEF) bp1:TM7IE =0	(2) Set the TM7IE flag of the TM7ICR register to "0" to disable the interrupt.
(3) Select the timer clock TMCKSEL2(0x03F43) bp0 :TM7IOSEL =0	(3) Select the external input by setting the TM7IOSEL flag of the timer clock selection register 2 (TMCKSEL2) to "0".
(4) Select the timer input TMINSEL2(0x03E45) bp3-2 :TMINSEL23-2 =10	(4) Set P15 to timer input by setting the TMINSEL23 to 2 flags of the timer input selection register 2 (TMINSEL2) to "10".
(5) Set the special function pin to input PADIR (0x03F3A) bp5:PADIR5 =0	(5) Set the PADIR5 flag of the port A direction control register (PADIR) to "0" to set PA5 pin to the input mode. Add pull-up/pull-down resistor, if necessary. [Chapter 4 I/O Ports]
(6) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =01 bp3-2:TM7PS1-0 =00	(6) Select fs to the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Besides, select 1/1 to the count clock source by the TM7PS1 to 0 flag.
(7) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0=00	(7) Set IGBT/timer startup factor to timer 7 count operation.
(8) Set the interrupt generation cycle TM7PR1(0x03F75,0x03F74) =0x0004	(8) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The set value should be 4, because the counting is 5 times. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(9) Select the timer clear source TM7MD2 (0x03F79) bp5:TM7BCR =1	(9) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a binary counter clear source.

Setup Procedure	Description
(10) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0 =10 bp3-2:TM7PS1-0 =00	(10) Select TM7IO to the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Besides, select 1/1(no dividing) to the count clock source by the TM7PS1 to 0 flag.
(11) Set the interrupt level TM7ICR (0x03FEF) bp7-6:TM7LV1-0 =10	(11) Set the interrupt level by the TM7LV1 to 0 flag of the timer 7 interrupt control register (TM7ICR). If the interrupt request flag is already set, clear the request flag. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(12) Enable the interrupt TM7ICR (0x03FEF) bp1:TM7IE =1	(12) Set the TM7IE flag of the TM7ICR register to "1" to enable the interrupt.
(13) Start the event count TM7MD1 (0x03F78) bp4:TM7EN =1	(13) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

Every time TM7BC reaches the falling edge of the TM7IO input, it counts up from 0x0000. When the TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock, and the value of TM7BC becomes 0x0000 to restart counting up.

Allow the setup procedures (6) to (10) to have the correct operation.

7.5 16-bit Timer Pulse Output

7.5.1 Operation

TM_nIO pin can output a pulse signal with a arbitrary frequency.

■ 16-bit Timer Pulse Output Operation (Timers 7, 8 and 9)

These timers can output $2 \times$ cycle signal, compared with the set value of the compare register 1 (TM_nOC1) and the 16-bit full count. Output pins are as follows.

Table:7.5.1 Timer Pulse Output Pin

	Timer 7	Timer 8	Timer 9
Pulse output pin	TM7IOA output/ TM7IOB output/ TM7IOC output	TM8IOA output/ TM8IOB output/ TM8IOC output	TM9IOA output/ TM9IOB output

Table:7.5.2 shows the timer interrupt generation sources and the flags that control the timer pulse output cycle.

Table:7.5.2 16-bit Timer Interrupt Generation Source and Timer Pulse Output Cycle (Timers 7, 8 and 9)

TM7MD2 register		Interrupt source	Timer pulse output cycle
TM7IRS1 flag	TM7BCR flag		
1	1	TM7OC1 compare match	Set value of TM7OC1 $\times 2$
0	1	TM7OC1 compare match	Set value of TM7OC1 $\times 2$
1	0	TM7OC1 compare match	Full count of TM7BC $\times 2$
0	0	Full count over flow	Full count of TM7BC $\times 2$
TM8MD2 register		Interrupt source	Timer pulse output cycle
TM8IRS1 flag	TM8BCR flag		
1	1	TM8OC1 compare match	Set value of TM8OC1 $\times 2$
0	1	TM8OC1 compare match	Set value of TM8OC1 $\times 2$
1	0	TM8OC1 compare match	Full count of TM8BC $\times 2$
0	0	Full count over flow	Full count of TM8BC $\times 2$
TM9MD2 register		Interrupt source	Timer pulse output cycle
TM9IRS1 flag	TM9BCR flag		
1	1	TM9OC1 compare match	Set value of TM9OC1 $\times 2$
0	1	TM9OC1 compare match	Set value of TM9OC1 $\times 2$
1	0	TM9OC1 compare match	Full count of TM9BC $\times 2$
0	0	Full count over flow	Full count of TM9BC $\times 2$

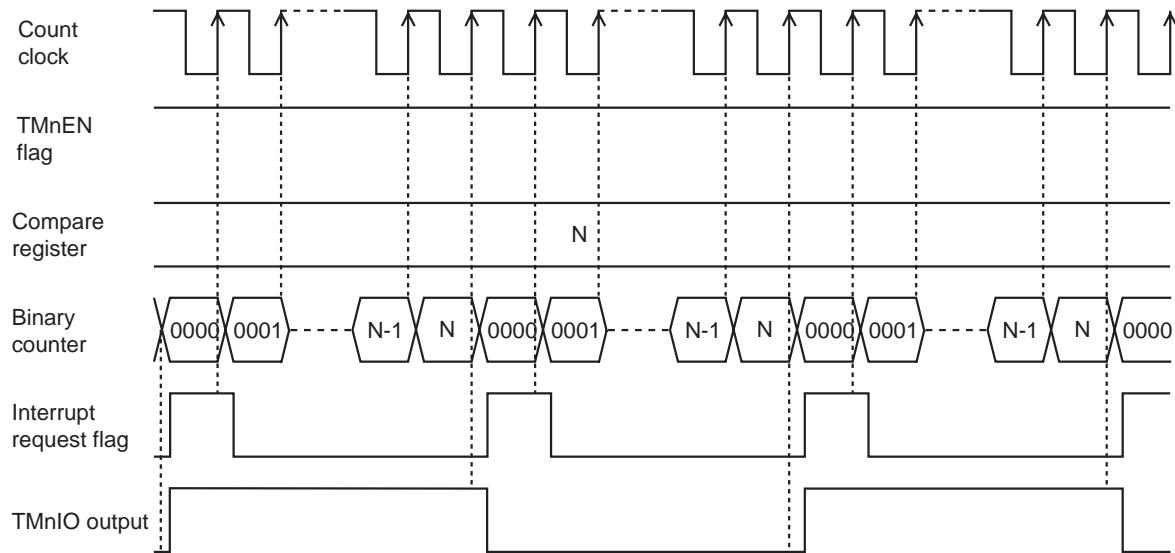


Figure 7.5.1 Count Timing of Timer Pulse Output (Timers 7, 8 and 9)

TMnIO output pin outputs $2 \times$ cycle, compared with the value of the compare register 1. If the binary counter reaches the compare value or full count overflow is occurred, the binary counter is cleared to 0x0000, and the TMnIO output (timer output) is inverted.



In the initial state after releasing reset, the timer pulse output is reset, and low output is fixed. Therefore, release the reset of the timer pulse output by setting the TMnCL flag of the TMnMD1 register to "0".



Regardless of whether the binary counter is stopped or operated, the timer output is "L", when the TMnCL flag of the TMnMD1 register is set to "1".



Reset release of the timer pulse output should be done when the timer count is stopped.



When operating timer pulse output with the divided clock source, set dividing ratio after returning from a reset of timer pulse output. Dividing ratio can be set at TMnPS1 to 0 of TMnMD1 register.

7.5.2 Setup Example

■ Timer Pulse Output Setup Example

TM7IO output pin outputs a 25 kHz pulse using timer 7. For this, select fpll as the clock source and set 1/2 cycle (25 kHz) to the timer 7 compare register (at fpll=10 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counting TM7MD1 (0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop the timer 7 counting.
(2) Set the special function pin PAOMD (0x03EE6) bp5:PAOMD5 =1 PADIR (0x03F3A) bp5:PADIR5 =1	(2) Set the PAOMD5 flag of the port A output mode register (PAOMD) to "1" to set PA5 as the special function pin. Set the PADIR5 flag of the port A direction control register (PADIR) to "1" to set the output mode. [Chapter 4 I/O Ports]
(3) Set the timer pulse TM7MD2 (0x03F79) bp4:TM7PWM =0	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "0" to select the timer pulse output.
(4) Select the timer clear source TM7MD2 (0x03F79) bp5:TM7BCR =1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the binary counter clear source.
(5) Release the reset of the timer pulse TM7MD1 (0x03F78) bp5:TM7CL =0	(5) Set the TM7CL flag of the TM7MD1 register to "0" to enable the pulse output.
(6) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(6) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the clock source by the TM7PS1 to 0 flag.
(7) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0=00	(7) Set IGBT/timer startup factor to timer 7 count operation.
(8) Set the timer pulse output generation cycle TM7PR1(0x03F75,0x03F74) =x00C7	(8) Set 1/2 of the timer pulse output cycle to the timer 7 preset register 1 (TM7PR1). To set 50 kHz by dividing 10 MHz, set as; 200-1=199 (0xC7) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7BC) and the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(9) Start the timer operation TM7MD1 (0x03F78) bp4:TM7EN =1	(9) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

TM7BC counts up from 0x0000. If TM7BC reaches the set value of the TM7OC1 register and TM7BC is cleared to 0x0000, the signal of the TM7IO output is inverted and TM7BC counts up from 0x0000 again.

7.6 16-bit Standard PWM Output (Only duty can be changed consecutively)

TMnIO pin outputs the standard PWM output, which is determined by the overflow timing of the binary counter, and the match timing of the timer binary counter and the compare register.

7.6.1 Operation

■ 16-bit Standard PWM Output (Timers 7, 8 and 9)

PWM waveform with an arbitrary duty is generated by setting a duty of PWM “H” period to the compare register 1 (TMnOC1). Its cycle is the time of the 16-bit timer full count overflow.

Table:7.6.1 shows the PWM output pin.

Table:7.6.1 PWM Output Pin

	Timer 7	Timer 8	Timer 9
PWM output pin	TM7IOA output/ TM7IOB output/ TM7IOC output	TM8IOA output/ TM8IOB output/ TM8IOC output	TM9IOA output/ TM9IOB output

■ Count Timing of Standard PWM Output (at Normal) (Timers 7, 8 and 9)

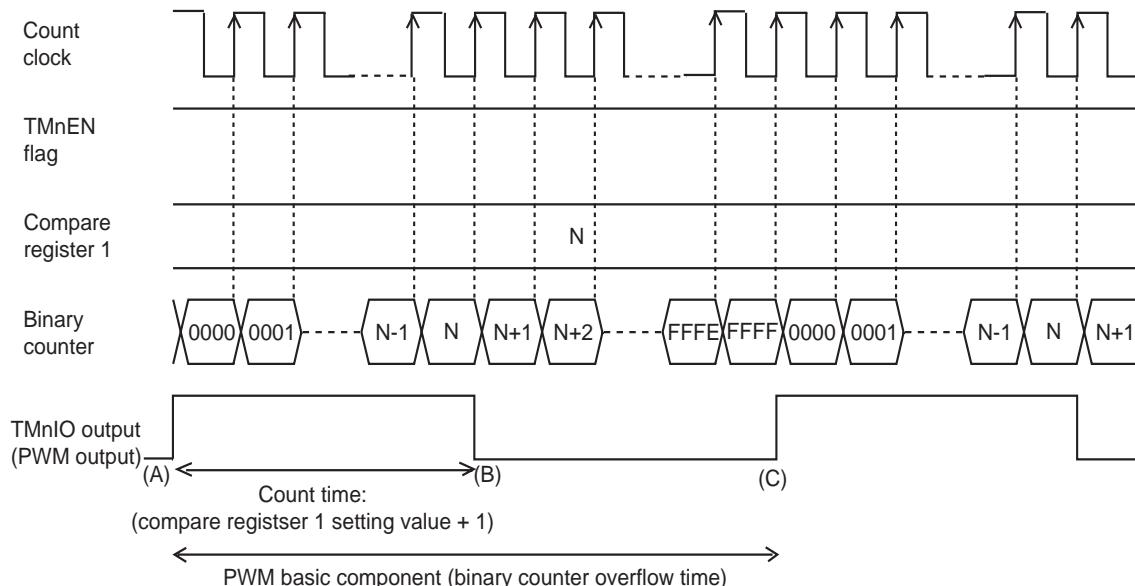


Figure:7.6.1 Count Timing of Standard PWM Output (at Normal)

■ Stop Condition of PWM Waveform, Polarity Selection (Timer 8)

Select the TM8IO output waveform for the time when the PWM operation is stopped by the TM8PWMF of the TM8MD3 register. Select the polarity of PWM output by the TM8PWMO.



Before starting the second PWM or later, clear the BC and PWM waveform by writing to the preset register as the PWM output waveform of the first cycle cannot be guaranteed.

PWM source waveform,

- (A) shows “H” until the binary counter reaches the compare register value from 0x0000.
- (B) shows “L” after the compare match, then the binary counter counts up till the overflow.
- (C) shows “H” again if the binary counter overflow.

■ Count Timing of Standard PWM Output (when compare register 1 is 0x0000) (Timers 7, 8 and 9)

Here is the count timing at setting 0x0000 to the compare register 1.

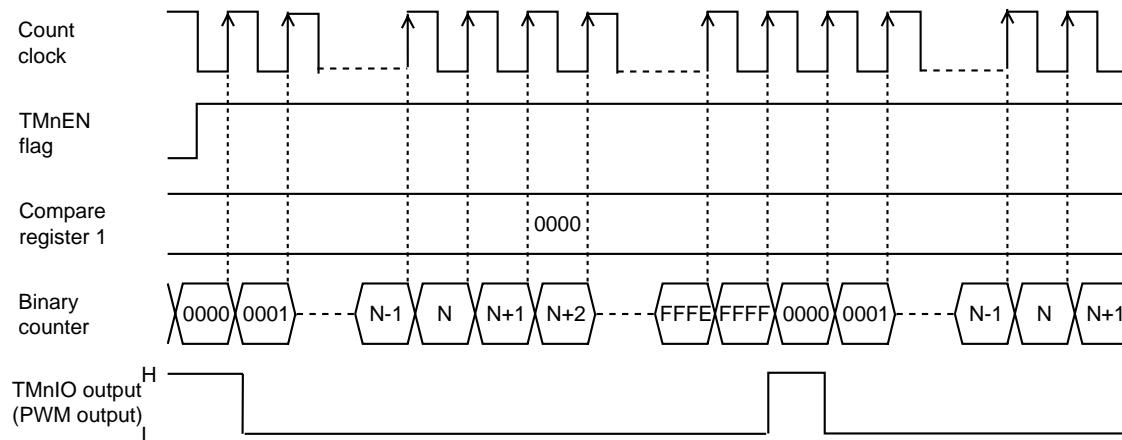


Figure:7.6.2 Count Timing of Standard PWM Output (when compare register 1 is 0x0000)

PWM output shows “H”, when TMnEN flag is stopped (at “0”).

■ Count Timing of Standard PWM Output (when compare register 1 is 0xFFFF) (Timers 7, 8 and 9)

Here is the count timing at setting 0xFFFF to the compare register 1.

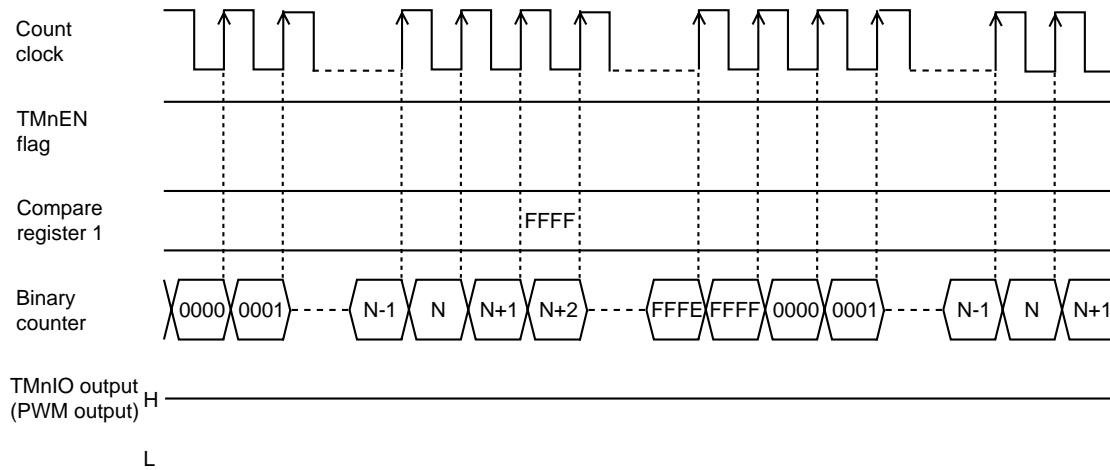


Figure:7.6.3 Count Timing of Standard PWM Output (when compare register 1 is 0xFFFF)



To output the standard PWM output, set the TMnBCR flag of the TMnMD2 register to “0” to select the full count overflow as the binary counter clear source and the PWM output set (“H” output) source.



The TMnOC1 compare match or the TMnOC2 compare match can be selected as a PWM output reset (“L” output) source with the TnPWMSL flag of the TMnMD2 register.



In the initial state of the PWM output, it is changed to “H” output from “L” output at the timing that the PWM operation is selected by the TMnPWM flag of the TMnMD2 register.



To guarantee the PWM waveform of the first cycle, after PWM operation is stopped, write to the preset register to clear the binary counter and the PWM waveform when restarting the PWM operation.

7.6.2 Setup Example

■ Standard PWM Output Setup Example

The TM7IOA output pin outputs the 1/4 duty PWM output waveform at 152.6 Hz with the timer 7 (at the high frequency oscillation, fpll=10 MHz). One cycle of the PWM output waveform is decided by the overflow of the binary counter. “H” period of the PWM output waveform is decided by the set value of the compare register 1. An example setup procedure, with a description of each step is shown below.

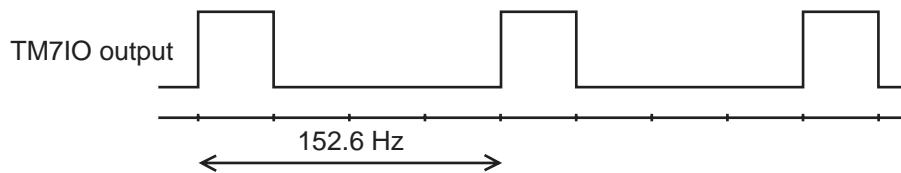


Figure 7.6.4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM7MD1 (0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to “0” to stop the timer 7 counting.
(2) Set the special function pin to output PAOMD (0x03EE6) bp5:PAOMD5 =1 PADIR (0x03F3A) bp5:PADIR5 =1	(2) Set the PAOMD5 flag of the port A output mode register (PAOMD) to “1” to set the PA5 pin as a special function pin. Set the PADIR5 flag of the port A direction control register (PADIR) to “1” to set the output mode. [Chapter 4 I/O Ports]
(3) Set the PWM output TM7MD2 (0x03F79) bp4:TM7PWM =1	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to “1” to select the PWM output.
(4) Set the standard PWM output TM7MD2 (0x03F79) bp5:TM7BCR =0	(4) Set the TM7BCR flag of the TM7MD2 register to “0” to select the full count overflow as the binary counter clear source.
(5) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(5) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.
(6) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0=00	(6) Set IGBT/timer startup factor to timer 7 count operation.

Setup Procedure	Description
(7) Set "H" period of the PWM output TM7PR1(0x03F75,0x03F74) =0x3FFF	(7) Set "H" period of the PWM output to the timer 7 preset register 1 (TM7PR1). To set 1/4 duty of the full count 65536, set as; $65536/4=16383$ (0x3FFF) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(8) Start the timer operation TM7MD1 (0x03F78) bp4:TM7EN =1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

TM7BC counts up from 0x0000. The PWM source waveform outputs "H" until TM7BC reaches the set value of the TM7OC1 register, then after the match it outputs "L". After that, TM7BC continues to count up. Once a overflow occurs, the PWM source waveform outputs "H" again, and TM7BC counts up from 0x0000, again.

7.7 16-bit High Precision PWM Output (Cycle/Duty can be changed consecutively)

The TMnIO pin outputs high precision PWM output, which is determined by the match timing of the timer binary counter and the compare register 1, and match timing of the binary counter and the compare register 2.

7.7.1 Operation

- 16-bit High Precision PWM Output Operation (Timers 7, 8 and 9)

The PWM waveform of any cycle/duty is generated by setting the cycle of PWM to the compare register 1 (TMnOC1) and setting the duty of the “H” period to the compare register 2 (TMnOC2).

- Count Timing of High Precision PWM Output (at Normal) (Timers 7, 8 and 9)

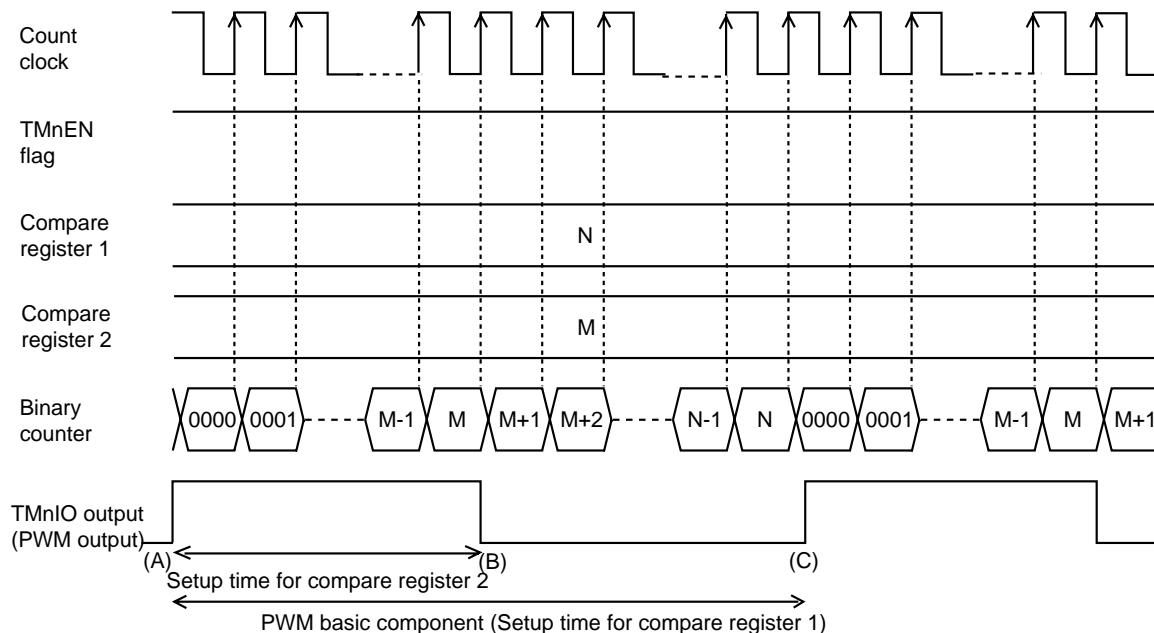


Figure:7.7.1 Count Timing of High Precision PWM Output (at Normal)

PWM source waveform,

(A) shows “H” until the binary counter reaches the compare register from 0x0000.

(B) shows “L” after the TMnOC2 compare match, the binary counter then counts up until the binary counter reaches the TMnOC1 compare register is cleared.

(C) shows “H” again, when the binary counter is cleared.

- Count Timing of High Precision PWM Output (When the compare register 2 is 0x0000) (Timers 7, 8 and 9)

Here is the count timing as the compare register 2 is set to 0x0000.

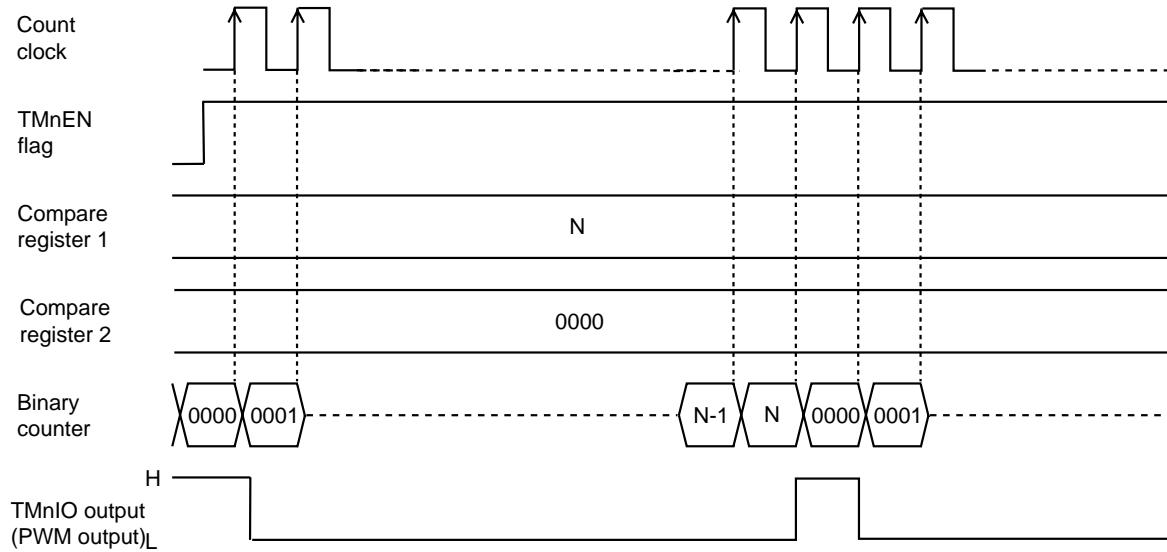


Figure:7.7.2 Count Timing of High Precision PWM Output (When the compare register 2 is 0x0000)

When the TMnEN flag is stopped (at “0”), the PWM output shows “H”.

- Count Timing of High Precision PWM Output (When the compare register 2 = the compare register 1-1) (Timers 7, 8 and 9)

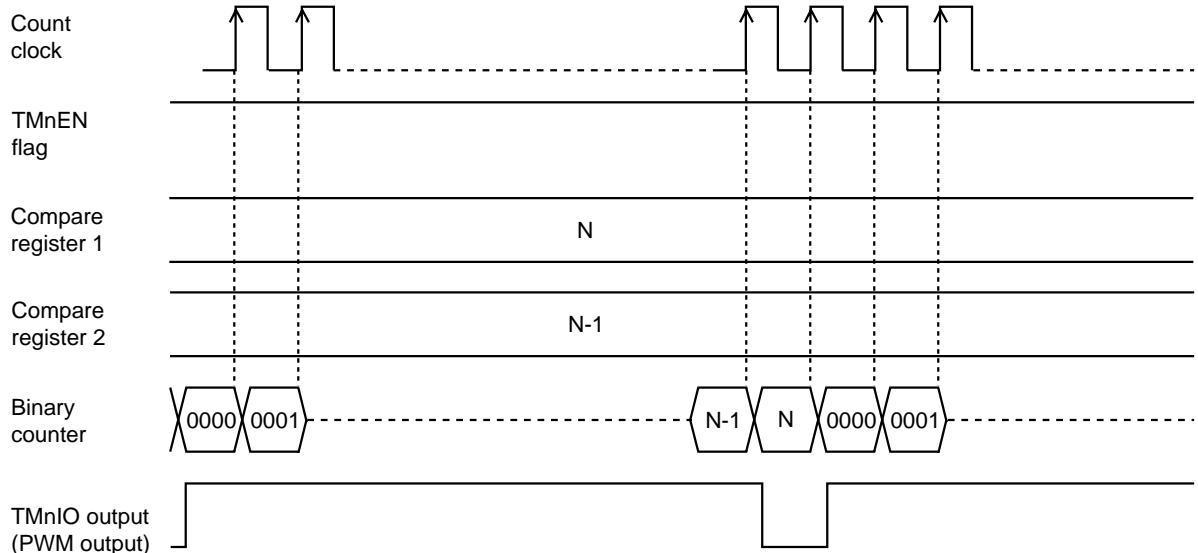


Figure:7.7.3 Count Timing of High Precision PWM Output (When the compare register 2 = the compare register 1-1)



To output the high precision PWM output, set the TMnBCR flag of the TMnMD2 register to “1” to select the TM7OC1 compare match as the clear source for the binary counter, and the set (“H” output) source of the PWM output.

Also, set the TnPWMLS flag to “1” to select the TMnOC2 compare match as the reset (“L” output) source of the PWM output.



In the initial state of the PWM output, it is changed to “H” output from “L” output at the timing that the PWM operation is selected by the TMnPWM flag of the TMnMD register.



Set as the set value of TMnOC2 < the set value of TMnOC1.

If it is set as the set value of TMnOC2 \geq the set value of TMnOC1, the PWM output is a “H” fixed output.

7.7.2 Setup Example

■ High Precision PWM Output Setup Example (Timer 7, Timer 8)

The TM7IOA output pin outputs the 1/4 duty PWM output waveform at 400 Hz with the timer 7. Select fpll/2 (at fpll=10 MHz) as the clock source. One cycle of the PWM output waveform is decided by the set value of the compare register 1. “H” period of the PWM output waveform is decided by the set value of the compare register 2. An example setup procedure, with a description of each step is shown below.

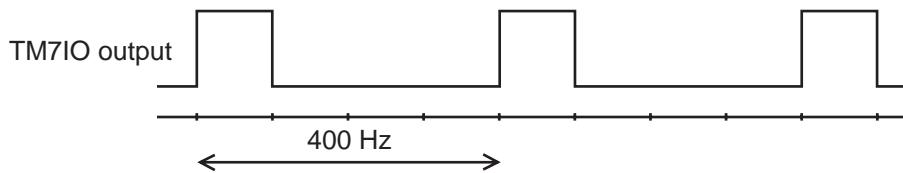


Figure 7.7.4 Pulse Width Measurement of External Interrupt 0

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to “0” to stop the timer 7 counting.
(2) Set the special function pin to output PAOMD (0x03EE6) bp5:PAOMD5 =1 PADIR (0x03F3A) bp5:PADIR5 =1	(2) Set the PAOMD5 flag of the port A output mode register (PAOMD) to “1” to set the PA5 pin as a special function pin. Set the PADIR5 flag of the port A direction control register (PADIR) to “1” to set the output mode. [Chapter 4 I/O Ports]
(3) Set the PWM output TM7MD2(0x03F79) bp4:TM7PWM =1	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to “1” to select the PWM output.
(4) Set the high precision PWM output TM7MD2(0x03F79) bp5:TM7BCR =1 bp6:T7PWMSL =1	(4) Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to “1” to select the TM7OC2 compare match as the duty decision source of the PWM output.
(5) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(5) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.
(6) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0=00	(6) Set IGBT/timer startup factor to timer 7 count operation.

Setup Procedure	Description
(7) Set the PWM output cycle TM7PR1(0x03F75,0x03F74) =0x61a7	(7) Set the PWM output cycle to the timer 7 preset register 1 (TM7PR1). To set 400 Hz by dividing 10 MHz, set as; $25000-1=24999$ (0x61A7) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), the timer 7 binary counter is initialized to 0x0000.
(8) Set the “H” period of the PWM output TM7PR2(0x03F7D,0x03F7C) =0x1869	(8) Set “H” period of the IGBT output to the timer 7 preset register 2 (TM7PR2). To set 1/4 duty of 25000 dividing, set as; $25000/4-1=6249$ (0x1869) At the same time, the same value is loaded the timer 7 compare register 2 (TM7OC2).
(9) Start the timer operation TM7MD1(0x03F78) bp4:TM7EN =1	(9) Set the TM7EN flag of the TM7MD1 register to “1” to operate the timer 7.

TM7BC counts up from 0x0000. The PWM source waveform outputs “H” until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs “L”. After that, TM7BC continues to count up. Once TM7BC matches the TM7OC1 register to be cleared, the PWM output waveform outputs “H” again and TM7BC counts up from 0x0000 again.

7.8 16-bit Timer Synchronous Output

7.8.1 Operation

If the binary counter of the timer reaches the set value of the compare register, port 8 outputs the value of the port 8 output register at the next count clock.

■ 16-bit Timer Synchronous Output Operation (Timer 7)

Port 8 outputs the value of the port 8 output register at a TM7OC1 compare register reaches the binary counter or at the interrupt request generation by the full count overflow. Only port 8 can be used in this operation, and each bit can be set individually.

■ Count Timing of Synchronous Output (Timer 7)

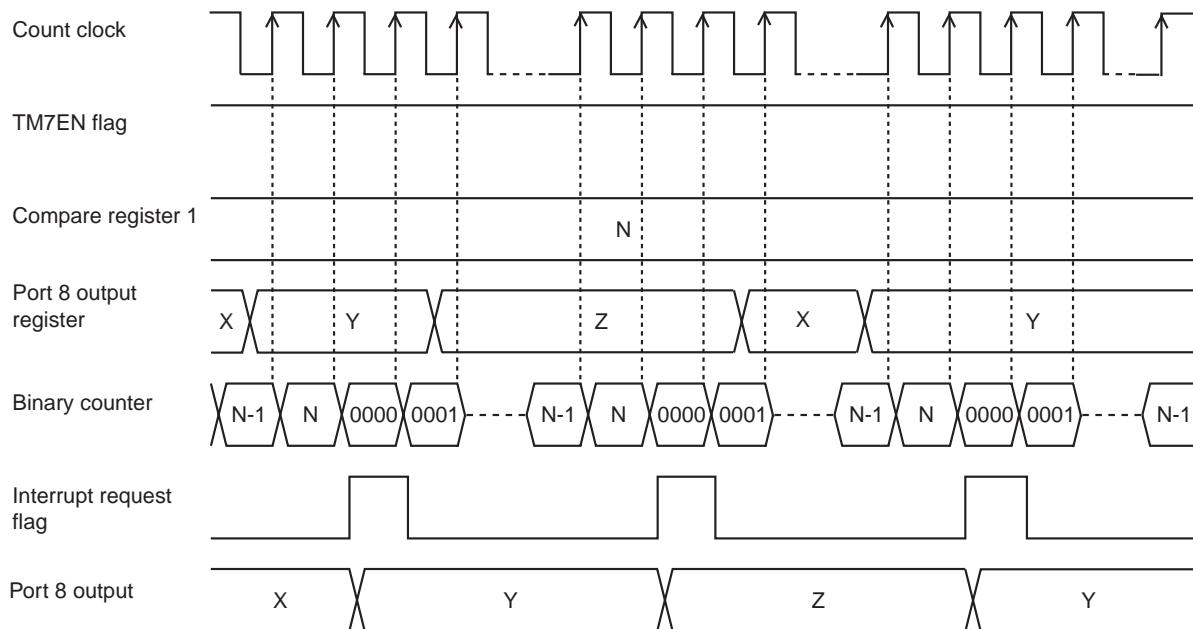


Figure:7.8.1 Count Timing of Synchronous Output (Timer 7)

Output pin outputs the port 8 output latch data at the interrupt request generation by the match of a binary counter and a compare register 1.

7.8.2 Setup Example

■ Synchronous Output Setup Example (Timer 7)

Here is an example to output the value of the port 8 output register from the synchronous output pin constantly (in every 100 µs) with the timer 7. As the clock source of the timer 7, fs/4 (fpll=4 MHz) is selected. An example setup procedure, with a description of each step is shown below;

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4 :TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop the timer 7 counting.
(2) Select the synchronous output event P8SEV(0x03EF8) bp1-0 :P8SEV1-0 =01	(2) Set the P8SEV1 to 0 flag of the pin control register (P8SYO) to "01" to set the synchronous output event to the timer 7 interrupt.
(3) Set the synchronous output pin P8SYO(0x03EF7) =0xFF P8DIR(0x03F38) =0xFF	(3) Set the port 8 synchronous output control register (P8SYO) to 0xFF to set the synchronous output pin. (P87 to P80:Synchronous output pin) Set the port 8 direction control register (P8DIR) to 0xFF to set the port 8 to the output pin. [Chapter 4 I/O Ports]
(4) Select the timer clear factor TM7MD2(0x03F79) bp5 :TM7BCR =1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the binary counter clear source.
(5) Select the count clock source TM7MD1(0x03F78) bp1-0 :TM7CK1-0 =01 bp3-2 :TM7PS1-0 =10	(5) Select fs as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/4 dividing as the count clock source by the TM7PS1 to 0 flag.
(6) Set the synchronous output event generation cycle TM7PR1(0x03F75,0x03F74) =0x0063	(6) Set the synchronous output event generation cycle to the timer 7 preset register 1 (TM7PR1). To set 10 kHz by dividing 1 MHz, set as; 100-1=99 (0x0063) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(7) Start the timer operation TM7MD1 (0x03F78) bp4 :TM7EN =1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer.

TM7BC counts up from 0x0000. If any data is written to the port 8 output register (P8OUT), TM7BC is set to the set value of TM7OC1 register and the synchronous output pin outputs the value of the port 8 output register in every time the interrupt request is generated.

7.9 16-bit Timer Capture

7.9.1 Operation

The value of the binary counter is read out at the timing of the external interrupt input signal which is synchronized to fpll, fs or the external event signal, at the timing of the timer 0 and timer 1 interrupts or at the timing of the writing operation with any value to the capture register.

■ Capture Operation with External Interrupt Signal as the Trigger (Timers 7, 8 and 9)

Input capture trigger is generated at the external interrupt signal. The capture trigger is selected by the timer n mode register 1 (TMnMD1) and the timer n mode register 2 (TMnMD2).

Selectable capture triggers and the interrupt flag setup are shown below.

Table:7.9.1 Capture Trigger

Capture trigger source	Timer 7 mode register 2		Timer 7 mode register 1	Timer 8 mode register 2		Timer 8 mode register 1
	T7ICT1-0	T7ICEDG0	T7ICEDG1	T8ICT1-0	T8ICEDG0	T8ICEDG1
IRQ0 falling edge	00(IRQ0)	1	0	00(IRQ0)	1	0
IRQ0 rising edge	00(IRQ0)	1	1	00(IRQ0)	1	1
IRQ0 both edges	00(IRQ0)	0	x	00(IRQ0)	0	x
IRQ1 falling edge	01(IRQ1)	1	0	01(IRQ1)	1	0
IRQ1 rising edge	01(IRQ1)	1	1	01(IRQ1)	1	1
IRQ1 both edges	01(IRQ1)	0	x	01(IRQ1)	0	x
IRQ2 falling edge	10(IRQ2)	1	0	10(IRQ2)	1	0
IRQ2 rising edge	10(IRQ2)	1	1	10(IRQ2)	1	1
IRQ2 both edges	10(IRQ2)	0	x	10(IRQ2)	0	x

Capture trigger source	Timer 9 mode register 2		Timer 9 mode register 1
	T9ICT1-0	T9ICEDG0	T9ICEDG1
IRQ0 falling edge	00(IRQ0)	1	0
IRQ0 rising edge	00(IRQ0)	1	1
IRQ0 both edges	00(IRQ0)	0	x
IRQ1 falling edge	01(IRQ1)	1	0
IRQ1 rising edge	01(IRQ1)	1	1
IRQ1 both edges	01(IRQ1)	0	x
IRQ2 falling edge	10(IRQ2)	1	0
IRQ2 rising edge	10(IRQ2)	1	1
IRQ2 both edges	10(IRQ2)	0	x
IRQ3 falling edge	11(IRQ3)	1	0
IRQ3 rising edge	11(IRQ3)	1	1
IRQ3 both edges	11(IRQ3)	0	x



If the system clock (fs) is selected as the capture clock and the capture operation is done during the TMnIO input or operation with fpll, an incomplete value at the count up of the binary counter may be written to the input capture register. To prevent this, use fs or synchronous TMnIO input as the count clock.

[Chapter 7. 7.4.1 Operation]



Capture trigger signals of the 16-bit timers n are generated by sampling the rising edge of the capture clock selected by the TMnCKSMP flag of the TMnMD3 register. Therefore, even if the capture trigger is input, the value of the binary counter is not loaded to the capture register until the rising edge of the next capture clock.

If the clock which is slower than CPU operation speed (fs) is set as the timer source clock, set the TMnCKSMP of the TMnMD3 register to fs.

Also, the interval of each capture trigger should be set more than 2 cycles of the clock which is set at the TMnCKSMP of the TMnMD3 register.



If the capture clock frequency is longer against the system clock, the value of the capture register may be read out before capturing.

- Capture Count Timing as Both Edges of External Interrupt Signal is selected as Trigger (Timers 7, 8 and 9)

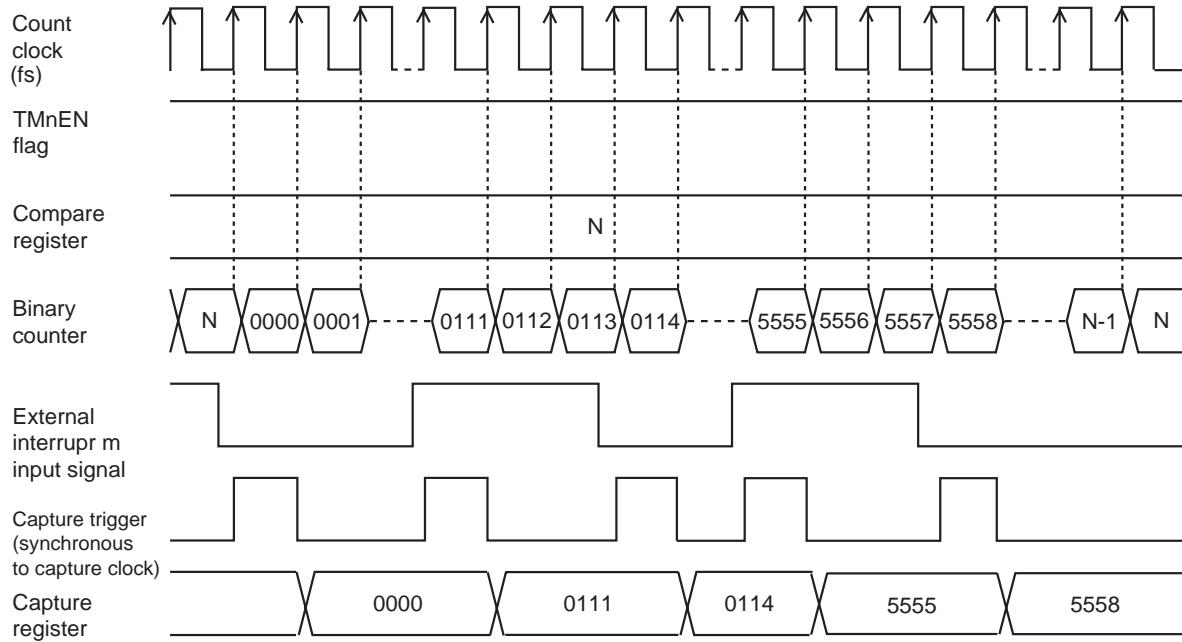


Figure:7.9.1 Capture Count Timing as External Interrupt Signal is selected as Trigger (Timers 7, 8 and 9)

A capture trigger is generated at the both edges of the external interrupt m input signal. In synchronized with this capture trigger, the value of binary counter is loaded to the input capture register. The value loaded to the capture register is depending on the value of the binary counter at the falling edge of the capture trigger. When the specified edge is selected as the capture trigger source, the capture trigger is generated only at that edge. The other count timing is the same as the count timing of the timer operation.



When the binary counter is used as a free counter which counts 0x0000 to 0xFFFF set the compare register 1 to 0xFFFF, or set the TMnBCR flag of the TMnMD2 to "0".



Even if an event is generated before the value of the input capture register is read out, the value of the input capture register can be rewritten.



In the initial state after releasing the reset, the generation of trigger by the external interrupt signal is disabled. Set the TnICEN flag of the TMnMD2 register to "1" to enable the trigger generation.



Capture trigger samples the external interrupt input signal by system clock is generated. When interrupt input signal is firster than the system clock cycle, the edge of the external interrupt input signal might not be able to be detected. Moreover, because the system clock stops in the STOP mode, the capture function can not be used.



When using th external interrupt signal as capture trigger, to make external interrupt input enable in IRQCNT.

■ Capture Operation Triggered by Writing Software (Timers 7, 8 and 9)

A capture trigger is generated by writing an arbitrary value to the input capture register (TMnIC). When writing a value to the register, the capture trigger is synchronized with the capture sampling clock which is set by the TMnCKSMP flag of the timer mode register 3, and a capture trigger is generated. At the timing of the capture trigger falling, the value of the binary counter can be loaded into the input capture register.

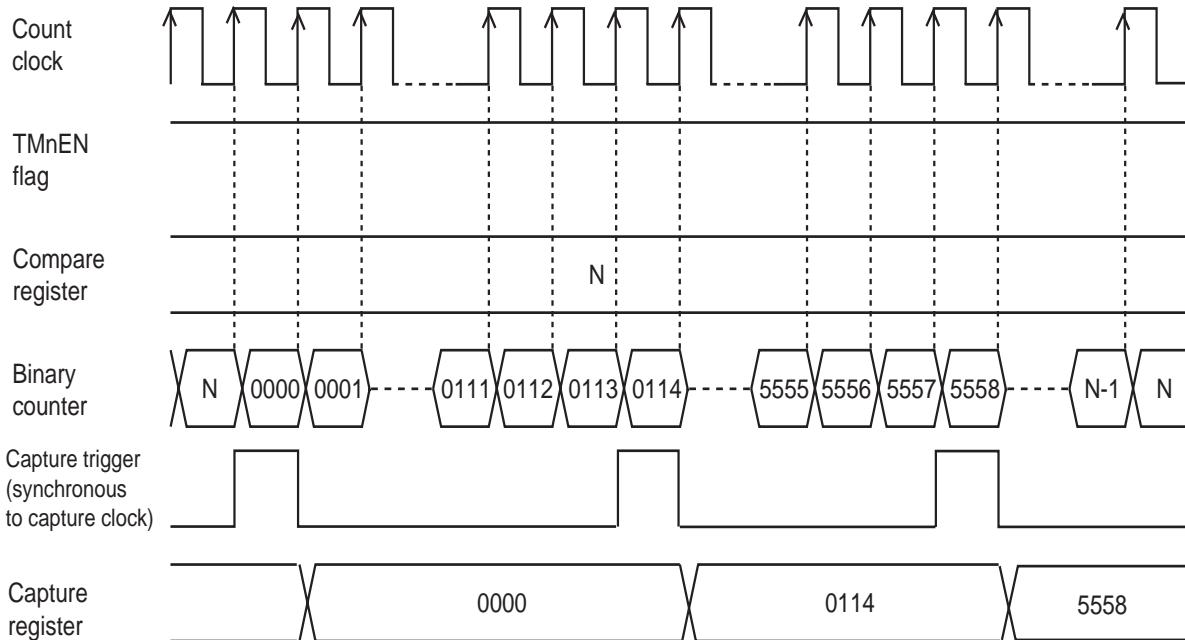


Figure:7.9.2 Capture Count Timing Triggered by Writing Software (Timers 7, 8 and 9)

The capture trigger is generated at the writing signal to the input capture register. The writing signal is generated at the last cycle of the writing instruction. In synchronized with this capture trigger, the value of the binary counter is loaded to the input capture register. The value is depending on the value of the binary counter at the falling edge of the capture trigger. The other timing is the same as the timer operation.



The writing to the input capture to generate the capture trigger should be done with 8-bit access instruction of the TMnICL register or the TMnICH register.
At this time, data is not actually written to the TMnIC register.



On hardware, there is no flag to disable the capture operation triggered by writing software.
Capture operation is enabled regardless of the TnICEN flag of the TMnMD2 register.



If the capture operation is done during the event count operation, an incomplete value at the count up of the binary counter may be written to the input capture register. To prevent this, use synchronous TMnIO input as the count clock.
[Chapter 7. 7.4.1 Operation]

■ Capture Operation as Timer 0 and 1 interrupts are selected as Trigger (Timers 7, 8 and 9)

A capture trigger of the input capture function is generated by the timer 0 and 1 interrupts signals. Select the capture trigger by the timer mode register 2 (TMnMD2) and the timer mode register 4 (TMnMD4). When the timer 0 and 1 interrupts signals are selected as the capture trigger, the edges of the capture trigger are disabled.

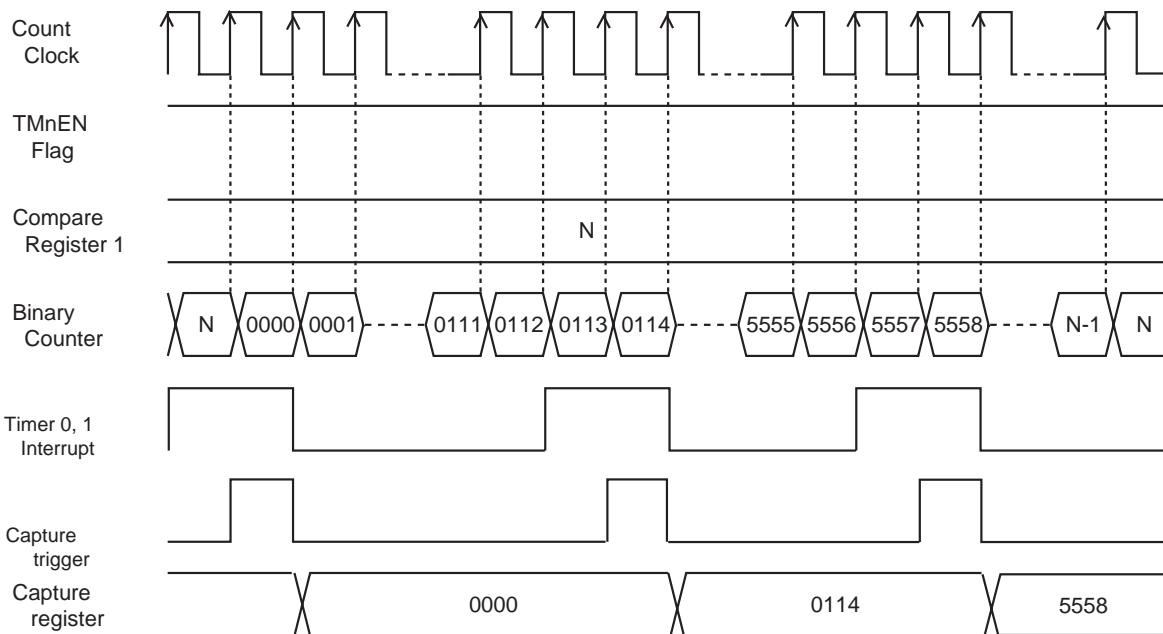


Figure:7.9.3 Capture Operation as Timer 0 and 1 interrupts are selected as Trigger (Timers 7, 8 and 9)



When the TnICT1-0 flag of the timer mode register 2 is set to x'11', a capture trigger of the input capture function is generated by the timer 0 and 1 interrupts signals. Select the capture trigger by the timer mode register 2 (TMnMD2) and the timer mode register 4 (TMnMD4). When the timer 0 and 1 interrupts signals are selected as the capture trigger, the edges of the capture trigger are disabled. When setting the capture clock as the count clock to execute the event count operation, the timer 0, 1 interrupt signal may not be recognized. To prevent this, select the synchronous TMnIO input as the clock source.

■ Binary Counter Clearance at the Timing of Capture (Timers 7, 8 and 9)

When selecting the external interrupt input signal or the timer 0 and 1 interrupts as the capture trigger, the binary counter can be cleared during capture operation by setting the TnCAPCLR flag of the timer mode register 4 (TMnMD4) to “1”. The binary counter can be cleared during timer count operation only.

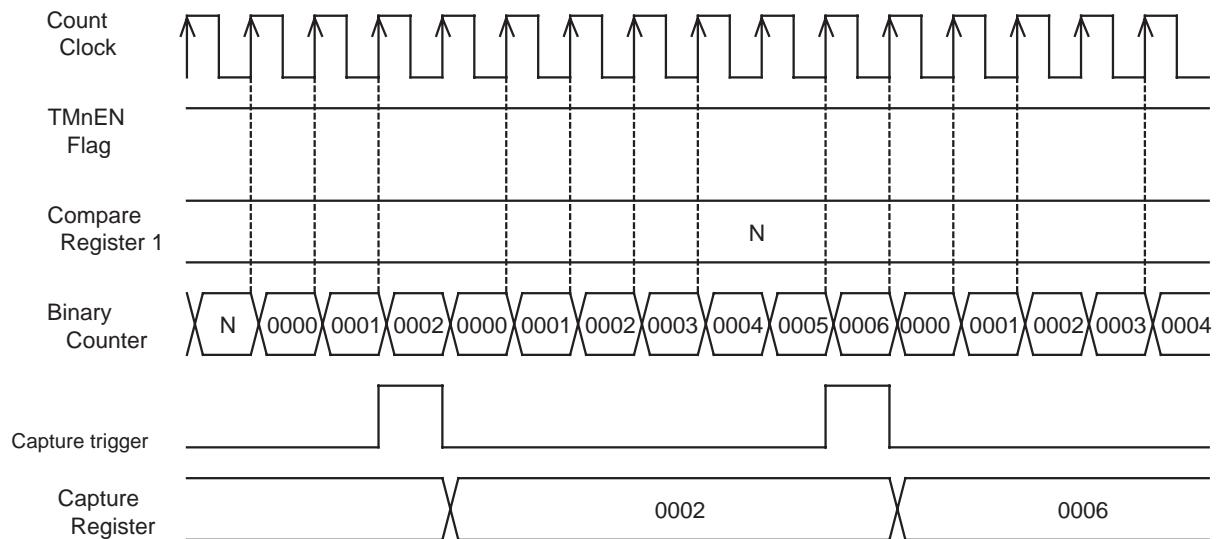


Figure:7.9.4 Binary Counter Clearance at the Timing of Capture (Timers 7, 8 and 9)

7.9.2 Setup Example

■ Capture Function Setup Example

Pulse width measurement is enabled by storing the value of the binary counter to the capture register at the interrupt generation edge of the external interrupt 0 signal with timer 7. The interrupt generation edge is specified to be the rising edge.

An example setup procedure, with a description of each step is shown below.

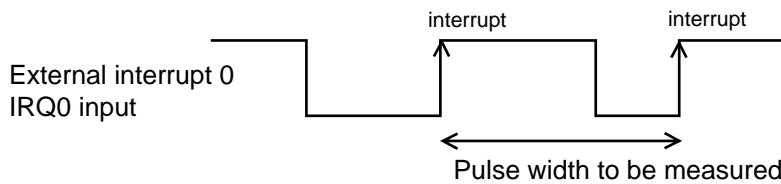


Figure 7.9.5 Pulse Width Measurement of External Interrupt 0 Input Signal

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop the timer 7 counting.
(2) Disable the interrupt IRQ0ICR(0x03FE2) bp1:IRQ0IE =0	(2) Set the IRQ0IE flag of the IRQ0ICR register to "0" to disable the interrupt.
(3) Select the timer clear source TM7MD2(0x03F79) bp5:TM7BCR =1	(3) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as the binary counter clear source.
(4) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(4) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing of fpll as the count clock source by the TM7PS1 to 0 flag.
(5) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0=00	(5) Set IGBT/timer startup factor to timer 7 count operation.
(6) Set the compare register TM7PR1(0x03F75,0x03F74) =0xFFFF	(6) Set 0xFFFF to the timer 7 preset register 1 (TM7PR1). At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(7) Select the capture trigger generation interrupt source TM7MD2(0x03F79) bp1-0:T7ICT1-0 =00	(7) Select the external interrupt 0 (IRQ0) input as the capture trigger generation source by the T7ICT1 to 0 flag of the TM7MD2 register.

Setup Procedure	Description
(8) Select the capture trigger generation edge TM7MD1(0x03F78) bp6:T7ICEDG1 =1 TM7MD2 (0x03F79) bp7:T7ICEDG0 =1	(8) Set the T7ICEDG1 flag of the TM7MD1 register to “1” to select the rising edge as the capture trigger generation edge. Also, set the T7ICEDG0 flag of the TM7MD2 register to “1” to enable the specify edge as the capture trigger generation source.
(9) Select the capture sampling TM7MD3(0x03F8E) bp7:TM7CKSMP =0	(9) Select the capture sampling as the count clock.
(10) Select the interrupt generation valid edge IRQ0ICR(0x03FE2) bp5:REDG0 =1	(10) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to “1” to select the rising edge as the interrupt generation valid edge.
(11) Set the interrupt level IRQ0ICR(0x03FE2) bp7-6:IRQ0LV1-0 =10	(11) Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register. If the interrupt request flag is already set, clear the request flag. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(12) Enable the interrupt IRQ0ICR(0x03FE2) bp1:IRQ0IE =1	(12) Set the IRQ0IE flag of the IRQ0ICR register to “1” to enable the interrupt.
(13) Enable the capture trigger generation TM7MD2(0x03F79) bp2:T7ICEN =1	(13) Set the T7ICEN flag of the TM7MD2 register to “1” to enable the capture trigger generation.
(14) Start the timer operation TM7MD1(0x03F78) bp4:TM7EN =1	(14) Set the TM7EN flag of the TM7MD1 register to “1” to operate the timer 7.

TM7BC counts up from 0x0000. At the timing of the rising edge of the external interrupt 0 input signal, the value of TM7BC is loaded to the TM7IC register. At that time, the pulse width between rising edge of the external interrupt input signal can be measured by reading the value of the TM7IC register through interrupt service routine, and calculating the difference between the capture values.

7.10 16-bit High Precision IGBT Output (Cycle/Duty can be changed consecutively)

High precision IGBT output starts counting by the external interrupt input signal as the trigger and output from TM7IO, TM8IO. Startup trigger can be selected by the external interrupt 0, 1 and 2 or starting of the timer 7 count operation. When counting starts, the operation is the same as the high precision PWM output.

7.10.1 Operation

■ IGBT Trigger Selection

IGBT trigger can be selected from IRQ0, IRQ1, IRQ2 and the start of the timer 7 count operation. Setup should be done at the T7IGBT0 and T7IGBT1 flag of the TM7MD3 register. When the startup is controlled from external of the microcontroller, one of IRQ0 to IRQ2 should be selected. This trigger detects the input level before activation. Either “H” or “L” level can be selected with the T7IGBTTR flag of the TM7MD3 register. When “1” (the rising edge) is selected, count operation continues while the trigger pin is “H”. When “0” (the falling edge) is selected, count operation continues while the trigger pin is “L”. To control the startup by the commands, TM7EN count operation should be selected. In that case, timer count operation or IGBT output are controlled by the TM7EN flag of the TM7MD1 register. When “1” (count operation) is selected, count continues counting until “0” (count stop) is set. Make sure to set the T7IGBT0, 1 of the TM7MD3 register before operating the TM7EN flag of the TM7MD1 register. In that case, setup of T7IGBTTR is neglected. The binary counter is cleared as the counting stops. The value is loaded from the preset register to the compare register in synchronization with the counter clock.

■ 16-bit High Precision IGBT Output (Timer 7)

The IGBT waveform of any cycle/duty is generated by setting the cycle of IGBT to the compare register 1 (TM7OC1) and setting the duty of the “H” period to the compare register 2 (TM7OC2). The 16 bit timer that can be used by high precision IGBT output is the timer 7.

Table:7.10.1 IGBT Output Pin

	Timer 7
IGBT output pin	TM7IOA output / TM8IOA output TM7IOB output / TM8IOB output TM7IOC output / TM8IOC output

Table:7.10.2 IGBT Trigger

	Timer 7 mode register 3	
	T7IGBT1-0	T7IGBTTR
IRQ0 falling edge	01 (IRQ0)	1
IRQ0 rising edge	01 (IRQ0)	0
IRQ1 falling edge	10 (IRQ1)	1
IRQ1 rising edge	10 (IRQ1)	0
IRQ2 falling edge	11 (IRQ2)	1
IRQ2 rising edge	11 (IRQ2)	0
TM7EN count operation	00	-

■ One shot Pulse Output Setup

One shot pulse output can be done by setting the T7ONESHOT flag of the TM7MD4 register to "1".

■ Count Timing of High Precision IGBT Output (At Normal) (Timer 7)

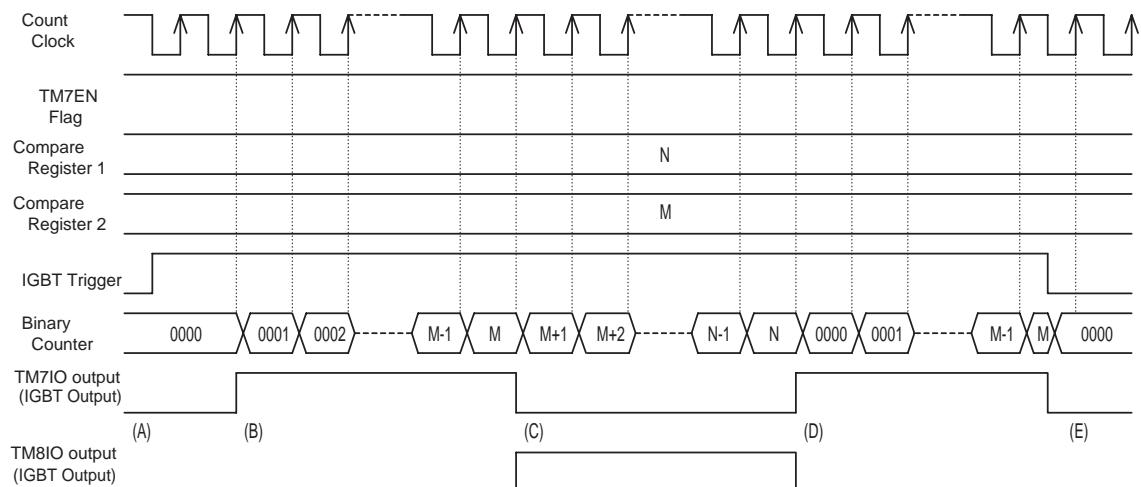


Figure:7.10.1 Count Timing of High Precision IGBT Output (At Normal)

(A) When IGBT trigger is input, IGBT operation becomes valid after 1 count clock. After IGBT output is valid, it is "L" until the next count clock.

(B) When IGBT trigger is valid, it is "H" during the period when the value of the binary counter reaches that of TM7OC2 from 0x0000. ("H" output from 0x0001 at the first operation cycle)

(C) After the TM7OC2 compare match, it is "L" and the binary counter counts up until the counter reaches the TM7OC1 compare register to be cleared.

(D) When the binary counter is cleared, it becomes "H" again.

(E) When IGBT trigger becomes invalid, the timer is initialized and IGBT output forcibly becomes "L".

■ Count Timing of High Precision IGBT Output (When the compare register 2 is 0x0000) (Timer 7)

The following shows the count timing as the compare register 2 is set to 0x0000.

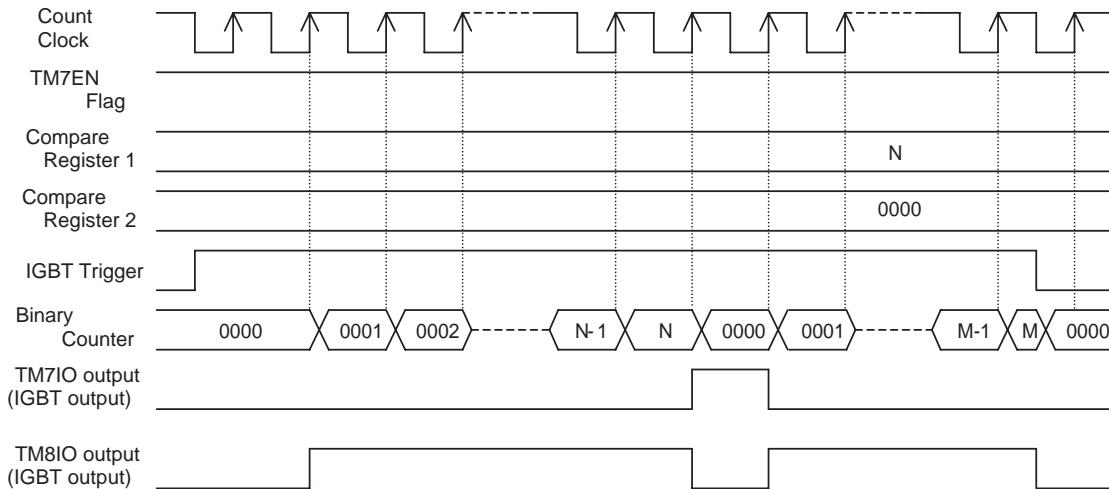


Figure:7.10.2 Count Timing of High Precision IGBT Output (When the compare register 2 is 0x0000)

When the TM7EN flag is set to “0” (stop status) and the T7IGBTDT of the TM7MD3 register is set to “0”, both TM7IO and TM8IO output “L”.

■ Count Timing of High Precision IGBT Output (When compare register 2 = compare register 1) (Timer 7)

The following shows the count timing when the value of the compare register 1 is set to the compare register 2.

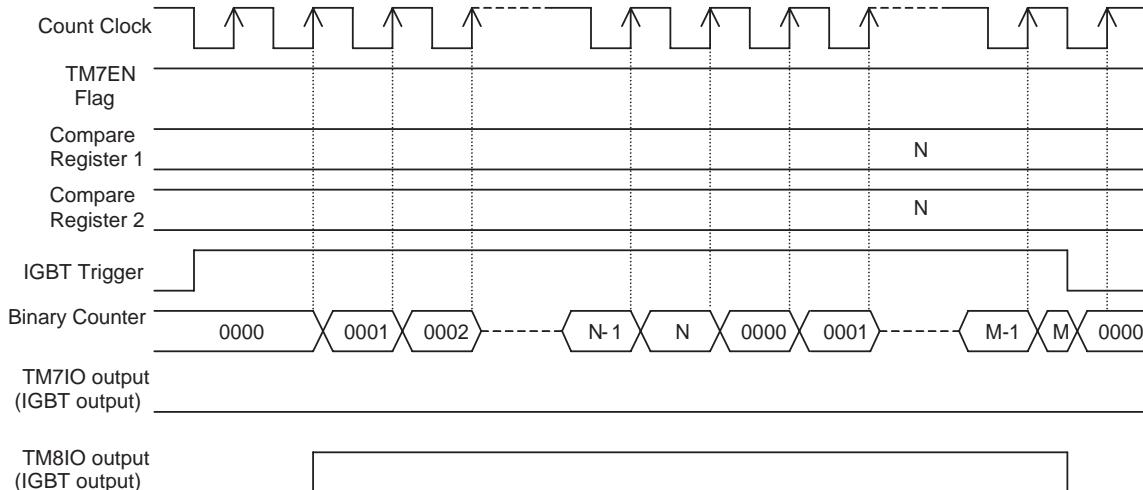


Figure:7.10.3 Count Timing of High Precision IGBT Output (When compare register 2 = compare register 1)



For high precision IGBT output, set the TM7BCR flag of the TM7MD2 register to "1" and select TM7OC1 compare match as the binary counter clear factor and IGBT output set ("H" output) factor. Also, set the T7PWMSL flag of the TM7MD2 register to "1" and select the TM7OC2 compare match as the IGBT output reset ("L" output) factor.



In the initial state of the IGBT output (TM7IO), when the IGBT output is selected by the T7IGBTEN of the TM7MD3 register, it is "L" output. After the trigger is input, it changes to "H" at the second cycle.



Set as TM7OC2 value \leq TM7OC1 value.

When TM7OC2 value $>$ TM7OC1 value, the IGBT output waveform is fixed to "H".

■ One Shot Pulse Output of High Precision IGBT Output (At Normal) (Timer 7)

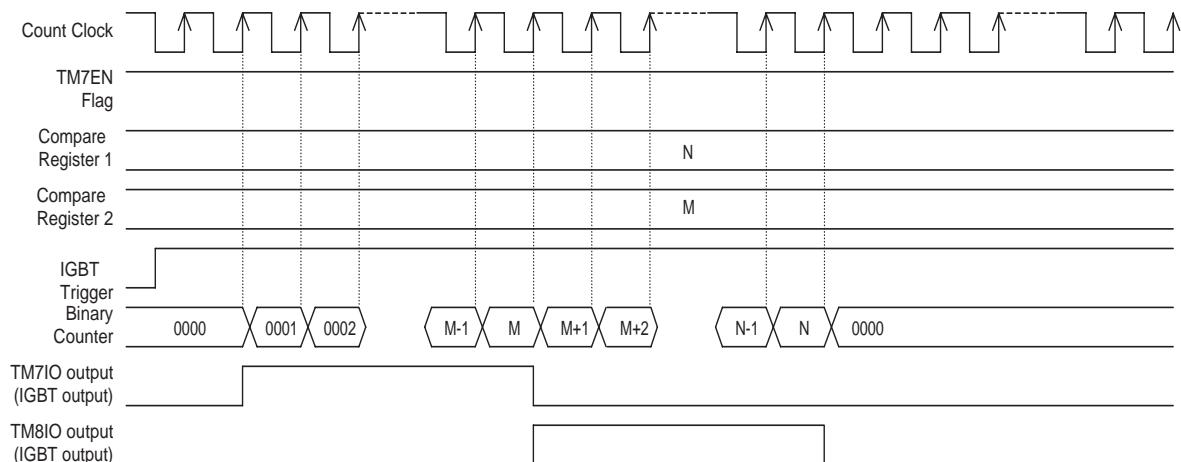


Figure:7.10.4 One Shot Pulse Output of High Precision IGBT Output (At Normal) (Timer 7)

- One Shot Pulse Output of High Precision IGBT Output (When the compare register 2 is 0x0000) (Timer 7)

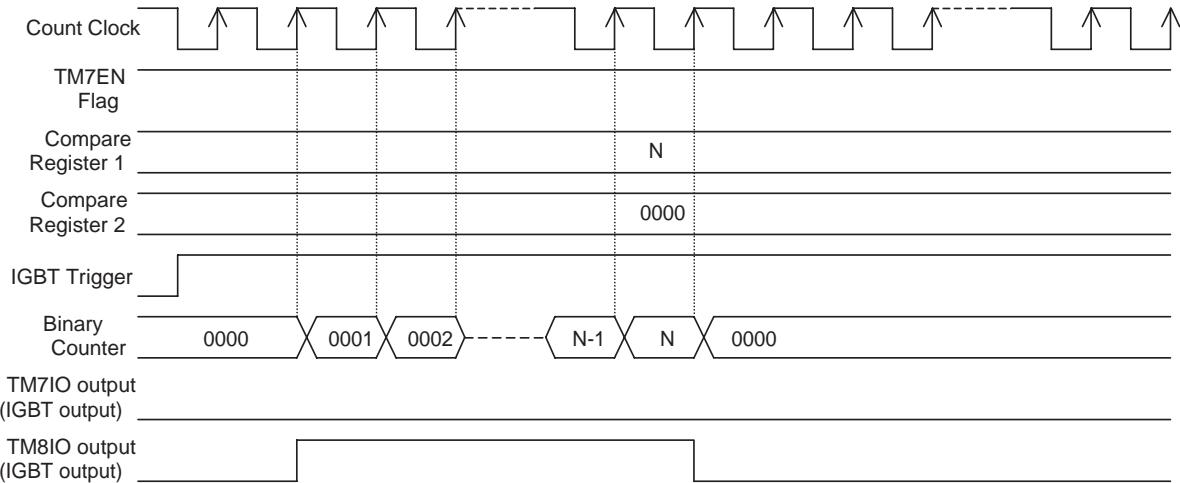


Figure:7.10.5 One Shot Pulse Output of High Precision IGBT Output (When the compare register 2 is 0x0000) (Timer 7)

- One Shot Pulse Output of High Precision IGBT Output (When compare register 2 = compare register 1) (Timer 7)

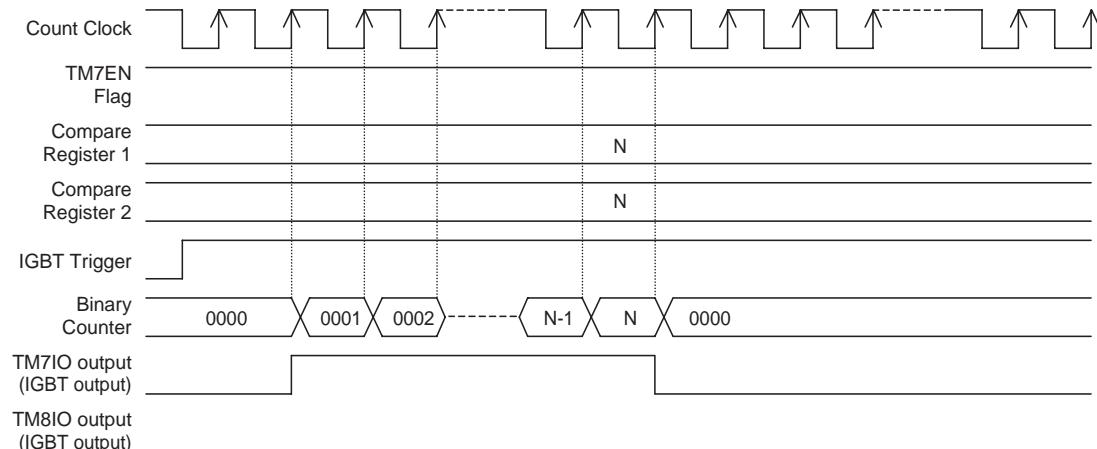


Figure:7.10.6 One Shot Pulse Output of High Precision IGBT Output (When compare register 2 = compare register 1) (Timer 7)

7.10.2 Setup Example

■ High precision IGBT Output Setup Example (Timer 7)

At the interrupt generation edge of the external interrupt 0 input signal, TM7IOA output pin outputs the waveform of 1/4 duty IGBT output waveform at 400 Hz using the timer 7. Select fpll (at fpll=10 MHz) as the clock source. Required period for one IGBT output waveform cycle depends on the set value of the compare register 1. “H” period of IGBT output waveform depends on the set value of the compare register 2.

An example setup procedure, with a description of each step is shown below.

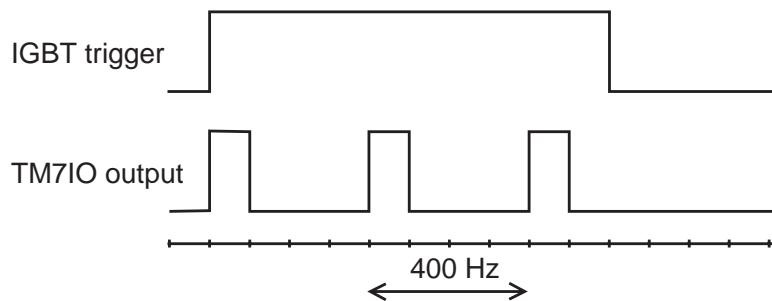


Figure 7.10.7 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to “0” to stop the timer 7 counting.
(2) Set the output of special function pins PAOMD(0x03EE6) bp5:PAOMD5 =1 bp6:PAOMD6 =1 PADIR(0x03F3A) bp5:PADIR5=1 bp6:PADIR6=1	(2) Set the PAOMD5 flag of the port A output mode register (PAOMD) to “1” to set the PA5 pin to the special function pin. Set the PAOMD6 flag of the port A output mode register (PAOMD) to “1” to set the PA6 pin to the special function pin. Set the PADIR5 flag of the port A direction control register (PADIR) to “1”, the PADIR6 flag to “1” to set the output mode. Add pull-up/pull-down resistor if necessary. [Chapter 4. I/O Ports]
(3) Set the timer output pin TM7MD2(0x03F79) bp4:TM7PWM =1 TM7MD1(0x03F78) bp5:TM7CL =0	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to “1” to set the output from PA5 pin to PWM output. Set the TM7CL flag of the timer 7 mode register 1 (TM7MD1) to “0” to enable timer output.
(4) Set the timer 8 output pin TM8MD4(0x03F6F) bp2:TM8SEL_A =1	(4) Set the TM8SEL_A flag of the timer 8 mode register 4 (TM8MD4) to “1” to set the output from PA6 pin to IGBT output.
(5) Set IGBT output TM7MD3(0x03F8E') bp2:TM7IGBTEN =1	(5) Set the T7IGBTEN flag of the timer 7 mode register 3 (TM7MD3) to “1” to select IGBT output.

Setup Procedure	Description
(6) Set the high precision IGBT output operation TM7MD2(0x03F79) bp5:TM7BCR =1 bp6:T7PWMSL =1 TM7MD4(0x03F6E) bp3:T7NODED =1	(6) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the clear factor of the binary counter. Set the T7PWMSL flag to "1" to select the TM7OC2 compare match as the duty determination factor of IGBT output. Set the T7NODED flag of the TM7MD4 register to "1" to select the IGBT waveform without dead time.
(7) Select IGBT trigger generation interrupt source TM7MD3(0x03F8E) bp1-0:T7IGBT1-0 =01	(7) Set the external interrupt 0 (IRQ0) input as IGBT trigger generation factor by the T7IGBT1-0 flag of the TM7MD3 register.
(8) Select the interrupt generation valid edge IRQ0ICR(0x03FE2) bp5:REDG0 =1	(8) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as the interrupt generation valid edge.
(9) Select IGBT trigger generation level TM7MD3(0x03F8E) bp4:T7IGBTTR=0	(9) Set the T7IGBTTR flag of the TM7MD3 register to "0" to set the IGBT trigger level to "H".
(10) Select IGBT trigger generation edge TM7MD2(0x03F79) bp7:T7ICEDG=1	(10) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the external interrupt specified edge as the IGBT trigger generation factor.
(11) Enable of external interrupt 0 input IRQCNT(0x03F3D) bp0:P20EN =1	(11) Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.
(12) Set the interrupt level IRQ0ICR(0x03FE2) bp7-6:IRQ0LV1-0 =10	(12) Set the interrupt level by the IRQ1LV1 to 0 flag of the IRQ0ICR register. If any interrupt request flag is already set, clear it. [Chapter 3.1.4 Maskable Interrupt Control Register Setup]
(13) Enable the interrupt IRQ0ICR(0x03FE2) bp1:IRQ0IE =1	(13) Set the TM7EN flag of the TM7MD1 register to "1" to start the timer 7.
(14) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(14) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.
(15) Set the IGBT output cycle TM7PR1(0x03F75, 0x03F74) =0x61A7	(15) Set the IGBT output cycle to the timer 7 preset register 1 (TM7PR1). To set 400 Hz by dividing MHz, set as; 25000-1=24999 (0x61A7) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to 0x0000.

Setup Procedure	Description
(16) Set “H” period of the IGBT output TM7PR2(0x03F7D, 0x03F7C) =0x1869	(16) Set the “H” period of the IGBT waveform to the timer 7 preset register 2 (TM7PR2). To set 1/4 duty of 25000 dividing, set as; $25000/4=6249(0x1869)$ At the same time, the same value is loaded to the timer 7 compare register 2 (TM7OC2).
(17) Start the timer operation TM7MD1(0x03F78) bp4: TM7EN= 1	(17) Set the TM7EN flag of the TM7MD1 register to “1” to operate the timer 7.

TM7BC counts up from 0x0000 at the interrupt generation edge of the external interrupt 0 input signal. The IGBT output waveform outputs “H” until TM7BC matches the set value of the TM7OC2 register. Once they match, it outputs “L”. After that, TM7BC continues to count up. Once TM7BC value matches the TM7OC1 register value to be cleared, the IGBT output waveform outputs “H” and TM7BC counts up from 0x0000 again.

7.11 16-bit Standard IGBT Output (Only duty can be changed consecutively)

Startup trigger can be selected by the external interrupt 0, 1 and 2 or starting of the timer 7 count operation. When counting starts, the operation is the same as the high precision PWM output.

7.11.1 Operation

■ IGBT Trigger Selection

IGBT trigger can be selected from IRQ0, IRQ1, IRQ2 and the start of the timer 7 count operation. Setup should be done at the T7IGBT0 and T7IGBT1 flag of the TM7MD3 register. When the startup is controlled from external of the microcontroller, one of IRQ0 to IRQ2 should be selected. This trigger detects the input level before activation. Either “H” or “L” level can be selected with the T7IGBTTR flag of the TM7MD3 register. When “1” (the rising edge) is selected, count operation continues while the trigger pin is “H”. When “0” (the falling edge) is selected, count operation continues while the trigger pin is “L”.

To control the startup by the commands, TM7EN count operation should be selected. In that case, timer count operation or IGBT output are controlled by the TM7EN flag of the TM7MD1 register. When “1” (count operation) is selected, count continues counting until “0” (count stop) is set. Make sure to set the T7IGBT0, 1 of the TM7MD3 register before operating the TM7EN flag of the TM7MD1 register.

■ 16-bit Standard IGBT Output (Timer 7)

The IGBT waveform of any duty is generated by setting the duty of “H” period to the compare register 1 (TM7OC1) and detecting the trigger that is generated by the external interrupt after the external interrupt interface block has passed. The cycle is the full count overflow time of the 16 bit timer. The following shows IGBT output pins, types of the selectable IGBT trigger, and the setting of the interrupt flags.

Table:7.11.1 IGBT Output Pin

	Timer 7
IGBT output pin	TM7IOA output / TM8IOA output TM7IOB output / TM8IOB output TM7IOC output / TM8IOC output

Table:7.11.2 IGBT Trigger

Timer 7 mode register 3		
	T7IGBT1-0	T7IGBTTR
IRQ0 falling edge	01 (IRQ0)	1
IRQ0 rising edge	01 (IRQ0)	0
IRQ1 falling edge	10 (IRQ1)	1
IRQ1 rising edge	10 (IRQ1)	0
IRQ2 falling edge	11 (IRQ2)	1
IRQ2 rising edge	11 (IRQ2)	0
TM7EN count operation	00	-

■ Count Timing of Standard IGBT Output (At Normal)

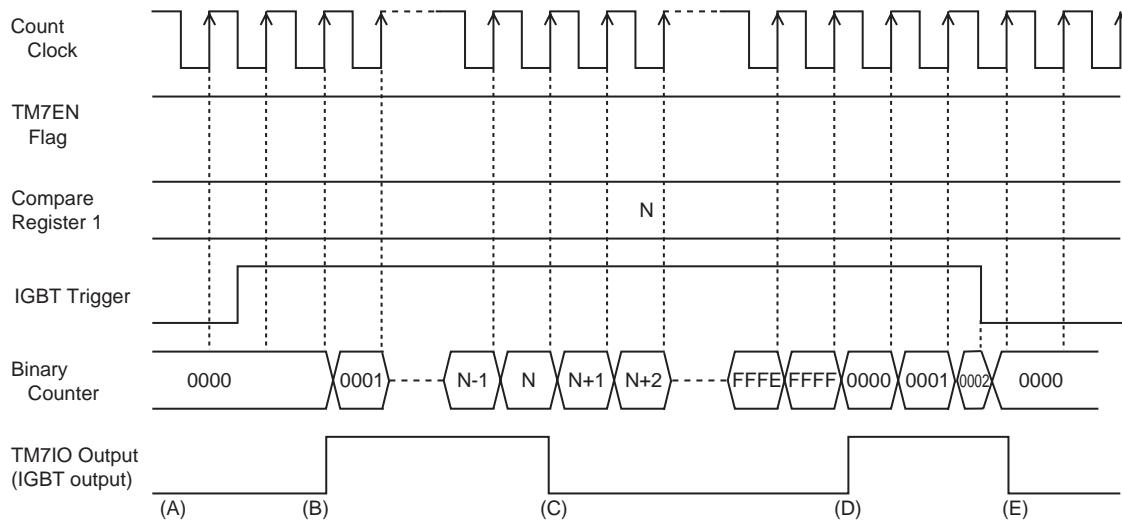


Figure:7.11.1 Count Timing of Standard IGBT Output (At Normal)

- (A) When IGBT trigger is input, IGBT operation becomes valid after 1 count clock. After IGBT output is valid, it is "L" until the next count clock.
- (B) When IGBT trigger is valid, it is "H" during the period when the value of the binary counter reaches that of TM7OC2 from 0x0000. ("H" output from 0x0001 at the first operation cycle)
- (C) After the TM7OC2 compare match, it is "L" and the binary counter counts up until the counter reaches the TM7OC1 compare register to be cleared.
- (D) When the binary counter is cleared, it becomes "H" again.
- (E) When IGBT trigger becomes invalid, the timer is initialized and IGBT output forcibly becomes "L".

■ Count Timing of Standard IGBT Output (When the compare register 1 is 0x0000) (Timer 7)

The following shows the count timing as the compare register 1 is set to 0x0000.

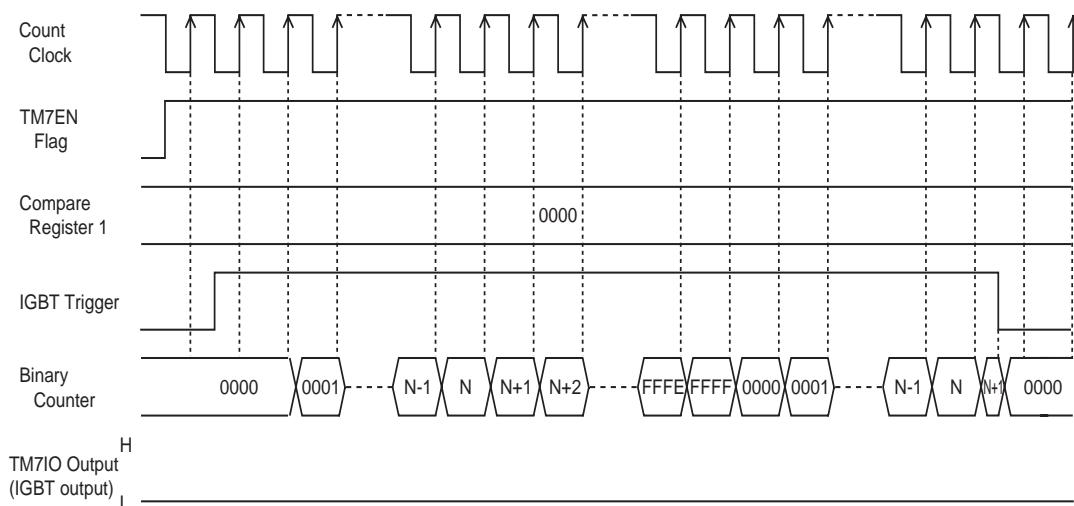


Figure:7.11.2 Count Timing of Standard IGBT Output (When the compare register 1 is 0x0000)

When TM7EN flag is set to "0" (stop status), IGBT output is "L".

■ Count Timing of Standard IGBT Output (When the compare register 1 is 0xFFFF) (Timer 7)

The following shows the count timing as the compare register 1 is set to 0xFFFF.

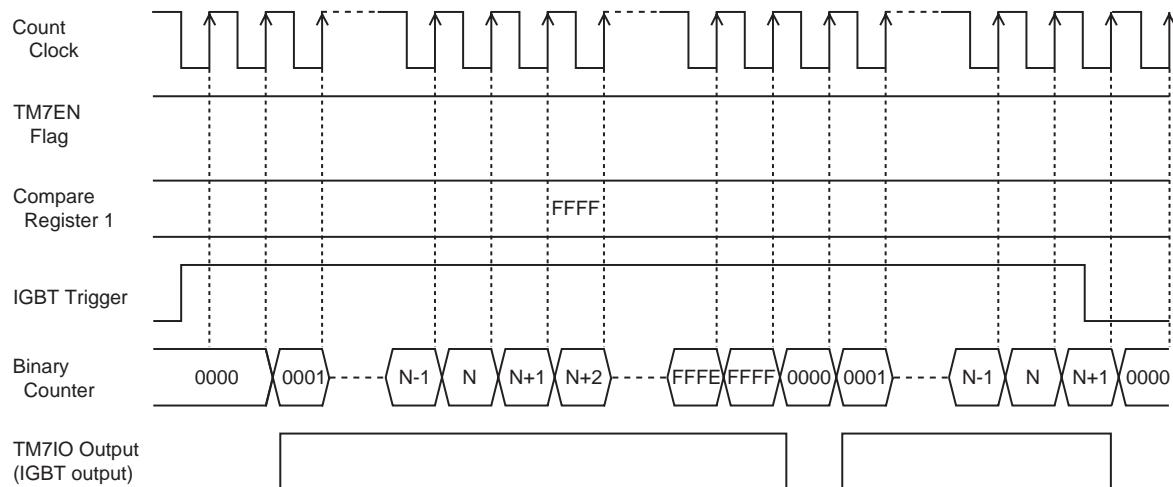


Figure:7.11.3 Count Timing of Standard IGBT Output (When the compare register 1 is 0xFFFF)



When used for standard IGBT output, set the TM7BCR flag of the TM7MD2 register to "0" and select the full count overflow as the binary counter clear factor and the IGBT output set ("H" output) factor.



TM7OC1 compare match or TM7OC2 compare match can be selected as the IGBT output reset ("L" output) factor by the T7PWMSL flag of the TM7MD2 register.

7.11.2 Setup Example

■ Standard IGBT Output Setup Example (Timer 7)

At the interrupt generation edge of the external interrupt 0 input signal, TM7IOA output pins output the waveform of 1/4 duty IGBT waveform at 152.59 Hz using the timer 7. Frequency for high speed operation (fpll) is 10 MHz. Required period for one IGBT output waveform cycle depends on the overflow time of the binary counter. “H” period of IGBT output waveform depends on the set value of the compare register 1.

An example setup procedure, with a description of each step is shown below.

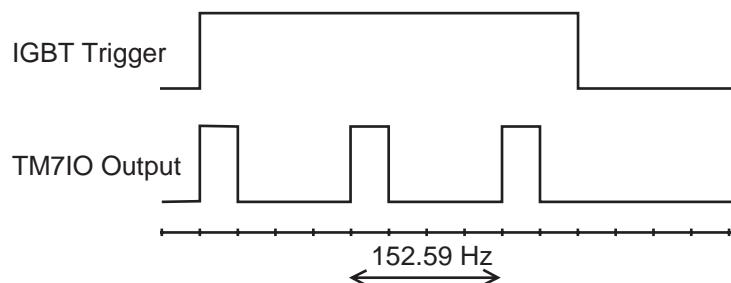


Figure 7.11.4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to “0” to stop the timer 7 counting.
(2) Set the special function pin to output PAOMD (0x03EE6) bp5:PAOMD5 =1 PADIR (0x03F3A) bp5:PADIR5 =1	(2) Set the PAOMD5 flag of the port A output mode register (PAOMD) to “1” to set the PA5 pin as a special function pin. Set the PADIR5 flag of the port A direction control register (PADIR) to “1” to set the output mode. [Chapter 4 I/O Ports]
(3) Set IGBT output TM7MD3(0x03F8E) bp2:T7IGBTEN =1 TM7MD2(0x03F79) bp4:TM7PWM =1 TM7MD1(0x03F78) bp5:TM7CL =0	(3) Set the T7IGBTEN flag of the timer 7 mode register 3 (TM7MD3) to “1”, the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to “1” to select IGBT output. Set TM7CL flag of the timer 7 mode register 1 (TM7MD1) to “0” to enable of timer output.
(4) Set the standard IGBT output operation TM7MD2(0x03F79) bp5:TM7BCR =0	(4) Set the TM7BCR flag of the TM7MD2 register to “0” to select the full count overflow as the clear factor of the binary counter.
(5) Select IGBT trigger generation interrupt source TM7MD3(0x03F8E) bp1-0:T7IGBT1-0 =01	(5) Set the external interrupt 0 (IRQ0) input as IGBT trigger generation factor by the T7IGBT1 to 0 flag of the TM7MD3 register.

Setup Procedure	Description
(6) Select the trigger level TM7MD3(0x03F8E) bp4:T7IGBTTR=1	(6) Set the T7IGBTTR flag of the TM7MD3 register to "1" to set the IGBT trigger level to "H".
(7) Select the dead time TM7MD4(0x03F6E) bp3:T7NODED =1	(7) Set the T7NODED flag of the TM7MD4 register to "1" to select without dead time.
(8) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(8) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.
(9) Set "H" period of the IGBT output TM7PR1(0x03F75, 0x03F74) = 0x3FFF	(9) Set the "H" period value of the IGBT output on the timer 7 preset register 1 (TM7PR1). Set the value as $65536 / 4-1 = 16383$ (0x3FFF) to make the IGBT output 1/4 duty of the full count 65536.
(10) Enable of external interrupt 0 IRQCNT (0x03F3D) bp0:P20EN =1	(10) Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.
(11) Start the timer operation TM7MD1(0x03F78) bp4: TM7EN= 1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to enable the operation of the timer 7. After "H" is input to the P20, IGBT is output from the PA5.

TM7BC is counting from 0x0000 by external interrupt 0 input signal. IGBT output waveform is "H". When the value of TM7BC register correspond with the setting value of TM7OC2 register, IGBT output waveform is "L". After that, TM7BC continues counting. Once the value of TM7BC register overflows, IGBT output waveform is "H" again and TM7BC is counting from 0x0000.

7.12 Dead Time IGBT Output

IGBT output with dead time generates the waveform, inclusive ON or OFF time delay, during the standard IGBT signal inversion. And the formed waveform is output through TM7IO and TM8IO pins. Startup trigger can be selected by the external interrupt 0, 1 and 2 or starting of the timer 7 count operation.

7.12.1 Operation

■ Dead Time IGBT Output Operation (Timer 7)

Dead time IGBT output can be selected at the T7NODED of the timer 7 mode register 4 (TM7MD4). Also, dead time can be set to the dead time preset register 1 and 2 (TM7DEADPR1, 2). Only the timer 7 of 16-bit timer can use dead time IGBT output functions.

■ IGBT Trigger Selection

IGBT trigger can be selected from IRQ0, IRQ1, IRQ2 and the start of the timer 7 count operation.

Setup should be done at the T7IGBT0 and T7IGBT1 flag of the TM7MD3 register. When the startup is controlled from external of the micro controller, one of IRQ0 to IRQ2 should be selected. This trigger detects the input level before activation. Either “H” or “L” level can be selected with the T7IGBTTR flag of the TM7MD3 register. When “1” is selected, count operation continues while the trigger pin is “H”. When “0” is selected, count operation continues while the trigger pin is “L”.

To control the startup by the commands, timer 7 count operation should be selected. In that case, timer count operation or IGBT output are controlled by the TM7EN flag of the TM7MD1 register. When “1” (count operation) is selected, count continues counting until “0” (count stop) is set. Make sure to set the T7IGBT0, 1 of the TM7MD3 register before operating the TM7EN flag of the TM7MD1 register. In that case, setup of T7IGBTTR is neglected. The binary counter is cleared as the counting stops. The value is loaded from the preset register to the compare register in synchronization with the counter clock.

■ Dead Time Count

Dead time counter counts the timer clock source. When the dead time insert is set as rising standard, set the period from the falling of TM8IO to the rising of TM7IO to the dead time preset register 1 (TM7DPR1) and the period from the falling of TM7IO to the rising of TM8IO to the dead time preset register 2 (TM7DPR2). Dead time is inserted for the period of the set value + 1. Only for the period from the IGBT output is enabled by the IGBT trigger to the first rising of TM7IO (in the case of the IGBT falling standard), the set value of the TM7DPR1 + 2 is inserted to the dead time. (1 count clock should be longer than usually.)

■ Count Timing of Dead Time IGBT Output (Timer 7)

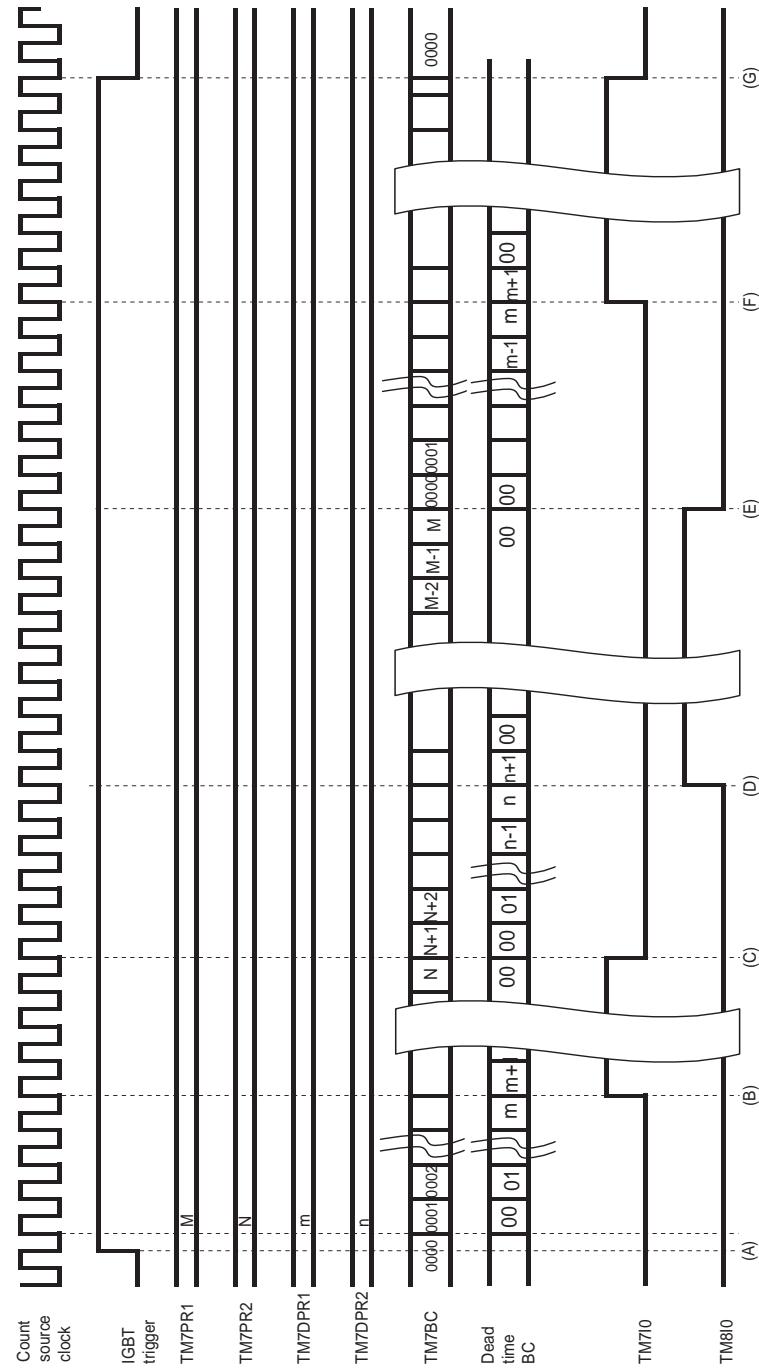


Figure:7.12.1 Count Timing of Dead Time IGBT Output (Timer 7)

Output waveform of the IGBT with dead time (at falling-edge standard)

- (A)TM7IO="L", TM8IO="L" until the IGBT trigger is input and become valid.
- (B)After the trigger is input and after 1 count clock rising edge of the next count clock + count clock × (value of the dead time preset register 1 + 1) output voltage of TM7IO is increased.
- (C)After the compare matching (the value of the binary counter matches that of TM7OC2), and after 1 count clock, output voltage of TM7IO is decreased.
- (D)After TM7IO output voltage is decreased and after count clock × (value of the dead time preset register 2 + 1), output voltage of TM8IO is increased.
- (E)After the compare matching (the value of the binary counter matches that of TM7OC1) and after 1 count clock, output voltage of TM8IO is decreased.
- (F)After TM8IO output voltage is decreased and after count clock × (value of the dead time preset register 1 + 1), output voltage of TM7IO is increased.
- (G)When IGBT trigger becomes invalid, both TM7IO and TM8IO become "L" right away.



Set as TM7OC2 value ≤ TM7OC1 value.

When TM7OC2 value > TM7OC1 value, the IGBT output waveform is fixed as TM7IO="L", TM8IO="L" at falling edge standard.



If IGBT trigger is enabled within 2 cycles of count clock after IGBT trigger is disabled, the following cases may occur:

- the value set in the preset register during IGBT operation may not be loaded to the compare register.
- the value set in the dead time preset register during IGBT operation may not be reflected.



If the event input (TM7IO) is selected as the count clock source, the following cases may occur when IGBT trigger is disabled:

- the value set in the preset register during IGBT operation may not be loaded to the compare register.
- the value set in the dead time preset register during IGBT operation may not be reflected.



When the event input (TM7IO) is selected as the count clock source, the value which is entered on the dead time preset register while IGBT operation halt may not be reflected. To prevent this, select the system clock (fs) as the count clock source and enter the value on the dead time preset register. Then, select the event input (TM7IO) as the count clock source and start the IGBT operation.



When IRQ0, IRQ1, or IRQ2 is selected as the IGBT trigger, the timing of IGBT operation start may delay up to 1 count clock.

■ One Shot Pulse Output Setup

One shot pulse can be output by setting the T7ONESHOT flag of the TM7MD4 register to “1”.

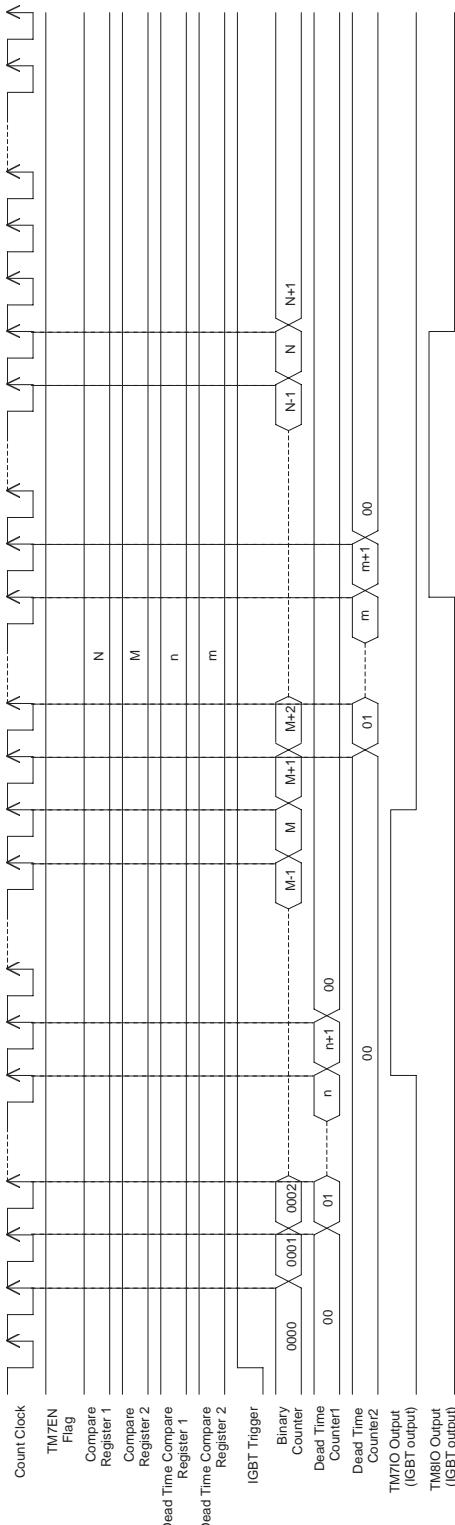


Figure:7.12.2 Count Timing of Dead Time IGBT One Shot Pulse Output (Timer 7)

■ Count Timing of Dead Time High Precision IGBT Output
(BC operation when IGBT trigger disable:T7IGBTCNT=1) (Timer 7)

Setting the T7IGBTCNT flag of the timer 7 mode register 4 (TM7MD4) to “1” can continuous operation of binary counter when IGBT trigger disable.

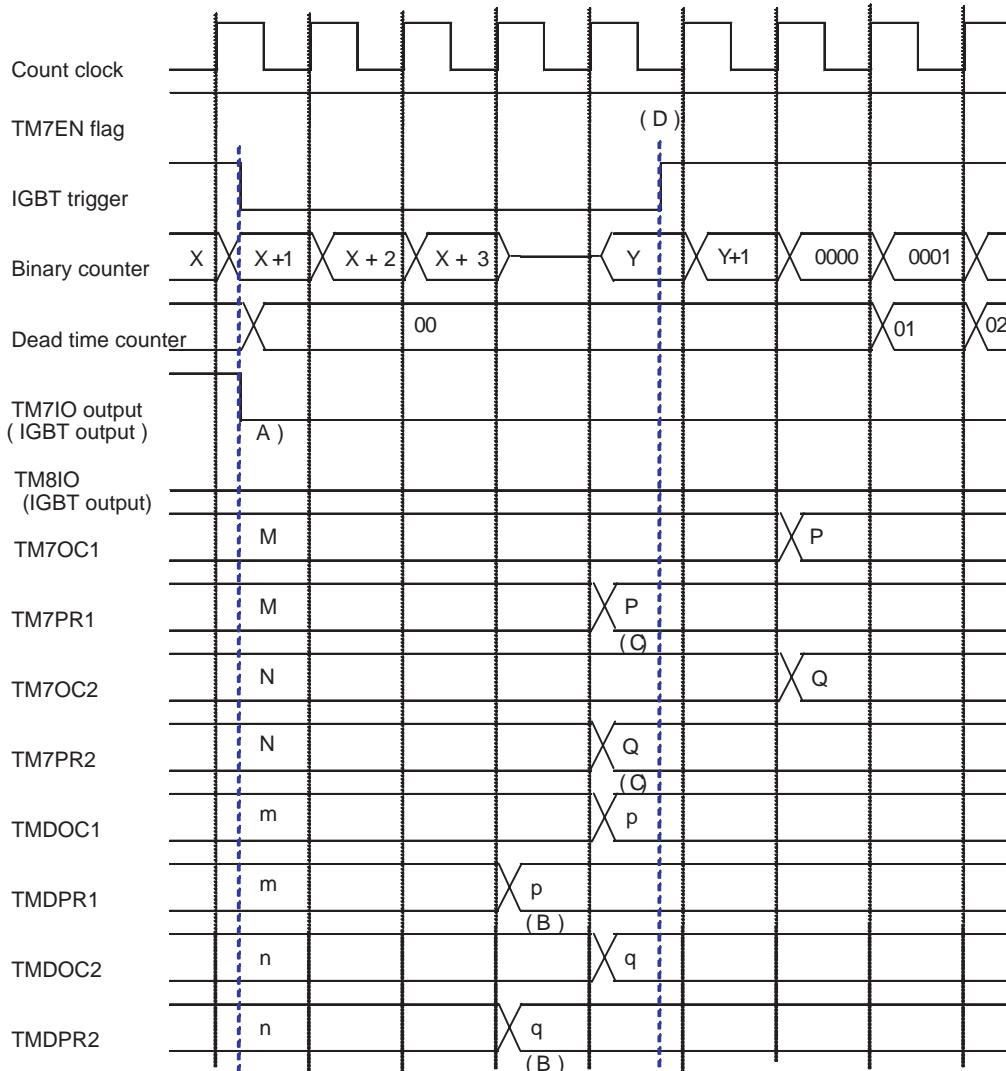


Figure:7.12.3 Count Timing of Dead Time High Precision IGBT Output
(BC operation when IGBT trigger disable:T7IGBTCNT=1) (Timer 7)

Dead time high precision IGBT output (at continuous counting/ falling-edge standard)

- (A) When the IGBT trigger becomes invalid, TM7IO=”L”, TM8IO=”L” and the dead time counter is cleared to “00”. At the time, binary counter continues counting.
- (B) If values are loaded to the dead time preset register when the IGBT trigger is invalid, values will be loaded to the dead time compare register at the rising edge of the next count clock.
- (C) Even if values are written to the preset register when the IGBT trigger is invalid, because binary counter is in operation, values will not be loaded to the compare register until the next compare match or the IGBT trigger becomes valid
- (D) When the IGBT trigger becomes valid again, binary counter is cleared to 0x0000 at the rising edge of after-2 count clock. Also, values are loaded from the preset register to the compare register.

- Count Timing of Dead Time High Precision IGBT Output (Trigger edge reception is disabled during active output:T7TRGACT=1)

Setting the T7TRGACT flag of the timer 7 mode register 4 (TM7MD4) to “1” enables IGBT output without disrupting PWM waveform even if IGBT trigger is disabled during IGBT output operation.

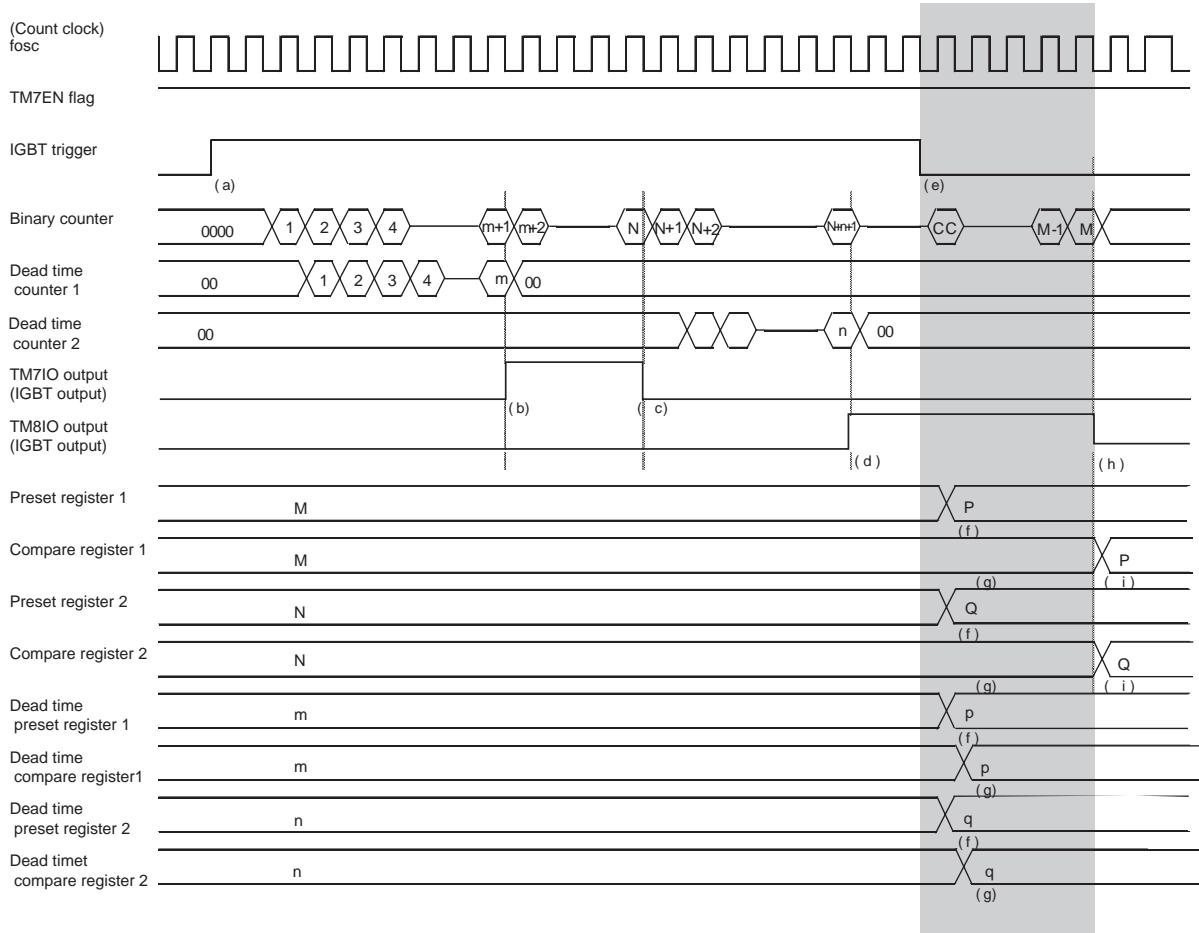


Figure:7.12.4 Count Timing of Dead Time High Precision IGBT Output (Trigger edge reception is disabled during active output:T7TRGACT=1)

- The IGBT trigger becomes valid the count operation begins.
- The value of the dead time counter 1 and the dead time compare register 1 match, and ‘H’ is output to TM7IO.
- The value of the binary counter and the compare register 2 match, and TM7IO = ‘L’. Also, the dead time counter 2 begins count operation.
- The value of the dead time counter 2 and the dead time compare register 2 match, and ‘H’ is output to TM8IO.
- The IGBT trigger becomes invalid but the binary counter continues count operation because T7TRGACT flag is valid.
- When the IGBT trigger is ‘L’ and IGBT output is in operation, values are written to the preset register 1 and 2, and the dead time preset register 1 and 2.
- Since the binary counter is in operation, values are not loaded to the compare register 1 and 2. However, the values same as the dead time preset register 1 and 2 are loaded to the dead time compare register 1 and 2 at the next count clock, as usual.
- The value of the binary counter and the compare register 1 match, and TM8IO becomes ‘L’. Also, the value of preset register 1 and 2 are loaded to the compare register 1 and 2.

7.12.2 Setup Example

■ Dead Time IGBT Output Setup Example (Timer 7)

At the interrupt generation edge of the external interrupt 0 input signal, TM7IO and TM8IO output pins output the waveform of 1/4 duty IGBT waveform at 200 Hz with 0.01 ms, 0.02 ms dead time by the falling standard using the timer 7. Select fpll/1 (at fpll=8.0 MHz) as the clock source. Required period for one IGBT output waveform cycle depends on the set value of the compare register 1. “H” period of IGBT output standard waveform depends on the set value of the compare register 2. Dead time period depends on the value of the dead time preset register 1 and 2.

An example setup procedure, with a description of each step is shown below.

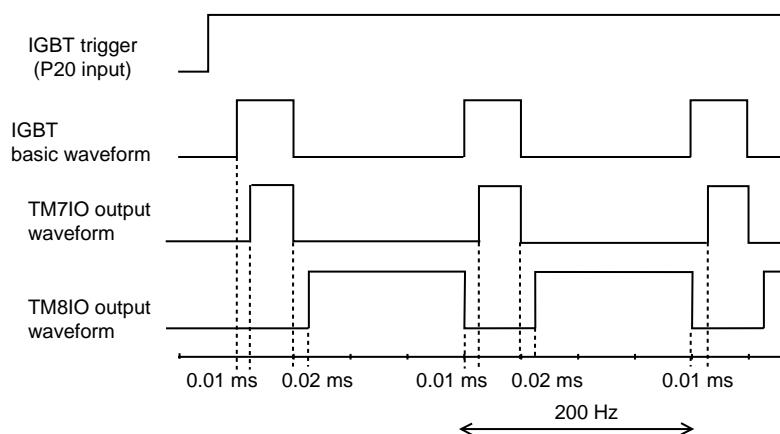


Figure 7.12.5 Output Waveform of TM7IO Output Pin and TM8IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to “0” to stop the timer 7 counting.
(2) Set the dead time IGBT output operation TM7MD2(0x03F79) bp5:TM7BCR =1 bp6:T7PWMSL =1	(2) Set the TM7BCR flag of the TM7MD2 register to “1” to select the TM7OC1 compare register match as the binary counter clear source. Also, set the T7PWMSL flag to “1” to select the TM7OC2 compare match as the duty decision source of the IGBT output.
(3) Select IGBT/timer startup factor TM7MD3(0x03F8E) bp1-0:T7IGBT1-0 =01	(3) Select the external interrupt 0 (IRQ0) input as the IGBT/timer startup factor by the T7IGBT1 to 0 flag of the TM7MD3 register.
(4) Select the interrupt generation valid edge TM7MD3(0x03F8E) bp4:T7IGBTTR =0	(4) Set the T7IGBTTR flag of the TM7MD3 register to “1” to set IGBT trigger level “H”.
(5) Set the dead time edge TM7MD3(0x03F8E) bp3:T7IGBTDT =0	(5) Set the T7IGBTDT flag of the timer 7 mode register 3 (TM7MD3) to “0” to select the falling standard as the dead time insert timing.

Setup Procedure	Description
(6) Enable of external interrupt 0 input IRQCNT (0x03F3D) bp0:P20EN =1	(6) Set P20EN flag of the IRQCNT register to “1” to enable of external interrupt 0 input.
(7) Set the interrupt level IRQ0ICR(0x03FE2) bp7-6:IRQ0LV1-0 =10	(7) Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register. If any interrupt request flag is already set, clear it.
(8) Enable the interrupt IRQ0ICR(0x03FE2) bp1:IRQ0IE =1	(8) Set the IRQ0IE flag of the IRQ0ICR register to “1” to enable the interrupt.
(9) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(9) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.
(10) Set the IGBT output cycle TM7PR1(0x03F75, 0x03F74) =0x9C3F	(10) Set the IGBT output cycle to the timer 7 preset register 1 (TM7PR1). To set 200 Hz by dividing 8.0 MHz, set as; 40000/4-1=39999 (0x9C3F) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(11) Set “H” period of the IGBT output TM7PR2(0x03F7D, 0x03F7C) =0x270F	(11) Set the “H” period of the IGBT waveform to the timer 7 preset register 2 (TM7PR2). To set 1/4 duty of 40000 dividing, set as; 40000/4-1=9999 (0x0x270F) At the same time, the same value is loaded to the timer 7 compare register 2 (TM7OC2).
(12) Set the dead time TM7DPR1(0x03F7E) = 0x4F TM7DPR2(0x03F7F) = 0x9F	(12) Set the period from the falling of the TM8IO to the rising of the TM7IO to the timer 7 preset register 1 (TM7DPR1) and from the falling of the TM7IO to the rising of the TM8IO to the timer 7 preset register 2 (TM7DPR2). To make dead time which is from the TM7IO falling to the TM8IO rising is 0.02 ms and from the TM8IO falling to the TM7IO rising is 0.01 ms, set 0x4F to the timer 7 dead time preset register 1 and 0x9F to the timer 7 dead timer preset register 2.
(13) Set the IGBT output TM7MD2 (0x03F79) bp4:TM7PWM =1 TM7MD3 (0x03F8E) bp2:T7IGBTEN =1 TM8MD4 (0x03F6F) bp2:TM8SEL =1 TM7MD1 (0x03F78) bp5:TM7CL =0	(13) Set TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to “1” and set T7IGBTEN flag of the timer 7 mode register 3 (TM7MD3) to “1” to select the dead time IGBT output. Set TM8SEL_A flag of the timer 8 mode register 4 (TM8MD4) to “1” to select the timer 7 IGBT output. Set TM7CL flag of the timer 7 mode register 1 (TM7MD1) to “0” to enable the timer output.

Setup Procedure	Description
(14) Set the output of special function pins PAOMD(0x03EE6) bp5:PAOMD5 =1 bp6:PAOMD6 =1 PADIR(0x03F3A) bp5:PADIR5=1 bp6:PADIR6=1	(14) Set the PAOMD5 flag of the port A output mode register (PAOMD) to “1” to set the PA5 pin to the special function pin. Set the PAOMD6 flag of the port A output mode register (PAOMD) to “1” to set the PA6 pin to the special function pin. Set the PADIR5 flag of the port A direction control register (PADIR) to “1”, the PADIR6 flag to “1” to set the output mode. Add pull-up/pull-down resistor if necessary. [Chapter 4. I/O Ports]
(15) Start the timer operation TM7MD1(0x03F78) bp4: TM7EN= 1	(15) Set the TM7EN flag of the TM7MD1 register to “1” to operate the timer 7. After “H” is input to P20 pin, IGBT is output from PA5, PA6.

TM7BC counts up from 0x0000. The IGBT output waveform outputs “H” until TM7BC matches the set value of the TM7OC2 register. Once they match, it outputs “L”. After that, TM7BC continues to count up. Once TM7BC value matches the TM7OC1 register value to be cleared, the IGBT output waveform outputs “H” and TM7BC counts up from 0x0000 again. TM7IO pin outputs dead time worth of IGBT output waveform. TM8IO pin outputs dead time worth of inverted IGBT output waveform.

7.13 16-bit Timer Cascade Connection

7.13.1 Operation

Cascading timers 7 and 8 forms a 32-bit timer.

■ 16-bit Timer Cascade Connection Operation (Timer 7 + Timer 8)

Timer 7 and timer 8 are combined to be a 32-bit timer. Cascading timer is operated at clock source of timer 7 which are lower 16 bits.

Table:7.13.1 Timer Function at Cascade Connection

	Timer 7+Timer 8 (32-bit)
Interrupt source	TM8IRQ,TM8OC2IRQ
Timer operation	✓
Timer pulse output	✓ (TM8IO output)
PWM output	✓
Synchronous output	-
Clock source	fpll fpll/2 fpll/4 fpll/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IOi input/16 TimerA output TimerA output/2 TimerA output/4 TimerA output/16
fpll:Machine clock (High frequency oscillation) fs:System clock [Chapter 2.6. Clock Switching]	

At cascade connection, the binary counter and the compare register are operated as a 32-bit register. At operation, set the TM7EN flag of the lower 16-bit timers to “1” to be operated. Also, select the clock source with the lower 16-bit timer. Other setup and count timing are the same as the 16-bit timer at independently operation.



At cascade connection, timer 8 interrupt factor is only counter-clear.



When timer 7 and timer 8 are used in the cascade connection, timer 8 is used as the interrupt request flag. Timer pulse output of timer 7 is "L" fixed output.
The interrupt request of timer 7 is not generated. But timer 7 interrupt should be disabled.



The preset registers (TM7PR1 and TM8PR1, TM7PR2 and TM8PR2) cannot be written at once that if the loading timing from the preset register to the compare register occurs at the same time as the writing timing of the preset register, the correct data is not loaded. To prevent this, it puts into the count stop condition and rewrite the preset register once.



Stop the timer in order to read out the correct value of the timer in cascade connection.

7.13.2 Setup Example (Timer Operation)

■ Cascade Connection Timer Setup Example (Timer 7 + Timer 8)

Setting example of timer function that the interrupt is constantly generated by cascade connection of timer 7 and timer 8, as 32-bit timer is shown. An interrupt is generated in every 100000 cycles (40 ms) by selecting source clock to $fs/2$ ($fpll=10\text{ MHz}$, $fs=fpll/2$).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM7MD1 (0x03F78) bp4:TM7EN= 0 TM8MD1 (0x03F88) bp7:TM8EN = 0	(1) Set the TM7EN flag of the timer 7 mode register (TM7MD1) to "0" and the TM8EN flag of the timer 8 mode register (TM8MD1) to "0" to stop the timer 7 and the timer 8 counting.
(2) Select the timer clear source TM7MD2 (0x03F79) bp5:TM7BCR =1	(2) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the binary counter clear source.
(3) Select the normal lower operation TM7MD2 (0x03F79) bp2:T7ICEN= 0 bp4:TM7PWM=0	(3) Set the T7ICEN flag and TM7PWM flag of the TM7MD2 register to "0" to select the normal timer operation.
(4) Set the cascade connection TM8MD3 (0x03F8F) bp0:TM8CAS=1	(4) Set the TM8CAS flag of the TM8MD3 register to "1" to connect the timer 7 and the timer 8 to the cascade.
(5) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0=01 bp3-2:TM7PS1-0=01	(5) Select fs as the clock source by the TM7CK1 to 0 of the TM7MD1 register. Also, select 1/2 of fs as the count clock source by the TM7PS1 to 0 flag.
(6) Select IGBT / timer activation factor TM7MD3 (0x03F8E) bp1-0:T7IGBT1-0=00	(6) Set the IGBT / timer activation factor to the timer 7 count.
(7) Set the interrupt generation cycle TM7PR1 (0x03F75, 0x03F74)=0x869F TM8PR1 (0x03F85, 0x03F84)=0x0001	(7) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1) and the timer 8 preset register (TM8PR1). (100000 cycles-1). At the same time, the same values as the preset registers are loaded to the timer 7 compare register 1 (TM7OC1) and the timer 8 compare register (TM8OC1), and the binary counters (TM7BC, TM8BC) are initialized to 0x00000.
(8) Disable the lower timer interrupt TM7ICR (0x03FEF) bp1:TM7IE=0	(8) Set the TM7IE flag of the timer 7 interrupt control register (TM7ICR) to "0" to disable the interrupt.

Setup Procedure	Description
(9) Set the upper timer interrupt level TM8ICR (0x03FF1) bp7-6:TM8LV1=0=10	(9) Set the interrupt level by the TM8LV1 to 0 flag of the timer 8 interrupt control register (TM8ICR). If any interrupt request flag is already set, clear it. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(10) Enable the upper timer interrupt TM8ICR (0x03FF1) bp1:TM8IE=1	(10) Set the TM8IE flag of the TM8ICR register to "1" to enable the interrupt.
(11) Start the lower timer operation TM7MD1 (0x03F78) bp4:TM7EN=1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

TM7BCL+TM7BCH+TM8BCL+TM8BCH counts up from 0x00000000 as a 32-bit timer.

When TM7BCL+TM7BCH+TM8BCL+TM8BCH reaches the set value of TM7OC1L+TM7OC1H+TM8OC1L+TM8OC1H register, the timer 8 interrupt request flag is set at the next count clock and the value of TM7BCL+TM7BCH+TM8BCL+TM8BCH becomes 0x00000000 to restart count up.

7.13.3 Setup Example (PWM Operation)

■ Cascade Connection PWM Output Setup Example (Timer 7 + Timer 8)

TM8IOA output pin outputs the 1/10 duty PWM output waveform at 1/60 Hz with the cascade connection of timer 7 and timer 8, as a 32-bit timer. Select fpll/1 (fpll=8 MHz, at operation) as the clock source. One cycle of the PWM output waveform is depending on the set value of the compare register 1. “H” period of the PWM output waveform is depending of the set value of the compare register 2.

An example setup procedure, with a description of each step is shown below.

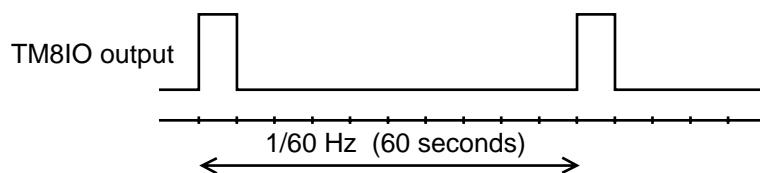


Figure 7.13.1 Output Waveform of TM8IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM7MD1 (0x03F78) bp4:TM7EN=0 TM8MD1 (0x03F88) bp7:TM8EN=0	(1) Set the TM7EN flag of the timer 7 mode register (TM7MD1) to “0”, the TM8EN flag of the timer 8 mode register (TM8MD1) to “0” to stop the timer 7 and the timer 8 counting.
(2) Set the special function pin to output PAOMD (0x03EE6) bp6:PAOMD6=1 PADIR (0x03F3A) bp6:PADIR6=1	(2) Set the PA0MD6 flag of the port A output mode register (PAOMD) to “1” to set the PA6 pin as the special function pin. Set the PADIR6 flag of the port Adirection control register (PADIR) to “1” to set the output mode. Add pull-up/pull-down register, if necessary. [Chapter 4. I/O Ports]
(3) Set the cascade connection TM8MD3 (0x03F8F) bp0:TM8CAS=1	(3) Set the TM8CAS flag of the TM8MD3 register to “1” to connect the timer 7 and the timer 8 to the cascade.
(4) Set the PWM output TM7MD2 (0x03F79) bp4:TM7PWM=1	(4) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to “1” to select the PWM output.
(5) Set the high precision PWM output operation TM7MD2 (0x03F79) bp5:TM7BCR=1 bp6:T7PWMSL=1	(5) Set the TM7BCR flag of the TM7MD2 register to “1” to select the TM7OC1 compare match as the binary counter clear source. Also, set the T7PWMSL flag to “1” to select the TM7OC2 compare match as the duty of the PWM output.
(6) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0=00 bp3-2:TM7PS1-0=00	(6) Select fpll as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.

Setup Procedure	Description
(7) Select IGBT timer activation factor TM7MD3 (0x03F8E) bp1-0:TM7IGBT1-0=00	(7) Set the IGBT / timer activation factor to the timer 7 count.
(8) Set the PWM output cycle TM7PR1 (0x03F75,0x03F74) = 0x37FF TM8PR1 (0x03F85,0x03F84) = 0x1C9C	(8) Set the PWM output cycle to the timer 7 preset register 1 (TM7PR1) and the timer 8 preset register 1 (TM8PR1). To set 1/60 Hz by dividing 8 MHz, set as; 480.000.000-1=479.999.999 (0x01C9C37FF') At the same time, the same values are loaded to the timer 7 compare register 1 (TM7OC1) and the timer 8 compare register 1 (TM8OC1), and the timer 7 binary counter (TM7BC) and the timer 8 binary counter (TM8BC) are initialized to 0x00000.
(9) Set "H" period of the PWM output TM7PR2 (0x03F7D,0x03F7C) = 0x6BFF TM8PR2 (0x03F8D,0x03F8C) = 0x02DC	(9) Set "H" period of the PWM output to the timer 7 preset register 2 (TM7PR2) and the timer 8 preset register 2 (TM8PR2). To set 1/10 duty of 480.000.000 dividing, set as; 480.000.000/10-1=47.999.999 (0x002DC6BFF) At the same time, the same values are loaded to the timer 7 compare register 2 (TM7OC2) and the timer 8 compare register 2 (TM8OC2).
(10) Start the timer operation TM7MD1 (0x03F78) bp4:TM7EN=1	(10) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7 and the timer 8.

TM7BCL + TM7BCH + TM8BCL + TM8BCH counts up from 0x00000000 as a 32-bit timer. The TM8IO outputs "H" until TM7BCL + TM7BCH + TM8BCL + TM8BCH reaches the set value of the TM7OC2L + TM7OC2H + TM8OC2L + TM8OC2H register. Once they match, it outputs "L". After that, TM7BCL + TM7BCH + TM8BCL + TM8BCH continues to count up, once TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H reaches the TM7BCL + TM7BCH + TM8BCL + TM8BCH register to be cleared, the TM8IO outputs "H" again and TM7BCL + TM7BCH + TM8BCL + TM8BCH counts up from 0x00000000 again.



In the initial state of the PWM output, "L" output is changed to "H" output as the PWM output is selected by the TM7PWM flag of the TM7MD2 register.



Set value should be set as;
TM7OC2L + TM7OC2H + TM8OC2L + TM8OC2H ≤
TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H.
If it is set as;
TM7OC2L + TM7OC2H + TM8OC2L + TM8OC2H ≥
TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H,
the PWM output is a "H" fixed output.

8

Chapter 8 Time Base Timer / Free-running Timer

8.1 Overview

This LSI has a time base timer and a 8-bit free-running timer (timer 6).

Time base timer is a 15-bit timer counter.

8.1.1 Functions

Table:8.1.1 shows the clock source and the interrupt generation cycle that timer 6 and time base timer can use.

Table:8.1.1 Clock Source and Generation Cycle

	Time base timer	Timer 6 (8-bit free-running)
8-bit timer operation	×	O
Interrupt	TBIRQ	TM6IRQ
Clock source	fpll fx	fpll fx fs $fpll \times 1/2^7$ *1 $fpll \times 1/2^{13}$ *1 $fx \times 1/2^{12}$ *2 $fx \times 1/2^{13}$ *2 synchronous fx synchronous $fpll \times 1/2^{12}$ *1 synchronous $fpll \times 1/2^{13}$ *1 synchronous $fx \times 1/2^{12}$ *2 synchronous $fx \times 1/2^{13}$ *2
Interrupt generation cycle	$fpll \times 1/2^7$ $fpll \times 1/2^8$ $fpll \times 1/2^9$ $fpll \times 1/2^{10}$ $fpll \times 1/2^{13}$ $fpll \times 1/2^{15}$ $fx \times 1/2^7$ $fx \times 1/2^8$ $fx \times 1/2^9$ $fx \times 1/2^{10}$ $fx \times 1/2^{13}$ $fx \times 1/2^{15}$	The interrupt generation cycle is decided by the arbitrary value written to TM6OC.
fpll: Machine clock (High speed oscillation) fx: Machine clock (Low speed oscillation) fs: System clock [Chapter 2. 2.6 Clock Switching] *1 Can be used when a clock source of time base timer is selected to 'fpll'. *2 Can be used when a clock source of time base timer is selected to 'fx'.		

8.1.2 Block Diagram

■ Timer 6, Time Base Timer Block Diagram

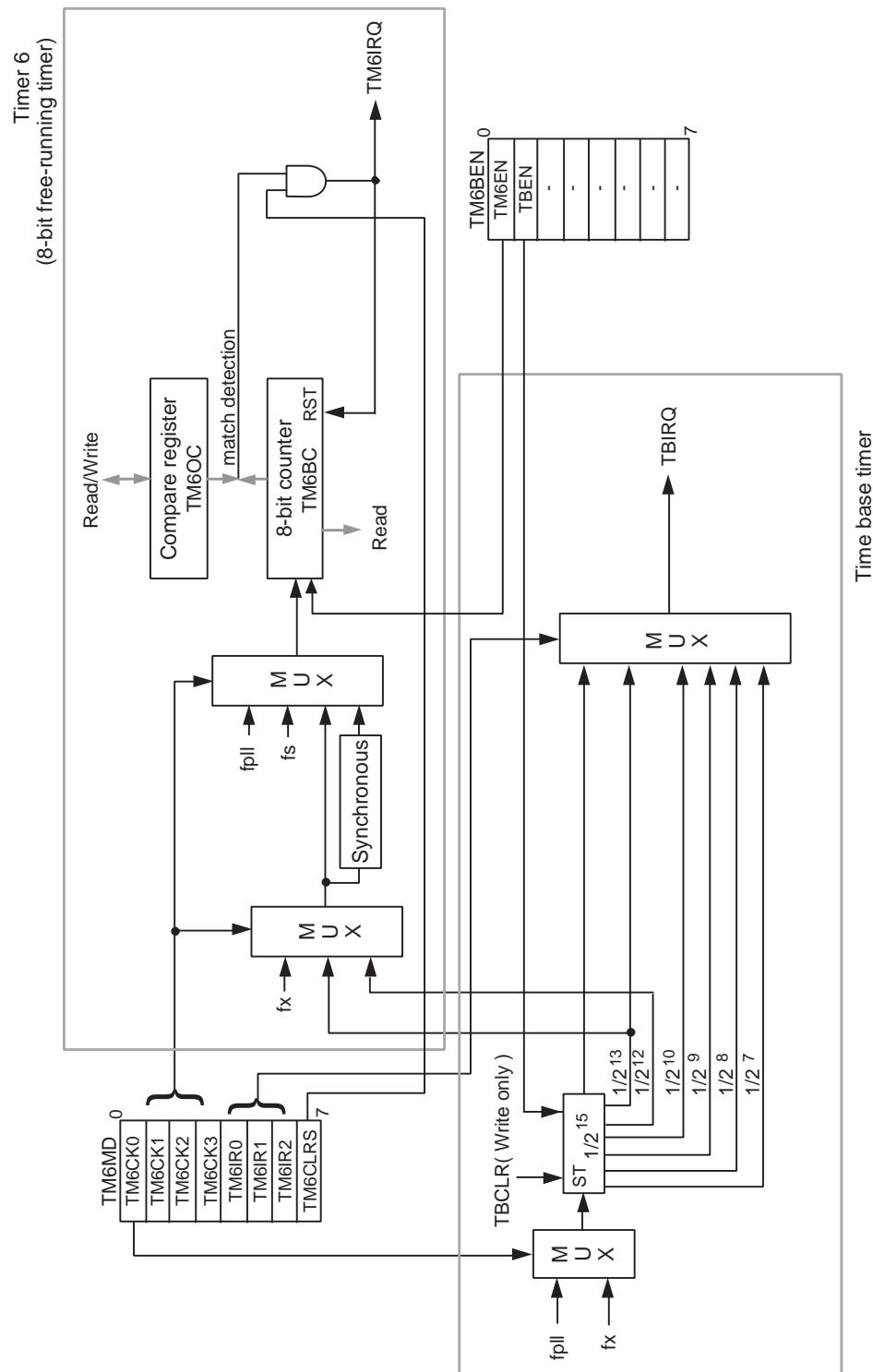


Figure 8.1.1 Block Diagram (Timer 6, Time Base Timer)

8.2 Control Registers

Timer 6 consists of binary counter (TM6BC), compare register (TM6OC), and is controlled by mode register (TM6MD). Time base timer is controlled by mode register (TM6MD) and time base timer clear register (TBCLR). Both timers are operated by the enable signal of the timer 6 enable register (TM6BEN).

8.2.1 Control Registers

Table:8.2.1 shows the registers that control timer 6, time base timer.

Table:8.2.1 Control Registers

	Register	Address	R/W	Function	Page
Timer 6	TM6BC	0x03F68	R	Timer 6 binary counter	VIII-5
	TM6OC	0x03F69	R/W	Timer 6 compare register	VIII-5
	TM6MD	0x03F6A	R/W	Timer 6 mode register	VIII-7
	TM6BEN	0x03F6C	R/W	Timer 6 enable register	VIII-6
	TM6ICR	0x03FED	R/W	Timer 6 interrupt control register	III-26
Time base timer	TM6MD	0x03F6A	R/W	Timer 6 mode register	VIII-7
	TBCLR	0x03F6B	W	Time base timer clear control register	VIII-5
	TBICR	0x03FEE	R/W	Time base interrupt control register	III-27

8.2.2 Programmable Timer Registers

Timer 6 is a 8-bit programmable counter.

Programmable counter consists of compare register (TM6OC) and binary counter (TM6BC).

Binary counter is a 8-bit up-counter. When the TM6CLRS flag of the timer 6 mode register (TM6MD) is "0" and the interrupt cycle data is written to the compare register (TM6OC), the timer 6 binary counter (TM6BC) is cleared to 0x00.

- Timer 6 Binary Counter (TM6BC:0x03F68)

bp	7	6	5	4	3	2	1	0
Flag	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

- Timer 6 Compare Register (TM6OC:0x03F69)

bp	7	6	5	4	3	2	1	0
Flag	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

Time base timer can be reset its operation by the software. Time base timer can be cleared by writing an arbitrary value to the time base timer clear control register (TBCLR).

- Time Base Timer Clear Control Register (TBCLR:0x03F6B)

bp	7	6	5	4	3	2	1	0
Flag	TBCLR7	TBCLR6	TBCLR5	TBCLR4	TBCLR3	TBCLR2	TBCLR1	TBCLR0
At reset	-	-	-	-	-	-	-	-
Access	W	W	W	W	W	W	W	W

8.2.3 Timer 6 Enable Register

This register controls the starting operation of the timer 6 and the time base timer.

■ Timer 6 Enable Register (TM6BEN:0x03F6C)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	Reserved	TBEN	TM6EN
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2	Reserved	Always set to "0". *
1	TBEN	Time base timer operation control 0:Stop 1:Operation
0	TM6EN	Timer 6 operation control 0:Stop 1:Operation



When the timer 6 is operated, the operation is not started unless the TM6EN flag of the TM6BEN register is set to "1".



When the time base timer is operated, the operation is not started unless the TBEN flag of the TM6BEN register is set to "1".



Always set "0" to the bp denoted by *.

8.2.4 Timer Mode Register

This is readable/writable register that controls timer 6 and time base timer.

■ Timer 6 Mode Register (TM6MD:0x03F6A)

bp	7	6	5	4	3	2	1	0
Flag	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	TM6CLRS	Timer 6 binary counter clear selection flag 0:Enable the initialization of TM6BC as TM6OC is written. 1:Disable the initialization of TM6BC as TM6OC is written. * TM6IRQ is disable as TM6CLRS = 0, TM6IRQ is enable as TM6CLRS = 1.
6-4	TM6IR2-0	Time base timer interrupt cycle selection 000:Time base selection clock $\times 1/2^7$ 001:Time base selection clock $\times 1/2^8$ 010:Time base selection clock $\times 1/2^9$ 011:Time base selection clock $\times 1/2^{10}$ 10:Time base selection clock $\times 1/2^{13}$ 11:Time base selection clock $\times 1/2^{15}$
3-1	TM6CK3-0	Timer 6 clock source selection 000:fpll 001:fs 010:fx 011:Synchronous fx 100:Time base selection clock $\times 1/2^{13}$ 101:Synchronous time base selection clock $\times 1/2^{13}$ 110:Time base selection clock $\times 1/2^{12}$ 111:Synchronous time base selection clock $\times 1/2^{12}$
0	TM6CK0	Time base timer clock source selection 0:fpll 1:fx

8.3 8-bit Free-running Timer

8.3.1 Operation

■ 8-bit Free-running Timer (Timer 6)

The generation cycle of the timer interrupt should be set in advance, by the set value of the compare register (TM6OC) and the clock source selection. When the binary counter (TM6BC) reaches the set value of the compare register, an interrupt request is generated at the next count clock and the binary counter is cleared to restart count up from 0x00.

Table:8.3.1 shows selectable clock source.

Table:8.3.1 Clock Source at Timer Operation (Timer 6)

Clock source	One count time		
	At fpll=10 MHz	At fpll=8.39 MHz	At fpll=2 MHz
fpll	100 ns	119.1 ns	500 ns
fx	30.5 μ s		
fs	200 ns	238.3 ns	1000 ns
fpll $\times 1/2^{12}$	409.6 μ s	487.6 μ s	2048 μ s
fpll $\times 1/2^{13}$	819.2 μ s	976.4 μ s	4096 μ s
fx $\times 1/2^{12}$	125 ms		
fx $\times 1/2^{13}$	250 ms		
fpll = 10 MHz, 8.39 MHz, 2 MHz fx = 32.768 kHz fs = fpll/2			

■ 8-bit Free-running Timer as a 1 Minute-timer, a 1 Second-timer

Table:8.3.2 shows the clock source selection and the TM6OC register setup, when a 8-bit free-running timer is used as a 1 minute-timer, a 1 second-timer.

Table:8.3.2 1 Minute-timer, 1 Second-timer (Timer 6) Setup

Interrupt Generation Cycle	Clock source	TM6OC register
1 min	$f_x \times 1/2^{13}$	0xEF
1 s	$f_x \times 1/2^{13}$	0x03
$f_x = 32.768 \text{ kHz}$		

When the 1 minute-timer (1 m.) is set on Table:8.3.2, the bp2 waveform frequency (cycle) of the TM6BC register is 1 Hz (1 s.). So, that can be used for adjusting the seconds.

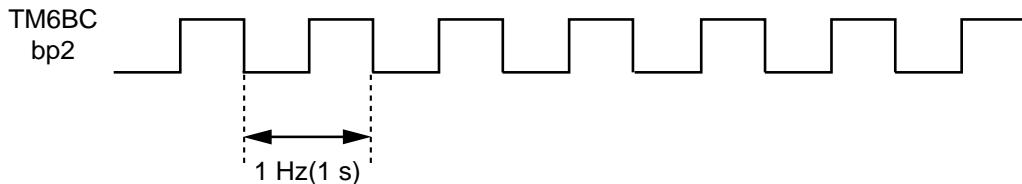


Figure:8.3.1 Waveform of TM6BC Register bp2 (Timer 6)



Switch the count clock after the timer operation is stopped, as the counting is not generated correctly during the timer operation.

■ Count Timing of Timer Operation (Timer 6)

Binary counter counts up with the selected clock source as a count clock.

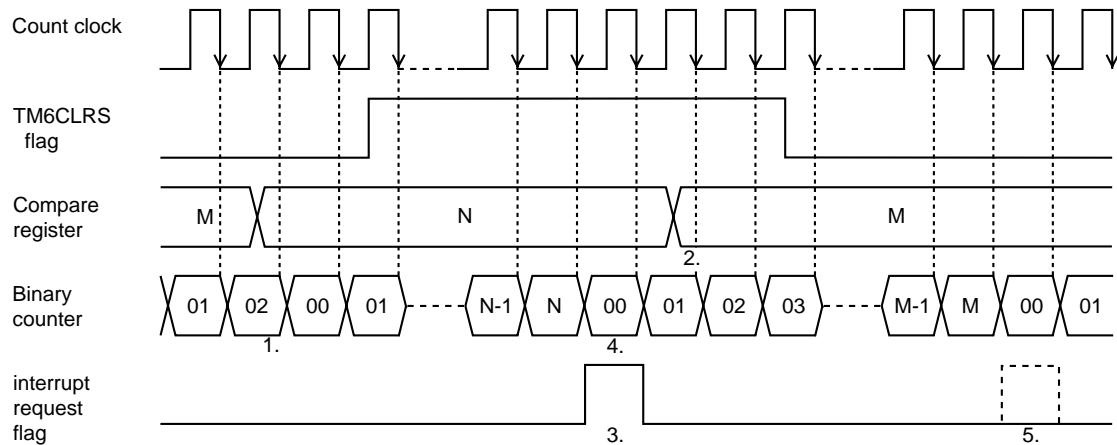


Figure 8.3.2 Count Timing of Timer Operation (Timer 6)

1. When any data is written to the compare register as the TM6CLRS flag is "0", the binary counter is cleared to 0x00.
2. Even if any data is written to the compare register as the TM6CLRS flag is "1", the binary counter is not cleared.
3. When the binary counter reaches the value of the compare register as the TM6CLRS flag is "1", an interrupt request flag is set at the next count clock.
4. When an interrupt request flag is set, the binary counter is cleared to 0x00 and restarts the counting.
5. Even if the binary counter reaches the value of the compare register as the TM6CLRS flag is "0", no interrupt request flag is set.



When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared at the next count clock.

So set the compare register as :

(Compare register setting) = (count till the interrupt request - 1)

However, the interrupt generation cycle when the compare register is set to "00" is the same as it is set to "01".



If fx is selected as the clock source in timer 6, when the binary counter is read on the operation while CPU is operating in the NORMAL mode, uncertain value on counting up may be read.

To prevent this, select the synchronous fx.



If fx is used as the clock source while CPU is operating in the NORMAL mode, the binary counter should be cleared before starting the timer operation. Also, when 0x00 is set to the compare register, the synchronous fx should be used.



If the smaller value than the binary counter is set to the compare register on the counting operation, the binary counter continues counting till overflow.(When TM6CLRS flag is "1".)



Up to 3 system clock is needed from Timer n interrupt request flag till the next interrupt request flag. During the period, an interrupt request flag is not generated at compare match.



When the fx is selected for the count clock source and the value of the compare register is rewritten while CPU is operating in the NORMAL mode, the operation cannot be ensured during the transition to the circle of the setting value.

To operate the timer in the expected circle from the beginning, stop the timer before rewriting the compare register, then start the timer operation.



When 'fx' is used as a clock source, it counts at "falling" of the count clock and in other uses, it counts "rising" of the count clock.



Count clock source should be changed with the timer interrupt is prohibited.



If the TM6CLRS flag of the TM6MD register is set to "0", TM6BC can be initialized at every rewriting of TM6OC register, but in that state the timer 6 interrupt is disabled. If the timer 6 interrupt should be used, set the TM6CLRS flag to "1" after rewriting the TM6OC register.



On the timer 6 clock source selection, if the time base timer output or the time base timer synchronous output is selected, the clock setup of time base timer is necessary.



The binary counter of the timer 6 and time base timer on this LSI operates/halts by the signal which is generated by sampling the TMnEN flag by the count clock.
When the fx input is selected as count clock source, note the following two points:

1. To read the binary counter value after timer halts, put the TMnEN flag down, wait 1 count cycle, and read the value.
When reading the value without waiting 1 count, program to read the binary counter multiple times. In this case, the read value is [count value-1]. After the timer halts, read the binary counter as follows:
 2. When halting the timer and changing its setting (clock selection, function switching, etc.), wait 1 count clock after putting the timer enable down and set the timer again.
If the setting is switched during timer operation, the timer operation is not guaranteed.
-

8.3.2 Setup Example

■ Timer Operation Setup (Timer 6)

Timer 6 generates interrupts constantly for timer function. Interrupts are generated in every 250 dividing (25 µs) by selecting fs (fpll = 10 MHz at operation) as clock source.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM6BEN(0x03F6C) bp0 :TM6EN =0	(1) Set the TM6EN flag of the TM6BEN register to "0" to stop the timer 6 counting.
(2) Enable the binary counter initialization TM6MD(0x03F6A) bp7 :TM6CLRS =0	(2) Set the TM6CLRS flag of the timer 6 mode register (TM6MD) to "0". At the time, the initialization of the timer 6 binary counter (TM6BC) is enabled.
(3) Disable the interrupt TM6ICR(0x03FED) bp1:TM6IE =0	(3) Set the TM6IE flag of the TM6ICR register to "0" to disable the interrupt.
(4) Select the clock source TM6MD(0x03F6A) bp3-1 :TM6CK3-1 =001	(4) Clock source can be selected by the TM6CK3 to 1 flag of the TM6MD register. Actually, fs is selected.
(5) Set the interrupt generation cycle TM6OC(0x03F69) =0xF9	(5) Set the interrupt generation cycle to the timer 6 compare register (TM6OC). At that time, TM6BC is initialized to 0x00.
(6) Enable the interrupt request TM6MD(0x03F6A) bp7 :TM6CLRS =1	(6) Set the TM6CLRS flag of the TM6MD register to "1" to enable the interrupt request generation.
(7) Set the interrupt level TM6ICR(0x03FED) bp7-6 :TM6LV1-0 =01	(7) Set the interrupt level by the TM6LV1 to 0 flag of the timer 6 interrupt control register (TM6ICR). If the interrupt request flag may be already set, clear them. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(8) Enable the interrupt TM6ICR(0x03FED) bp1 :TM6IE =1	(8) Set the TM6IE flag of the TM6ICR register to "1" to enable the interrupt.
(9) Start the TM6 operation TM6BEN(0x03F6C) bp0 :TM6EN =1	(9) Set the TM6EN flag of the TM6BEN register to "1" to start the timer 6.

As TM6OC is set, TM6BC is initialized to 0x00.

When TM6BC matches TM6OC, the timer 6 interrupt request flag is set at the next count clock and TM6BC is cleared to 0x00 to restart counting.

8.4 Time Base Timer

8.4.1 Operation

■ Time Base Timer (Time Base Timer)

Interrupt is constantly generated by a selected clock source and a interrupt generation cycle. Table:8.4.1 shows the interrupt cycle is combination with the clock source;

Table:8.4.1 Selection of Time Base Timer Interrupt Generation Cycle

Selected clock source	Interrupt generation cycle	
fpll	fpll × 1/2 ⁷	12.8 μs
	fpll × 1/2 ⁸	25.6 μs
	fpll × 1/2 ⁹	51.2 μs
	fpll × 1/2 ¹⁰	102.4 μs
	fpll × 1/2 ¹³	819.2 μs
	fpll × 1/2 ¹⁵	3.27 ms
fx	fx × 1/2 ⁷	3.9 ms
	fx × 1/2 ⁸	7.8 ms
	fx × 1/2 ⁹	15.6 ms
	fx × 1/2 ¹⁰	31.2 ms
	fx × 1/2 ¹³	250 ms
	fx × 1/2 ¹⁵	1 s

fpll =10 MHz fx =32.768 kHz

■ Count Timing Timer Operation (Time Base Timer)

The counter counts up with the selected clock source as a counter clock.

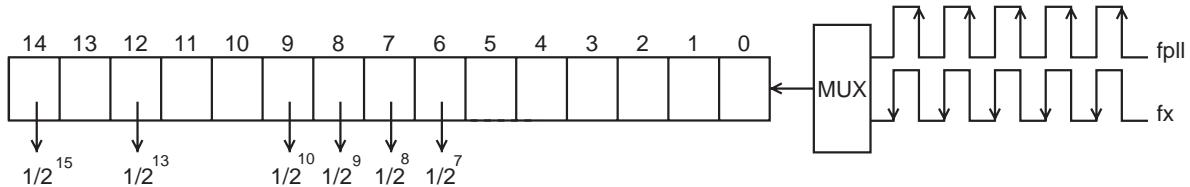


Figure:8.4.1 Count Timing of Timer Operation (Time Base Timer)

- When the selected interrupt cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set.



An interrupt may be generated at switching of the clock source. Enable the interrupt after switching the clock source.



The initialization can be done by writing an arbitrary value to the time base timer clear control register (TBCLR).

8.4.2 Setup Example

■ Timer Operation Setup (Time Base Timer)

An interrupt can be generated constantly with time base timer in the selected interrupt cycle. The interrupt generation cycle is $f_{PLL} \times 1/2^{13}$ (1 ms: $f_{PLL} = 8.192$ MHz) to generate interrupts.

An example setup procedure, with a description of each step is shown below

Setup Procedure	Description
(1) Stop the counter TM6BEN(0x03F6C) bp1 :TBEN =0	(1) Set the TBEN flag of the TM6BEN register to "0" to stop the time base timer counting.
(2) Select the clock source TM6MD(0x03F6A) bp0 :TM6CK0 =0	(2) Select f _{PLL} as a clock source by the TM6CK0 flag of the timer 6 mode register (TM6MD).
(3) Disable the interrupt TBICR(0x03FEE) bp1 :TBIE =0	(3) Set the TBIE flag of the TBICR register to "0" to disable the interrupt.
(4) Select the interrupt generation cycle TM6MD(0x03F6A) bp6-4 :TM6IR2-0 =100	(4) Select the selected clock $\times 1/2^{13}$ as an interrupt generation cycle by the TM6IR2 to 0 flag of the TM6MD register.
(5) Initialize the time base timer TBCLR(0x03F6B) =0x00	(5) Write value to the time base timer clear control register (TBCLR) to initialize time base timer.
(6) Set the interrupt level TBICR(0x03FEE) bp7-6 :TBLV1-0 =01	(6) Set the interrupt level by the TBLV1 to 0 flag of the time base interrupt control register (TBICR). If any interrupt request flag may be already set, clear them. [Chapter 3.1.4. Maskable Interrupt Control Register Setup]
(7) Enable the interrupt TBICR(0x03FEE) bp1 :TBIE =1	(7) Set the TBIE flag of the TBICR register to "1" to enable the interrupt.
(8) Start the time base timer operation TM6BEN(0x03F6C) bp1 :TBEN =1	(8) Set the TBEN flag of the TM6BEN register to "1" to start the time base timer.

- When the selected interrupt generation cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

Chapter 9 Remote Control Carrier Functions

9.1 Overview

Remote control carrier output functions can create the carrier wave for the remote control and output.

9.1.1 Functions

Table:9.1.1 shows the remote control carrier output functions.

Table:9.1.1 The remote control carrier output functions.

Remote control carrier output base timer selection	Timer 0 Timer 3
Duty selection	1/2 1/3 Timer output
Remote control carrier output enable factor	RMOEN
Remote control carrier output enable	"L" level output Remote control carrier output
PA0 special function selection	Timer 0 Remote control carrier output
P03 special function selection	Timer 0 Remote control carrier output
P10 special function selection	Timer 0 Remote control carrier output

Pins can be switched to RMOUTA/RMOUTB/RMOUTC.

RMOUTA(PA0)
RMOUTB(P03)
RMOUTC(P10)



On the text, if there is not much functional difference in pins A , B and C, "A", "B" and "C" of the pin names are omitted.



This function is not available in the STOP/HALT mode.

9.1.2 Block Diagram

■ Remote Control carrier Output Block Diagram

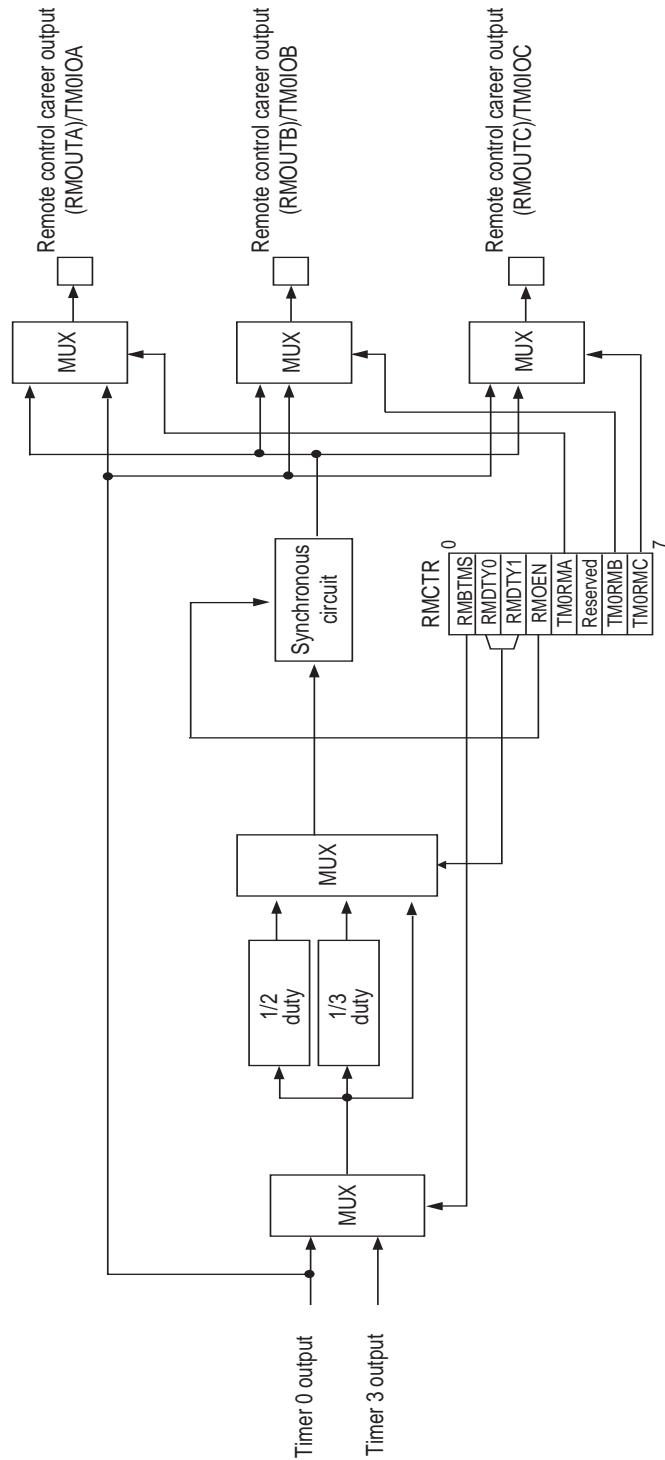


Figure:9.1.1 Remote Control carrier Output Block Diagram

9.2 Control Registers

9.2.1 Control Registers

Table:9.2.1 shows the registers that control the remote control carrier output.

Table:9.2.1 Control Registers

Registers	Address	R/W	Function	Page
RMCTR	0x03F6D	R/W	Remote control carrier output control register	IX-5
TM0MD	0x03F54	R/W	Timer 0 mode register	V-16
TM0OC	0x03F52	R/W	Timer 0 compare register	V-13
CK0MD	0x03F56	R/W	Timer 0 prescaler selection register	V-10
PAOMD	0x03EE6	R/W	Port A output mode register	IV-147
PADIR	0x03F3A	R/W	Port A direction control register	IV-146
P1OMD	0x03EE1	R/W	Port 1 output mode register	IV-27
P1DIR	0x03F31	R/W	Port 1 direction control register	IV-26
P0OMD	0x03EE0	R/W	Port 0 output mode register	IV-11
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-10

9.2.2 Remote Control carrier Output Control Register

- Remote Control carrier Output Control Register (RMCTR:0x03F6D)

bp	7	6	5	4	3	2	1	0
Flag	TM0RMC	TM0RMB	Reserved	TM0RMA	RMOEN	RMDTY1	RMDTY0	RMBTMS
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	TM0RMC	P10 special function output selection 0:Timer 0 output (TM0IOC) 1:Remote control carrier output (RMOUTC)
6	TM0RMB	P03 special function output selection 0:Timer 0 output (TM0IOB) 1:Remote control carrier output (RMOUTB)
5	Reserved	Always set to "0". *
4	TM0RMA	PA0 special function output selection 0:Timer 0 output (TM0IOA) 1:Remote control carrier output (RMOUTA)
3	RMOEN	Remote control carrier output enable 0:"L" level output 1:Remote control carrier output
2-1	RMDTY1-0	Remote control carrier duty selection 00:1/2 duty 01:1/3 duty 1-:1/1 duty
0	RMBTMS	Remote control carrier output base timer selection 0:Timer 0 output selection 1:Timer 3 output selection



When set RMOEN flag to “1”, don’t change the flags other than RMOEN flag.



Do not change RMDTY 1,0 flag, RMBTMS flag and TMORM flag with RMOEN flag at the same time. If change its at the same time, remote control carrier pulse isn’t correctly output.



The cycle of the remote control carrier output base timer is set to the system clock one cycle or more. If the cycle is set to one cycle or less, remote control carrier output isn’t correctly output.



Always set “0” to the bp denoted by *.

9.3 Operations

9.3.1 Operations

Remote control carrier output functions can create the carrier pulse for the remote control.

■ Operation of the remote control carrier output

Remote control carrier can be created by using the output signals of timer 0 and timer 3. Duty ratio is selectable from 1/1, 1/2, 1/3. Remote control carrier output signal can be output from the RMOUTA pin (PA0), the RMOUTB pin (P03), the RMOUTC pin (P10).

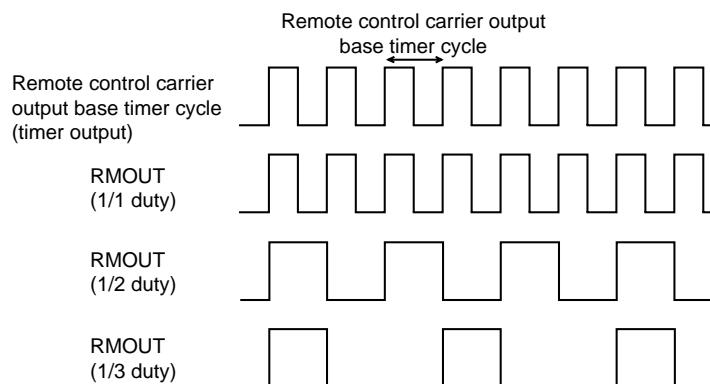


Figure 9.3.1 Remote Control carrier Output Signal Duty Ratio

■ Count Timing of Remote Control carrier Output Functions

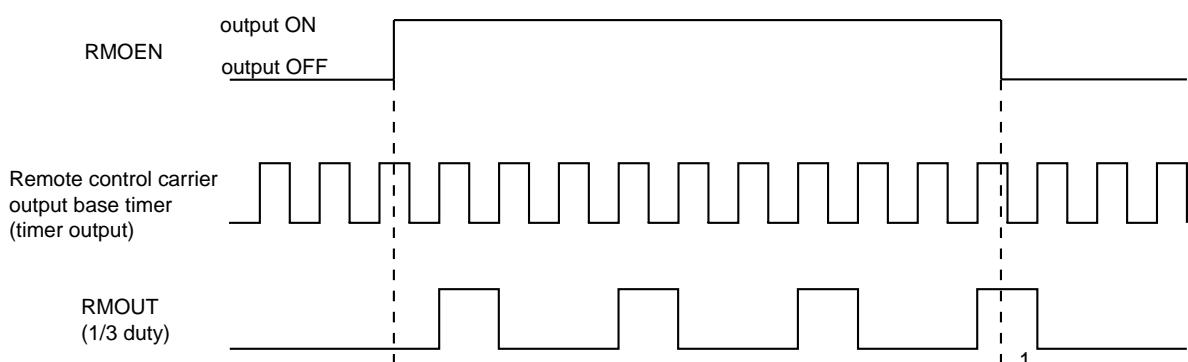


Figure 9.3.2 Count Timing of Remote Control carrier Output Functions

- Even if the RMOEN flag is switched OFF at the carrier output "H", the carrier wave is held by the synchronous circuit.

9.3.2 Setup Examples

■ Remote Control carrier Output Functions Setup (Timer 0 and 3)

The setup examples that 1/3 duty carrier pulse signal is output as 36.7 kHz for "H" period from the RMOUT pin with the timer 0 used for the remote control carrier output base timer are shown below. The clock source of the timer 0 selects fs/2 (at fs = 8 MHz). An example setup procedure, with a description of each step is shown below.

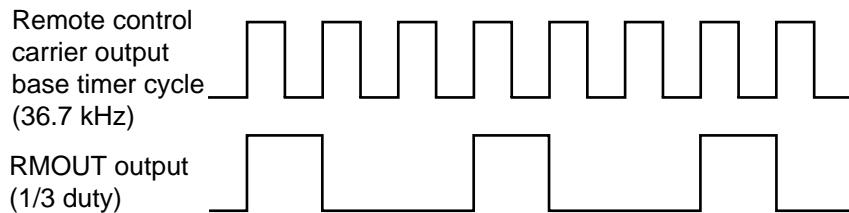


Figure 9.3.3 Output Wave of RMOUT Output Pin

Setup Procedure	Description
(1) Disable the remote control carrier output RMCTR(0x03F6D) bp3 :RMOEN =0	(1) Set the RMOEN flag of the remote control carrier output control register (RMCTR) to "0" to disable the remote control carrier output.
(2) Select the base cycle setup timer RMCTR(0x03F6D) bp0 :RMBTMS =0	(2) Set the RMBTMS flag of the RMCTR register to "0" to select the timer 0 as the setup timer of the base cycle.
(3) Select the carrier output duty RMCTR(0x03F6D) bp2-1 :RMDTY1-0 =01	(3) Set the RMDTY1, 0 flag of the RMCTR register to "0, 1" to select the duty to 1/3.
(4) Confirm the counter stop TM0MD(0x03F54) bp3 :TM0EN =0	(4) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop counting of the timer 0.
(5) Set the remote control carrier output of the special function pin PAOMD(0x03EE6) bp0 :PAOMD0 =1 PADIR(0x03F3A) bp0 :PADIR0 =1 RMCTR(0x03F6D) bp4 :TM0RMA =1	(5) Set the PAOMD0 flag of the port A output mode register (PAOMD) to "1" to set the PA0 pin to the special function pin. Set the PADIR0 flag of the port A direction control register (PADIR) to "1" to set the output mode. Set the TM0RMA flag of the RMCTR register to "1" to select the remote control carrier output.
(6) Select the timer general operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(6) Set the TM0PWM and TM0MOD flags of the TM0MD register to "0" to select the timer general operation.

Setup Procedure	Description
(7) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(7) Select the prescaler output to the clock source by the TM0CK2 to 0 of the TM0MD register.
(8) Select and enable the prescaler output CK0MD(0x03F56) bp3-1 :TM0PSC2-0 =0X0 bp0 :TM0BAS =1	(8) Select the fs/2 to the prescaler output by the TM0PSC2 to 0 flags, TM0BAS flag of the timer 0 prescaler selection register.
(9) Set the base cycle of the remote control carrier TM0OC(0x03F52) =0x36	(9) Set the base cycle of the remote control carrier by writing 0x36 to the timer 0 compare register (TM0OC). To get 2-times frequency of 36.7 kHz (73.4 kHz) that is divided $fs = 8 \text{ MHz}$, the setup value is set to $(fs/2 \text{ MHz} / 73.4 \text{ kHz}) - 1 = 54$ (0x36).
(10) Enable the remote control carrier output RMCTR(0x03F6D) bp3 :RMOEN =1	(10) Set the RMOEN flag of the RMCTR register to "0" to enable the remote control carrier output.
(11) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(11) Set the TM0EN flag of the TM0MD register to "1" to start the timer 0.

TM0BC starts the count up from 0x00. As The base cycle pulse that is set at the TM0OC is output from the timer 0, 1/3 of the remote control carrier pulse signal is output. If the RMOEN flag of the RMCTR register is set to "0", the output signal of the remote control carrier pulse is stopped.



When enabled the remote control carrier output during timer operation, the duty of remote control carrier ouput immediately after enabled can't guarantee.



When stop the remote control carrier output, execute the remote control carrier output stop setting (RMOEN=0). And after one cycle of the remote control carrier output base timer wait, stop the timer operation. If don't wait on cycle, the duty of remote control carrier ouput can't guarantee.

Record of Changes

The following shows the changes in the publication of “MN101E29G/F29G LSI User’s Manual” (From 1st Edition 4th Printing dated in January, 2008 to the 2nd Edition 1st Printing dated in March, 2012.)

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-2	16	Error correction	High speed mode has the normal mode which is based on 2-cycle clock (<u>fosc/2</u>) and the double speed mode which is based on <u>the same cycle clock with fosc</u> .	High speed mode has the normal mode which is based on 2-cycle clock (<u>fpll/2</u>) and the double speed mode which is based on <u>the not-devided clock with fpll</u> .
I-4,5		Specification addition	-	Add the description as (Peripheral function group interrupt)
From I-5 to the last		Error correction	<u>fosc</u>	<u>fpll</u>
I-6	Timer 3	Error correction	16bit cascade connected (timer2, <u>3</u>), 32-bit cascade connected (timer0, 1, 2, <u>3</u>)	16bit cascade connected (timer2), 32-bit cascade connected (timer0, 1, 2)
I-8	2 from the bottom	Error correction	Port <u>4</u> outputs the latched data, on the event timing of the synchronous output signal of timer	Port <u>8</u> outputs the latched data, on the event timing of the synchronous output signal of timer
I-11	10	Error correction	Serial4 -7-bit or 10-bit of slave address can be set.	Serial4 -7-bit of slave address can be set.
	1 from the bottom	Error correction	1/4 duty, <u>1/4</u> bias	1/4 duty, <u>1/3</u> bias
I-12	9-12	Description change	<u>VDD</u> , <u>VLC1</u> , <u>VLC2</u> , <u>VLC3</u>	<u>V_{DD5}</u> , <u>V_{LC1}</u> , <u>V_{LC2}</u> , <u>V_{LC3}</u>
	16	Error correction	Port -I/O ports LCD driver for segment : <u>54</u> pins	Port -I/O ports LCD driver for segment : <u>55</u> pins
I-13	Figure 1.3.1	Description change	<u>VDD</u> (1.8 capacity)	<u>VDD18</u> (1.8 capacity)
I-18	<u>V_{DD5}</u>	Description change	Apply 2.2 V to 5.5 V to <u>V_{DD}</u> and 0 V to <u>V_{SS}</u> .	Apply 2.2 V to 5.5 V to <u>V_{DD5}</u> and 0 V to <u>V_{SS}</u> .
	<u>V_{DD18}</u>	Description change	<u>V_{DD}</u> (Capacity 1.8V)	<u>V_{DD18}</u> (Capacity 1.8V)
	XI, XO	Description change	Other Function -	Other Function <u>P90, P91</u>
	NRST	Error correction	NO <u>19</u>	NO <u>12</u>
	NRST	Error correction	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. <u>30</u> kΩ)...	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. <u>50</u> kΩ)...
I-19	P27	Error correction	NO <u>19</u>	NO <u>12</u>
I-20,21		Error correction	<u>COMS</u> push-pull	<u>CMOS</u> push-pull

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-22	BUZZERx NBUZZERx	Error correction	P10MD and PA5MD	P10MD and P50MD
I-23	V _{REF+}	Error correction	Normally, the values of V _{REF+} = V _{DD} is used.	The values of 2.0 V ≤ V _{REF+} ≤ V _{DD5} is used.
I-25	V _{LC1}	Description change	V _{LC1} =V _{DD}	V _{LC1} =V _{DD5}
I-26	SEGx	Description change	... Connect to the segment pins of the LCD panel.	... Connect to the segment pins of the LCD display panel.
I-27	DMOD	Description change	Set always to V _{DD} .	Set always to V _{DD5} .
I-29	From 1.5.1 to the last page	Error correction	V _{DD}	V _{DD5}
1.5.1	Description change			
*3	Description change	VDD18 VDD5		V _{DD18} V _{DD5}
*4	Description change	The absolute maximum ratings are the limit values beyond which the LSI may be damaged <u>and proper operation is not assured.</u>		The absolute maximum ratings are the limit values beyond which the LSI may be damaged.
I-31	Table	Error correction	Crystal Oscillator [NORMAL mode:fs=fosc/2] Crystal Oscillator [Slow mode:fs=fx/2]	Crystal Oscillator [NORMAL mode] Crystal Oscillator [Slow mode]
Figure 1.5.1	Description addition			
Figure 1.5.2	Description addition			
I-32	Table	Error correction		

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)																																																																				
I-34	1	Description deletion	<u>The below current is a targeted specification.</u> <u>Please contact us for the latest specification.</u>	-																																																																				
	Table	Description change	-	Change the each characteristics and add contents 6																																																																				
	*8	Description deletion	Measured under conditions without load, <u>T_A=25°C</u> . (pull-up / pull-down resistors are unconnected.)	Measured under conditions without load. (pull-up / pull-down resistors are unconnected.)																																																																				
I-35	Parameter 11,12,17,18	Description Change	Input high voltage_1 Input low voltage_1 Input high voltage_2 Input low voltage_2	Input high voltage Input low voltage Input high voltage Input low voltage																																																																				
	Parameter 19	Error correction	<u>±5</u>	<u>±2</u>																																																																				
	Parameter 21	Error correction	V _{IN} =V _{SS}	V _{IN} =V _{DD5}																																																																				
I-36	Parameter 30,31	Description change	Input high voltage_1 Input low voltage_1	Input high voltage Input low voltage																																																																				
	Parameter 37	Error correction	LED output OFF	LED output ON																																																																				
I-37	Parameter 41	Description deletion	<u>41 : Input leak current</u>	-																																																																				
	Parameter 38,39,40,41	Description addition	Condition -	Condition <u>Figure:1.5.5</u>																																																																				
	Parameter 43,44,45,46	Description change	-	Parameter 43,44,45,46 changed.																																																																				
I-38	Figure 1.5.5	Description change	V _{DD}	V _{DD5}																																																																				
I-39	Table	Error correction	<table border="1"> <tr> <td>2</td><td>None-linearity error 1</td><td>V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF+} = 5.0 V, V_{REF-} = 0 V T_{AD} = 800 ns *12</td><td>±3</td><td>LS</td></tr> <tr> <td>3</td><td>Differential non-linearity error</td><td></td><td>±3</td><td>LS</td></tr> <tr> <td>4</td><td>Zero transition voltage</td><td>V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF+} = 5.0 V, V_{REF-} = 0 V T_{AD} = 1.00 μs *12</td><td>30</td><td>100 m¹</td></tr> <tr> <td>5</td><td>Full-scale transition voltage</td><td>4900 4970</td><td>m¹</td><td></td></tr> <tr> <td>6</td><td>fosc=8 MHz T_{AD} = 1.00 μs *12</td><td>12</td><td>28 μs</td><td></td></tr> <tr> <td>7</td><td>A/D conversion time f_x=32.768 kHz T_{AD} = 1.00 μs *12</td><td>183.12</td><td>427.28 μs</td><td></td></tr> <tr> <td>8</td><td>fosc=8 MHz T_{AD} = 1.00 μs *12</td><td>2.0</td><td>18.0 μs</td><td></td></tr> <tr> <td>9</td><td>Sampling time f_x=32.768 kHz T_{AD} = 1.00 μs *12</td><td>30.52</td><td>274.68 μs</td><td></td></tr> </table>			2	None-linearity error 1	V _{DD} = 5.0 V, V _{SS} = 0 V, V _{REF+} = 5.0 V, V _{REF-} = 0 V T _{AD} = 800 ns *12	±3	LS	3	Differential non-linearity error		±3	LS	4	Zero transition voltage	V _{DD} = 5.0 V, V _{SS} = 0 V, V _{REF+} = 5.0 V, V _{REF-} = 0 V T _{AD} = 1.00 μs *12	30	100 m ¹	5	Full-scale transition voltage	4900 4970	m ¹		6	fosc=8 MHz T _{AD} = 1.00 μs *12	12	28 μs		7	A/D conversion time f _x =32.768 kHz T _{AD} = 1.00 μs *12	183.12	427.28 μs		8	fosc=8 MHz T _{AD} = 1.00 μs *12	2.0	18.0 μs		9	Sampling time f _x =32.768 kHz T _{AD} = 1.00 μs *12	30.52	274.68 μs																												
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<table border="1"> <tr> <td>parameter</td><td>condition</td><td>conditions</td><td>min</td><td>typ</td><td>max</td><td>unit</td></tr> <tr> <td>a. Differential non-linearity error</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=800 ns *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>±30</td><td>±30</td><td>±30</td><td>LS</td></tr> <tr> <td>b. Differential settling</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=800 ns *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>±30</td><td>±30</td><td>±30</td><td>LS</td></tr> <tr> <td>c. Full-scale transition</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>4900</td><td>4900</td><td>4970</td><td>ns</td></tr> <tr> <td>d. A/D conversion time</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>427.28</td><td>427.28</td><td>427.28</td><td>μs</td></tr> <tr> <td>e. Sampling time</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>30.52</td><td>30.52</td><td>30.52</td><td>μs</td></tr> <tr> <td>f. Reference Voltage (V_{ref+})</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>2.0</td><td>2.0</td><td>2.0</td><td>V</td></tr> <tr> <td>g. Operating input voltage</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>±2.0</td><td>±2.0</td><td>±2.0</td><td>V</td></tr> <tr> <td>h. Ground connection point</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>±2.0</td><td>±2.0</td><td>±2.0</td><td>V</td></tr> <tr> <td>i. Load resistor</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>V_{DD}=5.0 V, V_{SS}=0 V, V_{REF+}=5.0 V, V_{REF-}=0 V T_{AD}=1.00 μs *12</td><td>4.0</td><td>4.0</td><td>8.0</td><td>kΩ</td></tr> </table>			parameter	condition	conditions	min	typ	max	unit	a. Differential non-linearity error	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =800 ns *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±30	±30	±30	LS	b. Differential settling	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =800 ns *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±30	±30	±30	LS	c. Full-scale transition	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	4900	4900	4970	ns	d. A/D conversion time	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	427.28	427.28	427.28	μs	e. Sampling time	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	30.52	30.52	30.52	μs	f. Reference Voltage (V _{ref+})	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	2.0	2.0	2.0	V	g. Operating input voltage	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±2.0	±2.0	±2.0	V	h. Ground connection point	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±2.0	±2.0	±2.0	V	i. Load resistor	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	4.0	4.0	8.0	kΩ
parameter	condition	conditions	min	typ	max	unit																																																																		
a. Differential non-linearity error	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =800 ns *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±30	±30	±30	LS																																																																		
b. Differential settling	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =800 ns *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±30	±30	±30	LS																																																																		
c. Full-scale transition	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	4900	4900	4970	ns																																																																		
d. A/D conversion time	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	427.28	427.28	427.28	μs																																																																		
e. Sampling time	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	30.52	30.52	30.52	μs																																																																		
f. Reference Voltage (V _{ref+})	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	2.0	2.0	2.0	V																																																																		
g. Operating input voltage	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±2.0	±2.0	±2.0	V																																																																		
h. Ground connection point	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	±2.0	±2.0	±2.0	V																																																																		
i. Load resistor	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	V _{DD} =5.0 V, V _{SS} =0 V, V _{REF+} =5.0 V, V _{REF-} =0 V T _{AD} =1.00 μs *12	4.0	4.0	8.0	kΩ																																																																		
<p>*12 T_{AD} is A/D conversion clock cycle. The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{ref+}=5 V, V_{SS}=0 V. Note) The voltage difference between V_{ref+} and V_{SS} should be set to more than 2 V.</p>		<p>T_{AD} is A/D conversion clock cycle. The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{ref+}=5 V, V_{SS}=0 V.</p>																																																																						
Note	Description addition	-	<p>The reference voltage input V_{ref+} pin uses value of 2.0 V ≤ V_{ref+} ≤ V_{DD5}. When input voltage is V_{ref+} < 2.0 V, there...</p>																																																																					
I-41	1.5.8	Specification addition	-	<p>1.5.8 Flash EEPROM Programming Condition</p>																																																																				

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
I-44	1	Description change	<u>V_{DD}</u>	<u>V_{DD5}</u>
	2	Description change	<u>V_{DD}</u>	<u>V_{DD5}</u>
	5	Description addition	-	<u>-V_{ref+}</u> Pin Connection
I-45	Table1.7.1	Error correction	-	<u>Table 1.7.1 is changed</u>
I-46	First Note	Description addition	-	<u>Oscillation between E29 series and E30 series which is added audio function to E29 is different.</u>
	Table1.7.2	Description addition	-	<u>Table 1.7.2 added.</u>
	Second & Third Note	Description change	-	<u>Second and Third Note moved from I-45 of Former Edition.</u>
I-50	The last line	Description addition	-	<u>[In using auto reset]</u> <u>- Microcontroller Power On in using Auto Reset (V_{DD5}=5V)</u> <u>Fig.1.7.8 Microcontroller Power On in using Auto Reset (V_{DD5}=5V)</u>
II-4	Table 2.1.3	Description addition	-	<u>AUCTR</u>
		Error correction	CPUM R/W *1	CPUM R/W
	3	Error correction	<u>*1 a part of bit is for read only</u>	-
II-8	PSW	Description addition	bp 7 ... Flag BKD ... At reset 0 ...	bp 7 ... Flag BKD ... At reset 0 ... <u>Access R/W ...</u>
II-9	Square	Description change	-Maskable Interrupt Enable (MIE) ... A '1' enables maskable interrupts; a '0' disables all maskable interrupts	-Maskable Interrupt Enable (MIE) ... <u>The setting the flag to "1"</u> enables maskable interrupts; <u>the setting to "0"</u> disables all maskable interrupts
II-10	Second Note	Description addition	-	<u>Make maskable interrupt enable flag (MIE) of processor status word (PSW) of prohibited all maskable interrupts ...</u>
II-12	First Key	Description addition	This LSI is designed for 8-bit data access. It is possible to transfer data in 16-bit increments with odd or all even addresses.	This LSI is designed for 8-bit data access. <u>When 16-bit data access is carried out, 8-bit data access is performed twice from the lower address.</u> It is possible to transfer data in 16-bit increments with odd or all even addresses.
II-15	Note	Description deletion	Fix the MMOD pin always to "L" or "H" level. Do not change the settings of this pin also after reset release.	Fix the MMOD pin always to "L" level. Do not change the settings of this pin also after reset release.
II-24	1	Description change	<u>The MN101E series</u> locates the special function registers...	<u>This LSI</u> locates the special function registers...
	Figure: 2.2.5	Error correction	<u>SC4TICR</u>	<u>SC4ICR</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-28	RCPSR	Error correction	110:Address pointer 6 (RC6AP (L/M/H))	110:Address pointer 6 (RC6AP (L/M/H)) <u>111:Setting Prohibited</u>
II-29	First Note	Description addition	-	<u>ROM correction address is set for 4th or later command from command that enable the ROM correction control.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
II-30	Second Note	Description addition	-	<u>ROM correction address is set for 4th or later command from command that enable the ROM correction control.</u>
II-34	18	Description change	After <u>the main program is started</u> , the instruciton fetched address and the set address to ROM...	After <u>4th or later command from command that enable the ROM correction control</u> , the instruciton fetched address and the set address to ROM...
II-37	Third Note	Description addition	-	<u>Alway set IRWE flag of memory control register (MEMCTR) to "0"...</u>
	Fourth Note	Description addition	-	<u>External expansion memory function does not guarantee AC timing. When using this function, refer to [Chapter 17 AC Timing Variable] and recommend the AC timing to be filled.</u>
	Fifth Note	Description addition	-	<u>If accessing the external expansion memory area, execute with 5 MHz or less of access rate.</u>
II-38	First Note	Description change	<u>Key</u> In the memory expansion mode, unused ...	<u>Note</u> In the memory expansion mode, unused ...
II-39	First Note	Description change	<u>Key</u> During single-chip mode, do not set the...	<u>Note</u> During single-chip mode, do not set the...
II-42	1	Change	This LSI has <u>three</u> sets of system clock oscillator (high speed oscillation, <u>multiplied high speed oscillation</u> , low speed oscillation) for <u>two</u> CPU operating modes (NORMAL and SLOW), ...	This LSI has <u>two</u> sets of system clock (<u>fs</u>) oscillator (high speed oscillation, low speed oscillation) <u>and PLL circuit to multiply high speed oscillation</u> , for <u>three</u> CPU operating modes (NORMAL, <u>PLL</u> and SLOW), ...
II-43	2	Description change	The CPU stops operating. But both of the oscillators remain operational in HALT0 and <u>only the high-frequency oscillator stops operating in HALT1</u> . <u>An interrupt returns the CPU to the previous CPU operating mode that is, to NORMAL from HALT0 or to SLOW from HALT1 or to PLL from HALT2.</u>	<u>The CPU stops operation. The oscillator or PLL are operating. An interrupt allows the CPU to operate.</u> <u>The high and low-frequency oscillators operate in HALT0. When an interrupt occurs, HALT0 enters into the normal operation state (NORMAL).</u> <u>...</u> <u>Both of the oscillators and PLL operate in HALT2. When an interrupt occurs, HALT2 enters into PLL modes.</u>
	18	Description change	The PLL-IDLE allows time for <u>the multiplied high-frequency oscillator</u> to stabilize when the software is changing from NORMAL to PLL mode.	The PLL-IDLE allows time for the <u>clock from PLL</u> to stabilize when the software is changing from NORMAL to PLL mode.
	23	Description addition	This LSI has <u>two</u> system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and...	This LSI has <u>three</u> system clock oscillation circuits. OSC <u>or PLL</u> is for high-frequency operation (NORMAL, <u>PLL</u> mode) and

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-44	Second Note	Description change	In <u>idle</u> state, the clock of the oscillator for ...	In <u>OSC-IDLE</u> state, the clock of the oscillator for ...
	Third Note	Description addition	-	<u>When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand...</u>
II-45		Description deletion	-	Page II-42 of the former edition deleted.
	Figure 2.5.2	Description change	Operation mode HALT0 OSCI/OSCO Oscillation System clock OSCI	Operation mode HALT0 (<u>HALT2</u>) OSCI/OSCO Oscillation(<u>PLL Oscillation</u>) System clock OSCI(<u>PLL</u>)
	3	Description change	1. <u>If the return factor is a maskable ...</u> 2. <u>Clear the interrupt request flag ...</u>	1. <u>Clear the interrupt request flag ...</u> 2. <u>If the return factor is a maskable ...</u>
II-46	First Note	Error correction	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock switching function (OSCDBL, OSCSEL1 and <u>OSCSEL2</u> flags) at the same time.	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock switching function (OSCDBL, OSCSEL1 and <u>OSCSEL0</u> flags) at the same time.
	Second Key	Description addition	... to clear interrupt request flag by software.	... to clear interrupt request flag by software. <u>After clear interrupt request flag, must clear the IRWE flag.</u>
	Second Note	Description addition	-	<u>The STOP, the HALT, the OSC1 or the OSC0 flags of the CPUM mode control ...</u>
II-47	1	Error correction	This LSI has <u>two</u> CPU operating modes, NORMAL and SLOW.	This LSI has <u>three</u> CPU operating modes, NORMAL, <u>PLL</u> and SLOW.
	First Note	Description addition	-	<u>We recommend selecting the oscillation stabilization time of slow oscillation after consulting with oscillator manufacturers.</u>
	Third Note	Description addition	-	<u>When SLOW mode, don't operate the peripheral circuits by a high-speed oscillation. A high-speed oscillation has stopped at the SLOW mode.</u>
II-48	1	Error correction	This LSI has <u>two</u> <u>PLL</u> operating modes, <u>NORMAL</u> and <u>PLL</u> .	This LSI has <u>three</u> CPU operating modes, NORMAL, PLL and SLOW.
	Program 1 line 2	Description addition	Program 1 BCLR (PLLCNT) 1...	Program 1 <u>BSET (XSEL)2 ; Built-in ROM access method setting</u> BCLR (PLLCNT) 1...
	First Note	Description addition	-	<u>When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand...</u>
	Program 3 line 2	Error correction	Program 3 MOV x'03', D0 ; A loop ...	Program 3 MOV x'43', D0 ; A loop ...
	Second Note	Description addition	-	<u>Necessary time for steady operation of PLL is 100 μs. The stabilization waiting time is inserted by software.</u>
	Third Note	Description addition	-	<u>Do neither multiplication setting of PLL nor oscillation start of PLL at the same time.</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-49	Figure 2.5.3	Error correction	<pre> graph TD A[NORMAL/SLOW mode] --> B[Disable all interrupts] B --> C[Enable interrupt which triggers return] C --> D[Set HALT/STOP mode] D --> E[HALT/STOP mode] style E fill:none,stroke:none E --- F["(Watchdog timer HALT : stop counting STOP : clear counter)"] </pre>	<pre> graph TD A[NORMAL/SLOW mode] --> B[Enable interrupt which triggers return] B --> C[Disable all interrupts] C --> D[Set HALT/STOP mode] D --> E[HALT/STOP mode] style E fill:none,stroke:none E --- F["(Watchdog timer HALT : stop counting STOP : clear counter)"] </pre>
II-50	Second Note	Description change	<u>Set bp5 of XSEL register (0x03F2F) before the transition to slow oscillation mode.</u>	<u>When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).</u>
II-51	First Note	Description change	<u>Key</u>	<u>Note</u>
	Second Note	Description change	<u>Key</u>	<u>Note</u>
	Third Note	Description change	<u>Set bp5 of XSEL register (0x03F2F) before the transition to slow oscillation mode.</u>	<u>When the transition to low-speed oscillation mode, wait the oscillation stabilization waiting time of low-speed oscillation enough after set bp5 of XSEL register (0x03F2F).</u>
	Fourth Note	Description addition	-	<u>When can't ensure to generate the return interrupt sources after transmission request for standby mode (HALT/STOP) by setting to CPUM register, refer to [2.5.6 Attention of Transition to Standby Mode].</u>
II-52	Chapter	Description addition	-	2.5.6 Attention of Transition to Standby Mode
II-53	5,9	Description change	low-frequency oscillation selection register (XSEL)	low-speed oscillation selection register (XSEL)
	Program 6 line 2	Description addition	Program 6 MOV x'20', (XSEL) ; Set... MOV x'02', (TM0MD) ; Select ...	Program 6 MOV x'20', (XSEL) ; Set... MOV x'FF', D0 <u>LOOP ADD -1, D0</u> <u>BNE LOOP</u> ; Loop to ... MOV x'02', (TM0MD) ; Select...
II-54	Page	Description addition	-	Low-speed oscillation is also ... - Low-speed oscillation selection register (XSEL) ...
II-55	Chapter	Description addition	-	2.5.8 Method for Accessing to Internal ROM
II-57	CPUM bp7	Description change	<u>Description Set always to "0"</u>	<u>Description Always set to "0" *</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-58	First Note	Error correction	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock switching function (OSCDBL, OSCSEL1 and <u>OSCSEL2</u> flags) at the same time.	Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock switching function (OSCDBL, OSCSEL1 and <u>OSCSEL0</u> flags) at the same time.
	Second Note	Error correction	Set the dividing ratio of oscillation clock to meet the operating condition (refer to Chapter 1 "Electrical Characteristics"). <u>When the dividing ratio is 1, the frequency of fosc should not exceed the maximum frequency of fs (fosc: high-speed oscillation clock, fs: system clock)....</u>	Set the dividing ratio of oscillation clock <u>and transition to the operation mode</u> to meet the operating condition (refer to Chapter 1 "Electrical Characteristics").
	Third Note	Description change	When system clock is over 10 MHz, set bp2 of XSEL register (0x03F2F) <u>before the setting of PLLCNT</u>	When system clock is over 10 MHz, set bp2 of XSEL register (0x03F2F) <u>and change the access method to built-in ROM area to handshake</u>
II-59	1	Description change	High-speed oscillation clock multiply function is to generate a clock , 2-fold, 3-fold, 4-fold, 5-fold, 6-fold, 8-fold and 10-fold of high-speed oscillation input from OSC1/OSC2.	High-speed oscillation clock multiply function is to generate a clock , <u>2/ 3/ 4/ 5/ 6/ 8/ 10-multiply</u> of high-speed oscillation input from OSC1/OSC2.
	Figure 2.7.1	Description change	<u>fold</u>	<u>multiply</u>
	PLLCNT bp7-4	Description change	Flag description 4' h0: 2-fold (Input frequency 4-7.5 MHz) 4' h1: 2-fold (Input frequency 7.5-10 MHz) 4' h2: 3-fold (Input frequency 4-5 MHz) 4' h3: 4-fold (Input frequency 4-7.5 MHz) 4' h4: 4-fold (Input frequency 7.5-10 MHz) 4' h5: 5-fold (Input frequency 4-6 MHz) 4' h6: 5-fold (Input frequency 6-8 MHz) 4' h7: 6-fold (Input frequency 4-5 MHz) 4' h8: 8-fold (Input frequency 4-5 MHz) 4' h9: 10-fold (Input frequency 4 MHz)	Flag description 4' h0: 2-multiply (Input frequency 4-7.5 MHz) 4' h1: 2-multiply (Input frequency 7.5-10 MHz) 4' h2: 3-multiply (Input frequency 4-5 MHz) 4' h3: 4-multiply (Input frequency 4-7.5 MHz) 4' h4: 4-multiply (Input frequency 7.5-10 MHz) 4' h5: 5-multiply (Input frequency 4-6 MHz) 4' h6: 5-multiply (Input frequency 6-8 MHz) 4' h7: 6-multiply (Input frequency 4-5 MHz) 4' h8: 8-multiply (Input frequency 4-5 MHz) 4' h9: 10-multiply (Input frequency 4 MHz)
	PLLCNT bp7-4	Error correction	Flag description ... 4' h9: 10-fold (Input frequency 4 MHz)	Flag description ... 4' h9: 10-multiply (Input frequency 4 MHz) 4' h10-15: Setting prohibited
	First Note	Description deletion	<u>When system clock is over 10 MHz, set bp 2 of XSEL register (0x03F2F) before the setting of PLLCNT.</u>	-
II-60	2 Setup proce- dure(1)(4)	Description change	2-fold	2-multiply
	Setup procedure	Description addition	-	(3) <u>MOV_0x43, D0</u> <u>LOOP ADD -1, D0</u> <u>BNE LOOP</u>
	Description	Description addition	-	(3) Wait PLL operation waiting time 100 <u>μs</u> by software.(4 MHz)

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-61	First Note	Description addition	The setup described above can not be done at the same time.	The setup described above can not be done at the same time. <u>When set PLL, has to switch by above setting.</u>
	Second Note	Description change	<u>Set in order of (3) and (2) for transition to NORMAL mode.</u>	<u>Switch in the bit order of (4) and (2) for transition to NORMAL mode.</u>
	Fifth Note	Description addition	-	<u>Don't set PLLSTART flag by the state of PLLEN flag = "0" of PLLCNT register.</u>
	First Key	Description addition	Refer to [2.5 Standby Function] for operation mode trasition.	Refer to [2.5 Standby Function] for operation mode trasition. <u>The direct transition from the slow mode to the PLL mode can not be enabled...</u>
	Sixth Note	Description addition	-	<u>When operated with the system clock (fs) > 10 MHz by using PLL mode, set bp2 of the XSEL register beforehand...</u>
	Seventh Note	Description addition	-	<u>The operation does not guaranteed if the system clock operates over 20MHz. Set the multiply number in 20MHz or...</u>
	II-62	Description change	This LSI is activated in NORMAL mode in which the base clock is <u>high frequency</u> .	This LSI is activated in NORMAL mode in which the base clock is <u>external high-speed oscillation</u> .
II-63	Third Note	Description addition	In this LSI, the oscillation (High-speed oscillation and Low speed oscillation) is stopped.	In this LSI, the oscillation (High-speed oscillation and Low speed oscillation) is stopped at reset.
	Square	Description addition	-	<u>- Reset Sequence at the time of Power Supply Injection.</u>
II-65	Figure 2.8.4	Error correction		
II-66	First Note	Description change	<u>Please set the value by which on oscillation circuit is stabilized enough to the waiting cycle for oscillation stability.</u>	For the oscillation stabilization wait cycle required for high-speed/low-speed oscillation, which is set by DLYS 1-0 flags, it is recommended to consult the oscillator manufacturer for determining appropriate values.
	Second Note	Description addition	-	<u>When recovering from STOP mode, more than 100 μs of oscillation stabilization wait cycle must be set for internal regulator output stabilization wait.</u>
	2 from the bottom	Description Deletion	*1 Do not use at the high-speed operation (NORMAL mode, PLL mode). Use at the low-speed operation (SLOW mode).	-

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
II-68	2	Description addition	-	<p><u>Auto reset function can be selected with ATRST pin (11 pin)</u></p> <ul style="list-style-type: none"> - In using auto reset --- ATRST pin (11 pin) : V_{DD5} level fixed - In not using auto reset --- ATRST pin (11 pin) : V_{SS} level fixed
	5	Description change	<u>After detecting a low voltage, NRST pin automatically becomes "L" level and reset operation is executed. When power supply voltage reaches reset cancellation voltage (VRST), NRST pin automatically becomes "H" and reset is cancelled.</u>	<u>When detecting a low voltage at auto reset function, NRST pin automatically becomes "L" level and reset operation is executed. When power supply voltage reaches reset cancellation voltage (VRST), NRST pin automatically becomes "H" and reset is cancelled.</u>
	Figure 2.9.1	Error correction	Figure:2.9.1 V_{DD} RST	Figure:2.9.1 <u>Auto Reset Detection Voltage</u> V_{DD5} NRST
	First Key	Description addition	-	<u>Refer to [Chapter I 1.5.7 Auto Reset Characteristics] for VRST.</u>
	First Note	Description addition	-	<u>When use the auto reset function, "L" level input to NRST pin has to keep at least 100 μs or more. Connect ...</u>
II-70	First Note	Description addition	-	<u>Don't set a number of bits at the same time.</u>
III-3	Table 3.1.1	Description addition	-	<u>IVBM=0</u> <u>IVBM=1 0x00104 0x00108 to 0x00178</u>
III-5	Figure 3.1.2	Description addition	Save PC, PSW, etc Restore PSW, PC, etc	Save PC, PSW, <u>HA</u> , etc Restore PSW, PC, <u>HA</u> , etc
III-6	Table 3.1.2	Description addition	Vector Addresses 0x04000 0x04078	Vector Addresses <u>IVBM = 0 IVBM = 1</u> <u>0x04000 0x00100</u> <u>0x04078 0x00178</u>
III-7	5	Error correction	For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupt simultaneously, vector 3 will be accepted.	For example, if a vector 3 set to level 1 and a vector 4 set to level 1 request interrupt simultaneously, vector 3 will be accepted.
	Figure 3.1.3	Error correction	Level1 Vector 3 Level2 Vector 4, 8	Level1 Vector 3, 4 Level2 Vector 8
III-8	Square	Error correction	1. The interrupt request flag (<u>xxxR</u>)	1. The interrupt request flag (<u>xxxIR</u>)
	Square	Description change	-	2. to 3. in Determination of Maskable Interrupt Acceptance changed
	Note	Description addition	-	<u>After accept of an interrupt, interrupt of same source is disregarded until ...</u>
III-9	8	Error correction	<u>BE</u> instruction is executed. (BKD is set and MIE is set	<u>BD</u> instruction is executed. (BKD is set and MIE is set
	16	Error correction	Non-Maskable interrupt is accepted (it to 0 (oob)).	Non-Maskable interrupt is accepted (it to 0 (00b)).
	Note	Description change	<u>The MN101C series does not reset the maskable interrupt enable (MIE) flag of the processor status word (PSW) to "0" when accepting interrupts.</u>	<u>The maskable interrupt enable (MIE) flag of the processor status word (PSW) is not set to "0" when accepting interrupts.</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-10	8	Error correction	<p><u>2. The contents of the handy addressing...</u></p> <p><u>Upper ...</u></p> <p><u>Lower...</u></p> <p><u>3. The contents of the program counter...</u></p> <p><u>PC bits 20 to 17...</u></p> <p><u>PC bits 16 to 9...</u></p> <p><u>PC bits 8 to 1...</u></p>	<p><u>2. The contents of the program counter...</u></p> <p><u>PC bits 7 to 0...</u></p> <p><u>PC bits 15 to 8...</u></p> <p><u>PC bits 19 to 16...</u></p> <p><u>3. The contents of the handy addressing</u></p> <p><u>Lower...</u></p> <p><u>Upper ...</u></p>
	Figure 3.1.5	Error correction		
III-11	Second Note	Error correction	The address bp6 to bp4, when program counter (PC [bit20 to bit17, bit0]) are...	The address bp6 to bp4, when program counter (PC [bit19 to bit16, bitH]) are ...
III-17	First Note	Description addition	-	<u>Interrupt request flag of interrupt control register is set by interrupt generation, the edge ...</u>
	Second Note	Description addition	-	<u>Always set IRWE flag of memory control register (MEMCTR) to "0" except in writing IR with ...</u>
	Third Note	Description addition	-	<u>Make processor status word (PSW) and maskable interrupt enable flag (MIE) of prohibited ...</u>
III-19	Third Note	Description addition	-	<u>When interrupt request of same bit and above-mentioned request flag by the software is generated ...</u>
III-20	Description	Description addition	(5) ... contents to clear the flags.	(5) ... contents to clear the flags. <u>It clears by this method because there is a possibility that internal interrupt ...</u>
	Description	Description addition	(6) ... interrupt control register (PERIIRQ).	(6) ... interrupt control register (PERIIRQ). <u>It clears by this method because there is a possibility that interrupt request flag has already been set.</u>
	Setup procedure	Description addition	-	<u>(7) Disable writing of the interrupt request flag.</u> <u>MEMCTR(0x03F01)</u> <u>bp2:IRWE =0</u>
	Description	Description addition	-	<u>(7) Clear the IRWE flag to disable writing of the interrupt request flag by software.</u>
	Setup procedure	Description deletion	(9) Clear the extended interrupt request flag <u>IRQEXPDT(0x03F4F)</u> <u>bp x:IRQEXPDTx=1</u>	-
	Description	Description deletion	(9) Write "1" in the appropriate flags of the internal interrupt extended interrupt factor holding register (IRQEXPDT) to clear the request flags.	-
	First Note	Description addition	-	<u>Extended interrupt request flag (IRQEXPDT) is set by interrupt generation regardless of setting</u>

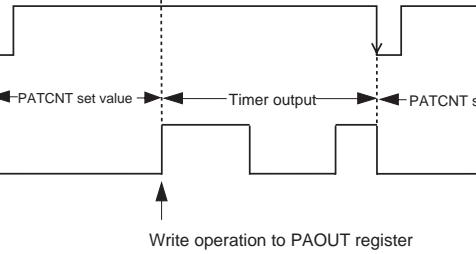
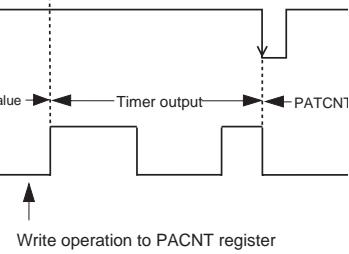
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-21	Square	Description addition	-	<u>- Example of Internal Interrupt Extended Interrupt Processing Program</u>
III-23	Second Note	Description addition	<u>Writing to the interrupt control register should be done after that all maskable interrupts are set to be disable by the MIE flag of the PSW register.</u>	<u>Make processore status word (PSW) and mascable interrupt enable flag (MIE) of prohibited all mascable interrupts (Set MIE flag to "0") before writing to interrupt control register (xxxICR). If writing to interrupt control register with setting MIE flag to "1", we can not guarantee normal operation.</u>
III-24	1,5	Error correction	<u>NMICTR</u>	<u>NMICR</u>
	3	Description addition	the external interrupt control register	the external interrupt control register(<u>IRQnICR</u>)
	10	Description deletion	<u>Setting IRQNPG or IRQNWDG flag to be "1" enables non-maskable interrupt request to be set compulsory.</u>	-
	NMICR bp0	Description change	Description <u>Set always to "0"</u>	Description <u>Always set to "0" *</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
III-26	bp1 bp0	Error correction	Flag <u>TM0IE</u> <u>TM0IR</u>	Flag <u>TMnIE</u> <u>TMnIR</u>
III-43	IRQEXPDT bp7	Description addition	Description Always set to "0"	Description Always set to "0" *
III-44	First Note	Description addition	-	<u>Peripheral Function Group Interrupt can not be used as a returning source from the standby mode.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
	Third Note	Description addition	-	<u>When interrupt request of same bit and above-mentioned request flag by the software is generated ...</u>
III-45	Chapter 3.2.3	Description addition	-	<u>3.2.3 Internal Interrupt Extended Interrupt Interface Block Diagram</u>
III-47 to 52	Figure 3.3.1 3.3.2 3.3.3 3.3.4 3.3.5	Error correction	<u>fosc</u>	<u>fpll</u>
	Figure 3.3.1 3.3.2 3.3.3 3.3.4 3.3.5 3.3.6	Description addition	"Stanby mode signal reverse" in "External Interrupt 1-4 Block Diagram" : <u>AND</u>	"Standby mode signal" in "External interrupt 1 to 4 block diagram" : <u>Delete</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-49	Figure 3.3.3	Error correction	<p>Diagram illustrating the error correction logic for NF2CTR. The circuit includes a Noise filter, Counter, MUX, Level detection circuit, Match detection circuit, and various control registers (LVLMD, EXLV1-4, REDG2, ICR2LVO, ICR2LV1).</p>	<p>Diagram illustrating the error correction logic for NF2CTR in the New Edition (2.1). The logic is similar to the former edition but with some changes in register names and connections.</p>
III-50	Figure 3.3.4	Error correction	<p>Diagram illustrating the error correction logic for NF4CTR. The circuit includes a Noise filter, Counter, MUX, Level detection circuit, Match detection circuit, and various control registers (LVLMD, EXLV1-4, REDG4, ICR4LVO, ICR4LV1).</p>	<p>Diagram illustrating the error correction logic for NF4CTR in the New Edition (2.1). The logic is similar to the former edition but with some changes in register names and connections.</p>
III-51	Figure 3.3.5	Error correction	<p>Diagram illustrating the error correction logic for NF4CTR. The circuit includes a Noise filter, Counter, MUX, Level detection circuit, Match detection circuit, and various control registers (LVLMD, EXLV1-4, REDG4, ICR4LVO, ICR4LV1).</p>	<p>Diagram illustrating the error correction logic for NF4CTR in the New Edition (2.1). The logic is similar to the former edition but with some changes in register names and connections.</p>
III-52	Figure 3.3.6	Error correction	<p>Detailed circuit diagram for Figure 3.3.6 showing the internal structure of the error correction logic for NF4CTR, including multiple noise filters, counters, and multiplexers.</p>	<p>Detailed circuit diagram for Figure 3.3.6 showing the internal structure of the error correction logic for NF4CTR in the New Edition (2.1), with some structural differences compared to the former edition.</p>
III-56	NF0CTR to NF4CTR	Error correction	Flag, Description bp3: <u>NFnEN0, ...</u> bp2-0: <u>PSnCNT2-0, ...</u>	Flag, Description bp3-0: <u>Reserved, Always set to "0".</u>
	2 from the bottom	Description Deletion	*1 Sampling function is incorporated only in IRQ2, 3. *2 bp3-0 is only NF2CTR, NF3CTR	-

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-58	2	Description change	Both edges interrupt control register (EDGDT) select interrupt edges of IRQ2 to 5. With this register, the edge to generate the interrupts is selected; both edges or the edge which is specified by the external interrupt control register (IRQ2ICR, IRQ3ICR, IRQ4ICR).	<u>Bp 2,3,5 of both edges interrupt control register (EDGDT) select interrupt edges of IRQ2 to 4.</u> With this register, the edge to generate the interrupts is selected; both edges or the edge which is specified by the external interrupt control register (IRQ2ICR, IRQ3ICR, IRQ4ICR). <u>When the edge detection circuit in the key interrupt block is used with bit common/bit independant or bit independant, the edge to generate the interrupt is selected; both edges or the edge which is specified by the external interrupt control register (IRQ5ICR) with the register selecting IRQ5 key interrupt edge.</u>
EDGDT	Description change	bp7 Description <u>Key interrupt both edges operation selection 1</u> 0:Programmable active edge interrupt selection 1:Both edges interrupt selection	bp7 Description <u>IRQ5 Key interrupt both edges operation selection (Enable at bp:0 EDGSEL0 = "1")</u> 0:Programmable active edge interrupt selection <u>(Specified with IRQ5ICR bp:5 REDG5)</u> 1:Both edges interrupt selection	
		bp5 Description 0:Programmable active edge interrupt selection	bp5 Description 0:Programmable active edge interrupt selection <u>(Specified with IRQ4ICR bp:5 REDG4)</u>	
		bp3 Description 0:Programmable active edge interrupt selection	bp3 Description 0:Programmable active edge interrupt selection <u>(Specified with IRQ3ICR bp:5 REDG3)</u>	
		bp2 Description 0:Programmable active edge interrupt selection	bp2 Description 0:Programmable active edge interrupt selection <u>(Specified with IRQ2ICR bp:5 REDG2)</u>	
		bp0 Description <u>Key interrupt both edges operation selection 2</u> 0:Falling edge ("L" level) 1:Rising edge ("H" level)	bp0 Description <u>IRQ5 Key interrupt selection</u> 0: <u>Key input Edge detection circuit bit common *</u> 1: <u>Key input Edge detection circuit bit independant</u>	
	Last line	Description addition	-	* <u>Detail of operation refers to [3.3.7 Key Input Interrupt].</u>
III-59	First Key	Description addition	-	<u>If the key input edge detection circuit is selected bit common with EDGSEL0 flag, the ...</u>
	Second Key	Description addition	-	<u>If the key input edge detection circuit is selected bit independant with EDGSEL0 flag ...</u>
	First Note	Description addition	-	<u>EDGSEL7 flag is enable only when the key input edge detection circuit is selected bit independant with EDGSEL0 flag ...</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
III-60	LVLMD	Description addition	bp5 Description External interrupt 4 Enable Input Level setup 0:L level 1:H level	bp5 Description External interrupt 4 Enable Input Level setup <u>(Enable at bp:4 LVLEN4="1")</u> 0:L level 1:H level
		Description addition	bp3 Description External interrupt 3 Enable Input Level setup 0:L level 1:H level	bp3 Description External interrupt 3 Enable Input Level setup <u>(Enable at bp:3 LVLEN3="1")</u> 0:L level 1:H level
		Description addition	bp1 Description External interrupt 2 Enable Input Level setup 0:L level 1:H level	bp1 Description External interrupt 2 Enable Input Level setup <u>(Enable at bp:2 LVLEN2="1")</u> 0:L level 1:H level
III-63	First Key	Description addition	... so that unknown value is not input.	... so that unknown value is not input. <u>If unknown value is input to pin, through current flow.</u>
III-64	Description	Error correction	(4) Set the <u>IRQ2E</u> flag of ...	(4) Set the <u>IRQ2E</u> flag of ...
III-65	Second Key	Description addition	... so that unknown value is not input.	... so that unknown value is not input. <u>If unknown value is input to pin, through current flow.</u>
III-67	Third Note	Description change	<u>Key</u>	<u>Note</u>
III-68	3	Description addition	...Also, if the key input pin becomes low level, it is possible from the standby mode.	... Also, if the key input pin becomes low level, it is possible <u>to return</u> from the standby mode. <u>When rising edge is set by the external interrupt 5 (ICR5IRQ), the key input default state is changed from "L" to "H".</u>
		Setup Procedure	Error correction (1) Set the key input to input P5DIR(0x03F35) bp <u>3</u> -0:P5DIR7-0=00000000	(1) Set the key input to input P5DIR(0x03F35) bp <u>7</u> -0:P5DIR7-0=00000000
III-70	Square	Description deletion	Noise remove Function Operation After sampling the input signal to ... , the previous level is sent. <u>It means that only the signal ...</u>	Noise remove Function Operation After sampling the input signal to ... , the previous level is sent.
III-72	Setup procedure	Description change	(1),(2),(3),(4),(5)	(1)→(2),(2)→(3),(3)→(4),(4)→(5),(5)→(6)
	Setup procedure	Description addition	-	<u>(1) External interrupt setup</u> <u>IRQCNT (0x03F3D)</u> <u>bp0:P20EN =1</u>
	Description	Description addition	-	<u>(1) Set the P20EN flag of the external interrupt setting register (IRQCNT) to "1" to set P20 to external interrupt.</u>
	Setup procedure	Error correction	(3) bp <u>2</u> -1	(3) bp7-5
	Setup procedure	Error correction	(4) bp <u>0</u>	(4) bp4
	3 from the bottom	Description change	Above (2) and (3) can be set at the same time.	Above (3) and (4) can be set at the same time.

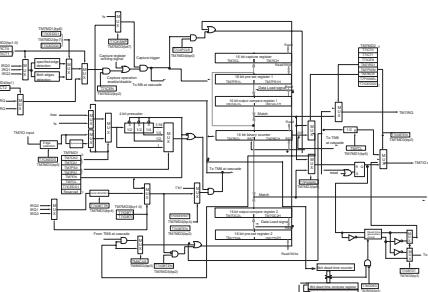
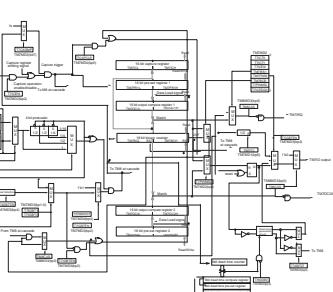
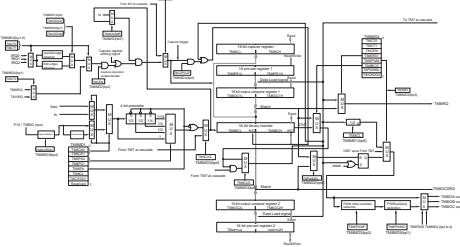
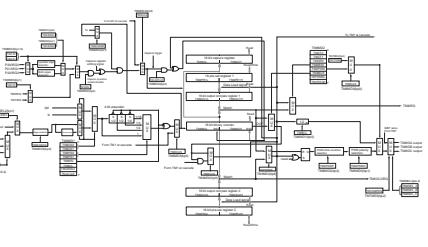
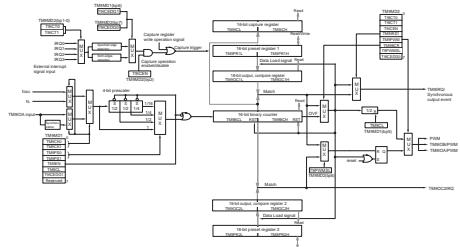
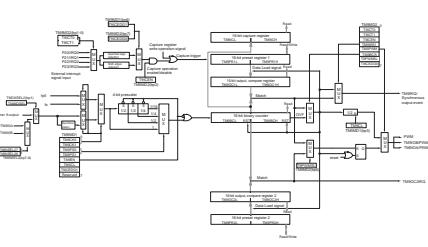
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IV-3	First Key	Description addition	-	<u>The values of pull-up/pull-down resistors should be calculated in the following ways based on the electrical ...</u>
IV-14 IV-28 IV-41 IV-54 IV-68 IV-82 IV-95 IV-110	2	Description addition	-	<u>The input level of P0 (P00 to P07) to P7 (P70 to P77) recognized "H" can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.</u>
	bp7 to bp0	Description change	<u>Port 7</u> <u>Port 6</u> <u>Port 5</u> <u>Port 4</u> <u>Port 3</u> <u>Port 2</u> <u>Port 1</u> <u>Port 0</u>	<u>Port 70 to Port 77</u> <u>Port 60 to Port 67</u> <u>Port 50 to Port 57</u> <u>Port 40 to Port 47</u> <u>Port 30 to Port 36</u> <u>Port 20 to Port 24</u> <u>Port 10 to Port 16</u> <u>Port 00 to Port 07</u>
IV-16-23	Chapter	Description addition	-	Add block diagram of each port 4.3.3 Block Diagram
IV-31-37	Chapter	Description addition	-	Add block diagram of each port 4.4.3 Block Diagram
IV-43-48	Chapter	Description addition	-	Add block diagram of each port 4.5.3 Block Diagram
IV-49	3 from the bottom	Error correction	... When the <u>SC4SBOS</u> flag of the serial interface 4 mode register 1 (SC4MD1) is "1", When the <u>SC4SBTS</u> flag of the serial interface 4 mode register 1 (SC4MD1) is "1", ...
IV-50	1	Error correction	... When the <u>SC2SBIS</u> flag of the serial interface 4 mode register 1 (SC4MD1) is "1", When the <u>SC4SBIS</u> flag of the serial interface 4 mode register 1 (SC4MD1) is "1", ...
IV-56-62	Chapter	Description addition	-	Add block diagram of each port 4.6.3 Block Diagram
IV-70-77	Chapter	Description addition	-	Add block diagram of each port 4.7.3 Block Diagram
IV-85-90	Chapter	Description addition	-	Add block diagram of each port 4.8.3 Block Diagram
IV-97-104	Chapter	Description addition	-	Add block diagram of each port 4.9.3 Block Diagram
IV-112-119	Chapter	Description addition	-	Add block diagram of each port 4.10.3 Block Diagram
IV-127 IV-139 IV-150 IV-163	3 or 2	Description addition	-	<u>The input level of P8 (P80 to P87) to PB (PB0 to PB7) recognized "H" can select 0.8 V_{DD5} or more or 0.54 V_{DD5} or more.</u>
	bp3 to bp0	Description change	<u>Port B</u> <u>Port A</u> <u>Port 9</u> <u>Port 8</u>	<u>Port B0 to Port B7</u> <u>Port A0 to Port A7</u> <u>Port 90 to Port 96</u> <u>Port 80 to Port 87</u>
IV-128-135	Chapter	Description addition	-	Add block diagram of each port 4.11.3 Block Diagram
IV-140-143	Chapter	Description addition	-	Add block diagram of each port 4.12.3 Block Diagram

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IV-146	Square	Error correction	-Port A Pull-up Resistor Control Register(<u>PAPLUD</u> :0x03F4A)	-Port A Pull-up Resistor Control Register(<u>PAPLU</u> :0x03F4A)
IV-151-158	Chapter	Description addition	-	Add block diagram of each port 4.13.3 Block Diagram
IV-164	Chapter	Description addition	-	Add block diagram of each port 4.14.3 Block Diagram
IV-166	Second Note	Description addition	-	<u>When real time output realease (the write operation to P8CNT1, P8CNT2 and PACNT) and the event generation ...</u>
IV-167	Figure 4.15.1	Error correction	 <p>The diagram illustrates the timing sequence for writing to the PAOUT and PACNT registers. It shows three signals: PATCNT set value (top), Timer output (middle), and PATCNT signal (bottom). In both cases, a write operation is triggered by a pulse on the PATCNT signal. The PATCNT set value is updated at the start of the pulse, and the Timer output is updated during the pulse.</p>	 <p>The diagram illustrates the timing sequence for writing to the PAOUT and PACNT registers. It shows three signals: PATCNT set value (top), Timer output (middle), and PATCNT signal (bottom). In both cases, a write operation is triggered by a pulse on the PATCNT signal. The PATCNT set value is updated at the start of the pulse, and the Timer output is updated during the pulse.</p>
IV-169	Square	Error correction	- Port 8 Synchronous Output (Timer 1,2 and 7) ... The port 8 output latched data is output from the port <u>7</u> at the timing of the TMnIRQ flag rising.	- Port 8 Synchronous Output (Timer 1,2 and 7)... The port 8 output latched data is output from the port <u>8</u> at the timing of the TMnIRQ flag rising.
V-3	Table Clock source of Time 1	Error correction	Synchronous <u>TM1O</u> input	Synchronous <u>TM1IO</u> input
V-11	CK1MD	Error correction	bp3-0 0X11 : fs/ <u>4</u> 1XX1 : fs/ <u>8</u>	bp3-0 0X11 : fs/ <u>8</u> 1XX1 : fs/ <u>4</u>
V-12	CK3MD	Error correction	bp3-0 0X11 : fs/ <u>4</u> 1XX1 : fs/ <u>8</u>	bp3-0 0X11 : fs/ <u>8</u> 1XX1 : fs/ <u>4</u>
V-26	Table	Description change	fosc=10 MHz	fpll=fosc=10 MHz
V-28	First Key	Description addition	... = (count till the interrupt request -1)	... = (count till the interrupt request -1) <u>However, the interrupt generation cycle when the compare register is set to "00" is the same as it is set to "01".</u>
	Third Key	Error correction	If the interrupt is enabled, the timer interrupt request ...	If the timer interrupt request flag may have already been set before timer is started, the timer interrupt request ...
V-29	First Key	Description deletion	If "00" is specified for the Compare Register (TMnOC), an interrupt timing is the same as if you set it to "01".	-
	First Note	Description addition	-	If CPU operation mode is changed (from NORMAL to SLOW) when the high-frequency oscillation clock (fpll) or ...

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
V-33	First Key	Description change	<u>Note</u>	<u>Key</u>
	First Note	Description addition	-	<u>Input from TMnIO should be used to a waveform, which has 2 times and over cycles of system clock (fs). If less than the above waveforms are input, it may not be counted correctly.</u>
V-34	Setup procedure	Error correction	(3) Set the special function pin to input PADIR(0x03F3A) bp0 :PADIRO =0	(3) Set the special function pin to input PADIR(0x03F3A) bp0 :PADIRO =0 <u>TMINSEL1(0x03E44)</u> <u>bp1-0: TMINSEL11-10=00</u> <u>TMCKSEL1(0x03E42)</u> bp0 :TM0IOSEL =0
	Description	Error correction	(3) Set the PADIRO flag of the port A direction control register (PADIR) to "0" <u>to set PA0 pin to input mode....</u>	(3) Set the PADIRO flag of the port A direction control register (PADIR) to "0", <u>TMINSEL11 to 10 flag of TMINSEL1 register to "00" and TM0IOSEL of TM0IOSEL1 register to "0" in order to set PA0 pin to input mode.</u>
	Setup procedure	Description deletion	(4) Select the count clock source <u>TM0MD(0x03F54)</u> <u>bp2-0 :TM0CK2-0 =X01</u>	-
	Description	Description deletion	(4) <u>Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.</u>	-
V-38	First Key	Description change	If any data is written to compare register when the binary counter is stopped, timer output is <u>reset to "L"</u> .	If any data is written to compare register when the binary counter is stopped, timer output is "L".
V-40	3	Error correction	(A) is "H" while <u>counting</u> up from 0x01 ...	(A) <u>TMnIO output is "H" while the value of binary counter count</u> up from 0x01 ...
	5	Error correction	(B) is "L" after the match to the value ...	(B) <u>TMnIO output is "L" after the value of binary counter match</u> to the value
V-42	5,6,8,9 Table 5.7.2	Error correction	<u>bits 4 and 5 of CK*MD</u> Table:5.7.2 <u>bit5, bit4</u>	<u>bits 5 and 6 of CK*MD</u> Table:5.7.2 <u>bit6, bit5</u>
V-43	First Note	Description addition	-	<u>Do not change the setting of Timer n prescaler selection register (CKnMD) during timer operation.</u>
V-44	Description	Description addition	(3) Set the TM0PWM flag of the TM0MD register to "1" and the TM0MOD flag to "0" to select the PWM operation.	(3) Set the TM0PWM flag of the TM0MD register to "1", <u>the TM0MOD flag to "0" and TM0POP flag to "0"</u> to select the PWM operation.
V-47	Description	Error correction	(2) Set the P8SEV1 to 0 flag of the pin control register (P8SEV) to "11" to set the synchronous output event to <u>the timer 2 interrupt</u> .	(2) Set the P8SEV1 to 0 flag of the pin control register (P8SEV) to "11" to set the synchronous output event to <u>the timer 1 interrupt</u> .
V-50	2 from the bottom	Error correction	... TMnEN flag is <u>ON</u> ("1") and TMnEN flag is <u>operated</u> ("1") and ...
V-51	Setup procedure(4)	Error correction	bp2-1 : TM0PSC1-0 = <u>X0</u>	bp3-1 : TM0PSC2-0 = <u>0X0</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
V-52	5.11.1	Description change	5.11.1 Operation	5.11.1 <u>16-bit Cascade Connection Operation</u>
	Square	Description deletion	<u>8-bit Timer Cascade Connection Operation</u>	Operation
	Table	Description change	Table 5.11.1 Timer Functions at Cascade Connection	Table 5.11.1 Timer Functions at <u>16-bit Cascade Connection</u>
V-53	Third key	Description change	At cascade connection, when ...	At <u>16-bit</u> cascade connection, when ...
	Second Note	Description addition	-	<u>Stop the timer in order to read out the value of timer connected in cascade</u>
V-54	Table	Description change	Table 5.11.2 Timer Functions in Cascade Connection	Table 5.11.2 Timer Functions in <u>24-bit</u> Cascade Connection
V-55	Second Key	Description change	At cascade connection, when ...	At <u>24-bit</u> cascade connection, when ...
	Third Note	Description addition	-	<u>Stop the timer in order to read out the value of timer connected in cascade</u>
V-56	Table	Description change	Table 5.11.3 Timer Functions in Cascade Connection	Table 5.11.3 Timer Functions in <u>32-bit</u> Cascade Connection
V-57	Second Key	Description change	At cascade connection, when ...	At <u>32-bit</u> cascade connection, when ...
	Third Note	Description addition	-	<u>Stop the timer in order to read out the value of timer connected in cascade</u>
V-58	Square	Description addition	- Cascade Connection Timer Setup Example (Timer 0 + Timer 2)	- <u>16-bit</u> Cascade Connection Timer Setup Example (Timer 0 + Timer 2)
	Description	Description addition	(1) Set the TM0EN flag ... , the TM1EN flag of the timer 1 mode register to "0" to stop ...	(1) Set the TM0EN flag ... , the TM1EN flag of the timer 1 mode register (<u>TM1MD</u>) to "0" to stop ...
	Setup Procedure(7)	Description change	<u>TMnOC</u> (0x03F52,0x03F53) = 0x09C3	<u>TM1OC,TM0OC</u> (0x03F53,0x03F52) = 0x09C3
VI-2	1	Description change	This timer is a 8-bit simple timer that can be used as a serial transfer clock, LCD <u>frequency or timer count</u> .	This timer is a 8-bit simple timer that can be used as a serial transfer clock, LCD <u>clock or 8 bit/16 bit timer count</u> .
	9	Description change	Table:6.1.1 shows <u>functions that can be used with each timer</u> .	Table:6.1.1 shows <u>clock sources of 8-bit simple timer</u> .
VI-3	Figure 6.1.1	Error correction		
VI-5	5	Description change	If any data is written to compare register the counting is stopped and binary counter is cleared to 0x00.	The binary counter to stop the count operation is cleared to 0x00.

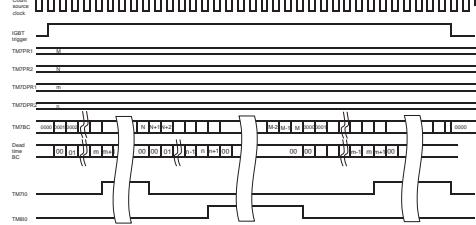
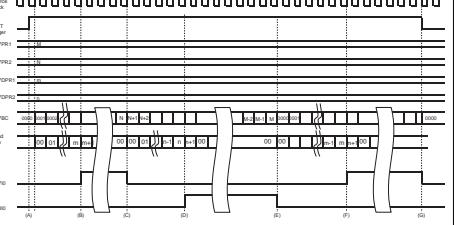
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VI-6	TMAMD1	Error correction	bp4 Flag : At reset : Access : Description : —	bp4 Flag : <u>Reserved</u> At reset : <u>0</u> Access : <u>R/W</u> Description : <u>Always set to "0"</u>
VI-7	TMAMD2	Error correction	bp7 : Access —	bp7 : Access <u>R/W</u>
		Error correction	bp6 Description <u>Timer A count control</u>	bp6 Description <u>Prescaler operation control</u>
VI-8	1	Description deletion	<u>8-bit simple timer contains one timer as an auxiliary function of "Chapter 5 8-bit Timers"</u> —	<u>8-bit simple timer in this LSI contains one timer as only a basic function of "Chapter 5 8-bit Timers".</u>
		Note	Description addition —	<u>When fpll is selected the clock source, prescaler operation control frag (PSGEN flag of TMAMD2 register) is set necessary before set TMAEN flag.</u>
VI-9	Figure 6.3.1	Description deletion		
		Description deletion	(A) If the value is written to the compare register during the TMAEN flag is stopped ("0"), the binary counter is cleared to 0x00.	-
	4	Description deletion	(E) When the TMAEN flag stops operating ("0"), the Internal Enable will be turned off at the next Count Clock. As a result, the binary counter stops counting.	(D) When the TMAEN flag stops operating ("0"), the binary counter stops counting and cleared to 0x00.
	11	Error correction	(E) When the TMAEN flag stops operating ("0"), the Internal Enable will be turned off at the next Count Clock. As a result, the binary counter stops counting.	(D) When the TMAEN flag stops operating ("0"), the binary counter stops counting and cleared to 0x00.
VI-10	Figure 6.4.1	Error correction		
		First Key	Description addition —	The output signal of this timer can use as the clock source of 8-bit timer/16-bit timer as well as above-mentioned the serial transfer clock.
VI-11	Description	Description deletion	(3) ... that the baud rate comes to 300 bps. <u>At that time, the timer A binary counter (TMABC) is initialized to 0x00.</u>	(3) ... that the baud rate comes to 300 bps.
VII-2	1	Description addition	The 16-bit timer has compare register with double buffer.	The 16-bit timer has compare register with double buffer <u>and single buffer</u> . The buffer can be selected.

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-3	Table 7.1.1	Error correction	<u>T7OC2IRQ</u> <u>T8OC2IRQ</u> <u>T9OC2IRQ</u>	<u>TM7OC2IRQ</u> <u>TM8OC2IRQ</u> <u>TM9OC2IRQ</u>
		Description addition	Clock source ... Synchronous TM7IO/16 input	Clock source ... Synchronous TM7IO/16 input <u>Timer A output</u> <u>Timer A output/2</u> <u>Timer A output/4</u> <u>Timer A output/16</u>
VII-4	Figure 7.1.1	Error correction		
VII-5	Figure 7.1.2	Error correction		
VII-6	Figure 7.1.3	Error correction		
VII-12	1	Description addition	Binary counter is a 16-bit up counter. If any data is written to a preset register when ...	Binary counter is a 16-bit up counter. If any data is written to a preset register <u>1</u> when ...
	TM7BCL	Error correction	At reset bp7-0: <u>0</u>	At reset bp7-0: <u>X</u>
	TM7BCH	Error correction	At reset bp7-0: <u>0</u>	At reset bp7-0: <u>X</u>
VII-16	1	Description addition	Binary counter is a 16-bit up counter. If any data is written to a preset register when...	Binary counter is a 16-bit up counter. If any data is written to a preset register <u>1</u> when ...
	TM8BCL	Error correction	At reset bp7-0: <u>0</u>	At reset bp7-0: <u>X</u>
	TM8BCH	Error correction	At reset bp7-0: <u>0</u>	At reset bp7-0: <u>X</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-19	1	Description addition	Binary counter is a 16-bit up counter. If any data is written to a preset register when ...	Binary counter is a 16-bit up counter. If any data is written to a preset register <u>1</u> when ...
VII-22	Description	Description addition	bp6 Buffer selection	bp6 <u>TM7OC1,2</u> buffer selection
	Description	Error correction	bp5 0: <u>Rising</u> edge	bp5 0: <u>Falling</u> edge
VII-23	TM7MD4	Error correction	bp7 Flag : <u>Reserved</u> Description : <u>Always set to "0".</u>	bp7 Flag : <u>T7TRGACT</u> Description : <u>Trigger reception flag of IGBT active outputting</u> 0:Enable 1:Disable
VII-26	Description	Description addition	bp6 Buffer selection	bp6 <u>TM8OC1,2</u> buffer selection
	Description	Error correction	bp4 1: <u>Rising</u> edge	bp4 1: <u>Both</u> edges
	Flag	Error correction	bp1 TM8PWM0	bp1 TM8PWM0
	First Note	Error correction	<u>When T8IGB** is not selected, set as</u> <u>T8IGBTEN=0</u> <u>T8IGBT1-0=00</u>	-
VII-31	TMCKSEL2	Error correction	bp2-0 1: <u>Simple timer</u>	bp2-0 1: <u>Timer A output</u>
VII-34	Third Note	Description addition	-	<u>Set the timer n mode register when the TMnEN flag of the TMnMD1 register is set to "0" to stop counting.</u>
	Fourth Note	Description addition	-	<u>When changing CPU operation mode (NORMAL mode to SLOW mode) at selecting the high oscillation clock ...</u>
VII-35	First Note	Description addition	-	<u>When a data is written to 16-bit timer preset register (TMnPR1, TMnPR2), it is recognized as a 8-bit unit data inside LSI even ...</u>
VII-37	First Key	Description addition	... till the interrupt generation-1)	<u>... till the interrupt generation-1)</u> <u>However, if "00" is specified for the compare register, an interrupt timing is the same as if you set it to "01".</u>
	First Note	Description change	<u>Up to 3 system clock is needed from Timer n interrupt request flag till the next interrupt request flag.</u> During ...	<u>Up to 3 system clock is needed till the next interrupt request flag generated.</u> During ...
	Third Key	Description change	<u>On the interrupt service routine, clear the timer interrupt request flag before the timer is started.</u>	<u>There is a possibility that the timer interrupt request flag has already been set before the timer is started, clear the timer interrupt request flag.</u>
	Second Note	Description change	<u>Key</u> <u>When the TMnEN flag of the TMnMD register is not changed with other bits, the binary counter may count up by switching operation.</u>	<u>Note</u> <u>The TMnEN flag of the TMnMD register is not changed with other bits. There a possibility of malfunctioning.</u>
VII-38	3	Error correction	200 ms	200 <u>μs</u>
	Description	Error correction	(8) Set the <u>TM7IC</u> flag of the TM7ICR register to "1" to enable the interrupt.	(8) Set the <u>TM7IE</u> flag of the TM7ICR register to "1" to enable the interrupt.

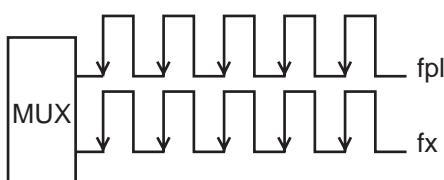
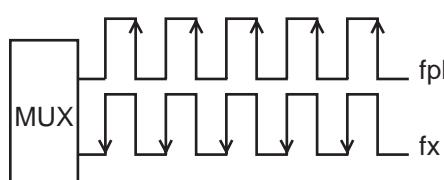
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-40	First Key	Description change	If the binary counter is read out during operation, incorrect data at counting up ...	If the event input (TMnIO input) is selected by count clock source, don't read ...
	Third Note	Error correction	... To prevent this, select the system clock (f_x) for the count clock source once, To prevent this, select the system clock (f_s) for the count clock source once, ...
	Fourth Note	Description change	The binary counter should not be read out after the timer operation is stopped ...	When the event input (TMnIO) input is selected as the count clock source, all pins from TMnIOA to TMnIOC are input mode. Therefore the procedure ...
VII-41	First Note	Description addition	-	Input from TMnIO should be used to a waveform, which has 2 times and over cycles of system clock (f_s). If less than the above waveforms are input, it may not be counted correctly.
VII-46	Second Key	Error correction	... the timer output is "L", when the TMnCL flag of the TMnMD2 register is set to "1".	... the timer output is "L", when the TMnCL flag of the TMnMD1 register is set to "1".
	Second Note	Description change	When the prescaler is operated by the timer pulse output,....	When operating timer pulse output with the divided clock source,....
VII-49	2	Description deletion	Select the TM8IO/TM8O output waveform..	Select the TM8IO output waveform..
VII-51	Figure 7.6.4	Error correction	400 Hz	152.6 Hz
VII-57	Description	Error correction	(8) ... <u>25000/4=6250</u> (0x1869) ...	(8) ... <u>25000/4-1=6249</u> (0x1869) ...
VII-61	First Key	Error correction	... To prevent this, use f_x or synchronous TMnIO input as the count clock...	... To prevent this, use f_s or synchronous TMnIO input as the count clock...
	First Note	Error correction	Capture trigger signals of the 16-bit timers <u>7</u> and <u>8</u> are generated by sampling the rising ...	Capture trigger signals of the 16-bit timers <u>n</u> are generated by sampling the rising ...
VII-63	First Key	Error correction	..., or set the TMnBCR flag of the TM7MD2 to "0".	..., or set the TMnBCR flag of the TMnMD2 to "0".
	First Note	Description addition	-	Capture trigger samples the external interrupt input signal by system clock ...
	Second Note	Description addition	-	When using the external interrupt signal as capture trigger, to make external ...
VII-64	Third Key	Description addition	-	If the capture operation is done during the event count operation, an incomplete ...
VII-67	Description	Error correction	(2) Set the IRQIE flag of ...	(2) Set the IRQ0IE flag of ...
VII-69	2	Error correction	TM7IO, TM8IO. Startup trigger can be ...	TM7IO, TM8IO. Startup trigger can be ...
	13	Error correction	.. Make sure to set the TM7IGBT0, 1 of Make sure to set the T7IGBT0, 1 of ...
	Table 7.10.1	Description deletion	Timer 8	-

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-74	Setup Procedure	Description addition	-	(3) Set the timer output pin <u>TM7MD2(0x03F79)</u> bp4:TM7PWM =1 <u>TM7MD1(0x03F78)</u> bp5:TM7CL =0
	Description	Description addition	-	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to set the output from PA5 pin to PWM output. Set the TM7CL flag of the timer 7 mode register 1 (TM7MD1) to "0" to enable timer output.
VII-75	Setup Procedure	Description addition	-	(11) Enable of external interrupt 0 input <u>IRQCNT (0x03F3D)</u> bp0:P20EN =1
	Description	Description addition	-	(11) Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.
VII-77	12	Error correction	.. Make sure to set the <u>TM7IGBT0</u> , 1 of Make sure to set the <u>T7IGBT0</u> , 1 of ...
	Table 7.11.1	Description deletion	Timer 8	-
VII-79	Figure 7.11.1	Error correction	<p>The diagram shows a sequence of events over time. The Count Clock is a square wave. The TM7EN Flag is asserted at the start. The Compare Register 1 value is shown as N. The IGBT Trigger signal rises at the start and remains high. The Binary Counter starts at 0000 and increments through various states (N-1, N, N+1, N+2, ..., FFFF, FFFF, 0000, 0001, ..., 0000) before returning to 0000. The TM7IO Output (IGBT output) is asserted at points (A), (B), (C), (D), and (E) corresponding to the rising edges of the counter reaching specific values.</p>	<p>The diagram shows a sequence of events over time. The Count Clock is a square wave. The TM7EN Flag is asserted at the start. The Compare Register 1 value is shown as N. The IGBT Trigger signal rises at the start and remains high. The Binary Counter starts at 0000 and increments through various states (N-1, N, N+1, N+2, ..., FFFF, FFFF, 0000, 0001, ..., 0000) before returning to 0000. The TM7IO Output (IGBT output) is asserted at points (A), (B), (C), (D), and (E) corresponding to the rising edges of the counter reaching specific values.</p>
	Figure 7.11.2	Error correction	<p>The diagram shows a sequence of events over time. The Count Clock is a square wave. The TM7EN Flag is asserted at the start. The Compare Register 1 value is shown as 0000. The IGBT Trigger signal rises at the start and remains high. The Binary Counter starts at 0000 and increments through various states (N-1, N, N+1, N+2, ..., FFFF, FFFF, 0000, 0001, ..., 0000) before returning to 0000. The TM7IO Output (IGBT output) is asserted at points (A), (B), (C), (D), and (E) corresponding to the rising edges of the counter reaching specific values.</p>	<p>The diagram shows a sequence of events over time. The Count Clock is a square wave. The TM7EN Flag is asserted at the start. The Compare Register 1 value is shown as 0000. The IGBT Trigger signal rises at the start and remains high. The Binary Counter starts at 0000 and increments through various states (N-1, N, N+1, N+2, ..., FFFF, FFFF, 0000, 0001, ..., 0000) before returning to 0000. The TM7IO Output (IGBT output) is asserted at points (A), (B), (C), (D), and (E) corresponding to the rising edges of the counter reaching specific values.</p>
VII-80	Figure 7.11.3	Error correction	<p>The diagram shows a sequence of events over time. The Count Clock is a square wave. The TM7EN Flag is asserted at the start. The Compare Register 1 value is shown as FFFF. The IGBT Trigger signal rises at the start and remains high. The Binary Counter starts at 0000 and increments through various states (N-1, N, N+1, N+2, ..., FFFF, FFFF, 0000, 0001, ..., 0000) before returning to 0000. The TM7IO Output (IGBT output) is asserted at points (A), (B), (C), (D), and (E) corresponding to the rising edges of the counter reaching specific values.</p>	<p>The diagram shows a sequence of events over time. The Count Clock is a square wave. The TM7EN Flag is asserted at the start. The Compare Register 1 value is shown as FFFF. The IGBT Trigger signal rises at the start and remains high. The Binary Counter starts at 0000 and increments through various states (N-1, N, N+1, N+2, ..., FFFF, FFFF, 0000, 0001, ..., 0000) before returning to 0000. The TM7IO Output (IGBT output) is asserted at points (A), (B), (C), (D), and (E) corresponding to the rising edges of the counter reaching specific values.</p>
	First Note	Description change	For standard IGBT output, set the TM7BCR flag of the TM7MD2 ...	When used for standard IGBT output, set the TM7BCR flag of the TM7MD2 ...

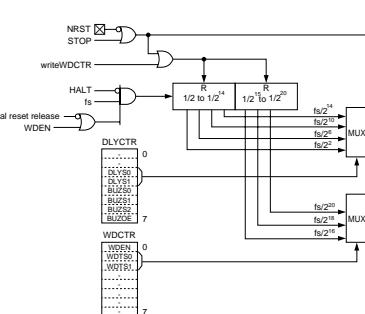
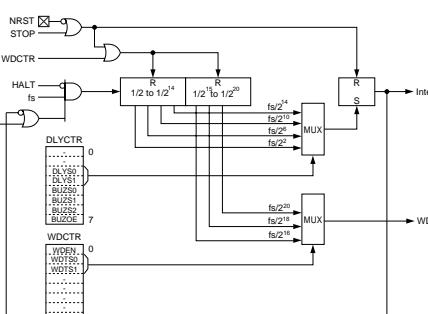
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-81	Setup Procedure	Error correction	(3) ... TM7MD3(0x03F8E) bp2: <u>TM7IGBTEN</u> =1 ...	(3) ... TM7MD3(0x03F8E) bp2: <u>TM7IGBTEN</u> =1 ...
	Setup Procedure	Description addition	(3) ... TM7MD2(0x03F79) bp4:PM7PWM =1	(3) ... TM7MD2(0x03F79) bp4:TM7PWM =1 <u>TM7MD1(0x03F78)</u> bp5:TM7CL =0
	Description	Description addition	(3) ... TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select IGBT output.	(3) ... the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select IGBT output. Set <u>TM7CL flag of the timer7 mode register 1 (TM7MD1)</u> to "0" to enable of timer output.
VII-82	Setup Procedure	Description addition	-	(10) Enable of external interrupt 0 input <u>IRQCNT (0x03F3D)</u> bp0:P20EN =1
	Description	Description addition	-	(10) Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.
	Last line	Description addition	-	<u>TM7BC</u> is counting from 0x0000 by external interrupt 0 input signal. IGBT ...
VII-83	15	Description change	To control the startup by the commands, <u>TM7EN</u> count operation ...	To control the startup by the commands, <u>timer7</u> count operation ...
	17	Error correction	.. Make sure to set the <u>TM7IGBT0</u> , 1 of Make sure to set the <u>T7IGBT0</u> , 1 of ...
VII-84	Figure 7.12.1	Description addition		
VII-85	3	Error correction	(B) After the trigger is input and after 1 count clock <u>falling</u> edge of the next count clock ...	(B) After the trigger is input and after 1 count clock <u>rising</u> edge of the next count clock ...
VII-87	Title	Error correction	(At continuous counting:T7IGBTCNT=1) (Timer 7)	(BC operation when IGBT trigger disable:T7IGBTCNT=1) (Timer 7)
	3	Description addition	-	Setting the T7IGBTCNT flag of the timer 7 mode register 4 (TM7MD4) to "1" can continuous operation of binary counter when IGBT trigger disable.
	Figure 7.12.3	Error correction	TM8IOM(IGBT output) <u>TMDEADPR1</u> <u>TMDEADPR2</u>	TM8IQ(IGBT output) TMDPR1 TMDPR2
		Error correction	Figure 7.12.3 Count Timing of Dead Time High Precision IGBT Output(<u>At continuous counting:T7IGBTCNT=1</u>) (Timer 7)	Figure 7.12.3 Count Timing of Dead Time High Precision IGBT Output(<u>BC operation when IGBT trigger disable:T7IGBTCNT=1</u>) (Timer 7)

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-88	Figure 7.12.4	Description change	dead <u>count binary</u> counter 1,2 dead <u>count</u> preset register 1,2 dead <u>count</u> compare register 1,2	dead <u>time</u> counter 1,2 dead <u>time</u> preset register 1,2 dead <u>time</u> compare register 1,2
	6	Description change	(B) The value of the dead <u>count binary</u> counter 1 and the dead <u>count</u> compare register 1 ...	(B) The value of the dead <u>time</u> counter 1 and the dead <u>time</u> compare register 1 ...
	7	Description change	(C)... Also, the dead <u>count binary</u> counter 2 begins count operation	(C) ... Also, the dead <u>time</u> counter 2 begins count operation
	9	Description change	(D) The value of the dead <u>count binary</u> counter 2 and the dead <u>count</u> compare register 2 ...	(D) The value of the dead <u>time</u> counter 2 and the dead <u>time</u> compare register 2 ...
	11	Error correction	(E) ... because <u>IGBT output</u> is valid.	(E) ... because <u>T7TRGACT flag</u> is valid.
	14	Description change	(F) ...and the dead <u>count</u> preset register 1 and 2.	(F) ...and the dead <u>time</u> preset register 1 and 2.
	15	Description change	(G) ...However, the values same as the dead <u>count</u> preset register 1 and 2 are loaded to the dead <u>count</u> compare register 1 and 2 at the next count clock, as usual.	(G) ...However, the values same as the dead <u>time</u> preset register 1 and 2 are loaded to the dead <u>time</u> compare register 1 and 2 at the next count clock, as usual.
	VII-89	Figure 7.12.5	IGBT waveform	IGBT <u>basic</u> waveform
	Setup Procedure	Error correction	(3)... bp1:0: <u>TM7IGBT1-0 =01</u>	(3)... bp1:0: <u>T7IGBT1-0 =01</u>
	Description	Error correction	(4)Set the T7IGBTTR flag of the TM7MD3 register to "1" to <u>select the rising edge as the interrupt generation valid edge</u> .	(4)Set the T7IGBTTR flag of the TM7MD3 register to "1" to <u>set IGBT trigger level to "H"</u> .
	Description	Error correction	(5)Set the T7IGBTDT flag of the timer 7 mode register 3 (TM7MD3) to "0" to select the falling standard as the dead time <u>edge</u> .	(5)Set the T7IGBTDT flag of the timer 7 mode register 3 (TM7MD3) to "0" to select the falling standard as the dead time <u>insert timing</u> .
	VII-90	Setup Procedure	Description addition	- <u>(6)Enable of external interrupt 0 input IRQCNT (0x03F3D) bp0:P20EN =1</u>
	Description	Description addition	-	<u>(6)Set P20EN flag of the IRQCNT register to "1" to enable of external interrupt 0 input.</u>
	Setup Procedure	Error correction	(8) ... bp1: <u>IRQ1IE =1</u>	(8) ... bp1: <u>IRQ0IE =1</u>
	Setup Procedure	Description Deletion	(10) ... TM7PR1(0x03F75, 0x03F74) =0x9C3F bp2:T7ICEN =1	(10) ... TM7PR1(0x03F75, 0x03F74) =0x9C3F
	Description (12)	Error correction	<u>TM7DEADPR1</u> <u>TM7DEADPR2</u>	<u>TM7DPR1</u> <u>TM7DPR2</u>

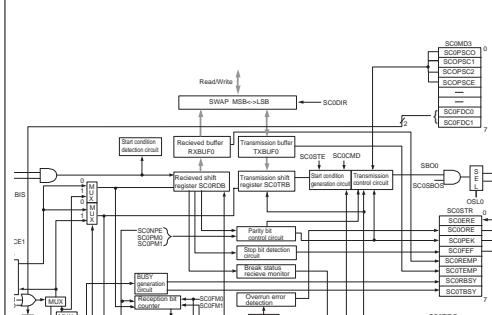
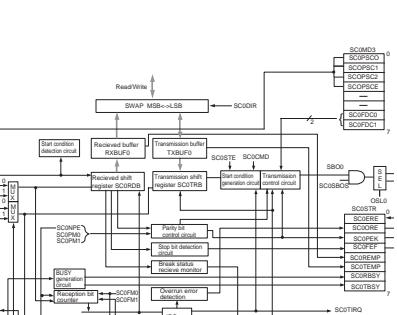
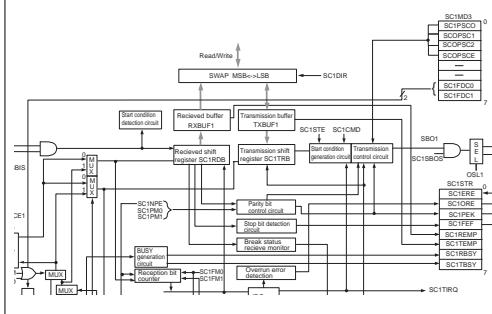
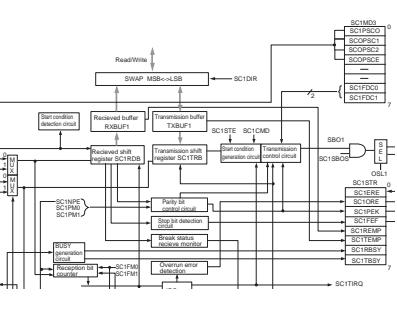
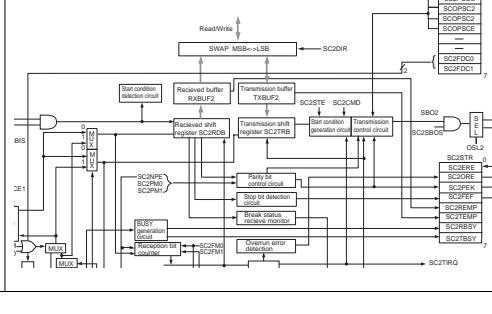
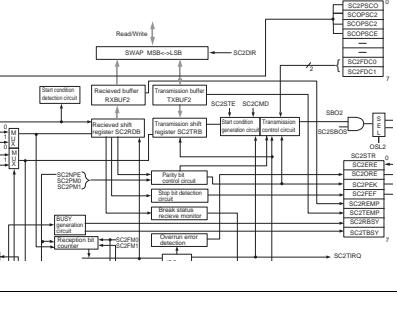
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VII-90	Setup Procedure	Description addition	(13) ... TM8MD3 (0x03F8F) bp2:TM8SEL =1	(13) ... TM8MD4 (0x03F6F) bp2:TM8SEL =1 <u>TM7MD1 (0x03F78)</u> bp5:TM7CL =0
	Description	Description addition	(13) ...Set TM8SEL_A flag of the timer 8 mode register 4 (TM8MD4) to "1" to select the timer 7 IGBT output.	(13) ...Set TM8SEL_A flag of the timer 8 mode register 4 (TM8MD4) to "1" to select the timer 7 IGBT output. <u>Set TM7CL flag of the timer 7 mode register 1 (TM7MD1) to "0" to enable the timer output.</u>
VII-91	Description	Error correction	(15) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7. After "H" is input to <u>P54</u> pin, IGBT is output from <u>P14</u> , <u>P15</u> .	(15) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7. After "H" is input to <u>P20</u> pin, IGBT is output from <u>PA5</u> , <u>PA6</u> .
VII-92	Table 7.13.1	Description change	Interrupt source <u>TM8IRQ1</u> , <u>TM8IRQ2</u>	Interrupt source <u>TM8IRQ</u> , <u>TM8OC2IRQ</u>
		Description addition	Clock source -	Clock source <u>TimerA output</u> <u>TimerA output/2</u> <u>TimerA output/4</u> <u>TimerA output/16</u>
VII-93	First Key	Description change	*At cascade connection, timer 8 interrupt factor is only counter-clear.	At cascade connection, timer 8 interrupt factor is only counter-clear.
	First Note	Error correction	... <u>Timer 7 interrupt should be disabled as the interrupt request of timer 7 is generated.</u>	... <u>The interrupt request of timer 7 is not generated. But timer 7 interrupt should be disabled.</u>
	Second Note	Error correction	... the correct data <u>may not be</u> loaded.	... the correct data <u>is not</u> loaded. <u>To prevent this, it puts into the count stop condition and rewrite the preset register once.</u>
	Second Key	Description addition	-	<u>Stop the timer in order to read out the correct value of the timer in cascade connection.</u>
VII-94	Setup Procedure	Error correction	(3) TM7MD2 (0x03F79) bp2 : T7ICEN =0 <u>TM7MD3 (0x03F6C)</u> bp1-0 : T7OUT1-0 =00	(3) TM7MD2 (0x03F79) bp2 : T7ICEN =0 <u>bp4 : TM7PWM =0</u>
	Description	Error correction	(3) Set the T7ICEN flag of the TM7MD2, 3 register to "0" to select the normal timer operation.	(3) Set the T7ICEN flag <u>and</u> TM7PWM flag of the TM7MD2 register to "0" to select the normal timer operation.
VII-95	Description	Error correction	(9) Set the interrupt level by the <u>TM8LS1</u> to 0 flag ...	(9) Set the interrupt level by the <u>TM8LV1</u> to 0 flag ...
VII-96	Setup Procedure	Error correction	(3) ... <u>TM8MD1(0x03F88)</u> bp6:TM8CAS=	(3) ... <u>TM8MD3(0x03F8F)</u> bp0:TM8CAS=
	Description	Error correction	(3) Set the TM8CAS flag of the <u>TM8MD1</u> register ...	(3) Set the TM8CAS flag of the <u>TM8MD3</u> register ...
VIII-4	3	Description change	Both timers are operated by the enable signal of the <u>TM6BEN</u> .	Both timers are operated by the enable signal of the <u>timer 6 enable register (TM6BEN)</u> .

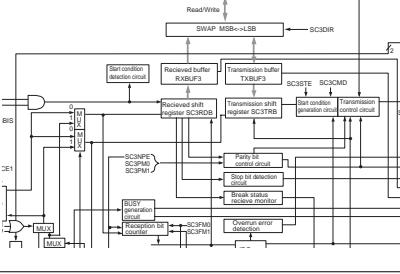
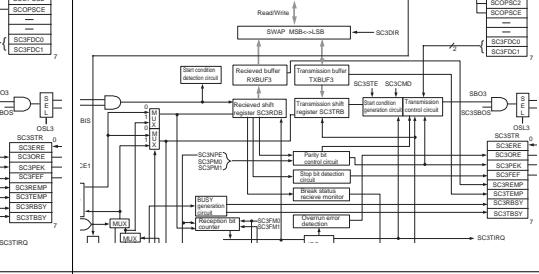
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
VIII-6	TM6BEN	Error correction	bp2 Flag : <u>z</u> At reset : <u>z</u> Access : <u>z</u>	bp2 Flag : <u>Reserved</u> At reset : <u>0</u> Access : <u>R/W</u>
VIII-11	First Key	Description addition	... = (count till the interrupt request - 1)	... = (count till the interrupt request - 1) <u>However, the interrupt generation cycle when the compare register is set to "00" is the same as it is set to "01".</u>
	First Note	Description addition	... when the binary counter is read on the operation, uncertain when the binary counter is read on the operation <u>while CPU is operationg in the NORMAL mode</u> , uncertain ...
	Second Note	Description addition	If fx is used as the clock source, the binary ...	If fx is used as the clock source <u>while CPU is operationg in the NORMAL mode</u> , the binary ...
	Fourth Note	Description addition	When the fx is selected for the count clock source and the value of the compare register is rewritten, the operation ...	When the fx is selected for the count clock source and the value of the compare register is rewritten <u>while CPU is operationg in the NORMAL mode</u> , the operation ...
VIII-13	Setup Procedure	Description addition	-	(1) Stop the counter <u>TM6BEN(0x03F6C)</u> <u>bp0 : TM6EN =0</u>
	Description	Description addition	-	(1) Set the TM6EN flag of the TM6BEN register to "0" to stop the timer 6 counting.
VIII-15	Figure 8.4.1	Error correction		
VIII-16	Setup Procedure	Description addition	-	(1) Stop the counter <u>TM6BEN(0x03F6C)</u> <u>bp1 : TBEN =0</u>
	Description	Description addition	-	(1) Set the TBEN flag of the TM6BEN register to "0" to stop the time base timer counting.
IX-5	bp7	Description change	0:TM0IOC 1:RMOUTC	0:Timer 0 output (TM0IOC) 1:Remote control carrier output (RMOUTC)
	bp6	Description change	0:TM0IOB 1:RMOUTB	0:Timer 0 output (TM0IOB) 1:Remote control carrier output (RMOUTB)
	bp4	Description change	0:TM0IOA 1:RMOUTA	0:Timer 0 output (TM0IOA) 1:Remote control carrier output (RMOUTA)
	bp2-1	Error correction	1- : <u>Timer output</u>	1- : <u>1/1 duty</u>
	bp0	Error correction	Remote control carrier base timer selection	Remote control carrier <u>output</u> base timer selection

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IX-6	First Note	Description addition	-	<u>When set RMOEN flag to "1", don't change the flags other than RMOEN flag.</u>
	Key	Description addition	-	<u>Do not change RMDTY 1.0 flag, RMBTMS flag and TMORM flag with RMOEN flag ...</u>
	Second Note	Description addition	-	<u>The cycle of the remote control carrier output base timer is set to the system clock ...</u>
	Third Note	Description addition	-	<u>Always set "0" to the bp denoted by *.</u>
IX-7	4	Error correction	Duty ratio is selectable from 1/2, 1/3, <u>Timer output</u> . Remote ...	Duty ratio is selectable from <u>1/1, 1/2, 1/3</u> . Remote ...
	Figure 9.3.1	Error correction	<p>Timer base cycle (36.7 kHz) RMOUT (1/2 duty) RMOUT (1/3 duty)</p>	<p>Remote control carrier output base timer cycle RMOUT (1/1 duty) RMOUT (1/2 duty)</p>
	Figure 9.3.2	Error correction	<p>Timer base cycle (36.7 kHz) RMOEN (output ON, output OFF) RMOUT (1/3 duty)</p>	<p>RMOEN (output ON, output OFF) Remote control carrier output base timer (36.7 kHz) RMOUT (1/3 duty)</p>
IX-8	First Key	Description deletion	<u>When RMOEN flag is changed, the base cycle and the duty selection timer ...</u>	-
	First Note	Description deletion	<u>Set the timer output over 1 cycle of the system clock. The remote control carrier output ...</u>	-
	Square	Description addition	Remote Control carrier Output Functions Setup	Remote Control carrier Output Functions Setup (<u>Timer0, Timer3</u>)
	2	Description addition	... RMOUT pin with the timer 0 are shown below RMOUT pin with the timer 0 used for the <u>remote control carrier output base timer</u> are shown below ...
	Figure 9.3.3	Error correction	<p>Timer 0 base cycle (36.7 kHz) RMOUT output (1/3 duty)</p>	<p>Remote control carrier output base timer cycle (36.7 kHz) RMOUT output (1/3 duty)</p>
	Description	Description addition	(6) Set the TM0PWM flag of the TM0MD register ...	(6) Set the <u>TM0PWM and TM0MOD</u> flags of the TM0MD register ...

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
IX-9	Setup Procedure	Error correction	(10) <u>Start the timer operation ...</u> (11) <u>Enable the remote control ...</u>	(10) <u>Enable the remote control ...</u> (11) <u>Start the timer operation ...</u>
	Description	Error correction	(10) <u>Set the TM0EN flag of the TM0MD ...</u> (11) <u>Set the RMOEN flag of the RMCTR ...</u>	(10) <u>Set the RMOEN flag of the RMCTR ...</u> (11) <u>Set the TM0EN flag of the TM0MD ...</u>
	First Note	Description addition	-	<u>When enabled the remote control carrier output during timer operation, the duty of remote control carrier output ...</u>
	Second Note	Description addition	-	<u>When stop the remote control carrier output, execute the remote control carrier output stop setting (RMOEN=0). And after ...</u>
X-2	Table 10.1.1	Description change	2^{16} of system clock 2^{18} of system clock 2^{20} of system clock	2^{16} of system clock <u>cycle</u> 2^{18} of system clock <u>cycle</u> 2^{20} of system clock <u>cycle</u>
X-3	Figure 10.1.1	Error correction		
X-5	WDCTR	Description change	bp5-3 <u>Set always to "0"</u>	Description <u>Always set to "0" *</u>
	WDCTR	Error correction	bp2-1 Watchdog runaway detect cycles <u>setup</u>	bp2-1 Watchdog runaway detect cycles <u>selection</u>
	First Note	Description addition	-	<u>Once WDEN flag is set to "1", WDEN flag can't be cleared to "0". But when ...</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
X-6	DLYCTR	Error correction	bp3-2 00 : <u>fs/2¹⁴</u> 01 : <u>fs/2¹⁰</u> 10 : <u>fs/2⁶ * 1</u> 11 : <u>fs/2² * 1</u>	bp3-2 00 : <u>2^{14} of system clock cycle</u> 01 : <u>2^{10} of system clock cycle</u> 10 : <u>2^6 of system clock cycle</u> 11 : <u>2^2 of system clock cycle</u>
	2	Error correction	*1: <u>Do not use at high-speed operation (NORMAL mode). Use at slow-speed operation (SLOW mode).</u>	-
	First Note	Description addition	-	<u>We recommend selecting the oscillation stabilization time of high-speed and slow-speed oscillation by set of DLYS1-0 ...</u>
	First Key	Description addition	-	<u>About buzzer function refer to [Chapter 11 Buzzer].</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
X-7	5	Description addition	As a result of the generation twice, consecutively, of the watchdog interrupt , ...	As a result of the generation twice, consecutively, of the watchdog interrupt (<u>WDIRQ</u>), ...
	First Note	Description addition	However, the watchdog timer stops during the HALT mode.	However, the watchdog timer stops during <u>the Stop mode and the HALT mode</u> .
	13	Error correction	... the watchdog timer detects errors when, <u>1. The watchdog timer overflows.</u> When the watchdog timer detects the watchdog timer detects errors when, The watchdog timer overflows. When the watchdog timer detects ...
X-8	2	Error correction	The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR). <u>The watchdog timer can be cleared</u> regardless of the writing data ...	The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR) regardless of the writing data ...
	9	Error correction	The system clock is decided by the CPU mode control register (CPUM).	The system clock is decided by <u>setting of</u> the CPU mode control register (CPUM).
	Table 10.3.1	Description change	<u>1. In NORMAL, IDLE, SLOW mode, the...</u> ... <u>7. The counting of ... is released.</u>	<u>Table 10.3.1</u>
	First Note	Description change	<u>Generally,</u> in the system use STOP mode is used or not in the execution of...	<u>Note</u> In the system use STOP mode is used or not in the execution of...
X-9	1, Description	Error correction	system clock	system clock <u>cycle</u>
	First Note	Error correction	The operation, just before the watchdog interrupt may be executed wrongly. <u>Therefore, if the watchdog interrupt is generated, initialize the system.</u>	The operation, just before the watchdog interrupt may be executed wrongly. <u>In that case, proper operation is not guaranteed.</u>
XI-3	Figure 11.1.1	Error correction		
XI-6	First Note	Description addition	-	<u>The BUZOE flag and BUZS2 to 0 flags should not be set at the same time.</u>
	First Key	Description addition	-	<u>DLYS 1 to 0 flag is setting flag of watchdog timer function. Refer to [Chapter 10 Watchdog Timer] for watchdog timer function.</u>
XI-7	First Key	Error correction	At the instant that the BUZOE flag is set to "0", the output of the buzzer becomes "Low".	At the instant that the BUZOE flag is set to "0", the output of the buzzer (<u>BUZZER</u> and <u>NBUZZER</u>) becomes "Low".

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XI-8	First Note	Error correction	... the buzzer output is switched <u>enable</u> from <u>disable</u> , the buzzer dividing counter is not cleared unless more than 1 clock of the low oscillation clock is secured.	... the buzzer output is switched <u>disable</u> from <u>enable</u> , the buzzer dividing counter is not cleared unless more than 1 clock of the low oscillation clock is secured. <u>When enable buzzer output again, enable buzzer output after waiting one clock of low-speed oscillation clock.</u>
XII-4	Table 12.1.3	Description deletion	<u>Communication style to Maximum transfer rate</u>	-
XII-6	Table 12.1.5	Error correction	Communication format Standard mode (100 Kbit/s) High-speed mode (400 Kbit/s)	Communication format Standard mode (100 bit/s) High-speed mode (400 bit/s)
XII-7	Figure: 12.1.1	Error correction		
XII-8	Figure: 12.1.2	Error correction		
XII-9	Figure: 12.1.3	Error correction		

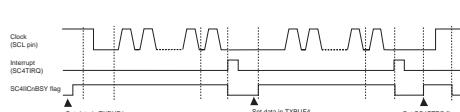
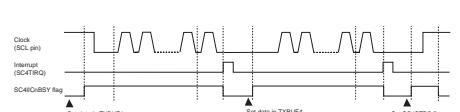
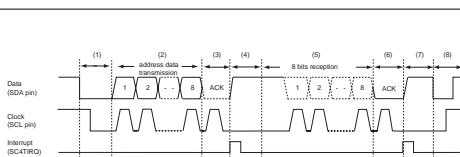
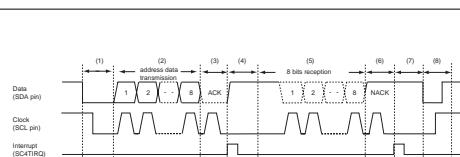
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-10	Figure: 12.1.4	Error correction		
XII-13,14, 15,16	PERIICR	Error correction	<u>0x03FFF</u>	<u>0x03FFE</u>
XII-16	First Note	Description addition	-	If changing the setting value of mode registers, execute rewriting after setting the serial forced reset...
	Second Note	Description addition	-	If changing the setting value of mode register (except for SC4STE flag, SC4STPC flag, IIC4REX flag and SC4ACK0 flag)...
XII-25	SCnMD1	Error correction	bp6 0 : Port 1 : Transfer clock I/O	bp6 0 : Port 1 : Serial clock I/O
		Error correction	bp5 Serial input control selection 0 : "1" input 1 : Serial input	bp5 Serial data input control selection 0 : "1" input 1 : Serial data input
XII-26	First Note	Description addition	-	If selecting the external clock (clock slave), set the internal clock that has the same or lower clock cycle to the external clock.
	First Key	Description addition	-	When set both bp5 of SCnSBIS flag and bp4 of SCnSBOS flag to "0", the serial forced reset is set and serial ...
	Second Note	Description addition	-	If setting the communication state of this serial interface to "UART", set the mode register (SCnMD1) to the serial ...
	First Note	Description addition	-	If changing the setting value of mode registers, execute rewriting after setting the serial forced reset...
XII-28	SCnMD3	Error correction	bp7-6 11 : Reserved	bp7-6 11 : Prohibited
	First Note	Description addition	-	If selecting the external clock (clock slave), set the internal clock that has the same or lower clock cycle to the external clock.
XII-32	First Note	Description addition	-	If changing the setting value of mode register (except for SC4STE flag, SC4STPC flag, IIC4REX flag and SC4ACK0 flag)...

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-33	SC4MD2	Error correction	bp7-6 ... <u>10 : Fix at "0" (Low) output</u> <u>01 : Final data hold</u> <u>11 : Reserved</u>	bp7-6 ... <u>01 : Final data hold</u> <u>10 : Fix at "0" (Low) output</u> <u>11 : Prohibited</u>
XII-34	SC4MD3	Description change	bp7-6 Flag, Description <u>bp7 SC4SMB, SM-Bus support selection</u> <u>bp6 Reserved, Always set "0"</u>	bp7-6 Flag, Description <u>bp7-6 Reserved, Always set to "0" *</u>
	SC4MD3	Error correction	bp1 Description ACK bit enable 0: <u>Enable</u> 1: <u>Disable</u>	bp1 Description ACK bit enable 0: <u>Disable</u> 1: <u>Enable</u>
	Second Note	Description change	<u>Set the data to the serial interface 4 mode register 3 by Mov instruction, not by BSET/BCLR control. If data is set by ...</u>	<u>Set the setting data to the serial interface 4 mode register 3 by Mov instruction once, not by BSET/BCLR control. After read ...</u>
	Third Note	Description change	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XII-35	1	Error correction	Serial interface 4 has <u>10</u> bits of the address set register.	Serial interface 4 has <u>7</u> bits of the address set register.
	Square	Description deletion	<u>- Reserved Register (Reserved: 0x03FB5)</u>	-
	First Note	Description addition	-	<u>Do not word access to SC4AD0 register</u>
XII-37	First Note	Description addition	-	<u>SC4ABT LST can not write "1"; can write "0" only.</u>
XII-41	SC5STR	Error correction	bp0 At reset <u>Q</u> Access <u>R</u>	bp0 At reset <u>-</u> Access <u>-</u>
XII-42	First Second Note	Description change	-	First and second Note moved from XII-43
XII-43	Square	Error correction	Transmission Data Buffer ... Whether during data loading period or not is determined by monitoring the transmission buffer empty flag SCnTEMP of <u>SCnsSTR...</u>	Transmission Data Buffer ... Whether during data loading period or not is determined by monitoring the transmission buffer empty flag SCnTEMP of <u>SCnSTR...</u>
XII-45	2 from the bottom	Error correction	<u>In master communication, communication blanks, from SCn(T)IRQ generation ...</u>	Communication blanks, from SCn(T)IRQ generation ...
XII-49	10	Error correction	At emergency reset, the status register (the SCnBRKF flag of the SCnMD2 register, all flags of the <u>SCnSTR register</u>) is initialized to the reset value,	At emergency reset, the status register (the SCnBRKF flag of the SCnMD2 register, <u>all flags of the SC0STR, SC1STR and SC2STR registers....</u>
	Table 12.3.5	Error correction	<u>Reserved</u>	<u>Prohibited</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-55	5	Error correction	<u>When transmission and reception are executed with the start condition "enable". "the start condition enable" should be ...</u>	<u>When transmission and reception are executed with the start condition "enable". "the start condition enable" should be</u>
	First Note	Description change	When <u>executing</u> transmission and reception at the same time, <u>select "start condition disabled"</u> to prevent malfunction.	When operating transmission and reception at the same time, <u>select "start condition disable"</u> ; otherwise, it may cause improper operations.
XII-56	4, 8 Figure 12.3.16	Error correction	<u>NORMAL</u> mode	<u>CPU operation</u> mode
XII-57	Table	Error correction	<u>OSL0 : 1, 0</u>	<u>OSL0 : 0→1, 1→0</u>
XII-58	Table	Error correction	<u>OSL1 : 1, 0</u>	<u>OSL1 : 0→1, 1→0</u>
XII-59	Table	Error correction	<u>OSL2 : 1, 0</u>	<u>OSL2 : 0→1, 1→0</u>
XII-60	Table	Error correction	<u>OSL3 : 1, 0</u>	<u>OSL3 : 0→1, 1→0</u>
XII-61	Table	Error correction	<u>OSL4 : 1, 0</u>	<u>OSL4 : 0→1, 1→0</u>
XII-62	Description	Error correction	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select " <u>prescaler operation</u> ".	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select " <u>prescaler count enable</u> ".
XII-63	Setup Procedure	Error correction	(8) Set the interrupt level SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10	(8) Set the interrupt level <u>PSW</u> <u>bp6 :MIE =0</u> SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10
	Description	Error correction	(8) Set the interrupt ...	(8) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt.</u> Set the interrupt ...
	Setup Procedure	Error correction	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Error correction	(9) ... prior to enabling the interrupt.	(9) ... prior to enabling the interrupt. <u>Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.</u>
	1	Error correction	*Each setup in (1) to (3), (6) to (7) and (8) to (9) can be set at the same time.	*Each setup in (1) to (3) and (6) to (7) can be set at the same time.
XII-64	First Key	Error correction	... <u>SC0SBIS</u> of the <u>SC0MD1</u> register must be set to "1" to select "serial data input"....	... <u>SCnSBIS</u> of the <u>SCnMD1</u> register must be set to "1" to select "serial data input"....
	Second Note	Description change	<u>Key</u> The transfer rate must be under 5.0 MHz ...	<u>Note</u> The transfer rate must be under 5.0 MHz ...

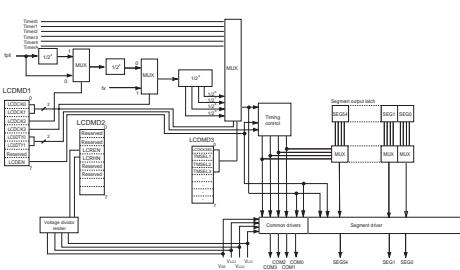
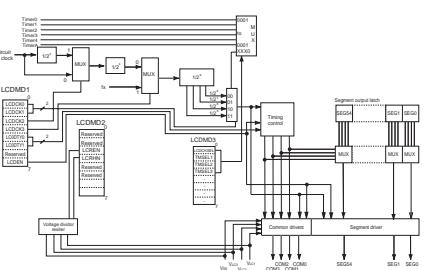
Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-65	Description	Error correction	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select " <u>prescaler operation</u> ".	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select " <u>prescaler count enable</u> ".
	Setup Procedure	Error correction	(5) Control the pin direction [set the pin corresponding to each serial] P0DIR (0x03F30) <u>bp2-1 :P0DIR2-1 =11</u>	(5) Control the pin direction [set the pin corresponding to each serial] P0DIR (0x03F30) <u>bp2 :P0DIR2 =0</u> <u>bp0 :P0DIR0 =0</u>
	Description	Error correction	(5) Set the P0DIR2 -1 flags of the port 0 pin direction control register (P0DIR) <u>to "11" to set p01 and p02 to output mode and p00 to input mode.</u>	(5) Set the P0DIR2 flag of the port 0 pin direction control register (P0DIR) <u>to "0" and set the P0DIR0 flag to "0" to set P00 and P02 to input mode.</u>
XII-66	Description	Error correction	(7) ... for serial 0, 1 and 2. <u>Set the SC1SBOS of the SC1MD1 register to "0" and the SC1SBIS and SC1SBTS flags to "1" to set ...</u>	(7) ... for serial 0, 1 and 2. <u>Set the SC1SBIS and SC1SBTS flags of the SC1MD1 register to "1" to set the SBI1 pin to the ...</u>
	Setup Procedure	Error correction	(8) Set the interrupt level SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10	(8) Set the interrupt level <u>PSW</u> <u>bp6 :MIE =0</u> SC1TICR(0x03FF8) bp7-6 :SC1LV1-0 =10
	Description	Error correction	(8) Set the interrupt ...	(8) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the interrupt ...</u>
	Setup Procedure	Error correction	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1	(9) Enable the interrupt SC1TICR (0x03FF8) bp1 :SC1TIE =1 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Error correction	(9) ... prior to enabling the interrupt.	(9) ... prior to enabling the interrupt. <u>Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.</u>
XII-67	1	Error correction	*Each setup (1) to (3) and (6) to (8) can be set at the same time.	*Each setup (1) to (3) and (6) to (7) can be set at the same time.
	First Note	Description deletion	<u>Set the SCnSBIS of the SCnMD1 register to "0" and select a port in order to operate ...</u>	-
	Second Note	Description change	<u>Key</u> The transfer rate must be under 5.0 MHz ...	<u>Note</u> The transfer rate must be under 5.0 MHz ...
	Third Note	Description addition	-	<u>Insert three NOP instructions right after the instruction of the transition to HALT, STOP mode.</u>
XII-68	First Note	Description addition	-	<u>If setting the communication state of this serial interface to "UART", set the mode ...</u>
XII-71	8	Description change	Set the next data to TXBUFn before the transmission complete interrupt SCnTIRQ is generated <u>since the previous data setup</u>	Set the next data to TXBUFn before the transmission complete interrupt SCnTIRQ is generated <u>since data is setup to transmission shift register</u>
XII-73	Figure 12.4.4	Description addition	Figure:12.4.4 Setup Value of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.4 Setup Value of UART Serial Interface Transfer Speed (decimal) <u>when setting devide-by-8 clock source</u>
XII-74	Figure 12.4.5	Description addition	Figure:12.4.5 Setup Value of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.5 Setup Value of UART Serial Interface Transfer Speed (decimal) <u>when setting devide-by-8 clock source</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-75	Figure 12.4.6	Description addition	Figure:12.4.6 Setup Value of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.6 Setup Value of UART Serial Interface Transfer Speed (decimal) <u>when setting devide-by-16 clock source</u>
XII-76	Figure 12.4.7	Description addition	Figure:12.4.7 Setup Value of UART Serial Interface Transfer Speed (decimal)	Figure:12.4.7 Setup Value of UART Serial Interface Transfer Speed (decimal) <u>when setting devide-by-16 clock source</u>
XII-80	Table	Error correction	<u>OSL0</u>	<u>OSL0</u>
XII-81	Table	Error correction	<u>OSL1</u>	<u>OSL1</u>
XII-82	Table	Error correction	<u>OSL2</u>	<u>OSL2</u>
XII-83	Table	Error correction	<u>OSL3</u>	<u>OSL3</u>
XII-84,85		Error correction	(1), (2), (3), (4), (5), (6), (7)	(1)→(7), (2)→(1), (3)→(2), (4)→(3), (5)→(4), (6)→(5), (7)→(6)
XII-85	Setup Procedure	Error correction	(8) Enable the interrupt IRQEPEN(0x03F4E) bp1 :IRQEPEN1 =1 PERIICR(0x03FFE) bp1 :PERIIE =1 SC1TICR (0x03FF5) bp1 :SC1TIE =1	(8) Enable the interrupt <u>PSW</u> <u>bp6 :MIE =0</u> IRQEPEN(0x03F4E) bp1 :IRQEPEN1 =1 PERIICR(0x03FFE) bp1 :PERIIE =1 SC1TICR (0x03FF8) bp1 :SC1TIE =1 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Error correction	(8) Set the IRQEPEN1 flag of ... clear the request flag.	(8) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt. Set the IRQEPEN1 flag of ... clear the request flag. Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.</u>
XII-86	Second Note	Description addition	-	When communication format of this serial interface set to "UART", set the Serial ...
XII-87	First Note	Description change	<u>Key</u> Make sure to set the SC4SBIS flag ...	<u>Note</u> Make sure to set the SC4SBIS flag ...
	Second Note	Description addition	-	<u>Nch open-drain should be used for pin format because the bus is switched ...</u>
XII-92	5	Description change	The stop condition should be requested only when this IIC occupies the bus as the master.	The stop condition should be requested only when this IIC occupies the bus as the master <u>and communication is completed</u> .
	First Note	Error correction	-	<u>Do not write to transmission buffer (TXBUF4) until bus busy flag BUSBSY (SCSTR1:bp3) is set to "0" after....</u>
XII-93	5	Description change	When it is detected that the data line (SDA4 pin) changes while the clock line (SCL4 pin) is "H" ...	When it is detected that the data line (SDA4 pin) changes while the clock line (SCL4 pin) is "H" <u>after start condition is detected....</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-94	7	Error correction	... transmission starts with the clock transmitted from the master. In slave reception, transmission starts with the clock transmitted from the master. <u>It is not necessary to set data to TXBUF4 register because bus line is automatically opened when NACK is received.</u> In slave reception, ...
	12	Error correction	... the address compare flag SC4ADD_ACC of SC4STR1 is set to "1" and ACK is automatically transmitted.	... the address compare flag SC4ADD_ACC flag of SC4STR1 register is set to "1" and ACK is automatically transmitted.
	8 from the bottom	Description change	... and the ACK bit is stored in the <u>SC4ACK0</u> of the SC4MD3 register....	... and the ACK bit is stored in the <u>SC4ACK0</u> flag of the SC4MD3 register ...
	3 from the bottom	Description change	... At slave operation, the transmission is finished by automatically releasing the data line (SDA4).	... At slave operation, <u>it is not necessary to set data to TXBUF4 register because the transmission is finished by automatically releasing the data line (SDA4).</u>
XII-95	4	Error correction	... ACK bit level for output can be set with <u>SC3ACK0</u> the <u>SC3MD3</u> register.	... ACK bit level for output can be set with <u>SC4ACK0</u> flag the <u>SC4MD3</u> register.
	7	Error correction	During master <u>communication, when competing with other master, data is compared; If the communication is ...</u>	During master <u>transmission, data bus(SDA) compares output data from this circuit with every 1-bit to detect the competition ...</u>
	2 from the bottom	Description addition	... timing of flag set/clear.	... timing of flag set/clear. <u>The time is required between the data is set to TXBUF4 register and the SC4IICBSY flag is set (the communication is started) at most the internal transfer clock 1 cycle.</u>
XII-99	Figure 12.5.11	Error correction		
	3	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the data is set to TXBUF4.
	9	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.
	15	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the SC4STPC flag is set.
XII-100	Figure 12.5.12	Error correction		
	8	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.
	11	Error correction	(6) ACK bit output	(6) NACK bit output
	14	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 2 clocks of the clock source when the SC4STPC flag is set.

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-101	7, 13	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.
XII-102	7	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the data is set to TXBUF4.
XII-103, 104	7, 13	Error correction	-	- The SC4IICBSY flag is set to "1" after the elapse of 1 to 10 clocks of the clock source when the dummy data is set to TXBUF4.
XII-105	Table	Error correction	Pin setup (flag setup) SC4SEL register ... <u>SC4SEL</u>	Pin setup (flag setup) SC4SEL register ... <u>OSL4</u>
XII-106	Table 12.5.6	Error correction	Pin : A <u>stream</u> (port 6)	Pin : A <u>system</u> (port 6)
	Table 12.5.6	Error correction	Master/Slave : Master	Master/Slave : Master (<u>Multimaster</u>)
	Description	Error correction	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select <u>prescaler operation</u> .	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select <u>"prescaler count enable"</u> .
	Description	Error correction	(3) Set the OSL4 flag of SC4SEL register to "0" to select A <u>stream</u> (port 6) for the I/O pin.	(3) Set the OSL4 flag of SC4SEL register to "0" to select A <u>system</u> (port 6) for the I/O pin.
XII-107	Setup Procedure, Description	Description change	(6), (7), (8), (9)	(6)
XII-108	Setup Procedure	Error correction	(10) Set the interrupt level SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10	(10) Set the interrupt level <u>PSW</u> <u>bp6 :MIE =0</u> SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10
	Description	Error correction	(10) Set the interrupt ...	(10) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt.</u> Set the interrupt ...
	Setup Procedure	Error correction	(11) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0	(11) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Description change	(11) ... enabling interrupts. [Chapter ...]	(11) ... enabling interrupts. <u>Set the MIE flag of the PSW to "1" to enable the all maskable interrupt.</u> [Chapter...]
XII-109	2	Error correction	*(1) and (2) can be set at once. *(6) to (10) can be set at once. * <u>Each setup in (11) and (12) can be set at once.</u> *(13) to (14) can be set at once.	*(1) and (2) can be set at once. * <u>Each setup in (8) and (9) can be set at once.</u> * <u>(10) to (11) can be set at once.</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XII-110	Table 12.5.7	Error correction	Pin : A <u>stream</u> (port 6)	Pin : A <u>system</u> (port 6)
	Table 12.5.7	Error correction	Master/Slave : Master	Master/Slave : Master (<u>Multimaster</u>)
	Description	Error correction	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select " <u>prescaler operation</u> ".	(1) Set the SC4PSCE flag of the SC4MD2 register to "1" to select " <u>prescaler count enable</u> ".
	Description	Error correction	(3) Set the OSL4 flag of SC4SEL register to "0" to select A <u>stream</u> (port 6) for the I/O pin.	(3) Set the OSL4 flag of SC4SEL register to "0" to select A <u>system</u> (port 6) for the I/O pin.
XII-111	Setup Procedure, Description	Description change	(6), (7), (8)	(6)
	Description	Error correction	(6) Set the SC4ACKS flag of the serial 4 mode register 3 (SC4MD3) to "1" to select "ACK bit enabled". ACK bit is received at transmission and the level setting of ACK bit with the <u>SC4ACKS flag is not needed</u> .	(6) Set the SC4ACKS flag of the serial 4 mode register 3 (SC4MD3) to "1" to select "ACK bit enabled". ACK bit is received at transmission and the level setting of ACK bit with the <u>SC4ACKO flag is not required</u> ...
	Setup Procedure	Error correction	(11) Set the interrupt level SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10	(11) Set the interrupt level <u>PSW</u> <u>bp6 :MIE =0</u> SC4ICR(0x03FFC) bp7-6 :SC4LV1-0 =10
	Description	Error correction	(11) Set the interrupt level by the <u>SL4LV1-0</u> flags ...	(11) <u>Set the MIE flag of the PSW to "0" to prohibit the all maskable interrupt</u> . Set the interrupt level by the <u>SC4LV1-0</u> flags ...
XII-112	Setup Procedure	Error correction	(12) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0	(12) Enable the interrupt bp1 :PERIIE =1 bp0 :PERIIR =0 <u>PSW</u> <u>bp6 :MIE =1</u>
	Description	Error correction	(12) ... Control Register Setup]	(12) ... Control Register Setup] <u>Set the MIE flag of the PSW to "1" to enable the all maskable interrupt</u> . [Chapter]
	Description	Error correction	(14) Communication complete interrupt (SC4TIRQ) is generated ...	(14) Communication complete interrupt (<u>SC4IRQ</u>) is generated ...
	1	Description addition	-	*(1) and (2) can be set at once. *Each setting in (9) to (10) can be set at once. *(10) to (11) can be set at once.
	First Note	Description addition	-	<u>Set each flag in accordance with the order of the setup procedure</u> . Activate the ...
XII-116	Table 12.6.2	Error correction	Item Clock pin (<u>SCI</u>)	Item Clock pin (<u>SCL</u>)
	Description	Error correction	(3) Set the <u>SC5SL</u> flag of the <u>OSL5</u> register ...	(3) Set the <u>OSL5</u> flag of the <u>SC5SEL</u> register ...

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XIII-3	First Note	Description addition	-	<u>This function can't be used ni STOP/HALT mode.</u>
	Second Note	Description addition	-	<u>Don't execute mode switching as follows: ...</u>
	First Key	Description addition	-	<u>To realize a low power consumption, ladder resistance is turned OFF before STOP/ HALT mode switching.</u>
	Third Note	Description addition	-	<u>The reference voltage input V_{ref+} pin uses value of $2.0 \text{ V} \leq V_{ref+} \leq V_{DD5}$. When ...</u>
XIII-6	ANCTR0	Error correction	bp2, 5-4 1XX:fs/16 <u>*as $T_{AD} > 800 \text{ ns}$</u>	bp2, 5-4 1XX:fs/16 <u>111:Prohibited</u> <u>*as $800 \text{ ns} \leq T_{AD} \leq 15.26 \mu\text{s}$</u>
XIII-8	ANCTR2	Error correction	bp6-5 11: <u>Continuous conversion</u> or Set ANST flag to "1"	bp6-5 11: <u>A/D conversion interrupt</u> or Set ANST flag to "1"
XIII-11	Fifth Note	Description addition	-	<u>If the flags of ANCTR0, ANCTR1 are changed during A/D conversion, we can't guarantee the operation and the result ...</u>
XIII-12	4	Error correction	Set the A/D conversion cycle (T_{AD}) more than 800 ns.	Set the A/D conversion cycle (T_{AD}) more than 800 ns <u>or less than 15.26 μs.</u>
	Table: 13.3.1	Error correction	244.14 μs 488.28 μs 976.56 μs 15.26 μs 1953.12 μs	244.14 μs <u>(no usable)</u> 488.28 μs <u>(no usable)</u> 976.56 μs <u>(no usable)</u> 15.26 μs 1953.12 μs <u>(no usable)</u>
	Square	Description change	A/D Conversion <u>Sampling</u> Time (T_S) Setup	A/D Conversion <u>Sample Hold</u> Time (T_S) Setup
XIII-13	Key	Error correction	... ,the valid edge should be assigned at REDG flag of <u>the continuous conversion control register (ANCTR2)</u> and ,the valid edge should be assigned at REDG flag of <u>the external interrupt control register (IRQ2ICR)</u> and ...
XV-3	Second Note	Error correction	Set bp0 of the low-speed oscillation <u>switching</u> register (XSEL) to "1" before the transition to the slow oscillation mode.	Set bp5 of the low-speed oscillation <u>selection</u> register (XSEL) to "1" before the transition to the slow oscillation mode.
XV-4	4	Error correction	Switching of normal port, common pin and <u>VLC</u> pin is controlled with the LCD output control register 0 (LCCTR0).	Switching of normal port, common pin and <u>V_{LC1}</u> pin to <u>V_{LC3}</u> pin are controlled with the LCD output control register 0 (LCCTR0).
	7	Error correction	Segment pin, common pin and <u>VLC</u> pin are switchable to I/O port in 1-bit unit.	Segment pin, common pin and <u>V_{LC1}</u> pin to <u>V_{LC3}</u> pin are switchable to I/O port in 1-bit unit.
XV-5	Figure 15.1.1	Error correction		

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XV-7	Table 15.2.2	Error correction	Table 15.2.2: <u>LCD Control Registers List</u>	Table 15.2.2: <u>LCD Mode Control Register 1</u>
	LCDMD1	Error correction	Flag bp5 <u>DUTY1</u> bp4 <u>DUTY0</u>	Flag bp5 <u>LCDTY1</u> bp4 <u>LCDTY0</u>
	LCDMD1	Error correction	bp6 description <u>Set always "0".</u>	bp6 description <u>Always set to "0" *.</u>
XV-8	Second Note	Description addition	-	<u>When the LCDEN flag of LCDMD1 register being set, do not change other flags of LCDMDn register to prevent malfunction.</u>
	Third Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-9	Table 15.2.3	Error correction	Table 15.2.3: <u>LCD Control Registers List</u>	Table 15.2.3: <u>LCD Mode Control Register 2</u>
	LCDMD2	Description change	bp7-4/1-0 Description <u>Set always "0".</u>	bp7-4/1-0 Description <u>Always set to "0" *.</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-10	Table 15.2.4	Error correction	Table 15.2.4: <u>LCD Control Registers List</u>	Table 15.2.4: <u>LCD Mode Control Register 3</u>
	LCDMD3	Description change	bp7-4 Description <u>Set always "0".</u>	bp7-4 Description <u>Always set to "0" *.</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-11	1	Error correction	... that switches Port I/O (P92 to 94) and nd VLC pins (<u>VLC1</u> to <u>VLC3</u>). The value of the LCCTR0 register is set I/O port at reset.	... that switches Port I/O (P84 to P87) and VLC pins (COM0 to COM3) and switches Port I/O (P92 to 94) and VLC pins (<u>VLC1</u> to <u>VLC3</u>). The value of the LCCTR0 register is set port at reset.
	Table 15.2.5	Error correction	Table 15.2.5: <u>LCD Control Registers List</u>	Table 15.2.5: <u>LCD Output Control Register 0</u>
	LCCTR0	Description change	bp3 Description Always set to "0".	bp3 Description Always set to "0" *.
XV-12	Key	Description change	If internal voltage booster circuit is used, ...	<u>P94(VLC1), P93(VLC2) and P92(VLC3) can be used as a port...</u>
	First Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XV-13-19	2	Error correction	... At reset, these ports are set to the <u>input</u> port.	... At reset, these ports are set to the port.
XV-13	Table 15.2.6	Error correction	Table 15.2.6: <u>LCD Control Registers List</u>	Table 15.2.6: <u>LCD Output Control Register 1</u>
XV-14	Table 15.2.7	Error correction	Table 15.2.7: <u>LCD Control Registers List</u>	Table 15.2.7: <u>LCD Output Control Register 2</u>
XV-15	Table 15.2.8	Error correction	Table 15.2.8: <u>LCD Control Registers List</u>	Table 15.2.8: <u>LCD Output Control Register 3</u>
XV-16	Table 15.2.9	Error correction	Table 15.2.9: <u>LCD Control Registers List</u>	Table 15.2.9: <u>LCD Output Control Register 4</u>
XV-17	Table 15.2.10	Error correction	Table 15.2.10: <u>LCD Control Registers List</u>	Table 15.2.10: <u>LCD Output Control Register 5</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XV-18	Table 15.2.11	Error correction	Table 15.2.11: <u>LCD Control Registers List</u>	Table 15.2.11: <u>LCD Output Control Register 6</u>
XV-19	Table 15.2.12	Error correction	Table 15.2.12: <u>LCD Control Registers List</u>	Table 15.2.12: <u>LCD Output Control Register 7</u>
XV-22	5	Error correction	... voltage V_{DD} for LCD panel drive can be used at higher voltage than the V_{DD5} power supply (usable at $V_{LCD} \leq V_{DD} \leq 5.5$ V).	... voltage V_{LCD} for LCD panel drive can be used at higher voltage than the V_{DD5} power supply (usable at $V_{LCD} \leq V_{DD5} \leq 5.5$ V).
XV-25	Figure 15.3.2	Error correction	LCD Power Supply Connection	LCD Power Supply Connection (<u>In external Voltage divider</u>)
	Key	Description change	... In Figure:15.3.3, a bypass capacitor C (0.01 μ F to 0.1 μ F) is used to lower the impedance of power supply.	... In Figure:15.3.3, a bypass capacitor C (<u>about</u> 0.1 μ F) is used to lower the impedance of power supply.
XV-26	Table 15.3.3	Description addition	Table: 15.3.3	Table: 15.3.3 <u>LCD voltage when using the internal voltage dividing resistor</u>
	First Key	Description addition	-	P94(V_{LC1}), P93(V_{LC2}) and P92(V_{LC3}) can be used as a port...
XV-28	5	Description change	Refer to XV-22. Figure:15.3.5 for the LCD power supply connection. Refer to <u>Chapter 15.4 LCD display</u> for connection of LCD panel.	Refer to XV-22. Figure:15.3.2 for the LCD power supply connection. Refer to [<u>Chapter 15 15.4 Display</u>] for connection of LCD panel.
	Description	Error correction	(3) Set COMSL3 to 0 flags of the LCD mode control register <u>1</u> (LCCTR1) ...	(3) Set COMSL3 to 0 flags of the LCD mode control register <u>0</u> (LCCTR0) ...
	Setup Procedure	Error correction	(5) ... bp5-4 : <u>DUTY1-0 = 00</u>	(5) ... bp5-4 : <u>LCDTY1-0 = 00</u>
XV-31	4	Error correction	[<u>Chapter 16. 15.4.1 LCD Display (static)</u>]	[<u>Chapter 15. 15.4.1 static</u>]
	Description	Error correction	(5) ... [<u>Chapter 15.4.2. Setup example (static)</u>]	(5) ... [<u>Chapter 15.4.1. static</u>]
XV-35	4	Error correction	[<u>Chapter 15.4.1 LCD Display (static)</u>]	[<u>Chapter 15. 15.4.3 1/2 Duty</u>]
	Setup Procedure	Error correction	(2) ... bp5-4 : <u>DUTY1-0= 10</u>	(2) ... bp5-4 : <u>LCDTY1-0= 10</u>
	Description	Error correction	(2) Set the <u>DUTY1</u> to <u>DUTY0</u> flags of ...	(2) Set the <u>LCDTY1</u> to <u>LCDTY0</u> flags of ...
XV-39	4	Error correction	[<u>Chapter 15.4.1 LCD Display (static)</u>]	[<u>Chapter 15. 15.4.5 1/3 Duty</u>]
	Setup Procedure	Error correction	(2) ... bp5-4 : <u>LCDDDTY1-0= 10</u>	(2) ... bp5-4 : <u>LCDTY1-0= 10</u>
XV-43	Setup Procedure	Error correction	(2) ... bp5-4 : <u>DUTY1-0= 10</u>	(2) ... bp5-4 : <u>LCDTY1-0= 10</u>
	Description	Error correction	(2) Set the <u>DUTY1</u> to <u>DUTY0</u> flags of ...	(2) Set the <u>LCDTY1</u> to <u>LCDTY0</u> flags of ...
	Description	Description addition	(5) Display "23" ... the segment output latch SEG0 to SEG7.	(5) Display "23" ... the segment output latch SEG0 to SEG7. [<u>Chapter 15 15.4.7 1/4 duty</u>]

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XVI-2	First Key	Error correction	... type of interrupt ATCn, a regular interrupt is generated after the automatic transfer ends.	... type of interrupt ATCn, <u>hardware handling</u> of a regular interrupt is generated after the automatic transfer ends.
	First Note	Description addition	-	<u>The order of an interrupt acceptance may be changed by software when setting each ...</u>
	Third Key	Description addition	-	<u>ATC1 can't be used in standby mode (HALT mode and STOP mode). ATC1 starts ...</u>
XVI-3	Table 16.1.1	Description addition	... Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt * Software startup	... Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt *1 Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt *1 Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt *1 Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt *1 Serial 0 transmission buffer empty, Serial 0 transmission complete interrupt *1 Software startup
XVI-4	First Note	Description addition	-	<u>Change the ATCn activation factor and the transfer mode while ATCn transfer is ...</u>
XVI-7	ATnCNT0	Error correction	bp7 Flag <u>FMODE</u>	bp7 Flag <u>FMODE</u>
	ATnCNT0	Description change	bp1 Description <u>Set always "0".</u>	bp1 Description <u>Always set to "0" *.</u>
	First Note	Description addition	-	<u>ATnACT flag of the ATCn control register0 (ATnCNT0) is cleared by hardware ...</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XVI-8	AT0CNT1	Description change	bp5 Description <u>Set always "0".</u>	bp5 Description <u>Always set to "0" *.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
	Third Note	Description addition	-	<u>Bp5 of the ATCn control register1 (ATnCNT1) may be set by hardware ...</u>
XVI-9	AT1CNT1	Description change	bp5 Description <u>Set always "0".</u>	bp5 Description <u>Always set to "0" *.</u>
	Second Note	Description addition	-	<u>Always set "0" to the bp denoted by asterisk.</u>
XVI-14	Second Key	Description addition	-	<u>When the software activation is selected as an activation factor of ATCn, maximum ...</u>
XVI-15	First Key	Description addition	... I/O space (special registers) 3 cycles	... I/O space (special registers) 3 cycles <u>LOAD cycle and STORE cycle are set as follows. An access timing corresponding to each memory space + 1 cycle</u>
XVI-16	First Note	Description addition	-	<u>Set the memory address while ATCn transfer is disabled (ATnEN flag of the ...</u>
XVI-17	First Note	Description addition	-	<u>Set the number of data transfer while ATCn transfer is disabled (ATnEN flag of the ...</u>

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XVI-18	12	Error correction	... ATCn is activated everytime when <u>timer 0 overflows</u> and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 <u>overflow</u>) is ATCn is activated everytime when <u>interrupt request of timer 0 interrupt generates</u> and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 <u>interrupt request generation</u>) is ...
	Second Note	Description addition	-	<u>Set the data transfer mode while ATCn transfer is disabled (ATnEN flag of the ...</u>
XVI-35	12	Error correction	... is set, the ATCn data transfer shuts down immediately. During this is set, the ATCn data <u>automatic</u> transfer shuts down immediately <u>after one byte transfer completed</u> . During this ...
XVI-36	12	Error correction	... is set, the ATCn data transfer shuts down immediately. During this is set, the ATCn data <u>automatic</u> transfer shuts down immediately <u>after one byte transfer completed</u> . During this ...
XVI-37	Setup Procedure	Error correction	-	(1) <u>Disable the data automatic transfer ATnCNT0 (AT0CNT0:0x03EC0,AT1CNT0:0x03ED0) bp0 :ATnEH = 0</u>
	Description	Error correction	-	(1) <u>Set the ATnEN flag of ATnCNT0 register to "0" to disable ATCn data automatic transfer.</u>
XVI-38	First Note	Description addition	-	<u>Set the ATCn data automatic transfer while ATCn transfer is disabled (ATnEN flag of ...</u>
XVII-5	First Note	Error correction	... The external wait count \geq WTHLD, RDHLD.	... The external wait count \geq WTHLD, RDHLD.
	Third Note	Description addition	To use AC timing variable function, set the EXW1-0 ... to "01" (1 wait) or "10" (2 wait).	To use AC timing variable function, set the EXW1-0 ... to "01" (1 wait) or "10" (2 wait). <u>If set to "11" (3 wait), the operation is not guaranteed.</u>
XVII-6	6	Error correction	... , <u>"hold"</u> means the expanded cycle of the hold time.	... , <u>"WTHLD0"</u> and <u>"WTHLD1"</u> means the expanded cycle of the hold time.
	First Note	Description addition	-	<u>In order to prevent through current, ..., pull-down resistor or level hold circuit etc.. (Please take special caution in the standby mode.)</u>
	Second Note	Description addition	-	<u>This function is for reference and does not guarantee AC timing. Please contact us if you consider using this function.</u>
XVII-7	Setup Procedure	Description addition	(2) Set the ACTMD register bp5-4 : WTHLD1-0 = 01	(2) Set the ACTMD register <u>ACTMD (0x03F06)</u> bp5-4 : WTHLD1-0 = 01
XVIII-2	Figure 18.1.1	Description change	-	Figure is changed
	First Note	Description Deletion	... (For instance, <u>in the case of MN101EF29G</u> , when block 1 and 2 are programmed separately, 2 programming count is added.) (For instance, when block 1 and 2 are programmed separately, 2 programming count is added.) ...
XVIII-3	Table 18.1.1	Description addition	Programming area MAIN DATA	Programming area MAIN DATA <u>BOOT</u>
		Description change	<u>Matsushita Electric Industrial Co., Ltd</u>	<u>Panasonic Corporation</u>
		Description deletion	-	Website column deleted.

Page	Line	Definition	Former Edition (1.4)	New Edition (2.1)
XVIII-5	4 from the bottom	Description change	<u>Matsushita Electric Industrial Co., Ltd</u>	<u>Panasonic Corporation</u>
XVIII-6	Figure 18.3.1	Description change		
	7	Description addition	Pins : :	Pins : <u>OSC1 (16 pin) : Clock input pin</u> <u>OSC1 (17 pin) : Clock input pin</u> :
	First Note	Description addition		<u>Please note that though the lower limit of microcontroller operation power voltage is 2.2V, in programming it is 2.7V</u>
XVIII-8	-	Specification addition	-	<u>18.4 Microcontroller Rewriting Mode</u>
XVIII-28	-	Specification addition	-	<u>18.5 Connecting the PX-FW2</u>
XVIII-30	-	Specification addition	-	<u>18.6 Component Value Calculations</u>
XVIII-34	-	Specification addition	-	<u>18.7 Flash Memory Programming Procedure</u>
XVIII-35	-	Specification addition	-	<u>18.8 Boot Area Programming Procedure</u>
XVIII-36	-	Specification addition	-	<u>18.9 ROM Programming Service</u>
XVIII-39	-	Specification addition	-	<u>18.10 Special Function Registers List</u>

Remark : Definition in the above table is classified according to the content of changes as follows.

Error correction, Description change, Description addition, Description deletion : For the description of LSI manual.

Specification change, Specification addition, Specification deletion : For microcontroller's specification.

The following shows the changes in the publication of “MN101E29G/F29G LSI User’s Manual” (From the 1st Edition 2nd Printing dated in May, 2006 to the 1st Edition 4th Printing dated in January, 2008.)

Page	Line	Definition	Former Edition (1.2)	New Edition (1.4)
II-17,18	Note	Description Addtion		<u>It is not guaranteed to ensure proper operation in accessing to unimplemented spaces, such as internal ROM/RAM spaces without memory (ROM/RAM) and special register spaces without special register.</u>

Remark : Definition in the above table is classified according to the content of changes as follows.

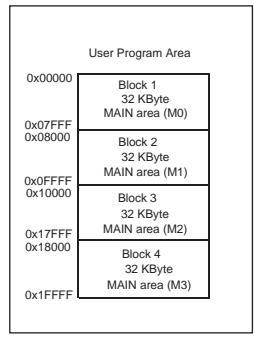
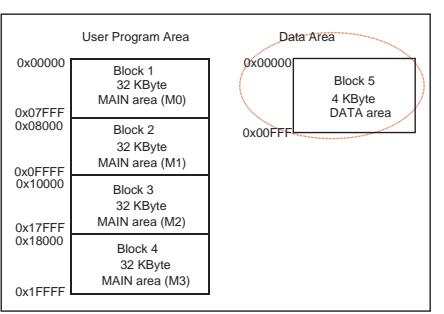
Error correction, Description change, Description addition, Description deletion : For the description of LSI manual.

Specification change, Specification addition, Specification deletion : For microcontroller's specification.

The following shows the changes in the publication of “MN101E29G/F29G LSI User’s Manual” (From the 1st Edition dated in March, 2005 to the 1st Edition 2nd Printing dated in May, 2006.)

Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
I-30	*2	Change	between power supply pin and the ground for latch-up prevention	between <u>V_{DD5}</u> power supply pin and the ground for latch-up prevention
	*3	Add	-	<u>T8OC2IRQ</u> -Timer 8 interrupt (16-bit timer)
I-39	Table	Change	40. MAX: <u>±400</u>	40. MAX: <u>±500</u>
II-23	Figure 2.2.5	Change	0x03EF9: <u>P8OMD2</u>	0x03EF9: <u>Reserved</u>
II-27	RCCTR0	Change	Flag bp7: <u>_</u> At reset bp7: <u>_</u> Access bp7: <u>_</u>	Flag bp7: <u>Reserved</u> At reset bp7: <u>0</u> Access bp7: <u>RW</u>
			0x <u>8FFFF</u>	0x <u>EFFFF</u>
			Flag bp4: <u>_</u> At reset bp4: <u>_</u> Access bp4: <u>_</u>	Flag bp4: <u>P0OMD4</u> At reset bp4: <u>0</u> Access bp4: <u>RW</u>
			bp4: <u>_</u>	<u>bp4: P03 special function setting</u> <u>0: TM0IOB/RMOUTB</u> <u>1: TM2IOB</u>
			bp3: I/O port, TM2IOB/RMOUTB selection 1: TM2IOB/RMOUTB	bp3: I/O port, <u>TM0IOB/TM2IOB/RMOUTB</u> selection 1: <u>TM0IOB/TM2IOB/RMOUTB</u>
			bp2 1: <u>SYSCLK</u>	bp2 1: <u>TM9IOB</u>
			bp1 1: <u>NBUZZER</u>	bp2 1: <u>TM8IOB</u>
			bp1 1: <u>BUZZER</u>	bp2 1: <u>TM7IOB</u>
IV-20	6 to 7 from the bottom	Change	To <u>read out the data of AC zero-cross, set the bp7, 4 of the noise filter control register (NFnCTR)</u> to "1",	To <u>use the detection function of AC zero-cross, set the bp7, 3 of the AC zero-cross detection interrupt control register (ACZCTR)</u> to "1",
IV-31	Last para-graph	Add	-	<u>P47 is also used as the serial 5 clock input pin. When the SEL12C flag ...</u>
IV-34	P4ODC	Change	-	P4ODC register Table is changed

Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
IV-40	P5ODC	Change	Flag bp1: <u>P5ODC</u> bp0: _ At reset bp1: 0 bp0: _ Access bp1: <u>R/W</u> bp0: _ bp0: _	Flag bp1: _ bp0: <u>P5ODC0</u> At reset bp1: _ bp0: 0 Access bp1: _ bp0: <u>R/W</u> bp0: Nch open-drain output selection 0: Push-pull output 1: Nch open-drain output
IV-42	BUZSEL	Change	Flag bp4: <u>P5OMD14</u> bp3: <u>P5OMD13</u> bp2: <u>P5OMD12</u> bp1: <u>P5OMD11</u>	Flag bp4: BUZSEL4 bp3: BUZSEL3 bp2: BUZSEL2 bp1: BUZSEL1
IV-66	P9OMD	Change	Flag bp4: <u>SYSCLK</u> bp4: I/O port, SYSCLK selection 0: Output 1: Not output	Flag bp4: Reserved bp4: Always set to "0".
IV-82	Table 4.15.1	Add	-	PACNT, Add Port 8
IV-83	-	Add	-	Add Port 8 description
V-51	The last paragraph	Change	TM0BC starts to count up from 0x00 with negative edge of the external interrupt 0 (IRQ0) input as a trigger. Timer 0 continues to...	At sampling the negative edge of the external interrupt 0 (IRQ0) input with the count clock, the internal enable is set. And after the setting, the next count clock makes
VI-9	The first key mark	Change	<u>the interrupt request flag is set and the binary counter is cleared, at the next count clock.</u> So set the compare register as: <u>Compare register setting = (count till the interrupt request -1)</u>	<u>the value of the internal count clock is inverted at the next count clock.</u> So set the compare register as: <u>Compare register setting = (count till the compare match -1)</u>
VII-56	Figure 7.7.4	Change	152.6 Hz	400 Hz
IX-9	Step (9)	Change	To get <u>1/2 dividing</u> of 36.7 kHz (73.4 kHz)	To get <u>2-times frequency</u> of 36.7 kHz (73.4 kHz)....
XI-3	Figure 11.1.1	Change		

Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
XII-7 to 12	Figure 12.1.1 to 12.1.2	Change		
XII-82	6	Change	-	Add IRQEXPEN
XV-13	1	Changeport I/O (P60 to P63, <u>P54</u> to P57)port I/O (P60 to P63, <u>P50</u> to P53)
	LCCTR3	Change	bp7: SEG23/ <u>Port54</u> selection 0: Port <u>54</u>	bp7: SEG23/ <u>Port53</u> selection 0: Port <u>53</u>
			bp6: SEG22/ <u>Port55</u> selection 0: Port <u>55</u>	bp6: SEG22/ <u>Port52</u> selection 0: Port <u>52</u>
			bp5: SEG21/ <u>Port56</u> selection 0: Port <u>56</u>	bp5: SEG21/ <u>Port51</u> selection 0: Port <u>51</u>
			bp4: SEG20/ <u>Port57</u> selection 0: Port <u>57</u>	bp4: SEG20/ <u>Port50</u> selection 0: Port <u>50</u>
XV-14	1	Changeport I/O (P50 to P53, P44 to P47)port I/O (<u>P54</u> to P57, P44 to P47)
	LCCTR4	Change	bp3: SEG27/ <u>Port50</u> selection 0: Port <u>50</u>	bp3: SEG27/ <u>Port57</u> selection 0: Port <u>57</u>
			bp2: SEG26/ <u>Port50</u> selection 0: Port <u>50</u>	bp2: SEG26/ <u>Port56</u> selection 0: Port <u>56</u>
			bp1: SEG25/ <u>Port51</u> selection 0: Port <u>51</u>	bp1: SEG25/ <u>Port55</u> selection 0: Port <u>55</u>
			bp0: SEG24/ <u>Port52</u> selection 0: Port <u>52</u>	bp0: SEG24/ <u>Port54</u> selection 0: Port <u>54</u>
XVI-8	-	Change	ATCn control register(AT0CNT1:0x03EC1, AT1CNT1:0x03ED1)	Changed to ATC0 control register1 (AT0CNT1:0x03EC1), ATC1 control register1(AT1CNT1:0x03ED1)
XVIII-2	10	Add	-	-Data area description is added
	Figure 18.1.1	Add		
XVIII-3	Table 18.1.1	Add	-	Data area field is added
			-	OBJECT Co., Ltd. field is added

Page	Line	Definition	Former Edition (1.0)	New Edition (1.2)
XVIII-5	The last line	Add	-	OBJECT Co., Ltd. description is added
XVIII-7	Table	Add	Frequency -	Frequency <u>2.0 to 20 MHz</u>
XVIII-7	Note	Add	-	Do not set the relation between micro-controller clock pin frequency and communication clock frequency to 1/20 or less.

Inquiries

If you have questions regarding technical information on this manual, please visit the following URL.

Panasonic Corporation

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