Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

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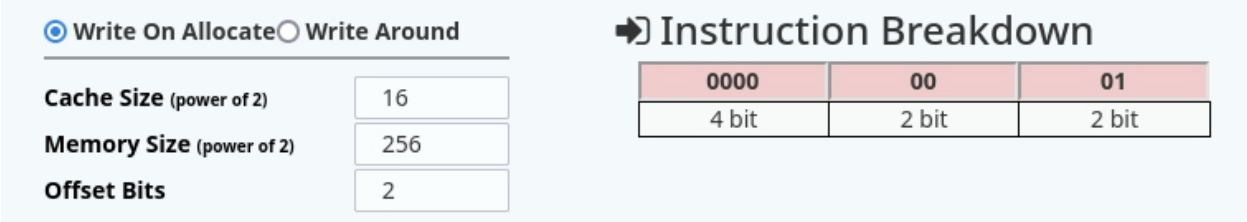
Week#____8_____ Number: ____1__

Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes.

a) Find Number of bits in tag, index and offset.



b)The processor generates requests as follows:
1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.
Find hit rate and miss rate.

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

(for entry 1)

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000	BLOCK 0 WORD 0 - 3	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

ii) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001	BLOCK 4 WORD 0 - 3	0
1	1	0000	BLOCK 1 WORD 0 - 3	0
2	1	0000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0

iii) Screenshot showing hit and miss rates

Statistics

Hit Rate : 38%

Miss Rate : 63%

List of Previous Instructions :

- **Load 1 [Miss]**
- **Load 4 [Miss]**
- **Load 8 [Miss]**
- **Load 5 [Hit]**
- **Load 14 [Miss]**
- **Load 11 [Miss]**
- **Load 13 [Hit]**
- **Load 38 [Miss]**
- **Load 9 [Miss]**
- **Load B [Hit]**
- **Load 4 [Miss]**
- **Load 2B [Miss]**
- **Load 5 [Hit]**
- **Load 6 [Hit]**
- **Load 9 [Miss]**
- **Load 11 [Hit]**

Week#___8_____ Number: ___2__

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Instruction Breakdown

011	100011	01011001
3 bit	6 bit	8 bit

b) Screenshot showing the Cache Table

32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	1	011	BLOCK E3 WORD 0 - 255	0
36	0	-	0	0
37	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- **Load 1B60D [Miss]**
- **Load 8D41 [Miss]**
- **Load 176D1 [Miss]**
- **Load 13AE8 [Miss]**
- **Load 181FA [Miss]**
- **Load 1495 [Miss]**
- **Load 186B3 [Miss]**
- **Load E359 [Miss]**
- **Load 1151D [Miss]**
- **Load 1A76A [Miss]**

Week#___8_____ Number: ___3__

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

Instruction Breakdown

TAG	INDEX	OFFSET
5 bit	5 bit	6 bit

(b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Instruction Breakdown

00000	00100	101000
5 bit	5 bit	6 bit

Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3	B. 4 W. 4	B. 4 W. 5	B. 4 W. 6	B. 4 W. 7	B. 4 W. 8	B.
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3	B. 5 W. 4	B. 5 W. 5	B. 5 W. 6	B. 5 W. 7	B. 5 W. 8	B.
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3	B. 6 W. 4	B. 6 W. 5	B. 6 W. 6	B. 6 W. 7	B. 6 W. 8	B.
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3	B. 7 W. 4	B. 7 W. 5	B. 7 W. 6	B. 7 W. 7	B. 7 W. 8	B.
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3	B. 8 W. 4	B. 8 W. 5	B. 8 W. 6	B. 8 W. 7	B. 8 W. 8	B.
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3	B. 9 W. 4	B. 9 W. 5	B. 9 W. 6	B. 9 W. 7	B. 9 W. 8	B.

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	1	00000	BLOCK 4 WORD 0 - 63	0
5	0	-	0	0

b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	1	00000	BLOCK 4 WORD 0 - 63	0
5	1	00100	BLOCK 85 WORD 0 - 63	0
6	1	00100	BLOCK 86 WORD 0 - 63	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics

Hit Rate : 33%

Miss Rate : 67%

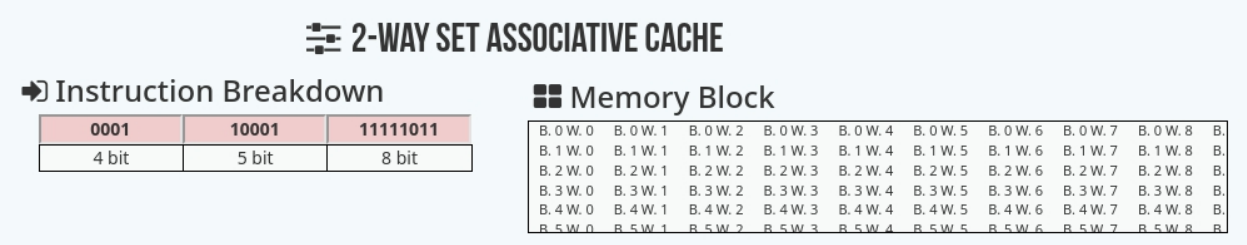
List of Previous Instructions :

- **Load 128 [Miss]**
- **Load 144 [Miss]**
- **Load 2176 [Miss]**
- **Load 2180 [Miss]**
- **Load 128 [Hit]**
- **Load 2176 [Hit]**

Week#___8_____ Number: ___4__

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

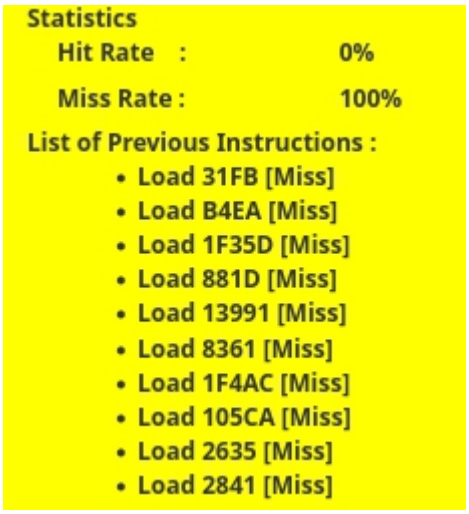


b) Screenshot showing the Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	1	4	B. 83 W. 0 - 255	0
4	0	-	0	0
5	1	8	B. 105 W. 0 - 255	0
6	1	1	B. 26 W. 0 - 255	0
7	0	-	0	0
8	1	4	B. 88 W. 0 - 255	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	1	1	B. 31 W. 0 - 255	0
18	0	-	0	0
19	1	f	B. 1F3 W. 0 - 255	0
20	1	5	B. B4 W. 0 - 255	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	1	9	B. 139 W. 0 - 255	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	1	1	BLOCK 28 WORD 0 - 255	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	1	f	BLOCK 1F4 WORD 0 - 255	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0

c) Screenshot showing hit and miss rates



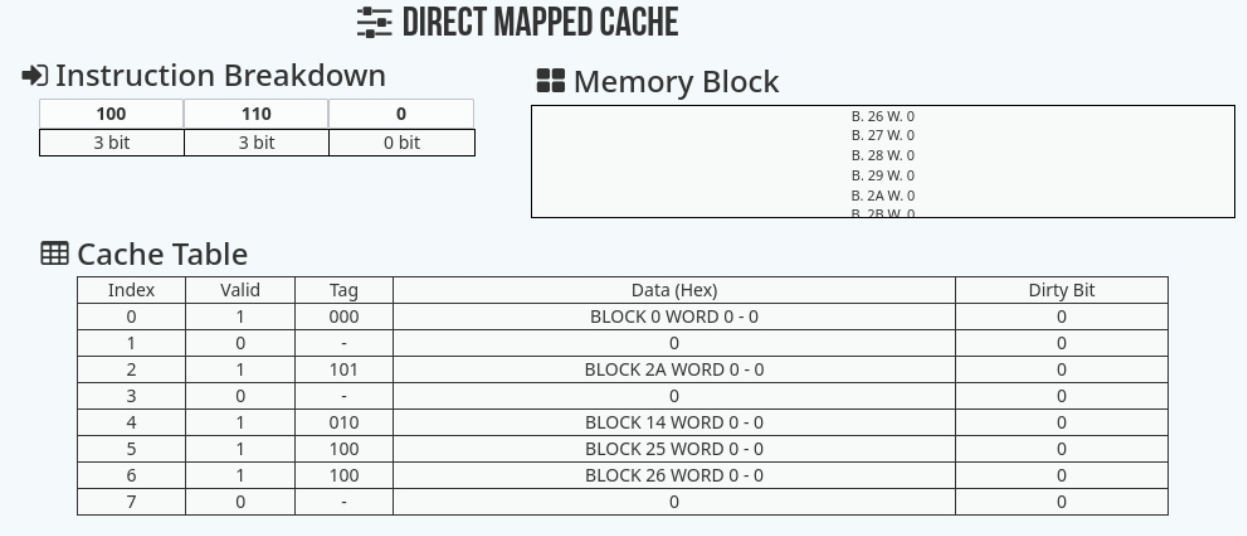
Week#___8_____ Number: ___5__

Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines

Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used.

The cache is mapped as

a) Direct Mapped



DIRECT MAPPED CACHE

Instruction Breakdown

100	110	0
3 bit	3 bit	0 bit

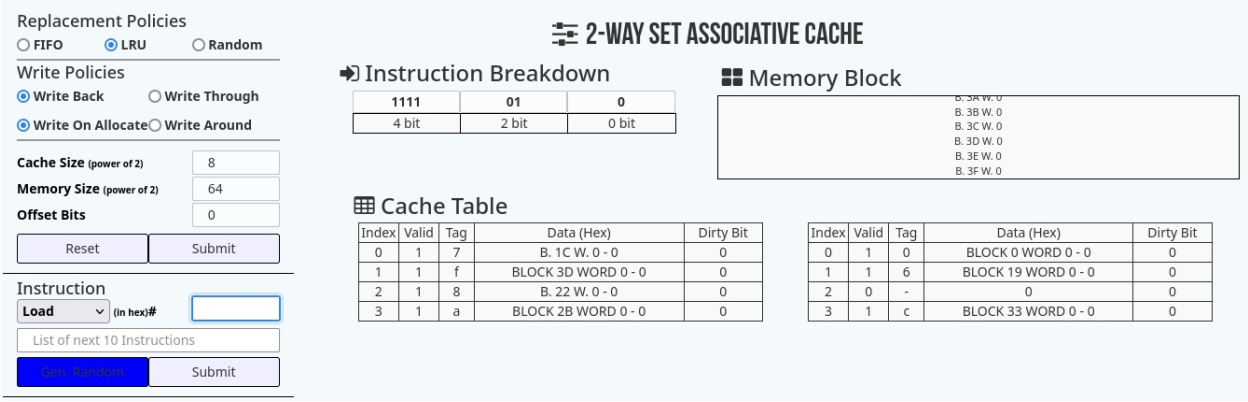
Memory Block

B. 26 W. 0
B. 27 W. 0
B. 28 W. 0
B. 29 W. 0
B. 2A W. 0
B. 2B W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 0	0
1	0	-	0	0
2	1	101	BLOCK 2A WORD 0 - 0	0
3	0	-	0	0
4	1	010	BLOCK 14 WORD 0 - 0	0
5	1	100	BLOCK 25 WORD 0 - 0	0
6	1	100	BLOCK 26 WORD 0 - 0	0
7	0	-	0	0

b) Two way set Associative



Replacement Policies
FIFO LRU Random
Write Policies
Write Back Write Through
Write On Allocate Write Around
Cache Size (power of 2) 8
Memory Size (power of 2) 64
Offset Bits 0
Reset Submit
Instruction
Load (in hex)#
List of next 10 Instructions
Gen. Random Submit

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

1111	01	0
4 bit	2 bit	0 bit

Memory Block

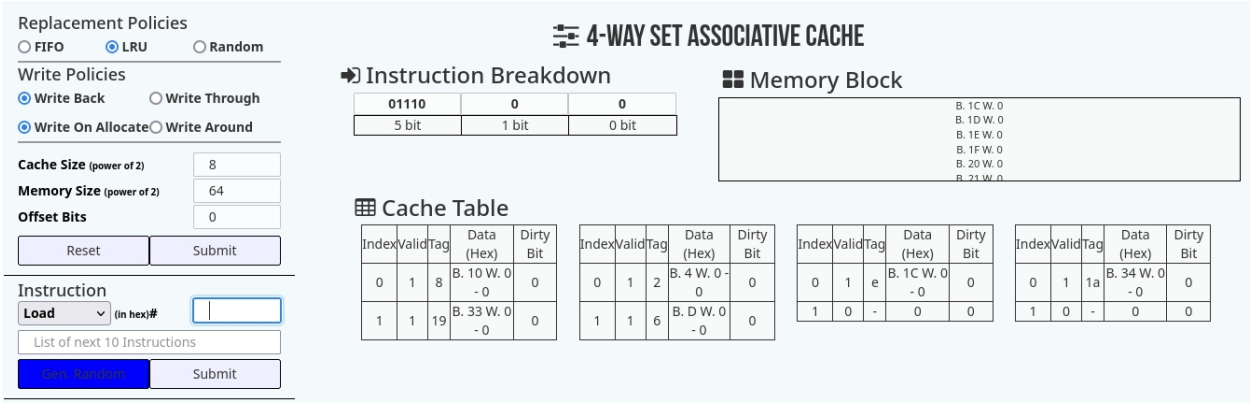
B. 3B W. 0
B. 3C W. 0
B. 3D W. 0
B. 3E W. 0
B. 3F W. 0

Cache Table

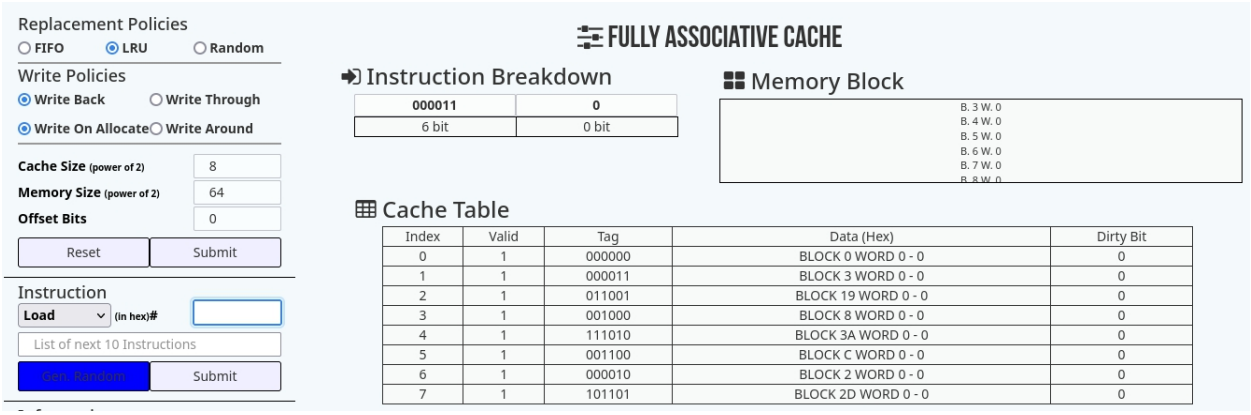
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	7	B. 1C W. 0 - 0	0
1	1	f	BLOCK 3D WORD 0 - 0	0
2	1	8	B. 22 W. 0 - 0	0
3	1	a	BLOCK 2B WORD 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	BLOCK 0 WORD 0 - 0	0
1	1	6	BLOCK 19 WORD 0 - 0	0
2	0	-	0	0
3	1	c	BLOCK 33 WORD 0 - 0	0

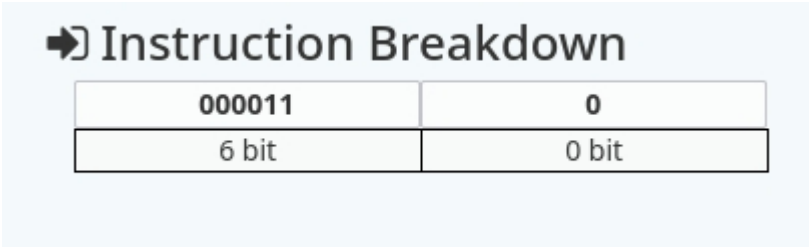
c) Four Way Set associative



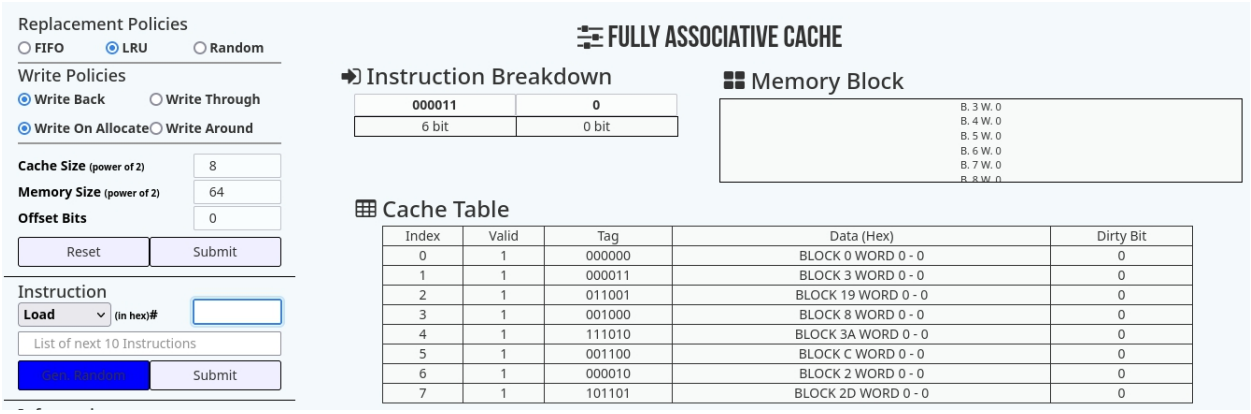
d) Fully Associative



a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



b) Screenshot showing the Cache Table



Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000	BLOCK 0 WORD 0 - 0	0
1	1	000011	BLOCK 3 WORD 0 - 0	0
2	1	011001	BLOCK 19 WORD 0 - 0	0
3	1	001000	BLOCK 8 WORD 0 - 0	0
4	1	111010	BLOCK 3A WORD 0 - 0	0
5	1	001100	BLOCK C WORD 0 - 0	0
6	1	000010	BLOCK 2 WORD 0 - 0	0
7	1	101101	BLOCK 2D WORD 0 - 0	0

c) Screenshot showing hit and miss rates

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- **Load 3 [Miss]**
- **Load 35 [Miss]**
- **Load 19 [Miss]**
- **Load 8 [Miss]**
- **Load 3A [Miss]**
- **Load C [Miss]**
- **Load 2 [Miss]**
- **Load 2D [Miss]**
- **Load 0 [Miss]**
- **Load 3 [Miss]**

Next Index: 2

Last Index: 1

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