P8 Pin	Register Description	GPIO Designation	Reg Offset	P9 Pin	Register Description	GPIO Designation	Reg on Offset	Beag	leBone Bla	ck GPIO (CHEA	T SHEET	3 1 2	GND GPIO1_6	GND P8
P8.3	gpmc_ad6	gpio1[6]	818	P9.11	gpmc_wait0	gpio0[30]	870						9	GPIO1_2	GPIO1_3
P8.4	gpmc_ad7	gpio1[7]	81C	P9.12	gpmc_be1n	gpio1[28]							⊳ 8	TIMER4/2_2	TIMER7/2_3
P8.5	gpmc_ad2	gpio1[2]	808	P9.13	gpmc_wpn	gpio0[31]	874						9 10	TIMER5/2 5	TIMER6/2 4
P8.6 P8.7	gpmc_ad3 gpmc_advn_ale	gpio1[3] gpio2[2]	80C 890	P9.14 P9.15	gpmc_a2 gpmc_a0	gpio1[18] gpio1[16]	848 840					0. 50.11	11 11	GPIO1 13	GPIO1_12
P8.8	gpmc_oen_ren	gpio2[2]	894	P9.16	gpmc_a3	gpio1[10]	84C					On P8 these	13	EHRPWM2B/0_23	GPIO0 26
P8.9	gpmc_be0n_cle	gpio2[5]	89C	P9.17	spi0_cs0	gpio0[5]	95C					pins are used	15 1		GPIO1_14
P8.10	gpmc_wen	gpio2[4]	898	P9.18	spi0_d1	gpio0[4]	958					by the new		GPIO1_15	
P8.11	gpmc_ad13	gpio1[13]	834	P9.19	uart1_rtsn	gpio0[13]	87C	ORDERED BY GPIO			eMMC flash	118	GPIO0_27	GPIO0_2_1	
P8.12	gpmc_ad12	gpio1[12]	830	P9.20	uart1_ctsn	gpio0[12]	978	OKDI	EREDBIG	PIO		memory i/f	19	EHRPWM2A/0_22	GPIO1_31
P8.13 P8.14	gpmc_ad9 gpmc_ad10	gpio0[23] gpio0[26]	824 828	P9.21 P9.22	spi0_d0 spi0_sclk	gpio0[3] gpio0[2]	954 950	Pin	Descr.	GPIO	Offs.	momory wi	22	GPIO1_30	GPIO1_5
P8.15	gpmc_ad15	gpio1[15]	83C	P9.23	gpmc_a1	gpio0[2]	844	l ———					23	GPIO1 4	GPI01_1
P8.16	gpmc_ad14	gpio1[14]	838	P9.24	uart1_txd	gpio0[15]	984	P8.25	gpmc_ad0	gpio1[0]	800		25	GPIO1 0	GPIO1 29
P8.17	gpmc_ad11	gpio0[27]	82C	P9.25	mcasp0_ahclkx	gpio3[21]	9AC	P8.24	gpmc_ad1	gpio1[1]	804		27 28 28	GPIO2 22	GPIO2_24
P8.18	gpmc_clk_mux0	gpio2[1]	88C	P9.26	uart1_rxd	gpio0[14]	980	P8.5 P8.6	gpmc_ad2	gpio1[2]	808 80C	On P8 these		-	
P8.19	gpmc_ad8	gpio0[22]	820	P9.27	mcasp0_fsr	gpio3[19]	9A4	P8.23	gpmc_ad3	gpio1[3]	810	pins are	30	GPIO2_23	GPIO2_25
P8.20	gpmc_csn2	gpio1[31]	884	P9.28	mcasp0_ahclkr	gpio3[17]	99C	P8.22	gpmc_ad4 gpmc_ad5	gpio1[4] gpio1[5]	814	used by the	31	UART5_CTSN/0_10	0 UART5_RTSN/0_11
P8.21 P8.22	gpmc_csn1 gpmc_ad5	gpio1[30] gpio1[5]	880 814	P9.29 P9.30	mcasp0_fsx mcasp0_axr0	gpio3[15] gpio3[16]	994 998	P8.3	gpmc_ad6	gpio1[6]	818	•	33	UART4_RTSN/0_9	UART3_RTSN/2_17
P8.23	gpmc_ad4	gpio1[4]	810	P9.31	mcasp0_axi0 mcasp0_aclkx	gpio3[16]	990	P8.4	gpmc_ad7	gpio1[7]	81C	new HDMI	35		UART3_CTSN/2_16
P8.24	gpmc_ad1	gpio1[1]	804	1 0.01	тосоро_солох	1 abico[11]	1 000	P8.12	gpmc_ad12	gpio1[12]	830	i/f	38		UART5_RXD/2_15
P8.25	gpmc_ad0	gpio1[0]	800					P8.11	gpmc_ad13	gpio1[13]	834		39 3	GPIO2 12	GPIO2_13
P8.26	gpmc_csn0	gpio1[29]	87C					P8.16	gpmc_ad14	gpio1[14]	838	This i/f is		_	
P8.27	lcd_vsync	gpio2[22]	8E0					P8.15	gpmc_ad15	gpio1[15]	83C	fairly simple	42	GPIO2_10	GPIO2_11
P8.28 P8.29	lcd_pclk	gpio2[24]	8E8 8E4					P9.15	gpmc_a0	gpio1[16]	840	to disable	44	GPIO2_8	GPIO2_9
P8.30	lcd_hsync lcd ac bias en	gpio2[23] gpio2[25]	8EC					P9.23	gpmc_a1	gpio1[17]	844	to disable	45	GPIO2_6	GPI02_7
P8.31	lcd_data14	gpio0[10]	8D8					P9.14	gpmc_a2	gpio1[18]	848			_	
P8.32	lcd_data15	gpio0[11]	8DC	Pin	Descr.	GPIO	Offs.	P9.16	gpmc_a3	gpio1[19]	84C		- 2		P9
P8.33	lcd_data13	gpio0[9]	8D4				_	P9.12	gpmc_be1n	gpio1[28]	87C		ω 4		C_3V3
P8.34	lcd_data11	gpio2[17]	8CC	P9.31	mcasp0_aclkx	gpio3[14]	990	P8.26 P8.21	gpmc_csn0	gpio1[29] gpio1[30]	880		က ဖ	V	DD_5V
P8.35	lcd_data12	gpio0[8]	8D0	P9.29 P9.30	mcasp0_fsx mcasp0_axr0	gpio3[15] gpio3[16]	994 998	P8.20	gpmc_csn1 gpmc_csn2	gpio1[30] gpio1[31]	884		<u>۸</u>	S	YS_5V
P8.36 P8.37	lcd_data10 lcd_data8	gpio2[16] gpio2[14]	8C8 8C0	P9.28	mcasp0_axr0 mcasp0_ahclkr	gpio3[10]	99C	1 0.20	gpino_03nz	gpio i[o i] i	004		9 01	PWR BUT	_ SYS RESETn
P8.38	lcd_data9	gpio2[14]	8C4	P9.27	mcasp0_anciki	gpio3[17]	9A4	Pin	Descr.	GPIO	Off:	S.	12 1	UART4_RXD/0_30	GPIO1_28
P8.39	lcd data6	gpio2[12]	8B8	P9.25	mcasp0_isi		9AC	P8.18	gpmc_clk_mu:	κ0 gpio2[1]	880	2	£ 4	UART4_TXD/0_31	EHRPWM1A/1_18
P8.40	lcd_data7	gpio2[13]	8BC		. –	•. •		P8.7	gpmc_advn_a	.	890		15 1	GPIO1 16	EHRPWM1B/1_19
P8.41	lcd_data4	gpio2[10]	8B0	Pin	Descr.	GPIO	Offs.	P8.8	gpmc_oen_rei		894		1 1 1	12C1_SCL/0_5	I2C1_SDA/0_4
P8.42	lcd_data5	gpio2[11]	8B4	P9.22	spi0_sclk	gpio0[2]	950	P8.10	gpmc_wen	gpio2[4]	898	3			
P8.43 P8.44	lcd_data2 lcd_data3	gpio2[8]	8A8 8AC	P9.21	spi0_d0		954	P8.9	gpmc_be0n_c	le gpio2[5]	890		19 20	I2C2_SCL/0_13	I2C2_SDA/0_12
P8.45	lcd_data0	gpio2[9] gpio2[6]	8A0	P9.18	spi0_d1	0,	958	P8.45	lcd_data0	gpio2[6]	8A0		22	UART2_TXD/0_3	UART2_RXD/0_2
P8.46	lcd_data1	gpio2[7]	8A4	P9.17	spi0_cs0	0, 1,	95C	P8.46	lcd_data1	gpio2[7]	8A4		23	GPIO1_17	UART1_TXD/0_15
'	_		·	P8.35	lcd_data12	gpio0[8]	8D0	P8.43	lcd_data2	gpio2[8]	8A8		25	GPIO3_21*	UART1_RXD/0_14
ORDE	ERED BY HEA	DER PIN		P8.33	lcd_data13	0, 1,	8D4	P8.44	lcd_data3	gpio2[9]	8A		27	GPIO3_19	SPI1_CS0/3_17
				P8.31 P8.32	lcd_data14	0, 1,	8D8 8DC	P8.41	lcd_data4	gpio2[10]			30 29	SPI1_D0/3_15	SPI1_D1/3_16
				P8.32 P9.20	lcd_data15 uart1 ctsn	0	978	P8.42 P8.39	lcd_data5 lcd_data6	gpio2[11] gpio2[12]	- 1		32	SPI1_SCLK/3_14	VADC
				P9.19	uart1_ctsn		87C	P8.40	lcd_data7	gpio2[12]			33	AIN4	AGND
				P9.26	uart1_rxd		980	P8.37	lcd_data7	gpio2[14]			38 35	AIN6	AIN5
				P9.24	uart1_txd	gpio0[15]	984	P8.38	lcd_data9	gpio2[15]			38	AIN2	AIN3
				P8.19	gpmc_ad8	gpio0[22]	820	P8.36	lcd_data10	gpio2[16]			39 3	AIN0	AIN1
					gpmc_ad9		824	P8.34	lcd_data11	gpio2[17]			μ 4	CLKOUT2/GPIO0 7	
				P8.13 P8.14	gpmc_ad10	gpio0[26]	828	P8.27	lcd_vsync	gpio2[22]		0	42	OLNOU12/GP100_/	GPIO3_20/18
				P8.17	gpmc_ad11	gpio0[27]	82C	P8.29	lcd_hsync	gpio2[23]			44		
				P9.11	gpmc_wait0		870	P8.28	lcd_pclk	gpio2[24]			45		
			<u> </u>	P9.13	gpmc_wpn	gpio0[31]	874	P8.30	lcd_ac_bias_e	n gpio2[25]] 8E	<u> </u>	* GPIO3	3_21 is also the 24.576MH	Iz clock for the HDMI Audio