



```

3  module sfp (out, in, thres, acc, relu, clk, reset);
4
5  parameter bw = 4;
6  parameter psum_bw = 16;
7
8  input clk;
9  input acc;
10 input relu;
11 input reset;
12
13 input signed [bw-1:0] in;
14 input signed [psum_bw-1:0] thres;
15
16 output signed [psum_bw-1:0] out;
17
18 reg signed [psum_bw-1:0] psum_q;
19
20
21 assign out = psum_q;          // Assign psum_q to out at the next clock edge
22
23 always @ (posedge clk) begin
24     if(reset) begin           // Synchronous Reset
25         psum_q <= 16'b0;
26     end
27     else if (acc) begin        // When acc == 1, psum_q will increment by in
28         psum_q <= psum_q + in;
29     end
30     else if (relu && psum_q < thres) begin // When relu == 1 and psum_q < thres, set psum_q to 0
31         psum_q <= 16'b0;
32     end
33     else begin                 // If none of the cases then set to same value
34         psum_q <= psum_q;
35     end
36 end
37
38 endmodule

```