# LAB 1

Implementing Binary Adders in VHDL

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# Contents

# 1 Abstract

In this report, an exploration of two different approaches to digital logic design was done: dataflow and structural. Two different implementations of a 2 bit full adder was made, and the corresponding testbenches. The VHDL feature of multiple architecture definitions was used to make the testing and implementation easier, by only needed to select a specific architecture instead of editing files.

# 2 Design

# 3 Testing & Simulation

# 4 Conclusion

# 5 References

# 6 Appendix