ECE 302 Lab - Project 2 Marking Guide

No.	Student Name	ID Number	Group No.
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Abstract			**5**
Briefly summarizes the specs and results of the lab			1
Mention the Rin and the gain of the CE stage			1
Mention the Rin and the gain of the CC stage			1
Mention the Rin and the gain of the whole circuit			2
Objectives			**5**
Mention 12 V/V ±5%			2
Mention R_{in} > 9 kΩ			2
Mention 9 V_{P-P} output without clipping			1
Design			**20**
Address why we took the approach of design and testing of both BJT amplifiers separately. What advantages does this offer you?			4
Explain and justify why CE stage was chosen			3
Explain and justify why CC stage was chosen			3
Show and explain calculations for the resistor values for the CE stage			5
Show and explain calculations for the resistor values for the CC stage			5
Simulation			**16**
Student 01	Simulation for the DC bias voltages (V_C, V_E, V_B) for both CC and CE stage		1
	Simulation for the CE stage showing Gain and output of 9 V_{P-P} without clipping		1
	Simulation for the CE stage to determine R_{in}		1
	Simulation for the CC stage showing Gain and output voltage		1
	Simulation for the CC stage to determine R_{in}		1
	Simulation for the entire circuit showing Gain and output of 9 V_{P-P} without clipping		1
	Simulation for the entire circuit to determine R_{in}		1
	All schematics should be neat, labeled and correct		1
Student 02	Simulation for the DC bias voltages (V_C, V_E, V_B) for both CC and CE stage		1
	Simulation for the CE stage showing Gain and output of 9 V_{P-P} without clipping		1
	Simulation for the CE stage to determine R_{in}		1
	Simulation for the CC stage showing Gain and output voltage		1
	Simulation for the CC stage to determine R_{in}		1
	Simulation for the entire circuit showing Gain and output of 9 V_{P-P} without clipping		1
	Simulation for the entire circuit to determine R_{in}		1
	All schematics should be neat, labeled and correct		1
Experimental Results			**14**
Comparison of design, simulation, and measured results; discrepancies discussed/explained; shows judgement/evaluation of design performance			1
DC bias voltages (V_C, V_E, V_B) for CE stage			1
Voltage waveforms of CE stage showing input and output			2

DC bias voltages (V_C, V_E, V_B) for CC stage			1
Voltage waveforms of CC stage showing input and output			2
Voltage waveforms of entire circuit (CC+CE) stage showing input and output			2
Gain for CE stage, Gain for CC stage, Gain for entire circuit			2
Rin for CC stage, Rin for entire (CE+CC) circuit with waveforms			2
Voltage waveform showing entire circuit output 9 V_{P-P} without clipping			1
Discussions			**10**
1. Does the order of the amplifiers matter? Why?			2
2. Comment on the stability of your amplifier. Did you face instability problems? What modifications, if any, were needed to the design and/or the circuit?			2
3. What is the intent of the impedance transformer? Why is it necessary?			1
4. Why is the high input impedance amplifier necessary?			2
5. In this lab we assumed that the input and output impedance is purely resistive. Is this a fair assumption? What are the issues with this assumption?			2
6. Were there any other difficulties you faced? What steps could you do to address these issues (even if you didn't actually do them or could not do them)?			1
Conclusions (properly summarizes results and findings)			**5**
Figures (figures are labeled, of good quality and readable)			**5**
Lab Report Total			**80**
Lab Marks (Individual)	1	2	
Lab 2a check in			3
Lab 2a check out			3
Lab 2b check in			3
Lab 2b check out			3
Lab 2c check in			4
Lab 2c check out			4
Lab Mark Total			**20**
Deductions			0
Lab 1 Total			**100**

Marked by: _____Signature: _____Date:_____