Nanoparticle Assembly Chambers



Tools for novel AI, biotech, and multi-function hardware



Al Hardware Approach Limitations

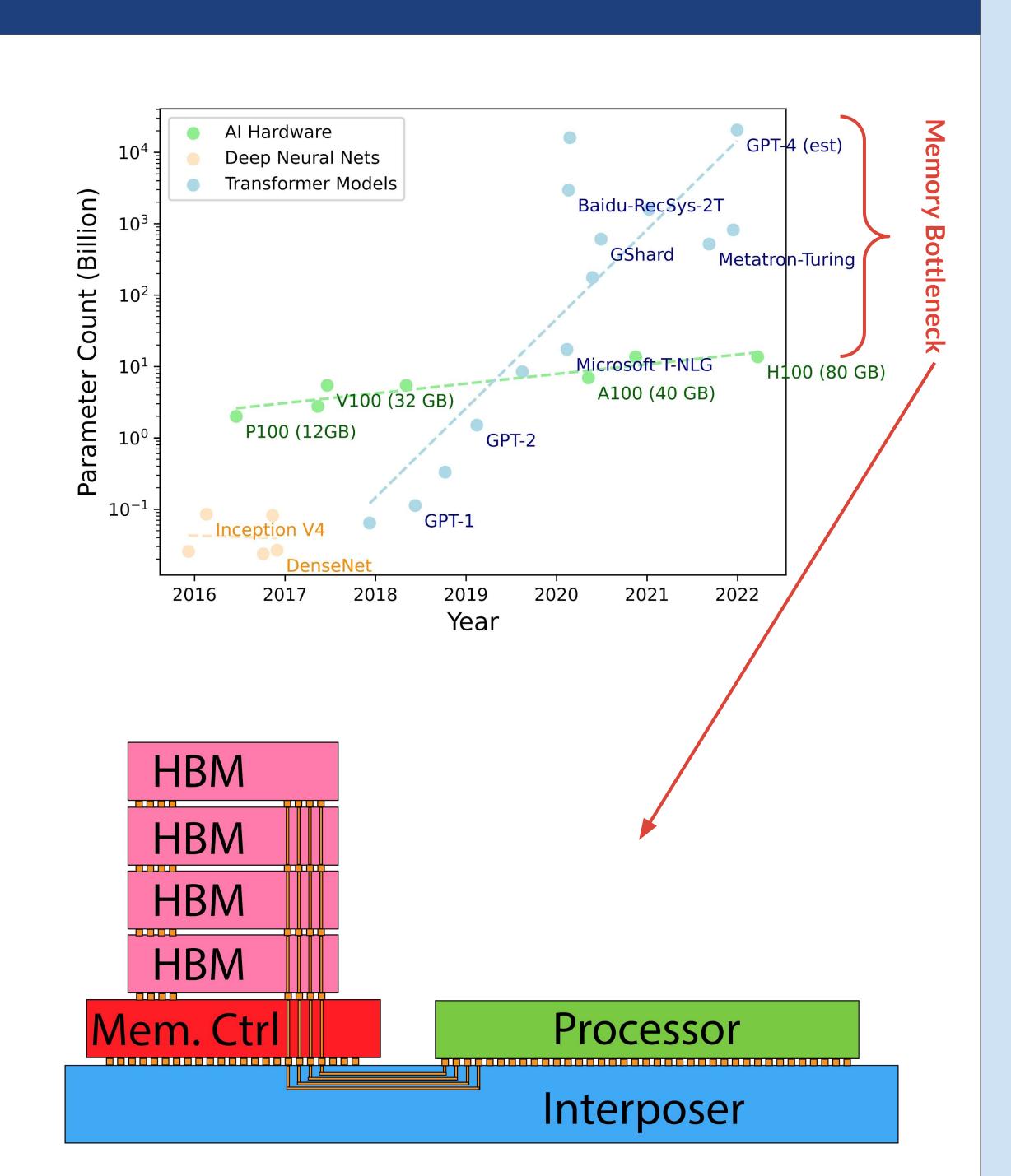
Mathematical Breakthroughs

- ☐ Larger AI models offer significant potential to revolutionize most economic sectors
- Current hardware approaches have struggled to keep pace with mathematical advances
- ☐ Increasing die size
- ☐ Increasing integration with packaging
- ☐ Fine tuning architecture

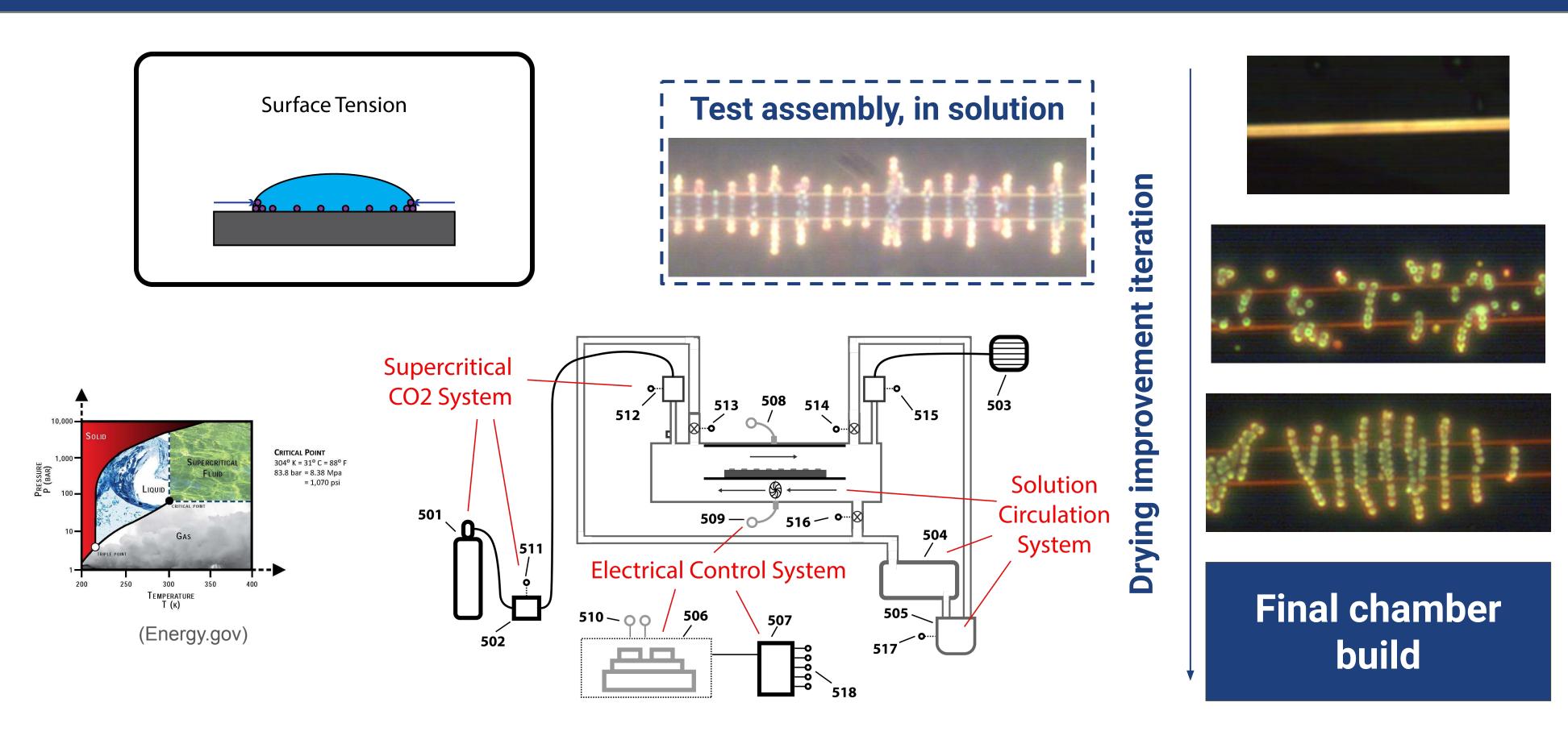
Physical Limitations

- Memory bottlenecks arise from physical fabrication and packaging constraints
- ☐ Interconnect pitches and via yield are improving incrementally

A *faster rate* of hardware improvement is necessary



Reducing Disruption with Supercritical Drying

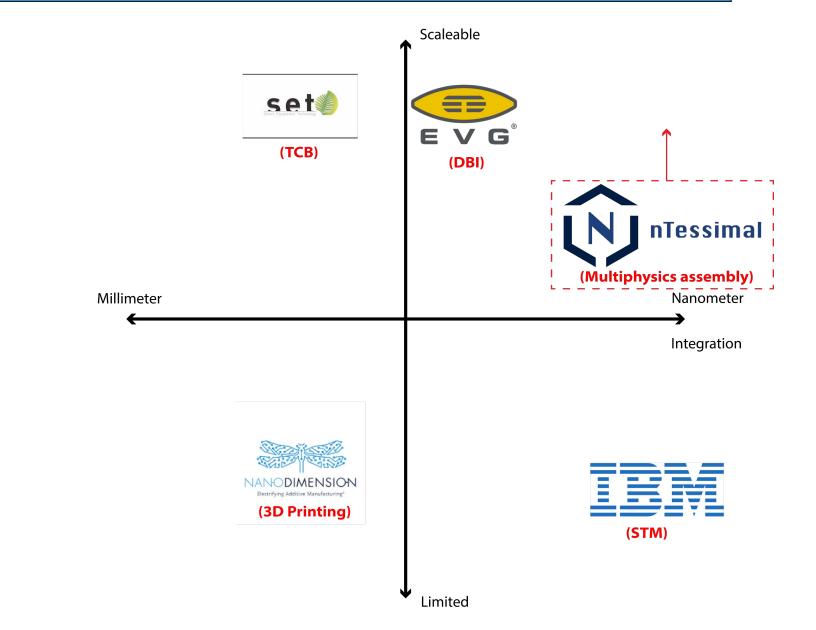


- ☐ Surface tension disrupts particles during drying
- ☐ Smaller particles, submicron, experience greater disruption
- ☐ Our patent pending assembly chamber incorporates in-situ supercritical drying to prevent disruption by movement and Brownian forces
- □ Supercritical CO₂ mixtures are compatible with appropriate permittivity/conductivity solvents at reasonable pressure/temperature

Evolutionary Device Level Integration

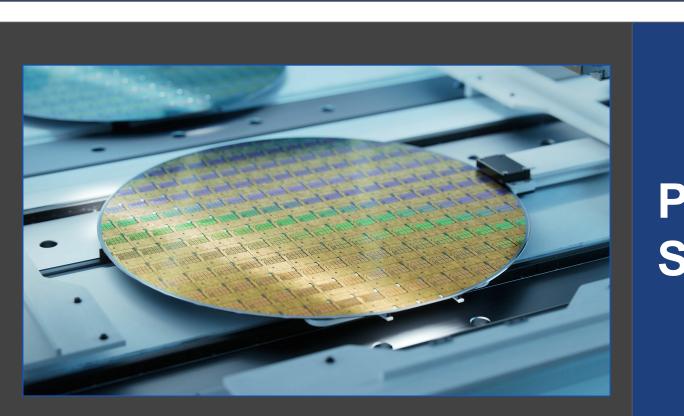
RDL detail not shown, for illustration purposes only **CNTFET** Photodiode Platelet Photodiode Wire Photon CMOS STT-RAM

- Nanoscale high density interconnects (nm vs. μm)
- Near & in-memory computing
- Higher density, shorter lines
- ☐ Larger materials set, fabricated off substrate
- ☐ CNTFETs (~5x switching speed, ~½ power)
- Multi-functional die
- Logic, memory, optical
- ☐ True 3D topology



Compatible with existing wafer level processing & larger scale integration Lithography defined integration allows for a potential >1,000x improvement over traditional packaging

Industries

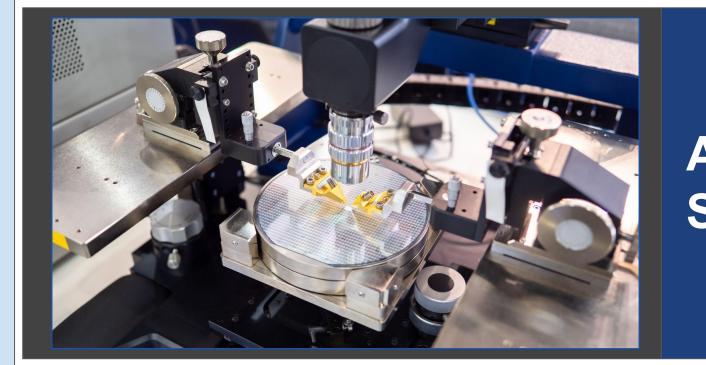


Pure-Play Semiconductor We received a NSF grant support letter from a semiconductor foundry, Skywater, who understands the value of patterning high purity CNFETs.

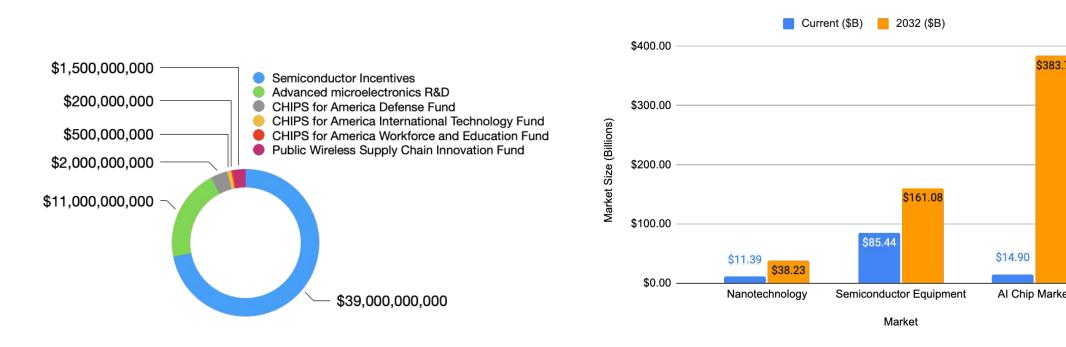


Biotechnology

We received a NSF grant support letter from EtectRx to increase manufacturability of microparticle based monitoring antenna and lab-on-chip solutions.

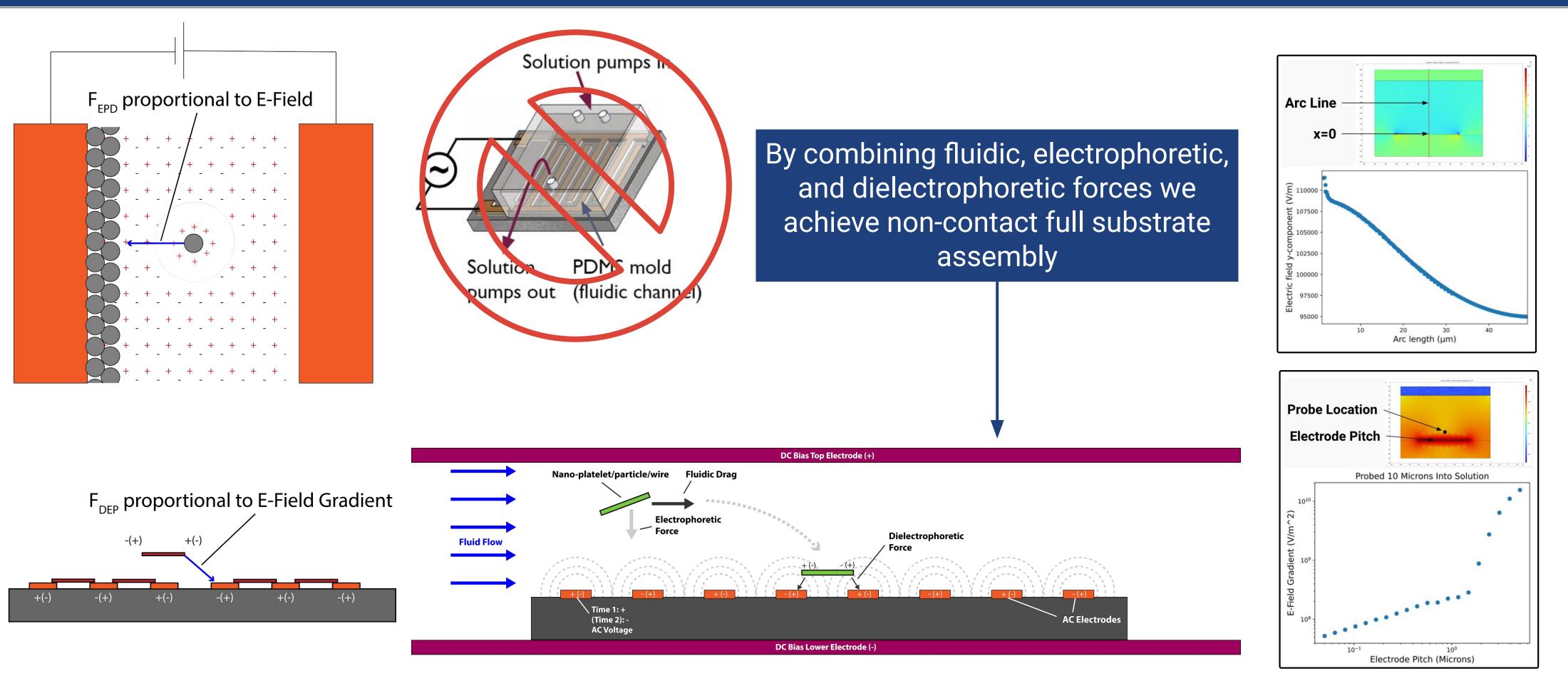


Advanced Substrates We're working with a glass substrate manufacturer, Samtec, on high aspect ratio via fill including novel materials.



Market growth and incentives bolster semiconductor equipment tailwinds

Multiphysics Nanoscale Assembly



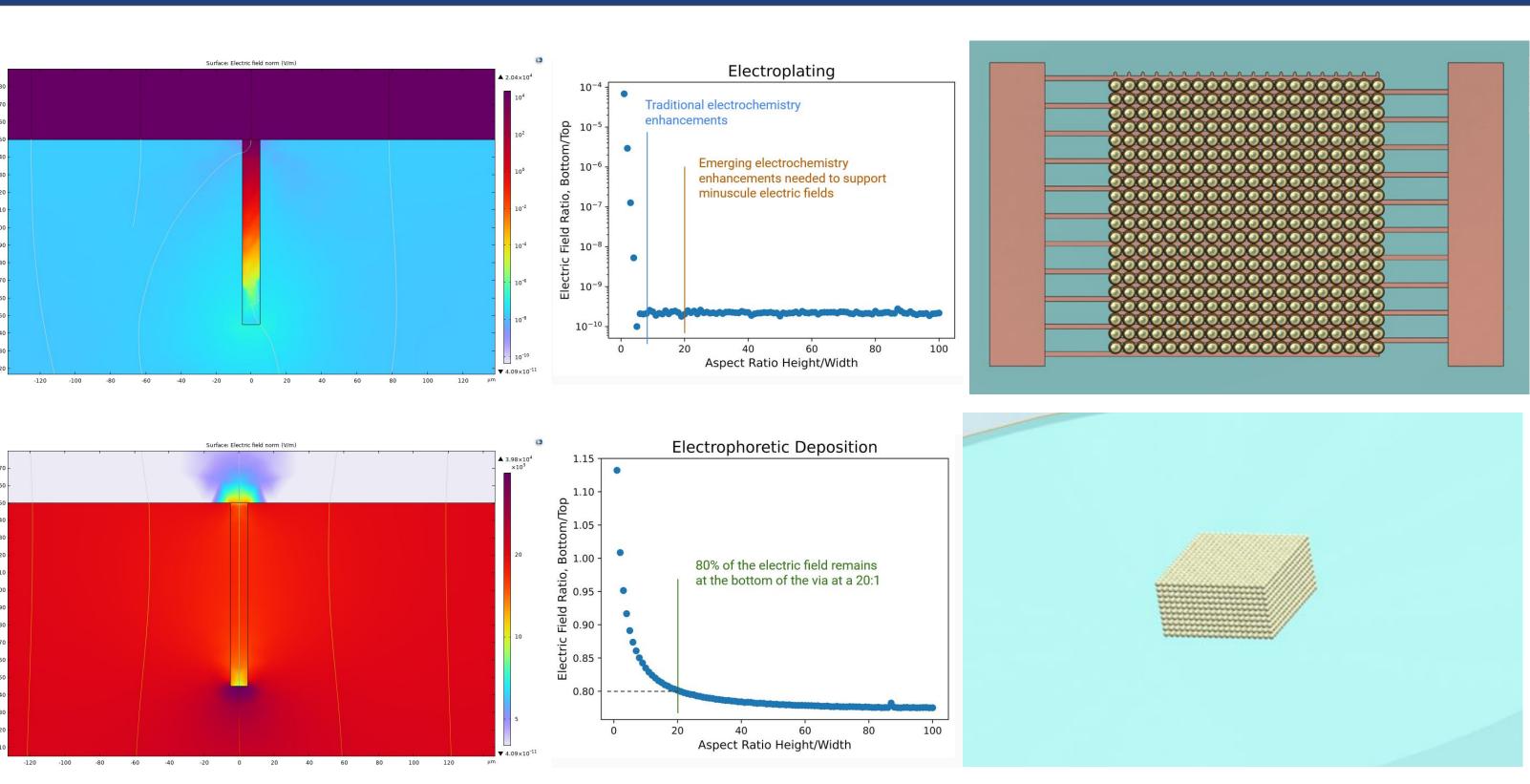
Microfluidic Channels + DEP

- Decreased patternable area
- Particle contamination
- Requires mechanical movement Non-contact
- Adhesion loss

Multiphysics Assembly

- ☐ Allows full wafer to be patterned simultaneously
- No movable parts during assembly

Additional Applications



High Aspect Ratio Via Fill

- ☐ Larger E-field gradients within via for ☐ Photonic crystals higher aspect ratio fill
- ☐ Greater variety of available materials ■ Non-plateable metals
- Dielectrics
- Magnetic materials
- Composites

- Photonics/Plasmonics
- Multi-particle quantum plasmonics
- Can be combined with photo-emitters/photo-detectors

Lab-On-Chip

- Nanowires functionalized off-chip
- Assembled on chip

Cost effective R&D chambers and application support can help customers develop novel IP