Ass_Syn_1.0

You have to synthesize Down_Counter.v file and generate Technology Dependent gate level netlist in Verilog format using standard cell library (scmetro_tsmc_cl013g_rvt_tt_1p2v_25c.db)

1. Using Design Compiler GUI

2. Using TCL scripts and run it through Design Compiler Shell

Required: -

1. The generated files during running design compiler GUI

2. The generated files and TCL script during running design compiler shell