Ryerson University

Department of Electrical
& Computer Engineering
Faculty of Engineering & Architectural Science

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|---|---|
| **Course Title:** | Low-Power Digital Integrated Circuits |
| **Course Number:** | ELE734 |
| **Semester/Year (e.g.F2016)** | F2022 |

| | |
|---|---|
| **Instructor:** | Dr.Andy Ye |

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|---|---|
| **Assignment/Lab Number:** | 4 |
| **Assignment/Lab Title:** | CMOS 1-Bit Full Adder |

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|---|---|
| **Submission Date:** | 12/06/2022 |
| **Due Date:** | 12/06/2022 |

| Student LAST Name | Student FIRST Name | Student Number | Section | Signature* |
|---|---|---|---|---|
| Sharma | Nabhanya | 500826185 | 4 | NS |
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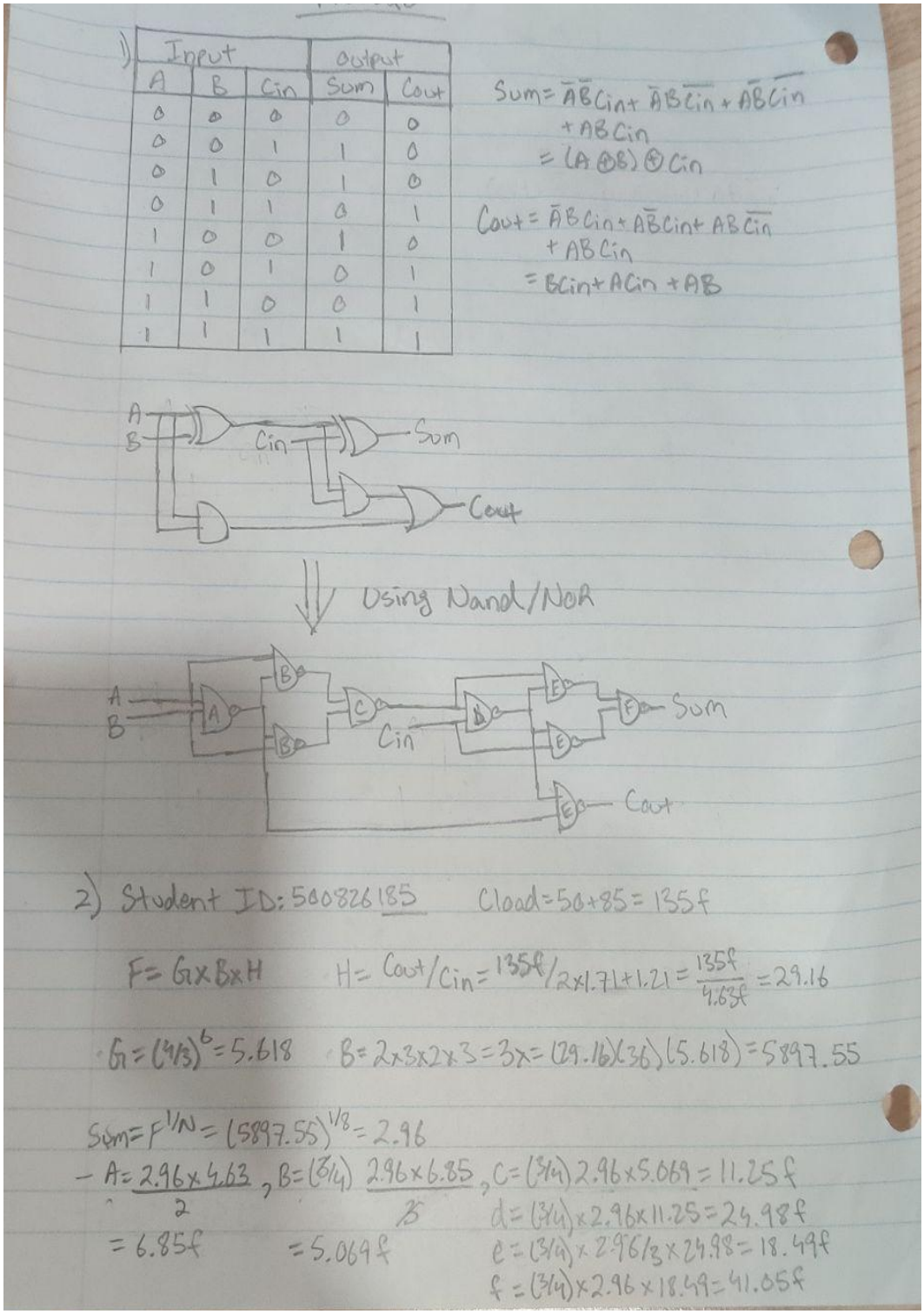
*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

## Objective

To implement a 1-bit full adder to verify its performance and measure its delay.

## Prelab



1)

| Input | | | output | |
|---|---|---|---|---|
| A | B | Cin | Sum | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

$Sum = \bar{A}\bar{B}Cin + \bar{A}B\bar{Cin} + A\bar{B}\bar{Cin} + ABCin$
$= (A \oplus B) \oplus Cin$

$Cout = \bar{A}BCin + A\bar{B}Cin + AB\bar{Cin} + ABCin$
$= BCin + ACin + AB$

A, B, Cin, Sum, Cout

Using Nand/Nor

A, B, Cin, Sum, Cout

2) Student ID: 500826185 $Cload = 50 + 85 = 135f$

$F = G \times B \times H$ $H = Cout/Cin = 135f/(2 \times 1.71 + 1.21) = \frac{135f}{4.63f} = 29.16$

$G = (4/3)^6 = 5.618$ $B = 2 \times 3 \times 2 \times 3 = 3x = (29.16)(36)(5.618) = 5897.55$

$Sum = F^{1/N} = (5897.55)^{1/8} = 2.96$

$A = \frac{2.96 \times 4.63}{2} = 6.85f$, $B = (3/4)\frac{2.96 \times 6.85}{3} = 5.069f$, $C = (3/4)2.96 \times 5.069 = 11.25f$

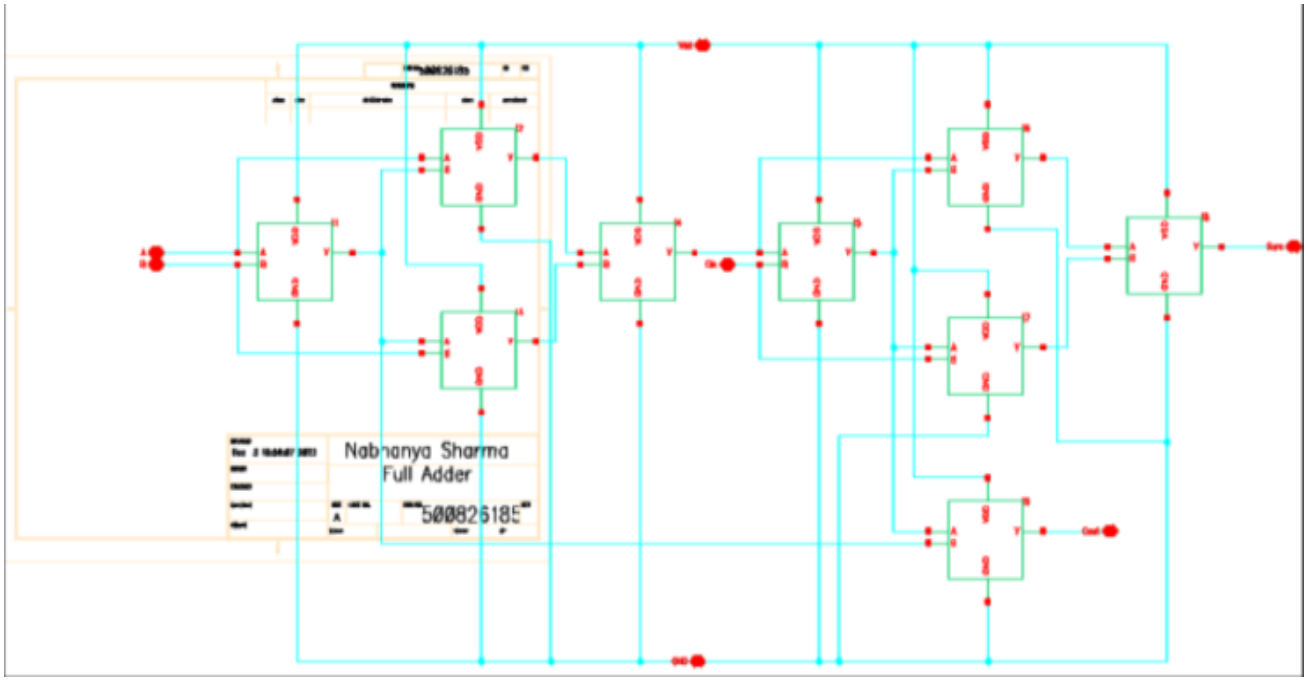
$d = (3/4) \times 2.96 \times 11.25 = 24.98f$

$e = (3/4) \times 2.96/3 \times 24.98 = 18.49f$

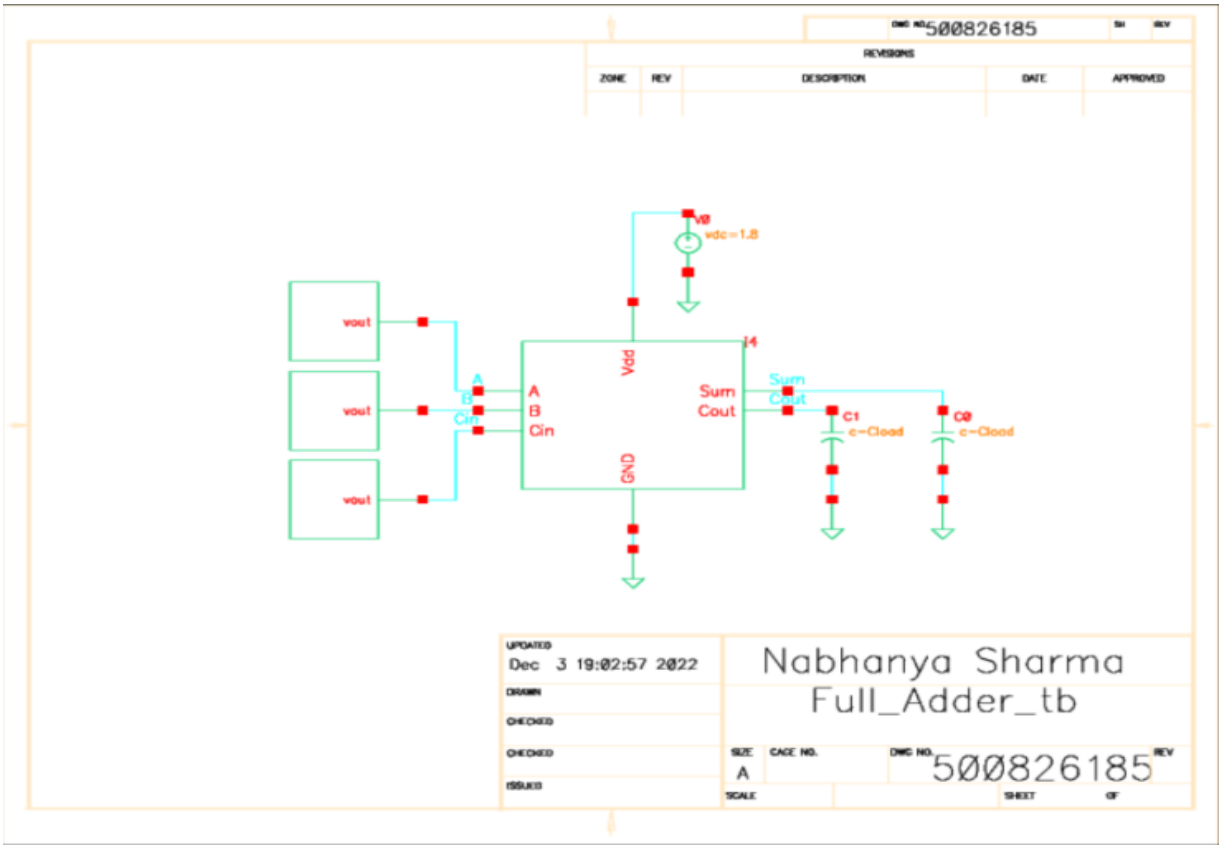
$f = (3/4) \times 2.96 \times 18.49 = 41.05f$

Post-Lab

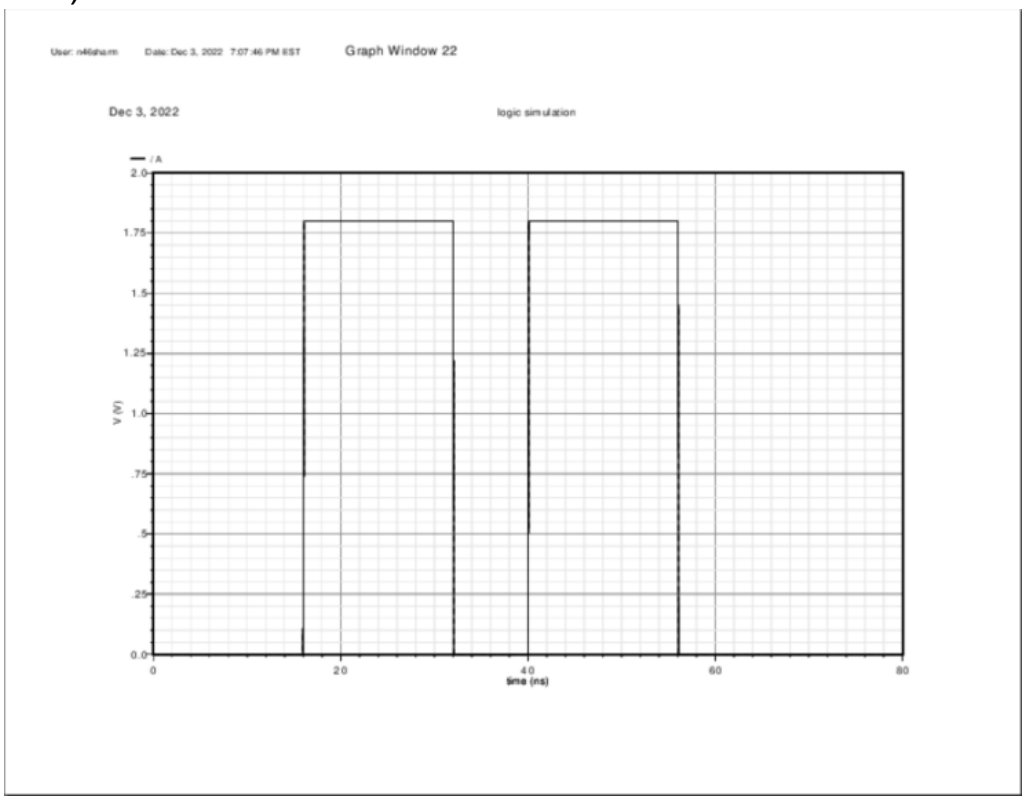
1)


Nabhanya Sharma
Full Adder
500826185

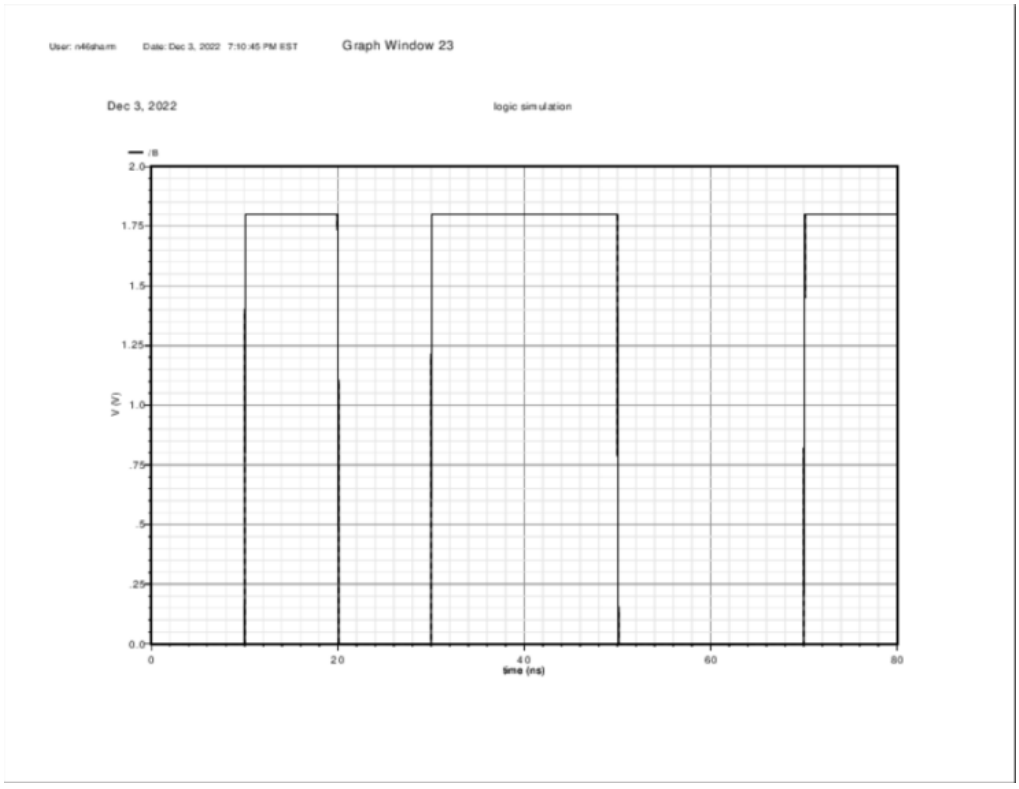
2)


500826185
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
V0
vdc=1.8
vout
vout
vout
A
B
Cin
Vdd
GND
Sum
Cout
C1
c=Cload
C0
c=Cload
UPDATED
Dec 3 19:02:57 2022
DRAWN
CHECKED
CHECKED
ISSUED
Nabhanya Sharma
Full_Adder_tb
SIZE
A
CAGE NO.
DWG NO.
500826185
REV
SCALE
SHEET

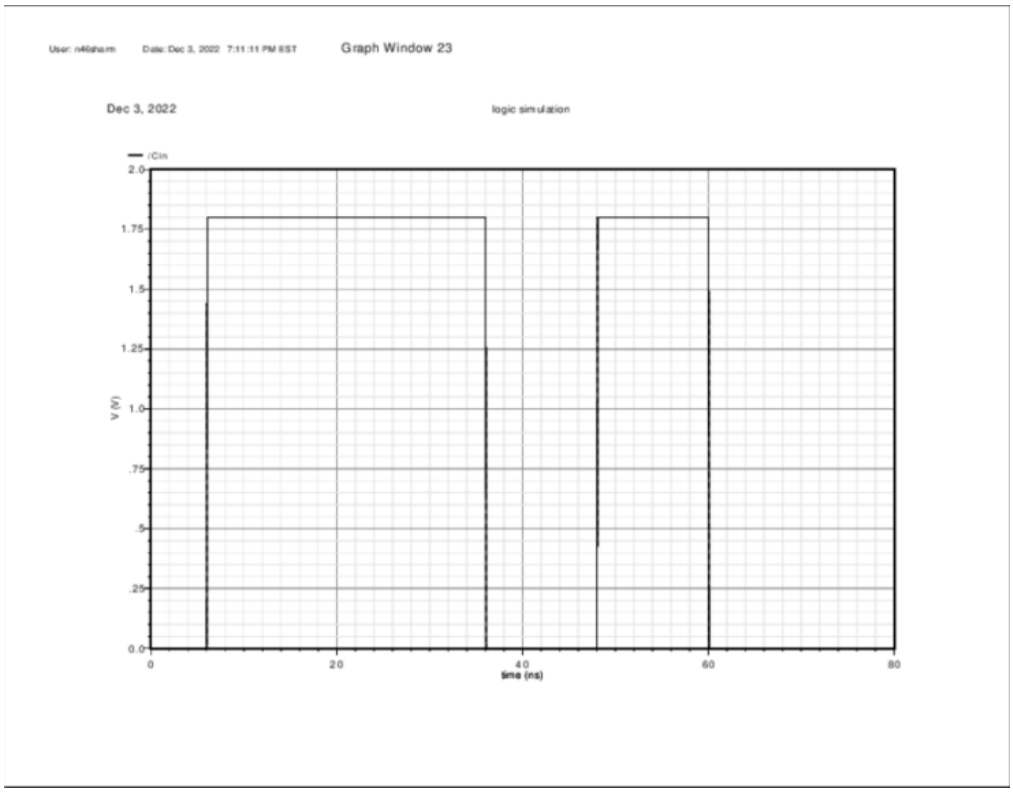
3) A:


Graph Window 22
Dec 3, 2022
logic simulation
/ A
V (V)
Time (ns)

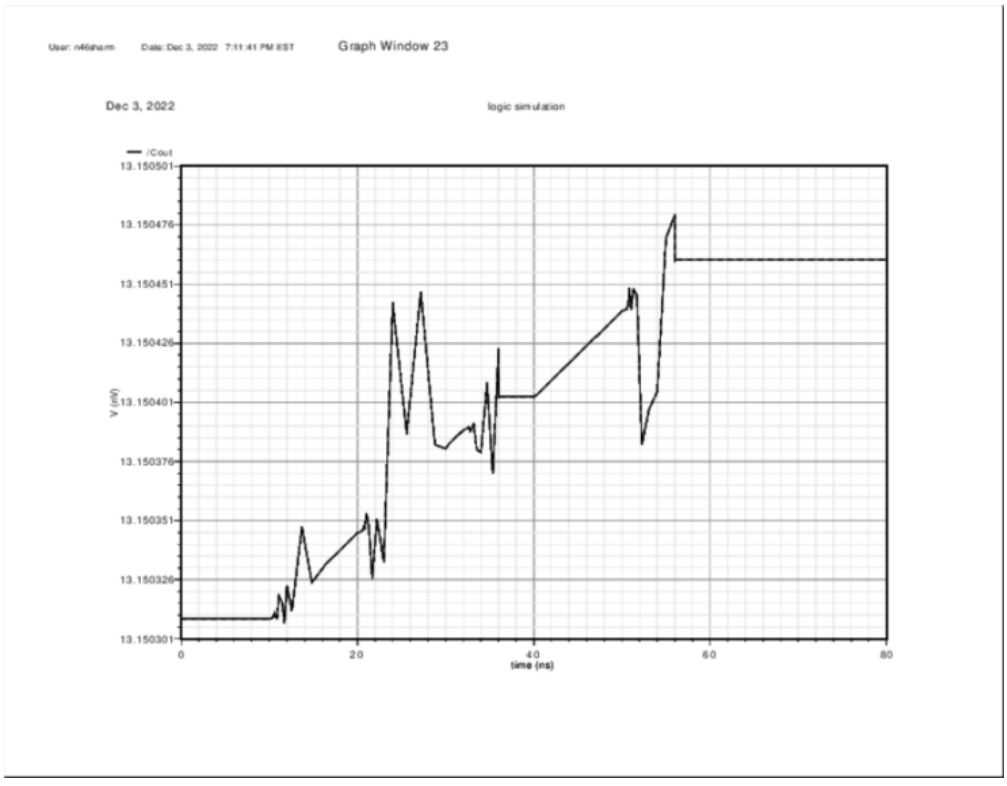
B:


Graph Window 23
Dec 3, 2022
logic simulation
/ B
V (V)
Time (ns)

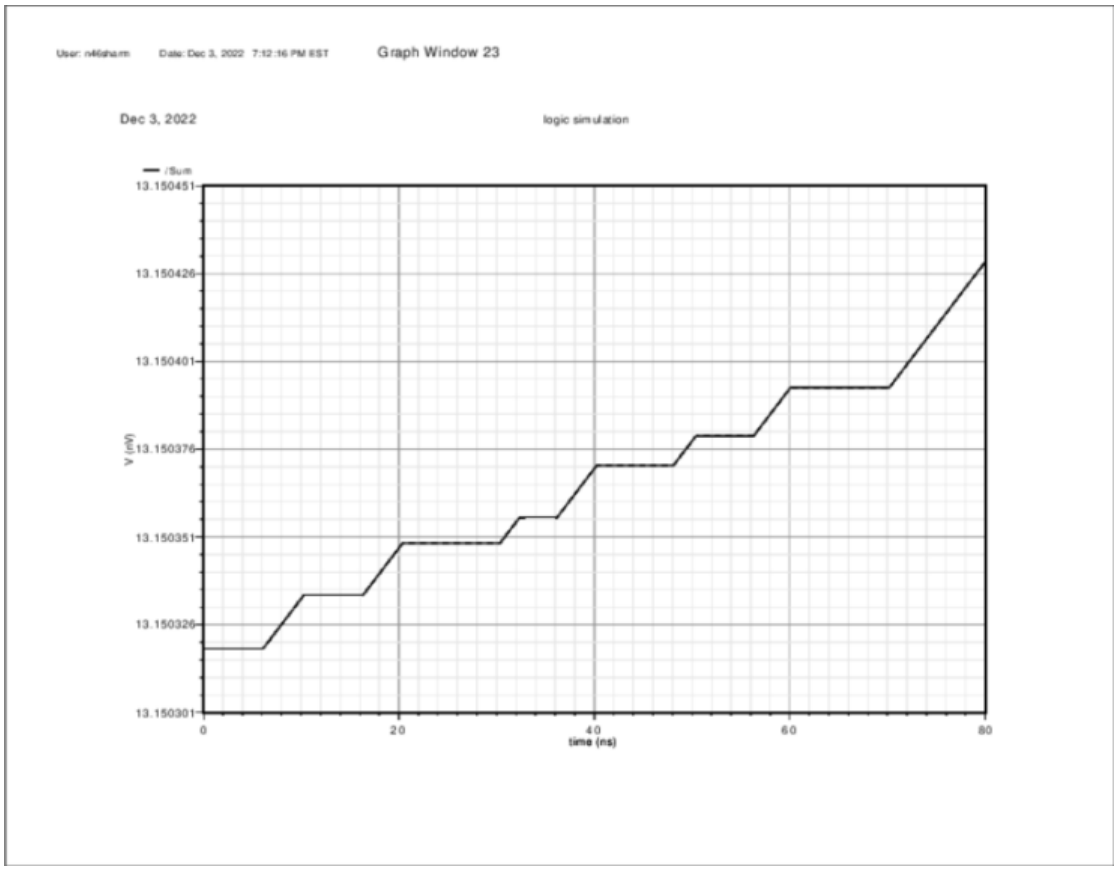
Cin:


User: n46shorm Date: Dec 3, 2022 7:11:11 PM EST
Graph Window 23
Dec 3, 2022
logic simulation
/Cin
2.0
1.75
1.5
1.25
1.0
.75
.5
.25
0.0
V (V)
0
20
40
60
80
time (ns)

Cout:


User: n46shorm Date: Dec 3, 2022 7:11:41 PM EST
Graph Window 23
Dec 3, 2022
logic simulation
/Cout
13.150501
13.150476
13.150451
13.150426
13.150401
13.150376
13.150351
13.150326
13.150301
V (mV)
0
20
40
60
80
time (ns)

Sum:




4)

| Net | Rising | Falling |
|---|---|---|
| A | 8.11 | 13.01 |
| B | 8.11 | 13.01 |
| Cin | 8.12 | 13.02 |
| Cout | | |

| | | |
|---|---|---|
| Sum | | |

## Conclusion

The 1-bit adder was constructed and explored for its performance and delay. However there do seem to be some errors as not all results seem to be correct. For example the Cout and Sum graphs are incorrect and because of that the delay calculations were not able to be calculated as well. This may be due to human error made during the implementation of the schematic or miscalculation in the prelab section.