# ECSE 318 Lab 2 Report Group 5

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# Lab Part 1\_ ALU:

```
Testing operation:
                         ADD=00000 //A+B=>C signed addition
                                                                        CarryOutEn_L:0
dec(signed) INPUTS: A:-32750
dec(unsigned) INPUTS: A: 32786
                                                                        CarryOutEn_L:0
                                               B: 32770
                                                                        CarryOutEn L:0
Testing operation:
                        ADDU=00001 //A+B=>C
                                                  unsigned addition
              INPUTS: A:8012
                                                                        CarryOutEn L:0
                                                                        CarryOutEn_L:0
                                                                        CarryOutEn_L:0
                                               B: 32770
                                                                        CarryOutEn L:0
                                                                                                 OUTPUTS: C:
Testing operation:
                       SUB=00010 //A-B=>C signed subtraction
              INPUTS: A:8012
                                                                        CarryOutEn L:0
                                                                                                 OUTPUTS: C:0010
              INPUTS: A:1000000000010010
                                                                        CarryOutEn_L:0
                                                                        CarryOutEn_L:0
                                                                        CarryOutEn_L:0
                                                  unsigned subtraction
Testing operation:
                                                                                                 OUTPUTS: C: 00000000000010000
OUTPUTS: C: 16
              INPUTS: A:1000000000010010
INPUTS: A:-32750
                                                                        CarryOutEn_L:0
dec(signed)
                                                                        CarryOutEn L:0
                                                                        CarryOutEn_L:0
                         TNC=00100
                                     //A+1=>C
Testing operation:
                                                   signed increment
              INPUTS: A:8012
                                                                        CarryOutEn_L:0
                                                                        CarryOutEn_L:0
dec(signed)
              INPUTS: A:-32750
                                                                        CarryOutEn_L:0
                                                                                                 OUTPUTS: C:-32749
dec(unsigned) INPUTS: A: 32786
                                                                                                 OUTPUTS: C: 32787
                                               B: 32770
                                                                        CarryOutEn_L:0
Testing operation:
                       DEC=00101 //A-1=>C signed decrement
              INPUTS: A:8012
                                                                        CarryOutEn L:0
                                                                                                  OUTPUTS: C:100000000010001
                                                                         CarryOutEn_L:0
dec (unsigned) INPUTS: A: 32786
                                               B: 32770
                                                                        CarryOutEn_L:0
                                                                                                 OUTPUTS: C: 32785
```

## **ALU TB: Arithmetic Operations**

```
Testing operation: AND=01000 //A AND B
               INPUTS: A:8012
                                                                           CarryOutEn_L:0
dec(signed) INPUTS: A:-32750
dec(unsigned) INPUTS: A: 32786
                                                 B: 32770
                                                                           CarryOutEn L:0
                                                                                                                                         vout:0
Testing operation: OR =01001 //A OR B
               INPUTS: A:8012
                                                                                                     OUTPUTS: C:8012
                                                                           CarryOutEn L:0
                                                                           CarryOutEn_L:0
dec (unsigned) INPUTS: A: 32786
                                                 B: 32770
                                                                           CarryOutEn L:0
                                                                                                     OUTPUTS: C: 32786
Testing operation: XOR=01010 //A XOR B
               INPUTS: A:8012
                                                                           CarryOutEn L:0
                                                                           CarryOutEn L:0
dec(signed)
                                                                           CarryOutEn_L:0
                                                                           CarryOutEn_L:0
Testing operation: NOT=01100 //NOT A
               INPUTS: A:8012
                                                                                                     OUTPUTS: C:7fed
                                                                                                    OUTPUTS: C:011111111111101101
OUTPUTS: C: 32749
                                                                           CarryOutEn L:0
```

**ALU TB: Logic Operations** 

```
SLL=10000 //logic left shift A by the amount of B[3:0]
Testing operation:
              INPUTS: A:8012
                                                                                             OUTPUTS: C:0048
             INPUTS: A:1000000000010010
                                                                     CarryOutEn_L:0
                                                                     CarryOutEn_L:0
                                                                                             OUTPUTS: C:
                        SRL=10001 //logic right shift A by the amount of B[3:0]
Testing operation:
bin INPUTS: A:1000000000010010 dec(signed) INPUTS: A:-32750
                                                                     CarryOutEn_L:0
                                                                     CarryOutEn L:0
                                                                     CarryOutEn_L:0
Testing operation: SLA=10010 //arithmetic left shift A by the amount of B[3:0]
                                                                                             OUTPUTS: C:0048
             INPUTS: A:-32750
                                                                     CarryOutEn_L:0
                                                                                             OUTPUTS: C:
                                             B: 32770
                                                                     CarryOutEn_L:0
Testing operation:
                       SRA=10011 //arithmetic right shift A by the amount of B[3:0]
             INPUTS: A:8012
hex
                                                                     CarryOutEn L:0
dec(signed)
                                                                     CarryOutEn_L:0
                                                                                             OUTPUTS: C: 57348
                                             B: 32770
                                                                     CarryOutEn L:0
```

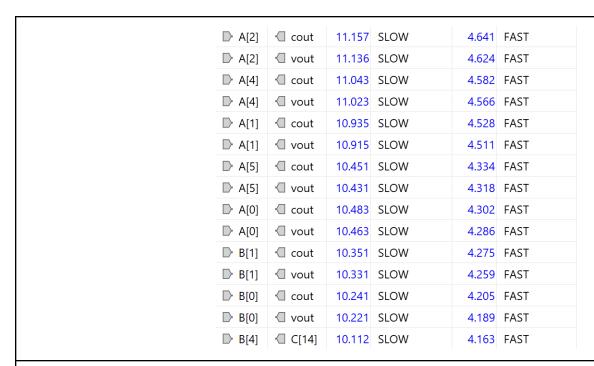
## **ALU TB: Shift Operations**

```
SLE=11000 //if A <= B then C(15:0) = <0...0001>
             INPUTS: A:8012
hex
                                                                    CarryOutEn L:0
                                                                    CarryOutEn_L:0
                                            B: 32770
                                                                    CarryOutEn L:0
                                                                                            OUTPUTS: C:
                        SLT=11001 //if A < B then C(15:0) = <0...0001>
Testing operation:
             INPUTS: A:8012
                                                                                            OUTPUTS: C:0000
                                                                    CarryOutEn_L:0
                                                                    CarryOutEn L:0
                                            B: 32770
                                                                    CarryOutEn_L:0
dec (unsigned) INPUTS: A: 32786
                                                                                            OUTPUTS: C:
                        SGE=11010 //if A >= B then C(15:0) = <0...0001>
Testing operation:
                                                                    CarryOutEn_L:0
dec(signed)
                                                                    CarryOutEn L:0
Testing operation:
                      SGT=11011 //if A > B then C(15:0) = <0...0001>
                                                                    CarryOutEn_L:0
dec(signed) INPUTS: A:-32750
                                                                                            OUTPUTS: C:
                                                                    CarryOutEn L:0
dec(unsigned) INPUTS: A: 32786
                                                                    CarryOutEn L:0
                       SEQ=11100 //if A = B then C(15:0) = <0...0001>
Testing operation:
             INPUTS: A:8012
                                                                    CarryOutEn L:0
                                                                    CarryOutEn_L:0
dec (unsigned) INPUTS: A: 32786
                                            B: 32770
                                                                    CarryOutEn_L:0
                                                                                            OUTPUTS: C:
Testing operation: SNE=11101 //if A != B then C(15:0) = <0...0001>
             INPUTS: A:8012
                                             B:8002
                                                                    CarryOutEn L:0
                                                                    CarryOutEn L:0
                                             B: 32770
                                                                    CarryOutEn_L:0
                                                                                            OUTPUTS: C:
```

**ALU TB: Set Condition Operations** 

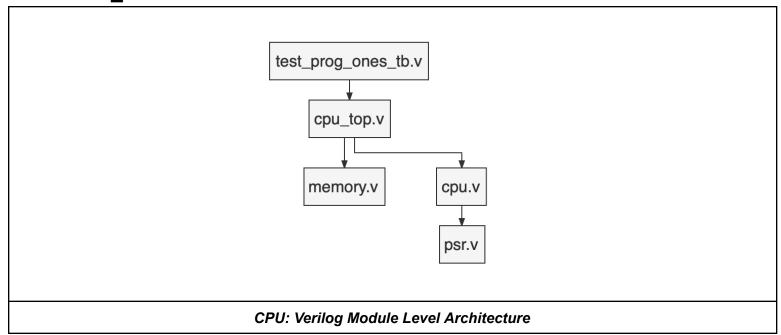
From Port	To Port	Max Delay	Max Process Corner	Min 1 Delay	Min Process Corner
□ B[4]		6.309	SLOW	2.620	FAST
□ B[5]	⟨□ C[11]	6.320	SLOW	2.620	FAST
□ B[6]	⟨□ C[11]	6.231	SLOW	2.591	FAST
□ B[7]	⟨□ C[11]	6.229	SLOW	2.590	FAST
	□ C[1]	6.076	SLOW	2.587	FAST
	□ C[1]	6.076	SLOW	2.587	FAST
	□ C[1]	6.076	SLOW	2.587	FAST
	□ C[1]	6.076	SLOW	2.587	FAST
□ B[4]		6.347	SLOW	2.584	FAST
□ B[5]		6.369	SLOW	2.583	FAST
□ B[4]		6.356	SLOW	2.575	FAST
□ B[5]		6.367	SLOW	2.575	FAST

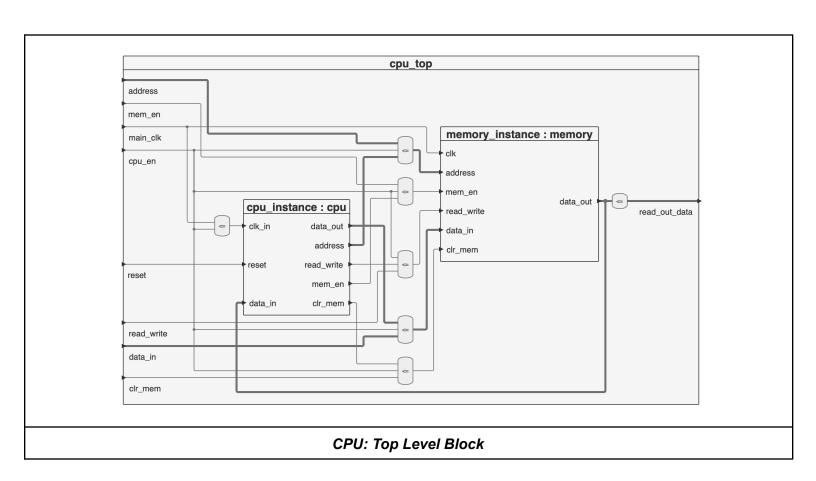
ALU Critical Path: B[4] to C[11] for behavioral addition (CLA), CLA is much faster

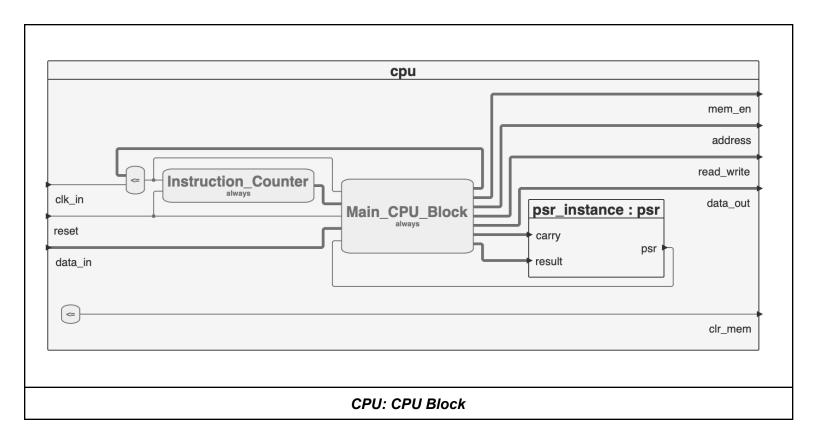


ALU Critical Path: A[2] to cout7 for behavioral addition (ripple carry adder)

# Lab Part 2\_ CPU:







CPU: N Complement Program Testbench

Assembly Program is commented in TB above

Successful result of program is stored back in MEM and read as output of TB

# Lab Part 3\_ OnesCounterCPU\_Program:

```
_____
PROGRAMING MODE
# PROGRAMING NUMBER OF ONES TEST PROGRAM...
# VALUES IN MEM:
 hX000 -> test_number
 hX001 -> 0
PROGRAM:
# ADRS -> INST, SRC, DEST
hX004 -> LD MEM0 REG0
# hX005 -> LD MEM1 REG2
hX006 -> SHF Left1 REG0
# hx007 -> branch no carry adrs 11
# hX008 -> ADD IMED 1 REG2
# hX009 -> ADD IMED 0 REG0
# hX00a -> BRANCH ZERO ADRS 12
hX00b -> BRANCH ALWAYS ADRS 6
# hX00c -> STR REG2 MEM1
# hX00d -> HLT
 RUNNING NUMBER OF ONES TEST PROGRAM...
 CHECKING MEMORY VALUE AT LOCATION 1, WHERE RESULT IS STORED
 NUMBER OF 1's IN 1010101010101010000100010001
 read out data in bin: 000000000000000000000000001100
 read_out_data in hex: 0000000c
 read out data in dec:
                             12
```

#### CPU: Ones Counter Program Testbench

Assembly Program is commented in TB above Successful result of program is stored back in MEM and read as output of TB

# Lab Part 4\_ MultiplierCPU\_Program:

```
PROGRAMING MODE
PROGRAMING MULTIPLICATION TEST PROGRAM...
VALUES IN MEM:
hX000 -> A VALUE = 0000000e
hX001 -> B VALUE = 0000000f
hX002 -> C INITIAL = 00000000
hX00f -> DECREMENT = ffffffff
ADRS -> INST SRC DEST
hX004 -> LD MEM0 REG0
hX005 -> LD MEM1 REG1
hX006 -> LD MEM2 REG2
hX007 -> LD MEMf REGf
hX008 -> ADD REG0 REG2
hX009 -> ADD REGF REG1
hX00a -> BRA ZERO ADRS00c
hX00b -> BRA POS ADRS008
hX00c -> STR REG2 MEM2
hX00d -> HLT
RUNNING MULTIPLICATION TEST PROGRAM...
*****************
CHECKING MEMORY VALUE AT LOCATION F3
MULTIPLIED 14 * 15, EXP RES: 210
read out data in bin: 00000000000000000000000011010010
read out data in hex:
                                  000000d2
read out data in dec:
                                     210
```

### CPU: Multiplication Program Testbench

Assembly Program is commented in TB above Successful result of program is stored back in MEM and read as output of TB