EECS 2021: Computer Organization
Winter 2019

Project (10%)
Simulation of RISC CPU using Verilog Hardware Design

Milestone 2 (5%)
Deadline: midnight Thursday, 28 March 2019
Upload your group's report in PDF or docx format to Moodle.
ONLY ONE report to be uploaded for each group.

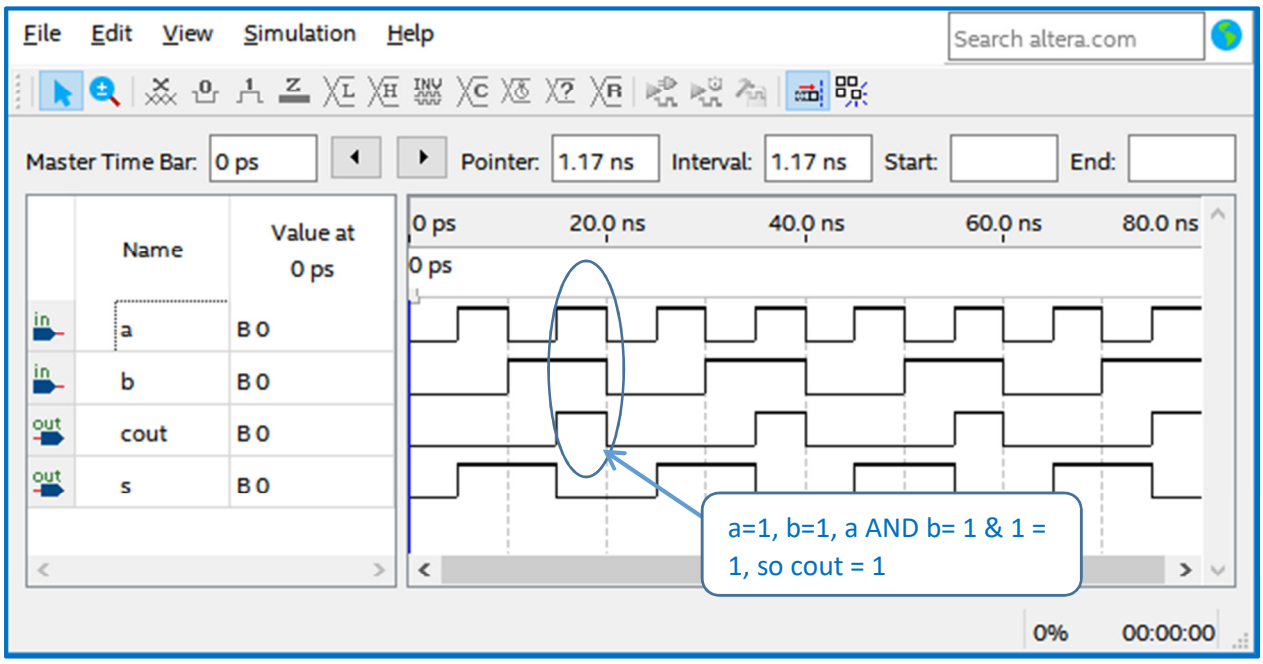
A. Read the RISC CPU Design Documentation

B. Based on the document and your Milestone 1 report, add the functionality of the RISC CPU by **one extra instruction**. Below are the instructions that you can choose from:
AND, JALR, ADDI, SRA, SRL, BNE, BGE, BLT, LUI, AUIPC

C. Edit your Milestone 1 report to include a section describing the design of your new instruction. **Please mention clearly**, which instruction your group is going to be implementing. Explain in detail, which modules you changed to include this new instruction. Describe why each change was needed and add any additional information (i.e. a table that shows the comparison of modules and i/o before and after the new instruction was added. Sample shown below:)

Before	After
5 parameters for ALU operations in control.v	6 parameters for ALU operation. The sixth one is shown here: *parameter ALUAND=5'b100000;*
No parameter for instruction AND in control.v	New parameter added in control.v *parameter AND=12'b100000000000;* Also as a result, we had to make all the other instructions' parameters become 12 bits in size.

D. Create a simulation waveform to show the functionality of your new instruction. Describe what values were initialized in which registers before you tested the instruction by using those registers as operands (i.e. Register x3 was initialized to 0x0F0F0F0F0F and x4 was set to 0xFF00FF00FF. Expected output for AND operation is 0x0F000F000F. The instruction used x5 as destination. Simulation diagram below shows content of x5. As can be seen, the value in x5 matches the correct expected result of AND operation. We have also added two other test case values to check that AND operation is being carried out correctly. Those two other cases are shown on the diagram itself with the operands and output described in the bubble.



(This is a sample only, your design does not use one-bit operands of course.)

E. Conclusion section: write what you learned from this project and this milestone.

F. Save only all your projects' Verilog and necessary text files (RAM, ROM etc.) along with your waveform (.vwf) files in a folder. Please do not send your whole Quartus project because it's huge in size. Add your new report (in .docx or .pdf format) and zip the folder. Your zipped folder name should be your group name and M2 or M1n2 to represent if you are submitting Milestone 2 only or Milestone 1 and 2 together. (i.e. mygroup_M2.zip or GroupZ_M1n2.zip). Upload to Moodle before deadline.

G. If you have any questions please ask on Moodle (after checking that someone else hasn't asked it already).