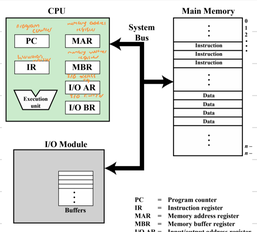
CPU & Bus

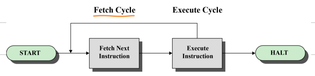
CPU

↳ instruction interpreter

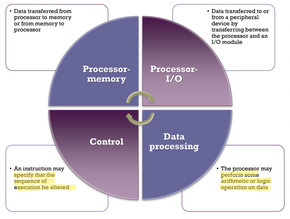
↳



↳



1. CPU fetch instruction from memory
2. Program counter hold the address to be fetched next
3. CPU increments the PC to fetch next instruction
4. Fetched ins. is loaded into IR
5. CPU interprets ins. and perform action



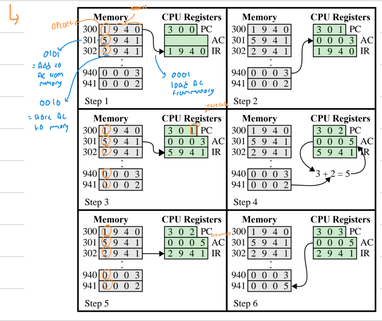
↳ Instruction

↳

(a) Instruction format

(b) Integer format

↳



↳ complex ↑, instruction count ↓

Interrupt

↳ 1. Program:-

resulted by ins. execution error

eg. divide by 0, etc...

2. Timer

perform cutain function on a schedule

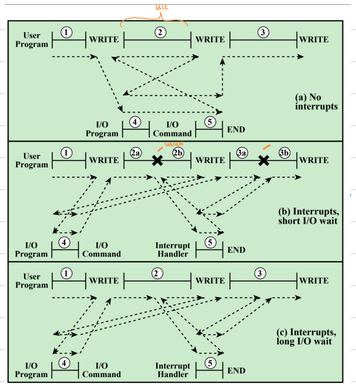
3. I/O

by I/O controller

4. Hardware Failure

Power failure / memory parity failure

↳



can do anything else

on program idle, can interrupt

on interrupt, program go idle

✖ = interrupt occurs during course of execution of user program

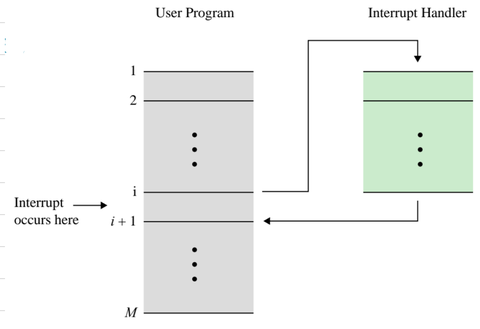
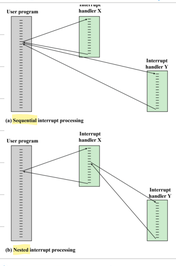


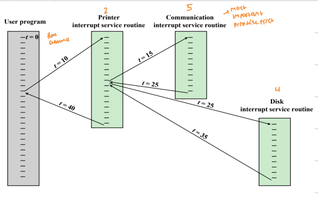
Figure 3.8 Transfer of Control via Interrupts

↳ Multiple Interrupts

↳ 1. Disable Interrupt



2. Define priorities



System Bus

↳ connects major components (processor, memory, I/O)

↳ 1. Data Lines

↳ Provide a path for moving data

↳ width of data bus

- Number of lines
- determine how many bits can be transferred
- key in determining overall system performance

2. Address Lines

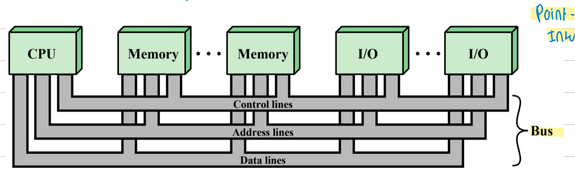
↳ designate the source / destination of data on the data bus

3. Control Lines

↳ control the access and the use of data and address line

↳ transmit command & timing info

(command: operations to be performed; timing: validity of data & address info.)



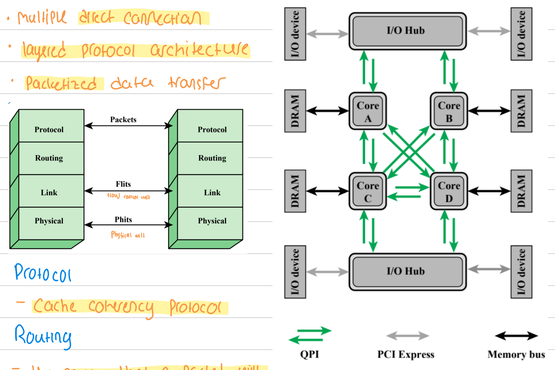
Point-to-Point Interconnect

↳ higher data rate, harder to sync

↳ QuickPath Interconnect (QPI)

↳ · multiple direct connection
- layered protocol architecture
- packetized data transfer

↳



Protocol

- Cache coherency protocol

Routing

- the route that a packet will traverse

Link

- flow control funct: QPI sender does not overwhelm receiver
- Error control funct: Detects & recover bit error

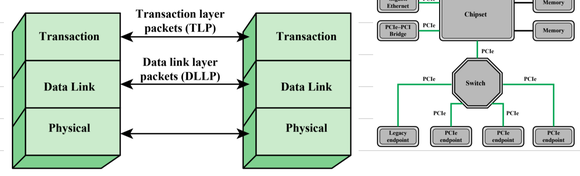
Physical

- transfer of data externally

↳ Peripheral Component Interconnect (PCI)

↳ · high bandwith, processor independent
- better performance for high speed I/O

↳



Transaction

- receive read & write request from software
- creates request packet for transmission to a destination via Data Link