Nathan Bellows

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Permanent Address
2132 Larry Dr. NE,
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Current Address
1406 Mayfield Dr. #102,
Ames IA, 50014

EDUCATION

Iowa State University — **Ames, Iowa**

Major: ***Bachelor of Science, Computer Engineering*** — **Expected Graduation- May 2022**

2nd Major: ***Bachelor of Arts, Music***

- GPA: 3.94

Linn-Mar High School — **Marion, Iowa**

- GPA: 4.00 — **Graduated May 2017**
- National Merit Finalist

TECHNICAL EXPERIENCE

Collins Aerospace – Cedar Rapids, IA

Software Engineering Intern (Remote) — **June 2020 – August 2020**

- Using C++ and Google Protocol Buffers, developed and tested significant features and plumbing for a software product with an upcoming release date.
- Provided live demonstrations and explanations of new features to the customer.
- Worked closely with the small development team to implement and combine features in parallel, using proper source control techniques (including CD/CI).
- Solved problems related to concurrency, portability and over-the-air data format, and client/server programming.
- Consulted datasheets and product contract to meet the expected product specifications and interface with proprietary hardware.
- Followed an AGILE-based planning system with weekly planning and daily status meetings.
- Gave and received code reviews for each feature pull request, catching breaking issues and providing areas for improvement.
- Combined Linux utilities and Docker containers to create an effective environment for remote development and testing of client/server software.

IDx Technologies *(Digital Diagnostics Inc.)* – Coralville, IA

R&D Engineering Intern — **June 2019 – August 2019**

- Developed for a real-product C++ codebase, involving the implementation of Convolutional Neural Networks and real-time image processing tasks.
- Refactored existing (C++) code for significant improvements to performance, readability, and maintainability. Implemented improved software design patterns.
  - Decreased benchmark memory usage by over 30 percent.
  - Decreased benchmark run time (increased speed) by over 10 percent.
  - Implemented multithreaded concurrency algorithms for potential performance gain in future networks.
- Implemented extensive, yet maintainable unit tests for near-complete test coverage.
- Engaged in frequent code reviews with other engineers to get feedback and make improvements.

TECHNICAL EXPERIENCE *(CONTINUED)*

Iowa State University Department of Engineering – Ames, IA

Teaching Assistant – CPRE 281: Digital Logic **August 2019 – December 2019**

- Gave weekly recitation for digital logic design course to full section of engineering students. Subject matter included Boolean logic and logic optimization, state machines, basic computer architecture, and Verilog programming of Altera Cyclone FPGAs.
- Provided one-on-one student assistance for completing lab assignments.
- Graded lab reports and exams.

Languages & Tools

- C++, C, VHDL, Verilog, Java, Java Spring framework, Bash, Tcl, OpenGL+GLSL, some Python
- Visual Studio, VS Code, Vim, Android Studio, Eclipse, IntelliJ IDEA, Code Composer Studio, Xilinx Vivado, ModelSim, Altera Quartus, MATLAB+Simulink, PSpice
- Git, GCC/Clang/MSVC/ld, Make/CMake/Ninja, various Linux utilities, WSL, Google Protobufs

Personal Projects

- Developed a C physics and effects engine to model and display ASCII effects such as fireworks.
- Created an automated bot moderator for Discord (online group communications service) in Java.
- Developed a string-conversion library in C++, involving several advanced C++ concepts such as templates and compile-time metaprogramming.
- Implemented various C++/Java library utilities to implement interesting algorithms and design patterns.

TECHNICAL COURSEWORK PROJECTS

Computer Engineering / Computer Science

- CPRE 480: Graphics Processing and Architecture
  - Used VHDL and Xilinx IP to design an implementation of significant portions of the OpenGL rendering pipeline in hardware, including programmable vertex/fragment shader processors, viewport transformation, primitive assembly, rasterization, and rendering. Developed a driver in C to manage OpenGL state and render the graphics on the hardware implementation. Ran the graphics processor on a Xilinx Artix-7 FPGA from a remote Linux machine and observed the output on a connected monitor. Explored architecture decisions for performance, robustness, debuggability, and FPGA timing closure.
- CPRE 381: Computer Organization and Assembly Level Programming
  - Designed a MIPS CPU with VHDL, supporting most of the core ISA. Implemented the CPU both in a single-cycle design and a pipelined design with proper forwarding and hazard detection. Verified behavior in ModelSim simulations.
- COMS 309: Software Development Practices
  - Developed an Android client and a Spring server (with MySQL database) for a simple online multiplayer game application. Made extensive use of Git source control with Gitlab Continuous Integration services. Implemented unit tests with the Mockito mocking framework.
- CPRE 288: Embedded Systems
  - Programmed TI TM4C microcontroller to control a Roomba robot and other peripheral devices, including UART, PWM, and LCD modules. Interpreted real-world sensor data to develop fully autonomous navigation and environment plotting.
- CPRE 281: Digital Logic
  - Designed CPU functional blocks (ALU, register file, Booth multiplier, etc.) with block diagrams and Verilog HDL. Tested on Altera Cyclone FPGAs.