A Study of MESI and MOESI Coherence Protocol

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ABSTRACT

The project is conducted to understand the influence of MESI and MOESI coherence protocols on cache misses in a multicore systems with two different L2 cache sizes. The study also analyzed the coherence bus transactions.

Keywords

MESI; MOESI

1. INTRODUCTION

As part of this project, we have looked into the influence of MESI and MOESI coherence protocols on cache misses and bus transactions in a multicore systems with different L2 cache sizes. The MESI and MOESI are invalidation based coherence protocols. The letters corresponds to Modified(M), Exclusive(E), Shared(S), Invalid(I) and Owned(O) states of cache lines.

Results are collected using PARSEC 3.0 workloads bodytrack, streamcluster, and vips. Bodytrack is a computer vision application which tracks a human body with multiple cameras through an image sequence. Streamcluster solves the online clustering problem. It uses data mining algorithms and used to study problems with streaming characteristics. Vips is based on the VASARI Image Processing System (VIPS).The benchmark includes fundamental image operations such as an affine transformation and a convolution[].

2. IMPLEMENTATION DETAILS

The MESI and MOESI simulator implements 3 level cache hierarchy with private L1 and L2 and shared LLC. We have used 2 cache configurations for this project as mentioned in Table 1. The cache hierarchy is inclusive with L1, L2 implemented as write-through and L2, LLC implemented as write-back. LRU is used as replacement policy at all cache levels.

In our simulation we have considered a miss as a coherence miss, The coherence misses we report are upper bound on actual coherence misses. This is because, if the block was evicted due to coherence invalidation and later same block is accessed. But in reality some of the blocks which contributed to these coherence miss(which we have counted as coherence misses) will be removed due to following two conditions,

- Too many lru evictions from l2 may evict the block before the actual coherence miss happens.
- Due to eviction of block from llc before the actual coherence miss happens in L2 cache.

PARSEC 3.0 workloads are run with input **simsmall**. Traces for these workloads are collected using PIN 3.6. Count of thread level memory access with overall read, write access for each workload is mentioned in Table 2 and Table 3

Table 1: Cache configurations

configurations	L1-Size	L2-Size	LLC-Size
config-1	32KB	256 KB	2048 KB
config-2	32 KB	512 KB	4096 KB

Table 2: PARSEC Workload Details

Thread_id	Bodytrack	Streamcluster	Vips
0	27189557	4985294	42205508
1	64958204	150909953	3487
2	63970965	150405402	2064
3	64292931	150291974	478475939
4	64623565	150048013	460917338
5	8290150	2516	0
6	0	1781	0
7	0	1692	0

Table 3: PARSEC Workload Details

Type	Bodytrack	Streamcluster	Vips
Reads	235631138	590338760	752956923
Writes	57694234	16307865	228647413
Total	293325372	606646625	981604336

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3. RESULTS

3.1 Cache and Coherence Misses

3.1.1 Bodytrack

Table 4 and Table 5 show cache and coherence misses for Bodytrack workload for configurations config-1 and config-2 in Table 1 respectively.

We can see from Table 4 that the variation in cache misses between MESI and MOESI is less than 1% for L1 and between 20 - 35 % for L2(for core 1 to 4). Coherence misses are reduced from MESI to MOESI.

We can also see from Table 5 that the variation in cache misses for L1 and L2 have come down significantly with increase in cache size, now the cache miss variation is between 2% - 5% for L2 (for core 1 to 4) as compared to 20 - 35 % in previous case. The coherence misses are increased from MESI to MOESI in almost all cores.

3.1.2 Streamcluster

Table 6 and Table 7 show cache and coherence misses for streamcluster workload for config-1 and config-2 in Table 1 respectively.

We can see from Table 6 and 7 that the variation in L1 and L2 cache misses between MESI and MOESI is less than 1% for most of the cores. Apart from this, the coherence misses are increased from MESI to MOESI for majority of cores in both config-1 and config-2. This may be due to the streaming characteristics of workload.

3.1.3 Vips

Table 8 and Table 9 show cache and coherence misses for vips workload for cache configurations config-1 and config-2 in Table 1 respectively.

We can see from Table 8 and 9 that the L2 misses are decreased from MESI to MOESI for cores 3,4 for config-1 but increased for config-2. This says, for vips, bigger L2 cache size with MOESI is not benefiting. Coherence misses are also increased from MESI to MOESI for core-3,4 for both cache configurations.

3.2 Bus transactions

As part of this task, we have collected number of state transitions in MESI and MOESI which flush data into the bus. The aim is to understand the impact of MESI and MOESI on bus bandwidth with different cache sizes. Results are collected for 2 cache configurations as mentioned in Table 1.

3.2.1 Bodytrack

Table 10 and 11 gives number of state transitions that flush data into bus for Bodytrack workload. For config-1, The number of bus transitions corresponding to M->I, E->I and S->I have decreased for all cores from MESI to MOESI.

For config-2, the number of M->I transitions are increased from MESI to MOESI. The number of other E->I and S->I have decreased same as config-1.

3.2.2 Streamcluster

Table 12 and 13 gives number of state transitions that flush data into bus for Streamcluster workload. Same as Bodytrack, the trend of decrease in number of bus transitions corresponding to M->I, E->I and S->I can be observed from MESI to MOESI.

3.2.3 Vips

Table 14 and 15 gives number of state transitions that flush data into bus for Vips workload. Same as Bodytrack and Streamcluster, the trend of decrease in number of bus transitions corresponding to M->I, E->I and S->I can be observed from MESI to MOESI.

The trend of decrease in number of sharers in MOESI can be inferred from decrease in S->I transitions for all workloads.

3.3 LLC Hits and Misses

Graphs in table 22 give details on comparison of llc accesses, hits and misses for MESI and MOESI. The llc accesses and hits are less for MOESI, but llc misses are more in MOESI than MESI.

The reason for less LLC accesses in MOESI is due to O state, many L2 misses are satisfied by L2 cache of adjacent cores with out going to LLC.

The reason for increase in LLC misses may be because, in MOESI, the probability of a block to be new is very high if it can not be found in any of the L2 caches. If the block was an old block, then it would have present in any of the other L2 cache. So such new blocks suffers a miss in LLC cache as well.

4. CONCLUSIONS

As part of this project we have studies the influence of MESI and MOESI coherence protocols on cache misses in a multicore systems with two different L2 cache sizes.

The results show that, cache and coherence misses are influenced by cache size with sometimes counterintuitive findings like that the L2 misses are increased from MESI to MOESI with increase in cache size. In general, Hits and miss count of l1 and l2 remain more or less equal. Real advantage of MOESI comes from the O state which makes the transfer of data possible within different l2 itself. MOESI will also decrease the bandwidth requirements of llc.

Table 4: Cache Misses(Bodytrack-config-1)

core_id	L1(MESI)	L1(MEOSI)	L2(MESI)	L2(MEOSI)	Coherence_Misses(MESI)	Coherence_Misses(MOESI)
Core-0	375355	375436	351853	352460	11040	9703
Core-1	2297171	2296657	143752	113333	18489	18479
Core-2	2245459	2244903	109230	78653	13499	13211
Core-3	2254306	2253935	113673	77924	13022	12664
Core-4	2279153	2278491	116466	79114	14282	13848
Core-5	139990	139990	118618	118656	26	27

Table 5: Cache Misses(Bodytrack-config-2)

core_id	L1(MESI)	L1(MEOSI)	L2(MESI)	L2(MEOSI)	Coherence_Misses(MESI)	Coherence_Misses(MOESI)
Core-0	374584	374607	218632	223430	13501	13492
Core-1	2296343	2296341	80046	76315	31758	33354
Core-2	2244772	2244768	57732	56563	26094	28062
Core-3	2253799	2253802	55904	54708	25473	26610
Core-4	2278338	2278343	57252	55934	27390	28375
Core-5	139384	139384	76681	76707	31	31

Table 6: Cache Misses(Streamcluster-config-1)

core_id	L1(MESI)	L1(MEOSI)	L2(MESI)	L2(MEOSI)	Coherence_Misses(MESI)	Coherence_Misses(MOESI)
Core-0	47286	47280	38260	38257	2129	2129
Core-1	5298931	5298552	1953286	1949866	575103	575381
Core-2	5257911	5257883	1965266	1961581	584356	584153
Core-3	5237123	5234548	1965028	1811414	581484	581498
Core-4	5263575	5264359	2032093	2010790	579036	579801
Core-5	101	101	101	101	30	30
core-6	92	92	92	92	21	26
core-7	85	85	85	85	21	21

Table 7: Cache Misses(Streamcluster-config-2)

core_id	L1(MESI)	L1(MEOSI)	L2(MESI)	L2(MEOSI)	Coherence_Misses(MESI)	Coherence_Misses(MOESI)
Core-0	47229	47226	31251	31430	2129	2129
Core-1	5295371	5294125	644638	587479	577037	577050
Core-2	5254166	5254166	602791	592417	584512	584512
Core-3	5231544	5231544	590051	589953	582115	582117
Core-4	5260862	5260862	588259	588098	580185	580184
Core-5	101	101	101	101	30	30
core-6	92	92	92	92	26	26
core-7	85	85	85	85	21	21

Table 8: Cache Misses(Vips-config-1)

core_id	L1(MESI)	L1(MEOSI)	L2(MESI)	L2(MEOSI)	Coherence_Misses(MESI)	Coherence_Misses(MOESI)
Core-0	843378	844883	829437	831220	4396	3281
Core-1	306	361	306	361	25	19
Core-2	387	439	387	439	88	69
Core-3	8917095	8917087	4272449	4237591	5437	5734
Core-4	8559426	8559356	4099845	4074638	5406	5772

Table 9: Cache Misses(Vips-config-2)

core_id	L1(MESI)	L1(MEOSI)	L2(MESI)	L2(MEOSI)	Coherence_Misses(MESI)	Coherence_Misses(MOESI)
Core-0	841793	842029	825960	825902	4432	4331
Core-1	271	315	271	315	63	25
Core-2	342	395	342	395	125	88
Core-3	8915919	8915941	4022820	4024829	7557	7726
Core-4	8558362	8558386	3870191	3870364	7600	7828

Table 10: No of transitions which Flush data into bus(Bodytrack-config-1)

core_id	M->I(MESI)	M->I(MEOSI)	E->I(MESI)	E->I(MEOSI)	S->I(MESI)	S->I(MEOSI)	M->S(MESI)	M->O(MEOSI)	O->I(MEOSI)
Core-0	291	284	3364	2591	9154	4899	9717	10521	3656
Core-1	21336	21545	101	81	4874	2273	5346	4809	2070
Core-2	4931	4927	215	152	10187	6443	11435	11197	3223
Core-3	5715	5681	402	357	8336	4603	12756	12720	3246
Core-4	5657	5644	235	216	9931	5709	10473	10357	3600
Core-5	21	20	3	0	72	10	1932	53	26

Table 11: No transitions which Flush data into bus(Bodytrack-config-2)

core_id	M->I(MESI)	M->I(MEOSI)	E->I(MESI)	E->I(MEOSI)	S->I(MESI)	S->I(MEOSI)	M->S(MESI)	M->O(MEOSI)	O->I(MEOSI)
Core-0	609	581	351	7	16712	10930	16338	16427	6238
Core-1	33986	34280	119	41	17414	9518	17261	18941	10135
Core-2	5704	5828	189	76	28155	15855	17484	18177	15024
Core-3	6757	6887	47	12	26378	13867	18557	19237	14376
Core-4	6804	6828	213	20	27956	15613	16378	17107	14209
Core-5	27	26	3	3	74	20	3977	4003	44

Table 12: No of transitions which Flush data into bus(Streamcluster-config-1)

core_id	M->I(MESI)	M->I(MEOSI)	E->I(MESI)	E->I(MEOSI)	S->I(MESI)	S->I(MEOSI)	M->S(MESI)	M->O(MEOSI)	O->I(MEOSI)
Core-0	51	51	1	1	2104	7	3803	3814	2097
Core-1	31724	31732	7	6	544185	76669	497131	497134	467769
Core-2	33067	33068	2	2	551397	83667	494673	494461	467531
Core-3	32903	32902	2	2	548700	82743	492809	492821	465971
Core-4	31822	31821	1	2	547331	82710	490146	490419	465389
Core-5	10	10	0	0	36	20	20	20	16
Core-6	7	7	0	0	36	20	18	18	16
Core-7	2	2	0	0	35	19	19	19	16

Table 13: No of transitions which Flush data into bus(Streamcluster-config-2)

core_id	M->I(MESI)	M->I(MEOSI)	E->I(MESI)	E->I(MEOSI)	S->I(MESI)	S->I(MEOSI)	M->S(MESI)	M->O(MEOSI)	O->I(MEOSI)
Core-0	51	51	1	0	2104	7	7898	7899	2097
Core-1	32090	32089	2	0	546551	78199	498055	498053	468383
Core-2	33074	33073	0	0	551583	83602	495371	495361	467982
Core-3	32908	32907	1	0	549351	83174	493389	493375	466183
Core-4	31826	31824	0	0	548509	82643	491269	491252	465868
Core-5	10	10	0	0	36	20	20	20	16
Core-6	7	7	0	0	36	20	18	18	16
Core-7	2	2	0	0	35	19	19	19	16

Table 14: No of transitions which Flush data into bus(Vips-config-1)

core_id	M->I(MESI)	M->I(MEOSI)	E->I(MESI)	E->I(MEOSI)	S->I(MESI)	S->I(MEOSI)	M->S(MESI)	M->O(MEOSI)	O->I(MEOSI)
Core-0	54	44	100	76	4813	2629	1590	984	913
Core-1	1	1	1	0	43	11	30	23	19
Core-2	27	22	29	26	166	73	67	60	46
Core-3	4046	4457	159	169	2337	657	4357	4388	1698
Core-4	4026	4488	808	809	2197	503	4395	4448	1743

Table 15: No of transitions which Flush data into bus(Vips-config-2)

core_id	M->I(MESI)	M->I(MEOSI)	E->I(MESI)	E->I(MEOSI)	S->I(MESI)	S->I(MEOSI)	M->S(MESI)	M->O(MEOSI)	O->I(MEOSI)
Core-0	57	54	105	97	4866	3301	1680	1514	1457
Core-1	1	1	0	1	85	17	60	30	26
Core-2	31	27	30	29	201	103	93	67	63
Core-3	6268	6431	152	149	2720	785	4732	4728	1955
Core-4	6479	6748	818	821	2582	551	4806	4815	2029

Column-1	Column-2
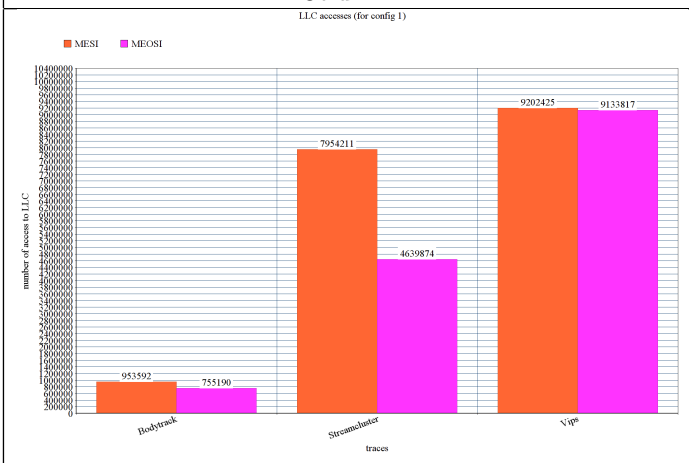	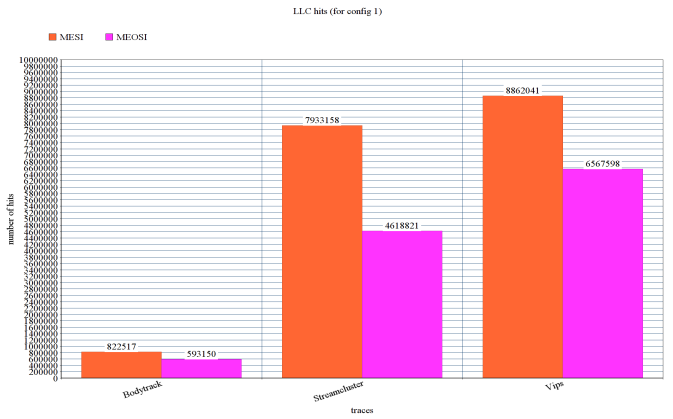
Table 16: Accesses-config-1	**Table 17: Hits-config-1**
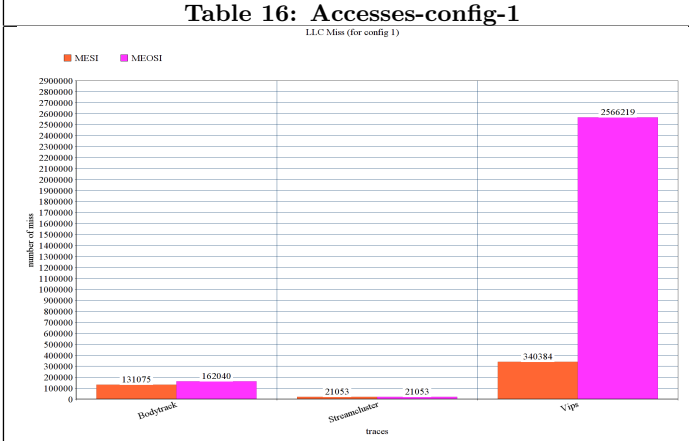	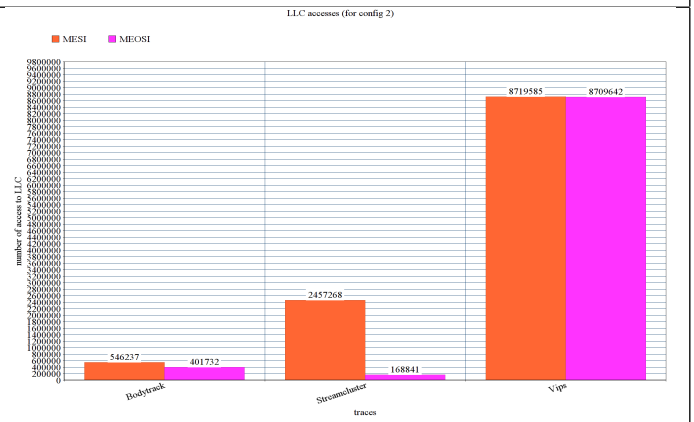
Table 18: Misses-config-1	**Table 19: Accesses-config-2**
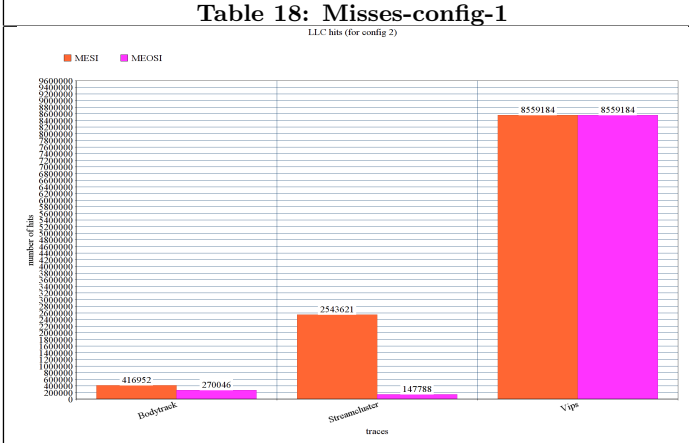	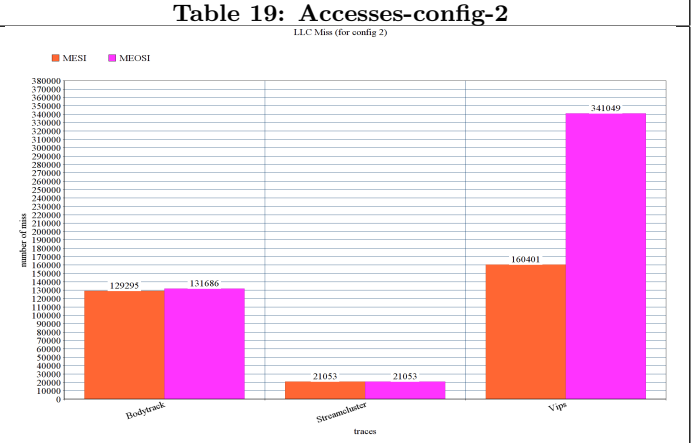
Table 20: Hits-config-2	**Table 21: Misses-config-2**

Table 22: LLC Details