

Ho Chi Minh City University of Technology
Faculty of Computer Science and Engineering



Lab Report

Logic Design with HDL

Assignment: Digital Clock

Authors:

Tạ Ngọc Nam

Vũ Nam Bình

Hồ Anh Dũng

Student's ID:

2152788

2152441

2052921

Instructors:

Dr. Pham Quoc Cuong

Completion date: 20th August, 2022

Contents

I. Introduction.....	3
1. Overview of the project	3
2. Equipments	3
II. Design	6
1. Block diagram	6
III. Implementation	7
IV. Inclusion	8
1. Completed work.....	8
2. Unfinished work.....	9
3. Future plan for the product	9
4. Working table	9
5. Source code and demo video.	10
6. References	10

I. Introduction

1. Overview of the project

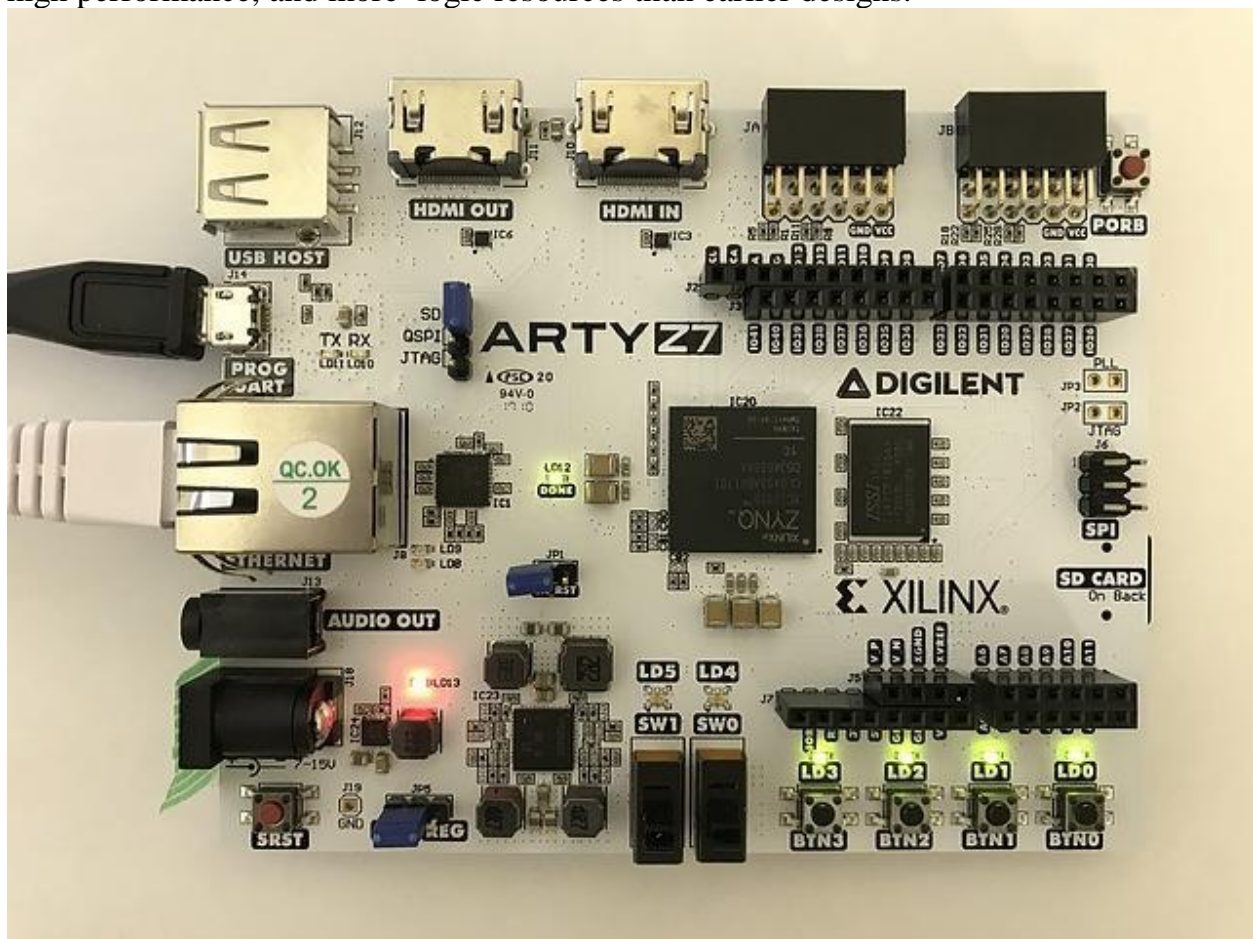
It has been widely used in industry thanks to the ongoing developments in science and technology, particularly in the electronics sector. Modern control techniques have many advantages over the use of control circuits assembled with discrete components in the field of control and automation, including small size, low cost, reliable working, and low power consumption.

Today, it is widely used in the field of control in appliances and products that support people's daily activities, such as washing machines, alarm clocks, etc., making our lives more streamlined and comfortable. Therefore, we have chosen the topic "Designing a perpetual calendar clock circuit with FPGA Arty Z7" to complete a big assignment in Logic Design with HDL, as well as to satisfy the desire to learn and make a specific electronic product.

2. Equipments

➤ FPGA Arty Z7 Board

The Arty Z7 FPGA is optimized for high performance logic, and offers more capacity, high performance, and more logic resources than earlier designs.



Key Features:

- Available shield I/O: 49
- Clock management tiles: 4
- Block RAM: 630 KB
- Flip-flops: 106,400
- Processor: Dual ARM Cortex A9
- 1 MSPS On-chip ADC
- FPGA Part: XC7Z020-1CLG400C
- Two standard Pmod ports: 16 Total FPGA I/O

The Arty Z7 board includes two tri-color LEDs, 2 switches, 4 push buttons, and 4 individual LEDs as shown in Figure 2.1. The push buttons and slide switches are connected to the Zynq PL via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a push button or slide switch was inadvertently defined as an output).

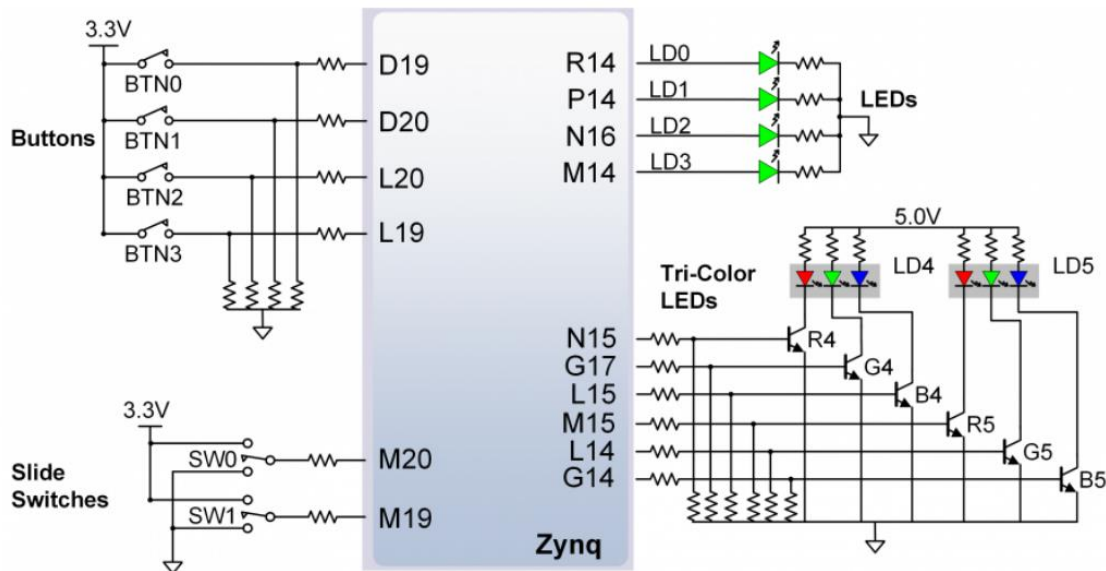
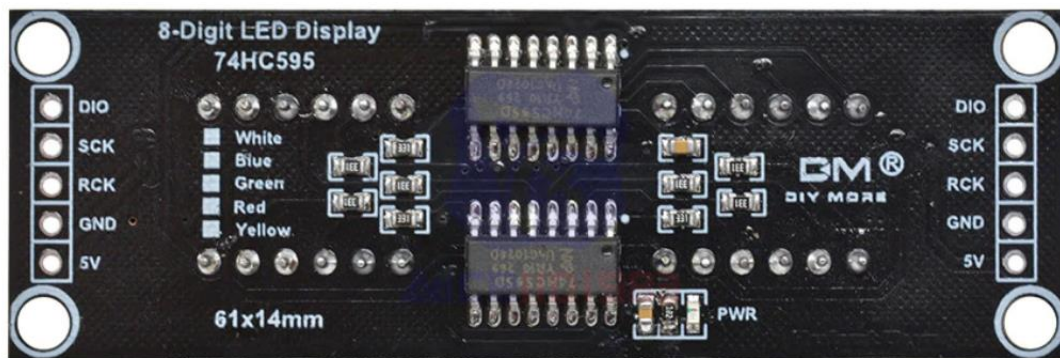
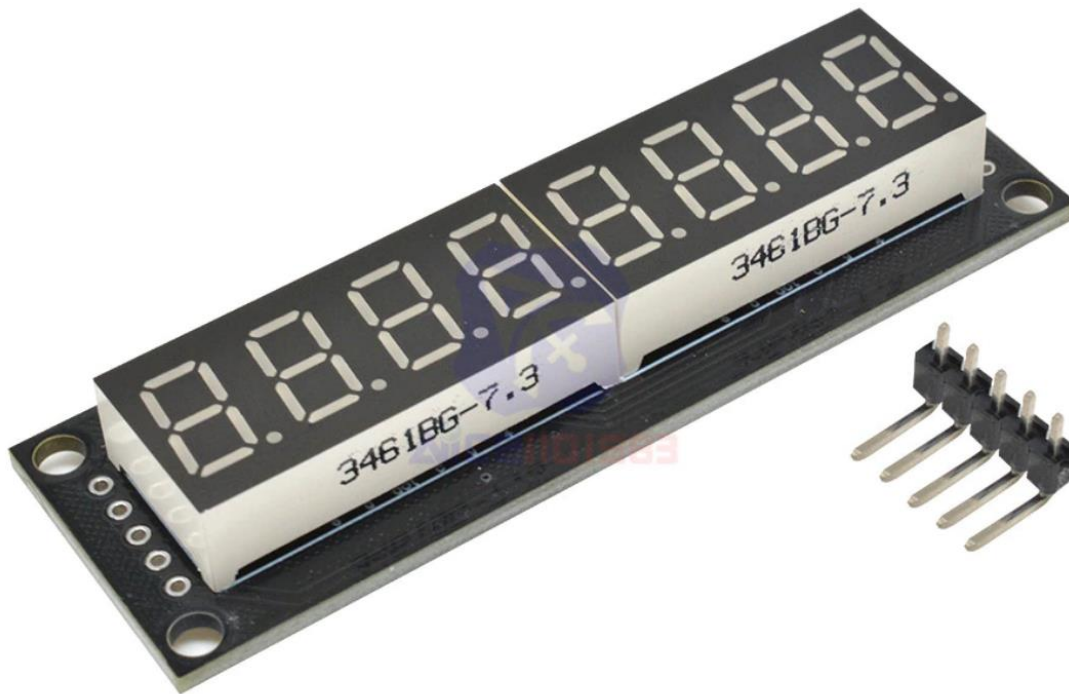


Figure 2.1

➤ **8 Bit 7 Segment LED Digital Display Tube 74HC595**



- **HIGH PERFORMANCE 74HC595 Driver Module:** This digital display tube adopts 74HC595 driver module, connects to digital IO via 3 pins, has stable performance.
- **8 BIT 7 SEGMENT DECIMAL:** This digital display tube has 8 bit and 7 segments, each digit has a decimal point, all points can be controlled individually.
- **GREEN LIGHT DISPLAY:** The LED digital display module contains 8 green LED word tubes, displaying the number clearly.
- **EASY USAGE:** The LED display digital tube is plug and play, no tedious wiring process is required, easy to connect and use.

- **PRECISE WIRING:** The digital display tube is produced with high quality PCB board, with accurate wiring and clear board path, and equipped with pin header, convenient and reliable.

II. Design

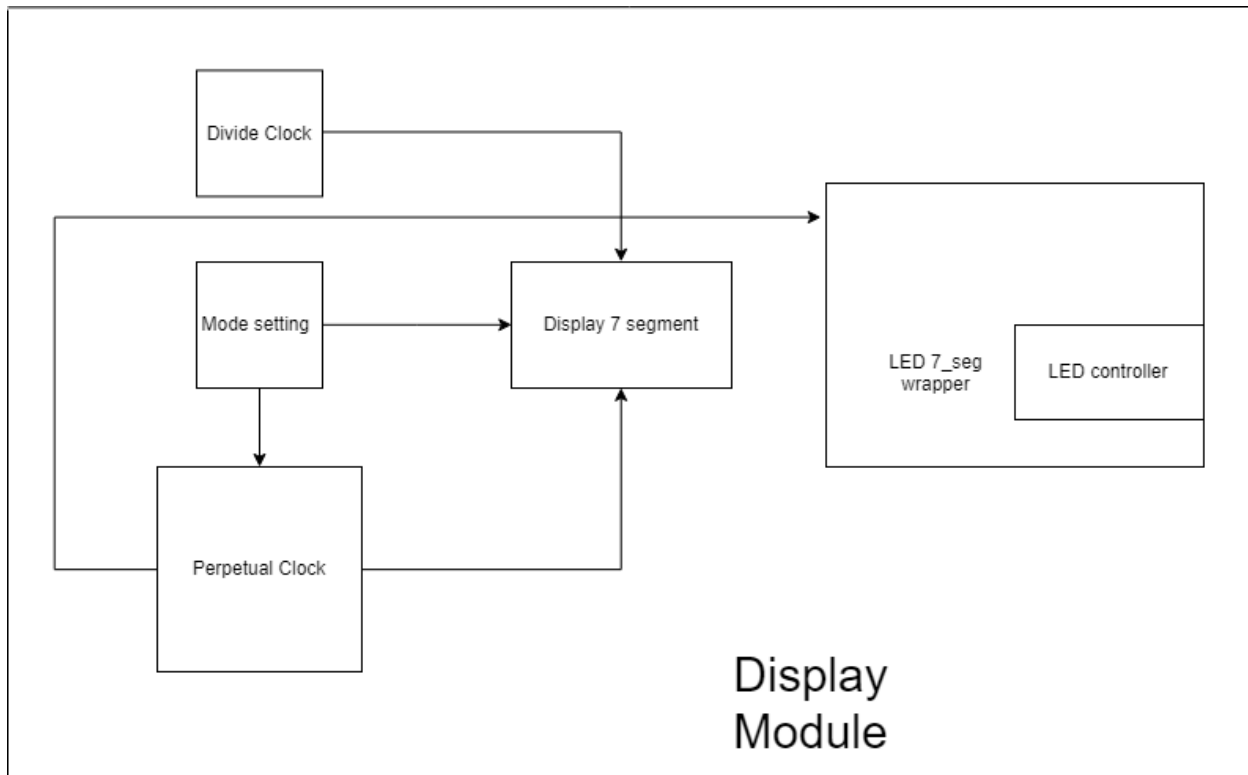
We implemented the digital clock that displays time in hours, minutes and seconds blinks in between the hour and minute display. The objective of our project is to implement all the basic functions of the digital clock which we find in our daily life routine.

List of the features implemented:

- Display hours, minutes, seconds on 7-segment LED.
- User can press button to switch to display day, month, year within certain seconds
- Allow the user to set default display mode (hour/date).

1. Block diagram

System design consists of a Top down approach. This system mainly performs functions Display the digital clock. These functions are implemented using divide clock, mode setting, LED module and display module.

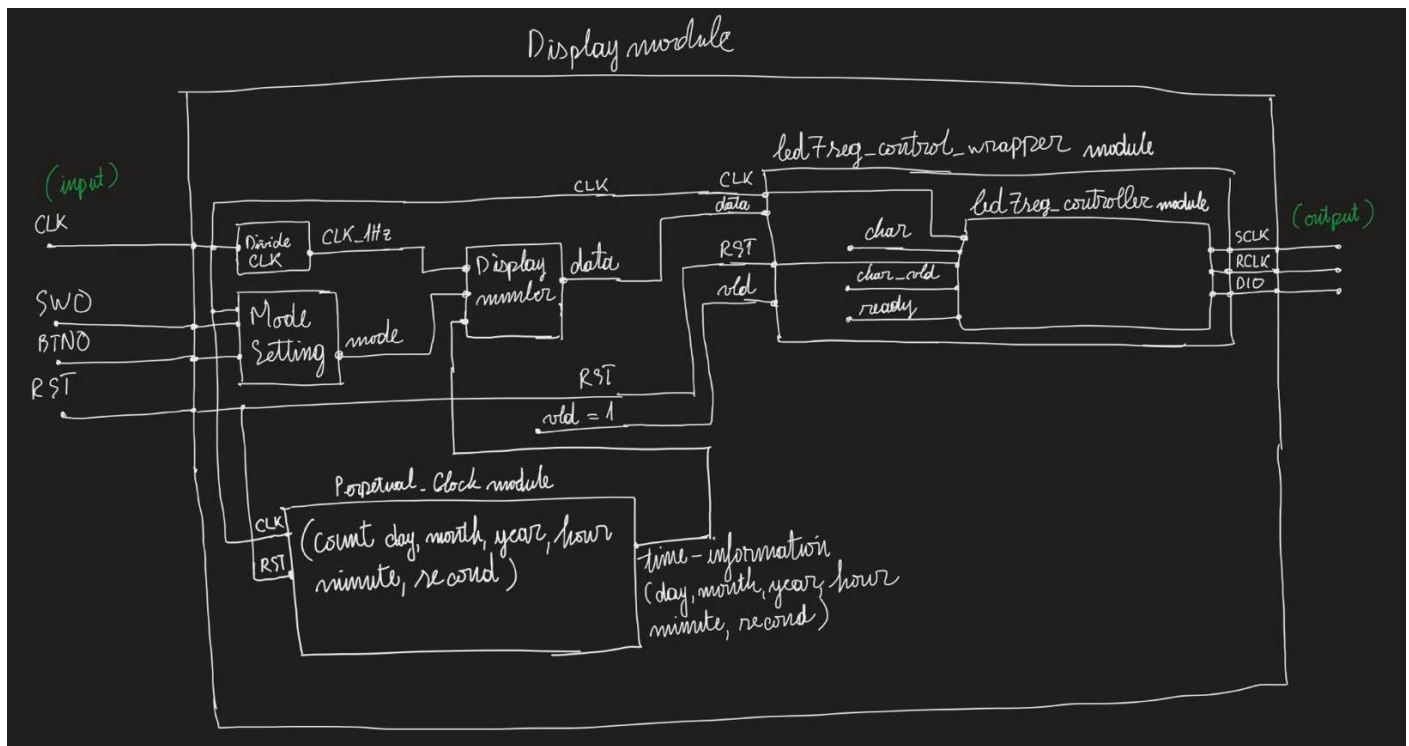


Block description:

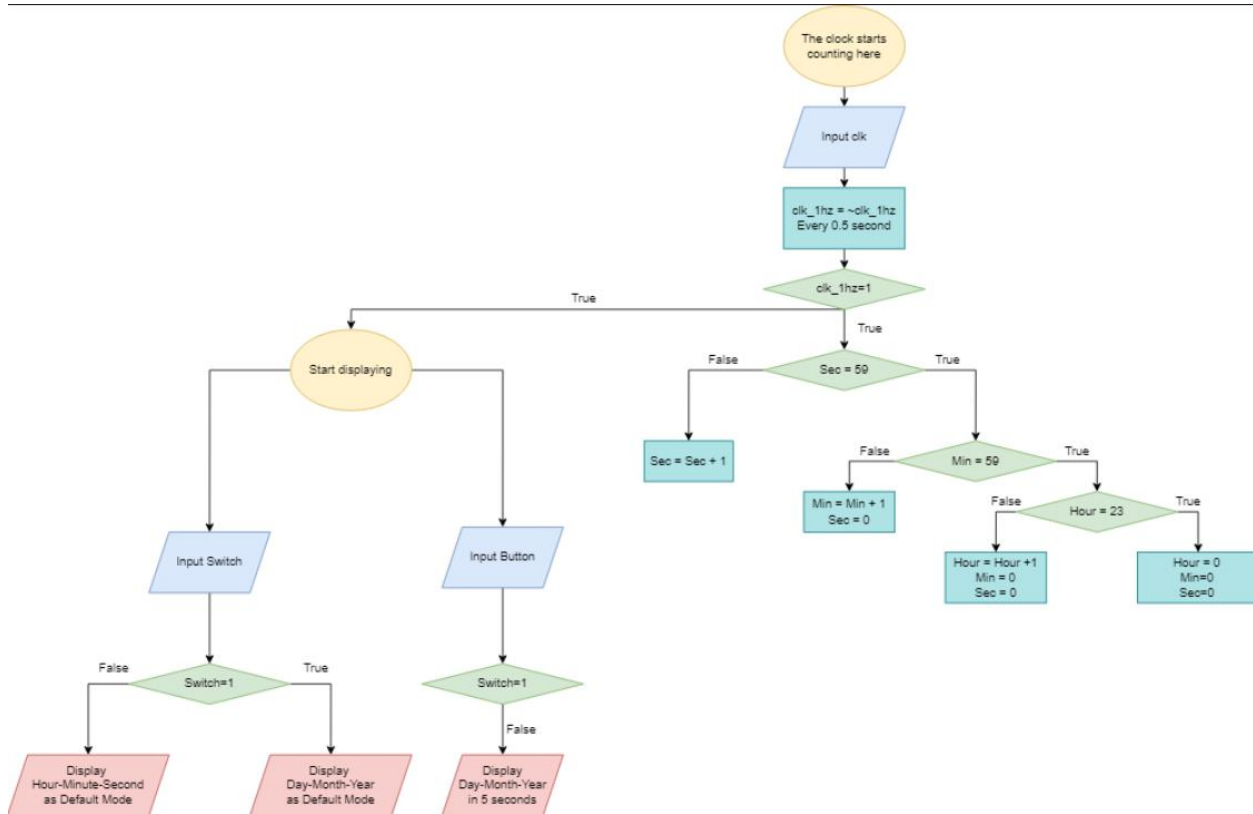
1. Divide clock:
It receives 50MHz and transfers to 1Hz (1 second).
2. Mode setting
This block provides two factors by using Button and Switch for the user to set up a wanted mode for the clock.
3. Perpetual clock module
It provides the ability to count day, month, year, hour, minute, second and send the signal to a led block to generate the exact result for the request.
4. LED 7_seg wrapper
The display module is executing a count. Four common anode seven segment displays are used for display purposes. For every one millisecond each display will get refreshed with the help of a multiplexer.

III. Implementation

After making an initial preparation for the digital clock, we started to implement the project by finishing a detailed block diagram and developing each function in order.



Block diagram for Digital clock



Flow chart of system processing

IV. Inclusion

1. Completed work

In general, the finished product has achieved the set design requirements:

- The Perpetual Calendar Clock counts the time accurately. The product is simple, lightweight and easy to use. The product uses civil current and is suitable for fixed placement.
- There are functions to display hours, minutes, day - day - month - year. By pressing the button BTN0, the LEDs display day/month/year in 5s and then turn back to hour/minute/second (the button is only affected if the LEDs are displaying hour/minute/second. This clock also provides two default mode displays: day/month/year and hour/minute/second. When switch SW0 is flipped to HIGH, it displays day/month/year; and when the switch is at LOW, it displays hour/minute/second.
- In addition to applying the knowledge learned in the processing subject, we also got acquainted and practiced with the Arty Z7 FPGA. These are the basic knowledge, serving the future of electronics. We were introduced to and used Vivado simulation software as it is a very important skill in the learning process. We can practice and apply the knowledge

we have learned to design a complete product with the logical and professional design process.

2. Unfinished work

In addition to the functions that have been achieved, the project has the following limitations:

- The circuit may not please the aesthetic for some personal evaluations.
- Do not have a variety of features such as setting other time zones, setting alarms, setting timers.

3. Future plan for the product

The topic can be developed into a multi-function clock by adding some features below:

- Adding the display of the lunar calendar
- Showing the temperature of the environment
- Setting up an alarm system with a short sound or favorite song.

4. Working table

Content	Mission	Members
Research for project	Determine the assignment, required design of the Digital clock	Ho Anh Dung, Vu Nam Binh, Ta Ngoc Nam
	Collect equipments and tools for project	Ho Anh Dung
	Assign work and make detailed plan	Ho Anh Dung, Vu Nam Binh, Ta Ngoc Nam
Design the system	Design the block diagram	Vu Nam Binh
	Design detailed function blocks	Vu Nam Binh, Ta Ngoc Nam
	Create initial simulation for the digital clock	Ta Ngoc Nam, Vu Nam Binh
	Coding for clock based on Arty Z7 board and LED	Ta Ngoc Nam, Vu Nam Binh
Final testing and Report	Testing and decoding after finishing demo	Ta Ngoc Nam
	Write report for the project	Ho Anh Dung

5. Source code and demo video.

[Display.v](#)

[Perpetual_Clock.v](#)

[mfe_led7seg_74hc595_controller_wrapper.v](#)

[mfe_led7seg_74hc595_controller.v](#)

Link video:

Case 28-02-2024:

<https://drive.google.com/file/d/1OL9KZugYTPyUMeFMgsGY40tvvJduMxij/view?usp=sharing>

Case 30-04-2023:

<https://drive.google.com/file/d/1YccPQ95NPU26ghUiyQRg0WyOcN8Sxq-T/view?usp=sharing>

Case 31-01-2024:

https://drive.google.com/file/d/101EsBGFtrFLPgUei_eHchLcxa2SjeDmK/view?usp=sharing

Case 31-12-2023: https://drive.google.com/file/d/11yZxvXr-gczDvCKrFKI6m_Its76DOjmu/view?usp=sharing

6. References

1. https://github.com/nxquangce/make-fpga-easier?fbclid=IwAR0_VMd56cJJy4ZNEhESopDfQqxyLC8ei2G5GrKs9bosJ5TezUPgr71iphw

End of the report.

THANKS FOR READING!