VIETNAM NATIONAL UNIVERSITY, HO CHI MINH CITY
UNIVERSITY OF TECHNOLOGY
FACULTY OF COMPUTER SCIENCE AND ENGINEERING


## LOGIC DESIGN PROJECT - CO3091

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## PROGRESS REPORT

# SPORT STOPWATCH

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# Contents

# Members list & Workload

| No. | Full name | Student ID | Contribution | Percentage of work |
|---|---|---|---|---|
| 1 | Vu Nam Binh | 2152441 | Design and implement IC55 timer, button, switch; write report | 100% |
| 2 | Hoang Tien Duc | 2152520 | 74LS192 and led 7 segments design on circuit; write report | 100% |
| 3 | Nguyen Duc Bao Huy | 2152089 | Design Proteus project and circuit design; write report | 100% |

# 1 Introduction

Sports watch is one of the most useful gadgets nowadays, especially for either professional or amateur athletes or even normal users. The name "sports watch" implies that this type of watch is equipped with multiple features to support playing sports or sometimes in competition!

In this project, we aim to implement a sport watch with some basic features by using **Logic Design**'s knowledge with **integrated-circuit (ICs)**. This is actually an interesting topic for us to complete although it's quite difficult while only using ICs to implement this project. After all, this project gave us more chances to work with hardware and improve our problem-solving skill.

# 2 Requirement

We All functions of this sportwatch in general are:

- Count-up Mode.
- Count-down Mode.
- Modify count-up time.
- Modify count-down time.
- Stop counting.
- Continue counting.
- Reset.

Obviously, ***accuracy*** plays an important role in determining the result of a sport competition. Therefore, we will implement this watch with the smallest time unit is millisecond. It means that we have 2 digits are for millisecond, 2 digits are for second and 2 others are for minute.

# 3 Schematic and Video

In case, you can not open the schematic on Proteus or videos we uploaded through BKEL site, please check at here.

# 4 Explanation

## 4.1 Introduction to IC 74LS08, 74LS32 and 74LS04

These 3 ICs are extremely popular when we talk about electrical circuits. Therefore, we will not introduce these things in details:

***Firstly***, IC 74LS08 is a Quadruple 8-bit Two Input AND Gate IC. This type of IC is used in electrical circuits that need the AND logic. It has 4 AND Gates and each of them has two inputs, one ouput. The operating voltage range is from +4.75V to +5.25V but +5V is recommended.

***Secondly***, IC 74LS32 is a Dual Input OR Gate with Quad package. This type of IC is used in electrical circuits that need the OR logic. Like IC 74LS08, this IC also has 4 OR Gates and each of them has two inputs, one output. The supply voltage is in the range from +5V to +7V.

***Thirdly***, IC 74LS04 is a Two Input Quadruple 8-bit NOT Gate IC. This type of IC is used in electrical circuits that need the NOT logic. It has in total 6 input pins corresponding to 6 output pins. The operating voltage range is from +4.75V to +5.25V but +5V is recommended.

## 4.2 Introduction to IC 74LS47

This is not a new but also not an old IC to many people. It is used to support converting a BCD value into a pattern to drive a 7 segment LED. Binary Coded Decimal (or BCD) is an encoding method in which each digit of a number is represented by its own binary sequence (usually four bits). Below is the schematic of this IC:

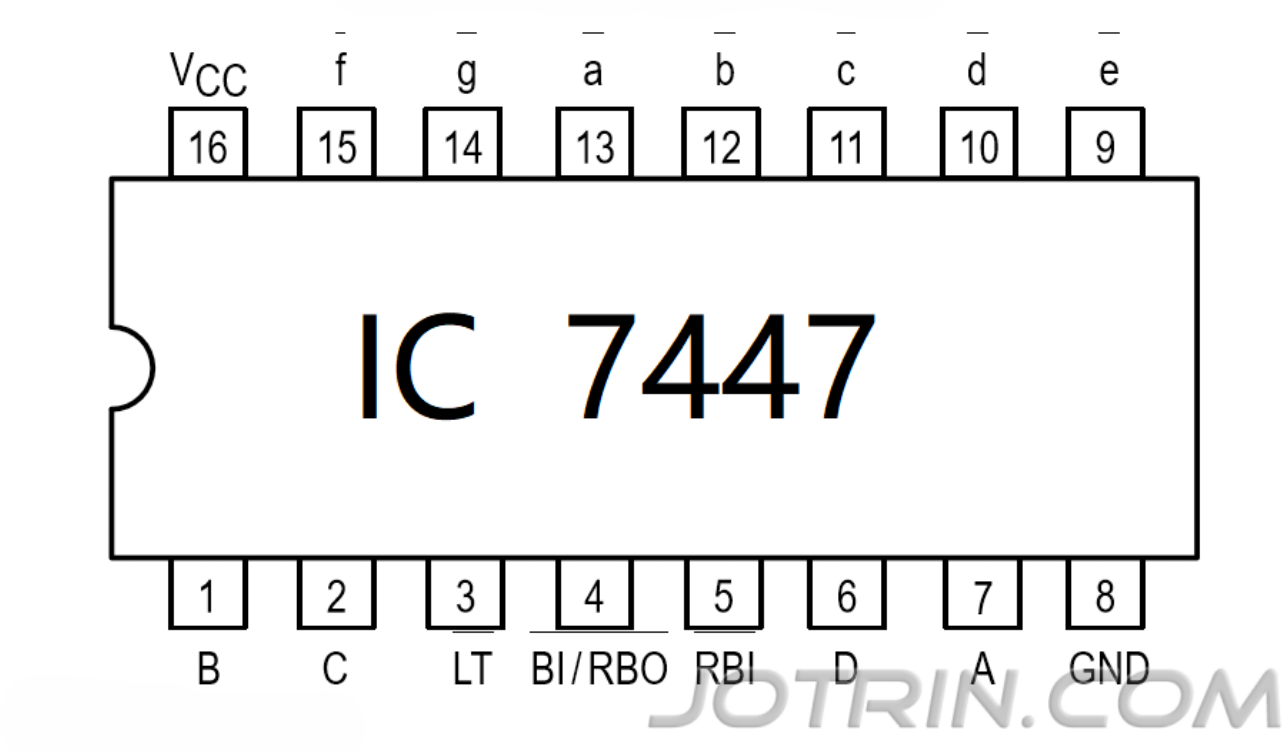


**Figure 1:** IC 74LS47 Schematic

This IC has 16 pins:

- **PIN 1, 2, 6 AND 7** are inputs corresponding to 4 bits B, C, D, A with D is the MSB and A is LSB.
- **PIN 9, 10, 11, 12, 13, 14** are ouputs corresponding to f, g, a, b, c, d, e with a, b, d, d, e, f here representing 7 inputs for the segment of 7 segment LED.
- **PIN 8** is the GND.
- **PIN 16** is VCC which is highly recommended to be connected with a 5V power. We should not provide a higher voltage power than this value so as to ensure the IC works stably.
- **PIN 3 (LT-LAMPTEST)** is just a pin to check whether the 7 segment LED, which is connected to this IC, can work normally or not. If we connect this pin to mass, all segments will turn on and if there is a segment turning off, this 7 segment LED has problem.
- **PIN 4 BI/RB0** is connected to high level, if not, the LED will not light.
- **PIN 5 RBI** is connected to high level.

**Principle Operation:** The IC receive 4-bit input from IC 74LS192, which will be introduced right below. Then it will convert this BCD value to 7 outputs corresponding to 7 inputs of the 7 segment LED.

## 4.3 Introduction to IC 74LS192

This is a synchronous 4-bit Up/Down Decade Counter. The word **"synchronous"** here implies that this IC works based on a clock pulse. It can be used in count-up or count-down mode depending on inputs. Below is the schematic of this type of IC:

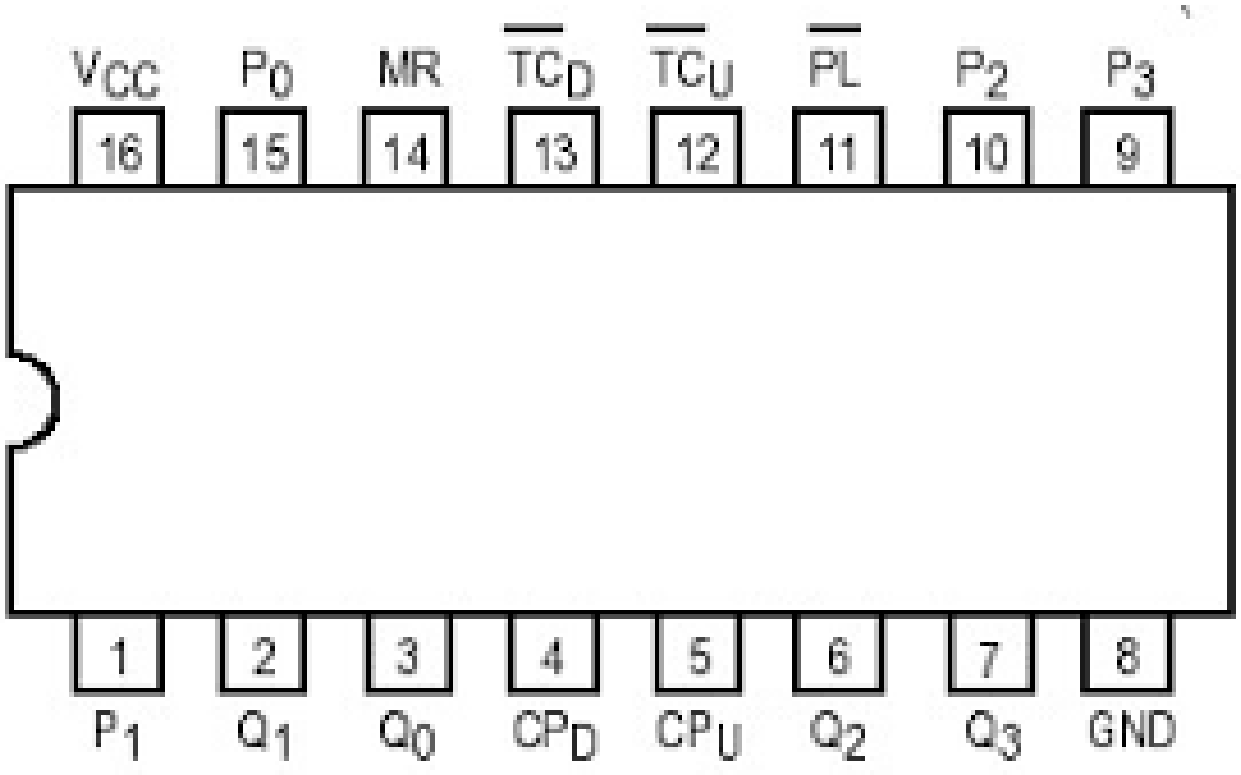


**Figure 2:** IC 74LS192 Schematic

- Pin 1, 9, 10, 15 are parallel data inputs, which means groups of inputs can be sent simultaneously.
- Pin 2, 3, 6, 7 are outputs of FlipFlop, which will be connected to the IC 74LS47 above to decode to drive the 7 segment LED.
- Pin 4 is the input count-down clock pulse.

- Pin 5 is the input count-up clock pulse.
- Pin 8 is connected to GND.
- Pin 11 is asynchronous parallel load input.
- Pin 12 is the count-up output signal. This pin is always output HIGH, only when the IC counts up to 9 and the Up Input is triggered then this pin will be LOW. Then, this pin will be HIGH again.
- Pin 13 is the count-down output signal. This pin has also the same characteristic as the Pin 12, which we introduce right above.
- Pin 14 is asynchronous master reset input.
- Pin 16 is the VCC.

This is the **TRUTH TABLE** for this IC:

**MODE SELECT TABLE**

| MR | $\overline{PL}$ | $CP_U$ | $CP_D$ | MODE |
|---|---|---|---|---|
| H | X | X | X | Reset (Asyn.) |
| L | L | X | X | Preset (Asyn.) |
| L | H | H | H | No Change |
| L | H | ⌐ | H | Count Up |
| L | H | H | ⌐ | Count Down |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

**Figure 3:** Truth Table IC 74LS192

As you can see on the figure above, the count-up mode will be on if the Clock-Pulse Down ($CP_D$) corresponding to input Pin 4 is connected to high level, $\overline{PL}$ corresponding to input Pin 11 is connected to high level, $MR$ corresponding to Pin 14 is connected to low level and the ($CP_U$) will be connected to the output of the module NE555, which is used to create a 1 Hz Clock Pulse. Notice that we can get a high or low level when connect the pin with the VCC or the Ground, respectively. The principle operation for other modes is also the same.

## 4.4 Introduction to clock-generating circuit using IC555

In this assignment, we use a clock-generating circuit on proteus simulation which is made up of some electrical components including resistor, capacitor, electronic capacitor and IC555.

### 4.4.1 Operation principle

Timer IC555 has 3 operating modes namely Monostable, Bistable and Astable modes. In this project, we consider only astable mode so we will explain this mode in detail.

Here is the inside figure of the clock-generating circuit:

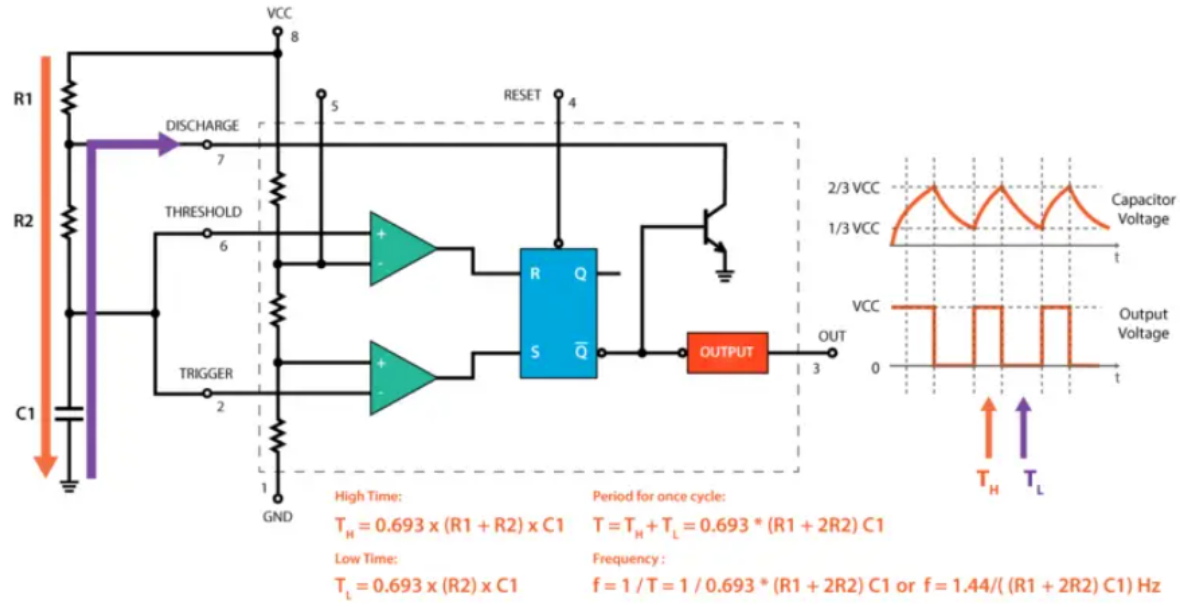


**Figure 4:** Structure of generating-clock circuit using IC555

The principle operation of this circuit is that the output is **HIGH** only when **R is 0 and S is 1** and no change when both R and S are 0 (R and S are input of the FlipFlop). In the figure you can see, there are 2 OPAMP comparators (ouput is 1 when the input at positive pin has higher voltage than the negative). Therefore, we need to somehow **modify these 2 comparators** such that we can achieve the output signal as expected. Because the ouputs from 2 OPAMP comparators will be used as the inputs R and S of the FlipFlop.

Here, the solution is that the input of these 2 comparators will be connected to **THRESHOLD, TRIGGER, 1/3 Voltage Supply and 2/3 Voltage Supply**.

***Initially***, the capacitor $C_1$ starts charging and the **TRIGGER, THRESHOLD voltage** now are **lower than 1/3** so the ouput of the 2 comparators at R-input and S-input respectively 0 and 1 so the **output OUT is now 1**.

***Then***, after the TRIGGER voltage reaches 1/3 Supply voltage, nothing changes because now R and S are 0. Then, when the **THRESHOLD and TRIGGER** voltage **reach 2/3 supply voltage**, R is now 1 and S is now 0 leading the **output OUT to be 0**. Now, the ***capacitor starts discharging***.

***After that***, the **capacitor voltage toggles** between **1/3 and 2/3 VCC** while the **output toggles** between **1 and 0**. Therefore, the **key here** is to **calculate** exactly the **value of R1, R2 and C1** such that the **time toggling between 1/3 and 2/3 VCC** is equal to **1 second**.

$T\_on$ and $T\_off$ is the time of high and low clock signal in 1 cycle so we have to choose values of R1, R2 and C1 such that the addition of these 2 time values returns 1. However, as you can see in the formula, there is appearances of ln(2) so we **can not generate** an **exact 1Hz clock pulse** here but we can choose values that approximates the result to 1. Here, we use **R1 = 470 Ω, R2 = 470kΩ and C1 = 1.5uF**.

In the real circuit, to simplify the complexity of the circuit, we can use the module NE555. This electrical component is actually a module integrating all components in the figure above inside a small module as below:


**Figure 5:** Module NE555

With this module, we can modify the clock pulse by using a screwdriver to turn the knob placed on top of 2 blue blocks. However, because this component is cheap, we can not know exactly the output clock pulse (there will not be any screen to display the value for an electrical component with the low price only 15 thousand VND). Therefore, to use this module, we have to use an osciloscope to measure the output frequency for accurate usage in the future.

# 5 Working Principle

## 5.1 The routine of IC 74LS192

The operation of the IC 74LS192 is characterized by straightforward logic. Certainly, let's incorporate that information into the explanation. The utilization of two IC 74LS192 components is integral to the representation of a two-digit number ranging from 00 to 99. In this configuration:

**Count-up Mode:**

- The first IC 74LS192 controls the count-up operation, progressing from 0 (0000) to 9 (1111). Upon reaching 9 and transitioning back to 0, the Terminal Count Up (TCU) signal undergoes a change from HIGH to LOW (H to L). This transition serves as an input trigger for the second IC 74LS192.
- The second IC 74LS192, triggered by the TCU signal, functions as the tens digit counter. It advances by one count, representing the tens place of the two-digit number.

**Count-down Mode:**

- The first IC 74LS192 manages the count-down operation, decrementing from 9 (1111) to 0 (0000). Upon reaching 0 and transitioning back to 9, the Terminal Count Down (TCD) signal undergoes a change from HIGH to LOW (H to L). This transition serves as an input trigger for the second IC 74LS192.
- The second IC 74LS192, triggered by the TCD signal, functions as the tens digit counter during count-down, decrementing by one count.

The combination of the count-up and count-down operations of the two ICs collectively represents a two-digit number. The first IC manages the units digit, while the second IC handles the tens digit, effectively displaying a comprehensive range from 00 to 99.

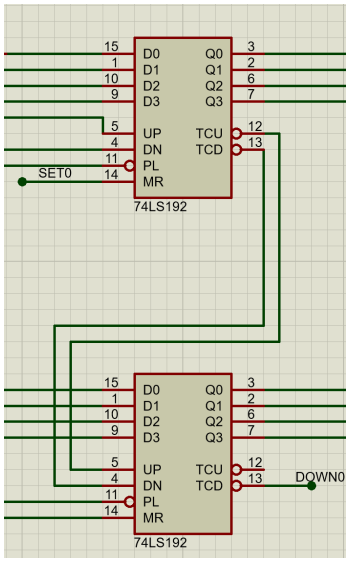


**Figure 6:** How 2 IC 74LS192 are connected.

While the count-down mode effectively cycles from 99 to 0 and back to 99, this functionality falls short of meeting the requirements for a comprehensive sports timer, and similarly to the count-up mode. In the next two section, we will address this limitation by implementing enhancements to ensure the correct countdown function necessary for a sports timer.

## 5.2 Restricted Count-down Implementation

To achieve the desired countdown functionality of 59 to 0 and back to 59, modifications are required in the existing schematic. Instead of the default countdown from 99, we introduce logic gates to monitor the output

value.

Upon reaching 00 and subsequently counting back to 99, a logic gate is employed to detect if the output value is 99. At this juncture, the system triggers a PRESET operation, initializing the value based on the tens initial input ($B_0B_1B_2B_3 = 0101$) to set it at 59 instead of being 99. Subsequently, the countdown resumes from this value, ensuring the accurate sports timer countdown sequence. This logic is repeated, enabling a continuous countdown from 59 to 0 and back to 59, aligning with the intended functionality of the sports timer.

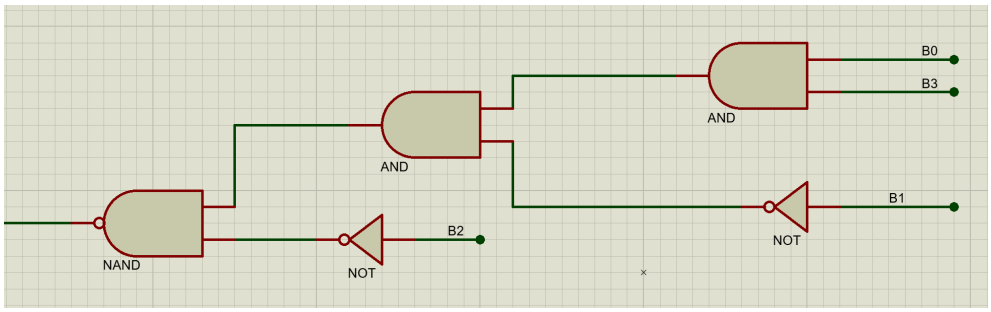


**Figure 7:** A custom circuit for customize the count-down value.

The core concept behind the implementation of logic gates is to trigger a PRESET operation when the tens of seconds/minutes reach 9, causing the output to transition to 0 at the PL port. This ensures that the value is reset to the initial configuration: 0101-1001 (59) instead of the default 1001-1001, which is 99.

| B0 | B1 | B2 | B3 | Output |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 |
| All other cases | | | | 1 |

**Figure 8:** Truth table of the circuit.

## 5.3 Restricted Count-up Implementation

To optimize the countdown functionality from 0 to 59 and back to 0, adjustments are made to the conventional schematic. Instead of the default count-up from 0 to 99 and back to 0, the system is now engineered to precisely count up from 0 to 59 and seamlessly return to 0.

In details, upon reaching 59 and advancing to 60, a placed logic gate monitors the output value. If the output registers 60, a RESET operation is triggered, reverting the value to 0. Subsequently, the countdown resumes from this reset point. This iterative process ensures the accurate implementation of the sports timer counting up function, traversing the range from 0 to 59 and cyclically returning to 0.

The schematic presented above illustrates the logic governing the verification of the output value as 60 and provides a streamlined method for confirming whether the tens digit reaches 6.

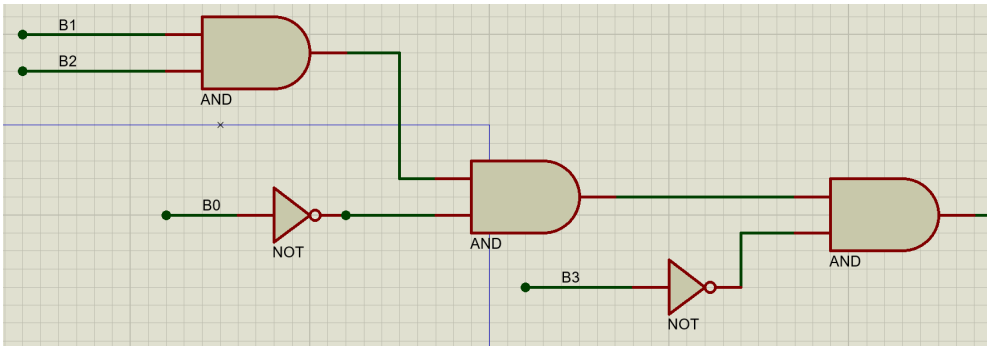


**Figure 9:** A custom circuit for customize the count-up value.

When the tens digit reaches 6, the system triggers the output to 1 at the MR port, initiating a RESET operation for the tens digit. This action resets the value to 0, resulting in the representation of 00 instead of 60 in the sports timer countdown function.

| B0 | B1 | B2 | B3 | Output (SET 6_TO_0) |
|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 |
| All other cases | | | | 0 |

**Figure 10:** Truth table of the circuit.

## 5.4 Make connection between second and minute

### 5.4.1 Count-down mode

In this section, our focus is on establishing the connection between the second and minute components during the counting-down mode. The strategy involves leveraging the TCD signal, which transitions from LOW to HIGH when the timer counts down from 59 to 0 and back to 59. This signal serves as a pivotal input for the minute component, specifically through the DN gate. By utilizing the TCD signal as input, we enable the minute component to count down every 60 seconds during this phase. The schematic above visually illustrates the successful implementation of this interconnection.

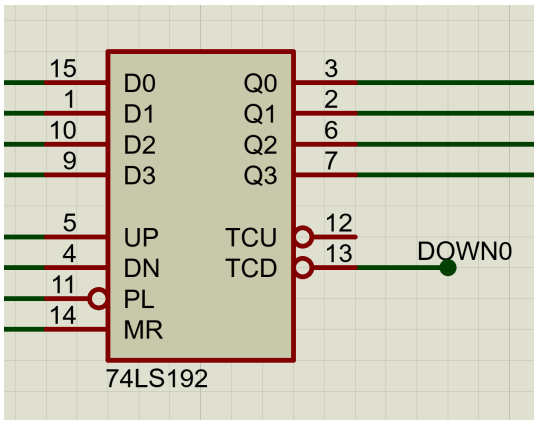


**Figure 11:** How second and minute are connected in count-down mode.

As the countdown progresses from 00 to 59, the TCD signal undergoes a transition to 0. This transition is complemented by the SET_MINUTE and SET_SECOND signals consistently maintaining a HIGH state

when the button is released. The resulting truth table captures and illustrates these key states in the system's behavior.

| TCD output of first 74LS192 | DN input of second 74LS192 |
|---|---|
| 0 | 0 |
| 1 | 1 |

**Figure 12:** Truth table of the connection.

### 5.4.2 Count-up mode

In the implementation of the connection between the second and minute components in counting up mode, we encounter a more complicated process compared to counting down mode. The complexity arises when the timer is counting up from 0 to 59 and resets to 0. In this scenario, the standard transition of Terminal Count Up (TCU), occurring when changing from 59 to 0, is altered due to the introduction of additional logic gates.

To address this, we capitalize on the logic that examines the value, ensuring that when it changes from 59 to 0, the TCU signal is not directly triggered. Instead, we utilize the logic that checks if the value is 60, triggering the SET_6_TO_0_MINUTE output to transition from LOW to HIGH. This alteration prompts the MR (Master Reset) input to transition to HIGH, subsequently initiating a RESET operation and resetting the value to 0. This intricate sequence ensures the seamless transition from 59 to 0 in the counting up mode, facilitating a controlled and accurate synchronization between the second and minute components.

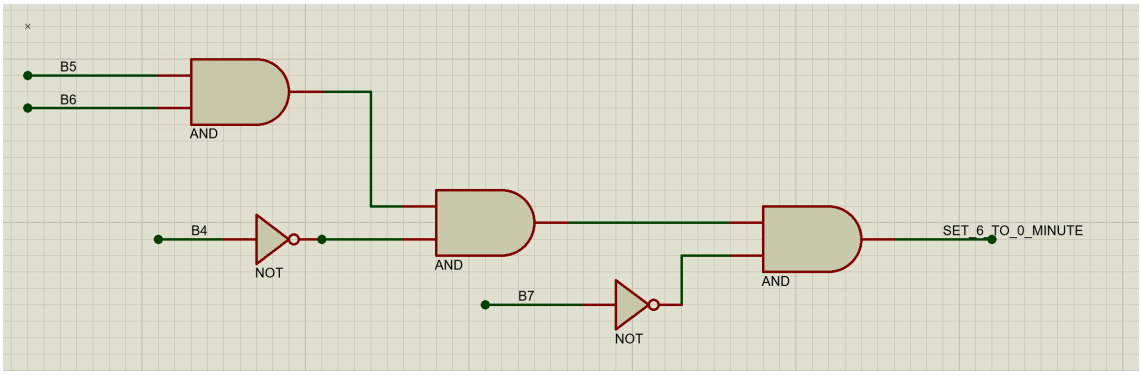


**Figure 13:** SET_6_TO_0_MINUTE schematic.

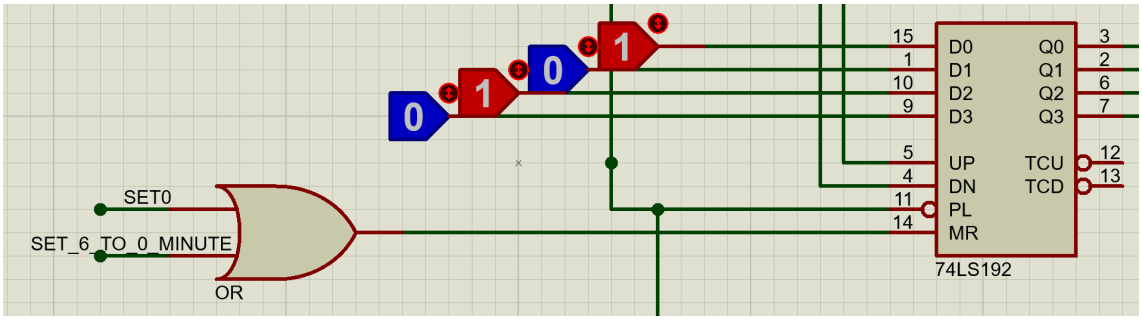


**Figure 14:** How SET_6_TO_0_MINUTE connects to MR port.

# 6 Function Implementation

In this section, we introduce the implementation of essential functionalities for the sports stopwatch, enabling dynamic control over start, stop, pause, reset operations, and manually setup the initial minute and second .

## 6.1 Button Debouncing

Mechanical buttons cause an unpredictable bounce in the signal when toggled. There are various ways to implement debouncing circuits for buttons. In this project, a simple debouncing circuit is implemented to generate only a single pulse when pressing a button on logic design. As shown in the figure below, when a button on logic design is pressed and released, there are many unexpected up-and-down bounces in the push-button signal. The debouncing circuit only generates a single pulse with a period of the slow clock without bouncing as we expected.

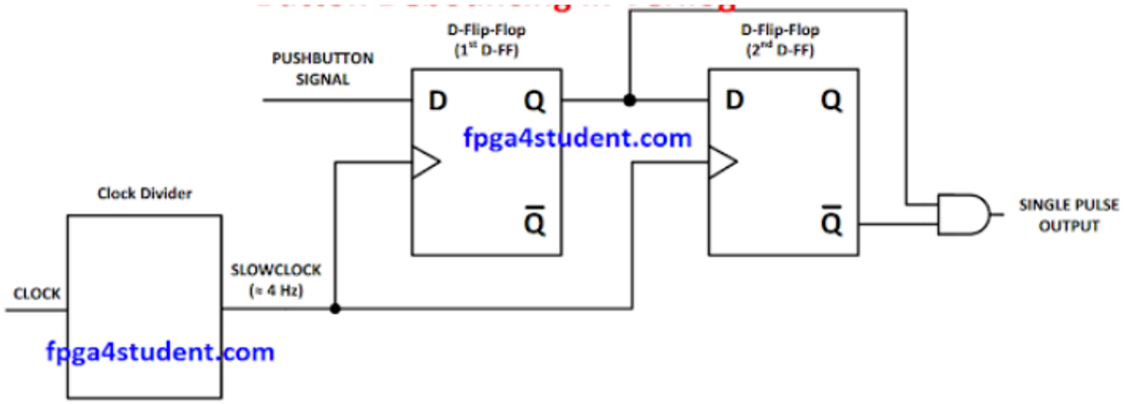


**Figure 15:** Debouncing Circuit for buttons on logic design.

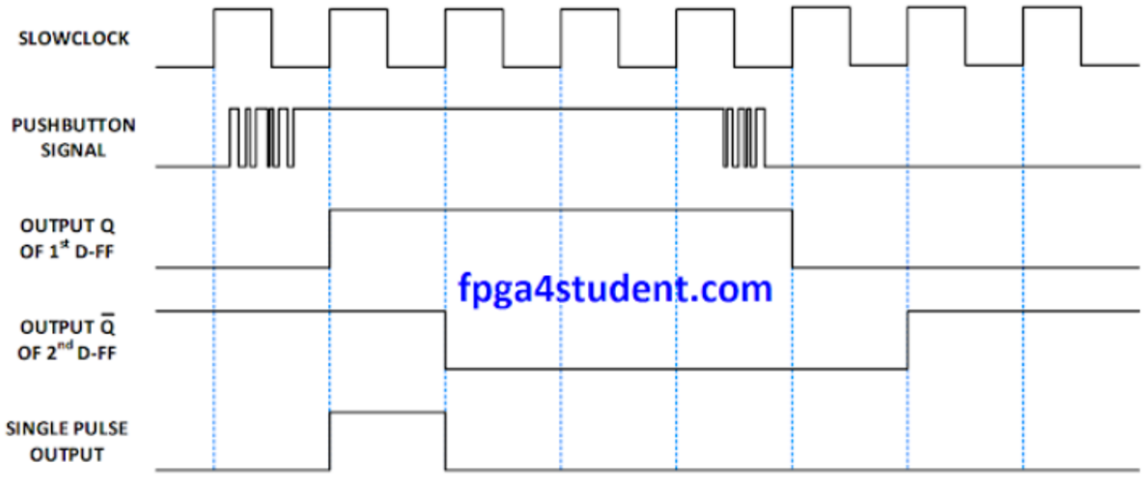


**Figure 16:** Expected waveform from the debouncing circuit.

## 6.2 Stop the timer

In the count-down mode, a critical consideration is ensuring that when the timer reaches 00:00, it remains unaffected by external triggers and ceases countdown operations. This functionality is safeguarded by a specific section of the schematic.

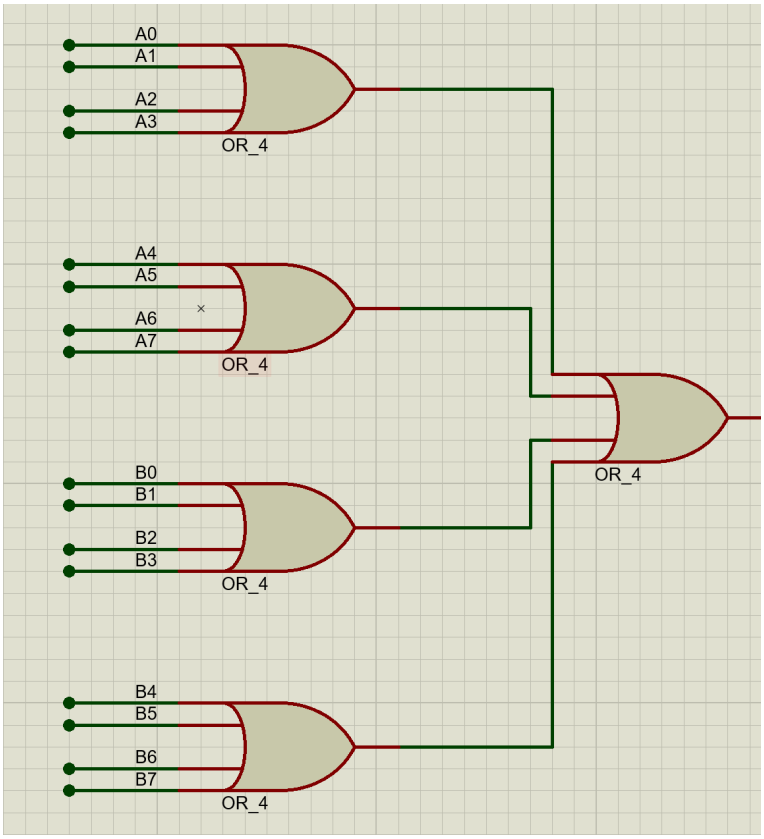


**Figure 17:** Schematic to check if the timer reaches 00:00.

Here, the values of $A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, B_0, B_1, B_2, B_3, B_4, B_5, B_6, B_7$ collectively represent 0, indicating the time is 00:00. Consequently, the output is set to 0, acting as a preventative measure against the timer being triggered by the clock and preventing it from continuing the countdown process. However, in the whole picture, it need to connect to some other logic gates to control the timer and we can see it in the full schematic.

## 6.3 Start/Stop and Mode

To facilitate the start/stop functionality and mode selection of the timer, two switches, namely **switch_START/STOP** and **switch_MODE**, play a pivotal role. The operation of these switches is outlined as follows:

**switch_START/STOP:**

- When switch_START/STOP is set to 0, the timer is paused permanently.
- Conversely, when switch_START/STOP is set to 1, the timer starts counting.

**switch_MODE:**

- When set to 0, the timer operates in count-up mode.
- Conversely, when set to 1, the timer operates in count-down mode.

The key objective is to ensure that the timer remains unaffected by the clock when stopped (switch_START/STOP = 0 and don't care about the status of switch_MODE), while resuming counting (either up or down) when started (switch_START/STOP = 1), contingent on the selected mode (switch_MODE = 0 for count-up, switch_MODE = 1 for count-down).

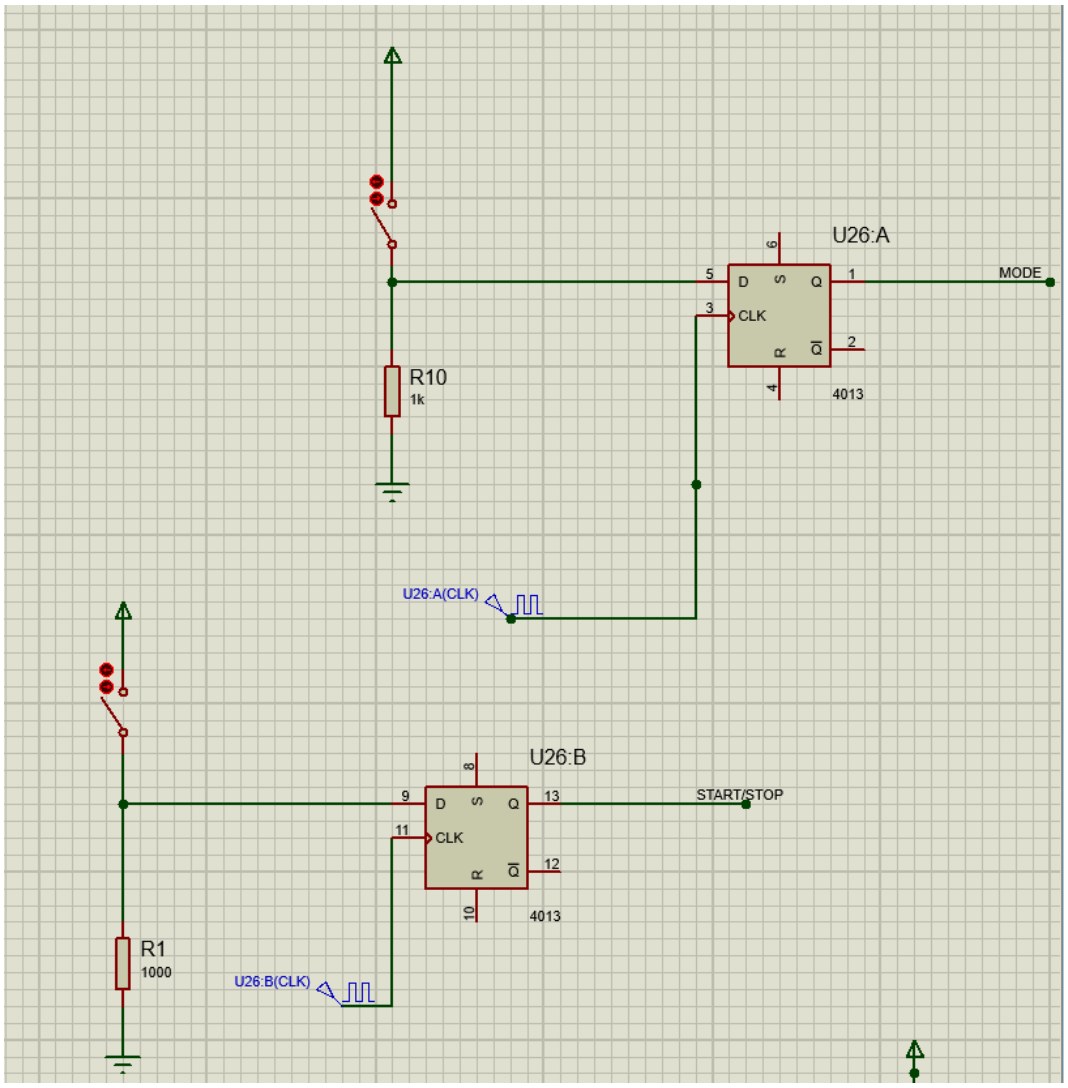


**Figure 18:** 2 switches to control start/stop and mode function.

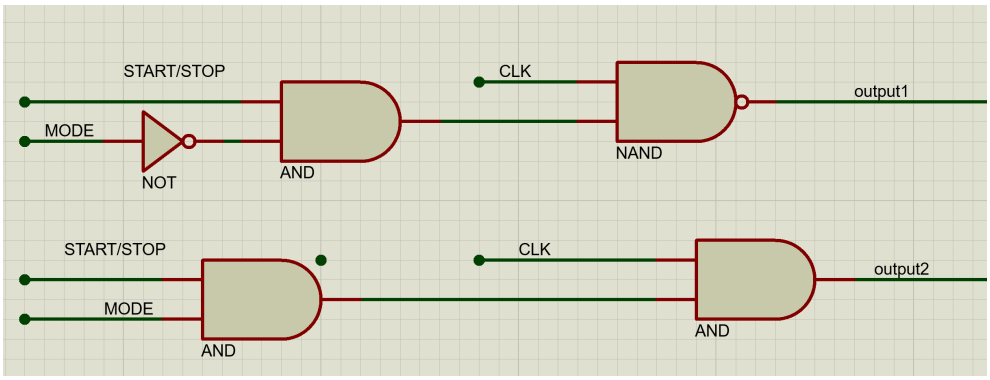


**Figure 19:** Start/stop schematic.

| START/STOP | MODE | CLK | Output1 | Output2 |
|---|---|---|---|---|
| 0 | X | L – H - L | 1 | 0 |
| 1 | 0 | L – H - L | H – L - H | 0 |
| 1 | 1 | L – H – L | 1 | L – H – L |

**Figure 20:** Start/stop schematic.

Consider the outputs of this schematic, denoted as output1 and output2.

**Timer Stop Condition:** When the timer is in a stopped state (switch_START/STOP = 0), both Output1 and Output2 remain constant. This signifies that the timer is no longer susceptible to being triggered by the clock, ensuring a halted state.

**Timer Start in Count-Up Mode:** Upon initiating the timer (switch_START/STOP = 1) with the mode set to count up (switch_MODE = 0), only Output1 is activated by the clock, while Output2 remains constant at 0. This configuration ensures that the timer exclusively counts up in an automated manner.

**Timer Start in Count-Down Mode:** Conversely, when starting the timer (switch_START/STOP = 1) with the mode set to count down (switch_MODE = 1), only Output2 is triggered by the clock, and Output1 remains constant at 1. This specific arrangement ensures the timer exclusively counts down in an automated fashion.

## 6.4 Reset

Incorporating a user-friendly reset functionality into our design, we enable users to reset the timer to zero at their discretion, particularly when operating in count-up mode.

Drawing inspiration from the truth table and the operational characteristics of the IC 74LS192 outlined in Part 2, the reset mechanism hinges on the Master Reset (MR) input. The operational principle is succinctly encapsulated as follows:

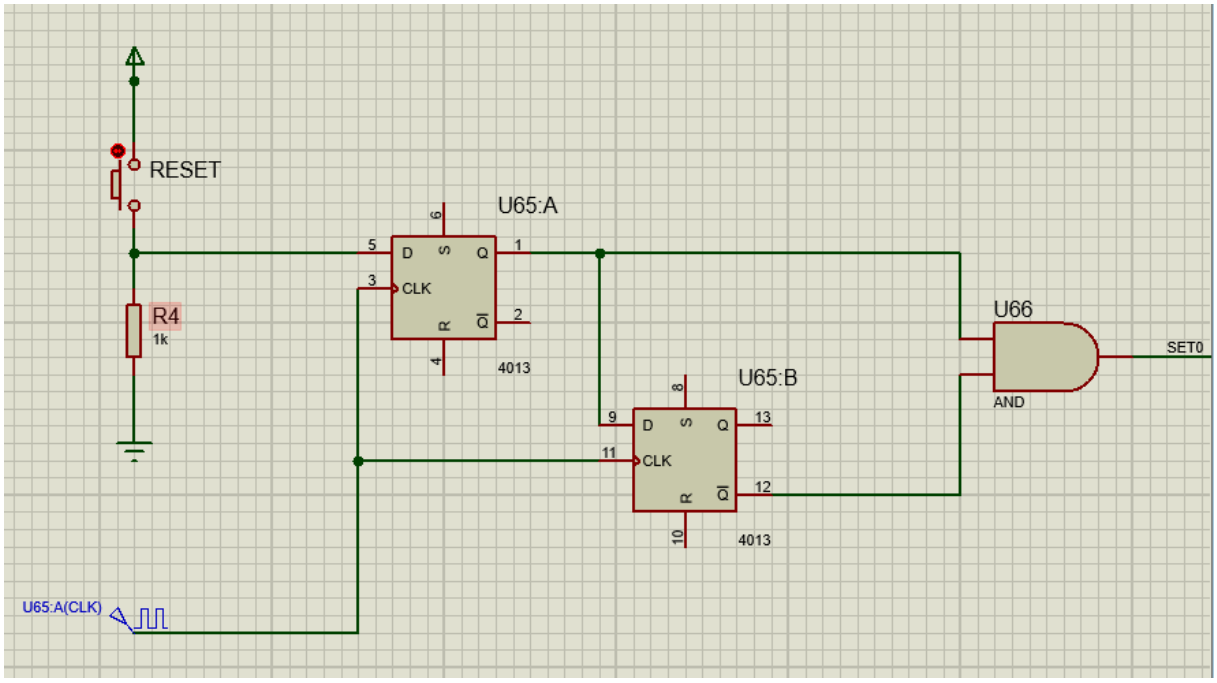


**Figure 21:** How RESET button is designed.

**Reset Trigger:** When the user presses the RESET button, the MR input is driven to a HIGH state (MR

= 1), initiating the reset operation. This action effectively resets the value of the timer to zero.

**Non-Reset Operations:** Conversely, upon releasing the RESET button, the MR input returns to a LOW state (MR = 0). In this state, the timer seamlessly transitions into other operational modes, accommodating manual count-up/count-down and automatic count-up/count-down functions.

This reset design, implemented by connecting the RESET button to the MR inputs of the four IC 74LS192 units, provides users with an intuitive and responsive means to reset the timer when desired, enhancing overall user control and experience.

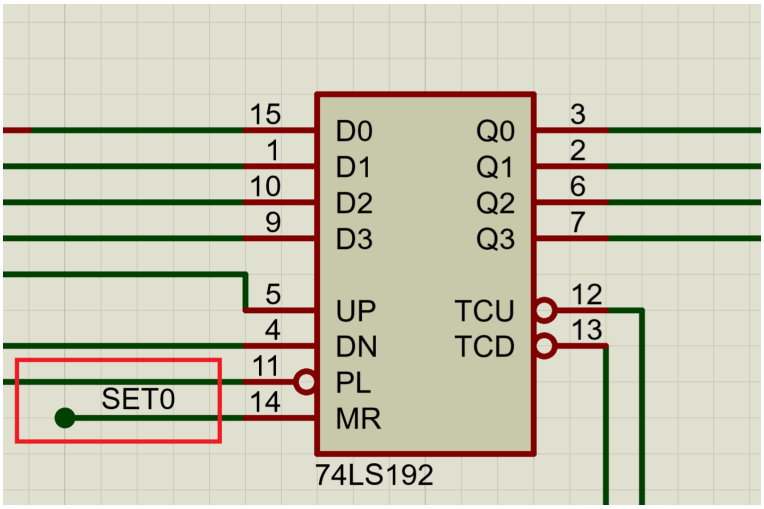


**Figure 22:** RESET button is connected to MR gate.

## 6.5 Manual Initialization of Minute and Second

To facilitate precise manual adjustments of the initial time, we have incorporated four dedicated buttons: SET_MINUTE_BTN, SET_MINUTE_DOWN_BTN, SET_SECOND_BTN, and SET_DOWN_SECOND_BTN. These buttons are strategically designed to allow users to configure the initial time of the timer according to their specific requirements.

The buttons designated for manual minute and second adjustments are exclusively designed to function when the timer is in a stopped state (switch_START/STOP = 0). This intentional design serves two primary purposes:

1. This approach aligns with real-world sport timers that prioritize accuracy and fairness. By allowing manual adjustments only when the timer is stopped, users can ensure precise setting of minute and second values without compromising the integrity of the timing mechanism.
2. From a logical perspective, when the timer is in paused state (switch_START/STOP = 0) the output becomes disengaged from the clock signal. This ensures static output, enabling precise and controlled adjustments to minute and second values with ease and accuracy.

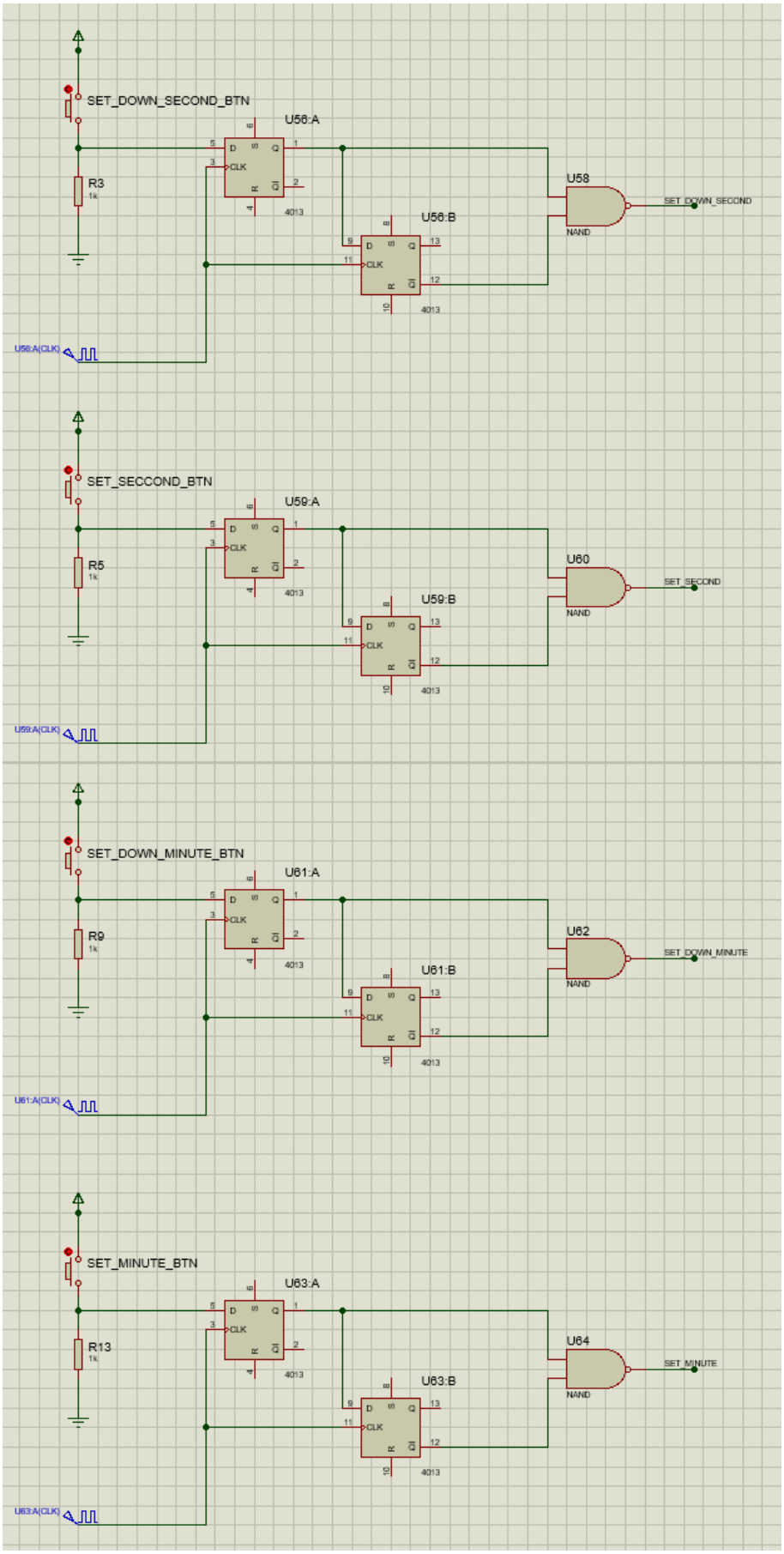


**Figure 23:** 4 buttons in schematic.

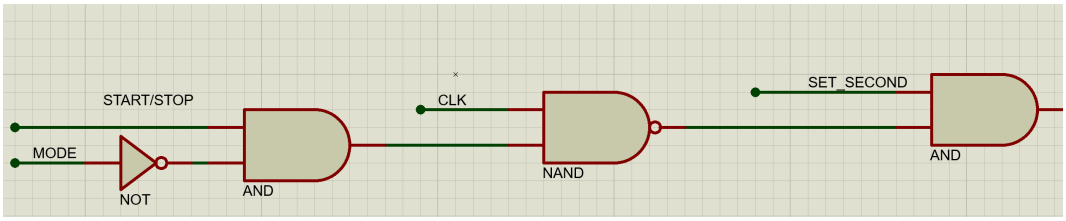


**Figure 24:** A part schematic represents how SET_SECOND works.

In **Start/Stop and Mode**, we established that when the timer is paused (switch_START/STOP = 0), the output remains unaffected by continuous clock pulses. In this state, the output, after passing through a NAND gate, consistently maintains a HIGH level. When triggered from HIGH to LOW, the SET_SECOND button effectively initiates a corresponding transition in the final output from HIGH to LOW. This intentional design allows for manual modification of the second and minute values, providing users with precise control over the timer settings during halted periods.

# 7 Conclusion

Throughout the implementation of the sports stopwatch project, we have demonstrated a deep understanding and application of logic design principles and integrated circuits (ICs). We have utilized ICs such as 74LS08, 74LS32, 74LS04, 74LS47, and 74LS192 to create a comprehensive sports timing device with features including count-up mode, count-down mode, start/stop functionality, and manual time adjustments. The project has enriched our skill set through valuable hands-on experience in hardware implementation, problem-solving, and collaborative teamwork, particularly enhancing proficiency in schematic design, circuit analysis, and the practical application of logic gates and flip-flops.

# References

[1] 74LS192 datasheet.

[2] 555 timer Pulse Generator circuits | astable mode

[3] Verilog code for debouncing buttons on FPGA

[4] 7447 - 7447 BCD to 7-Segment Decoder/Driver Datasheet