Introduction to Hspice

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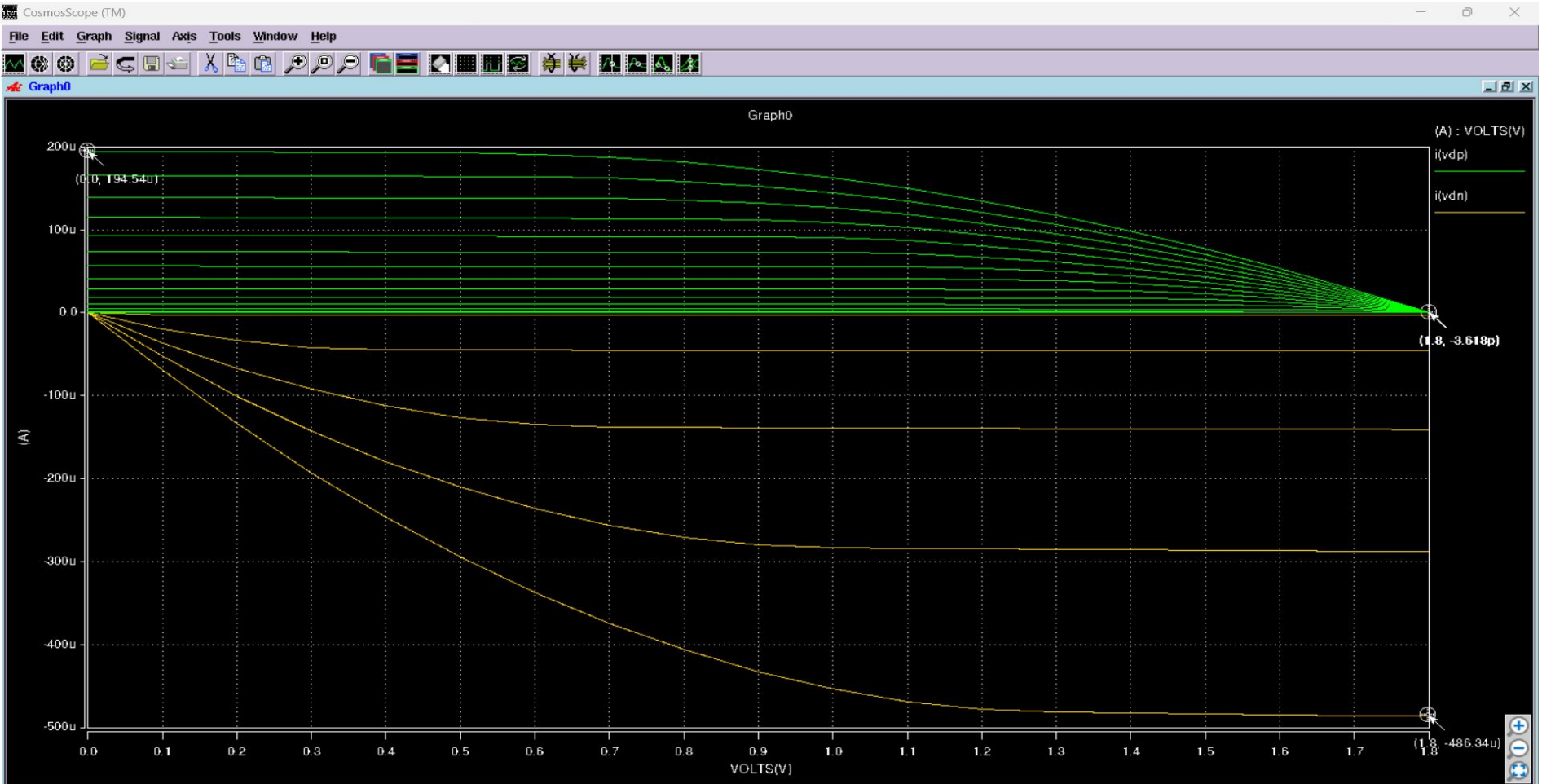
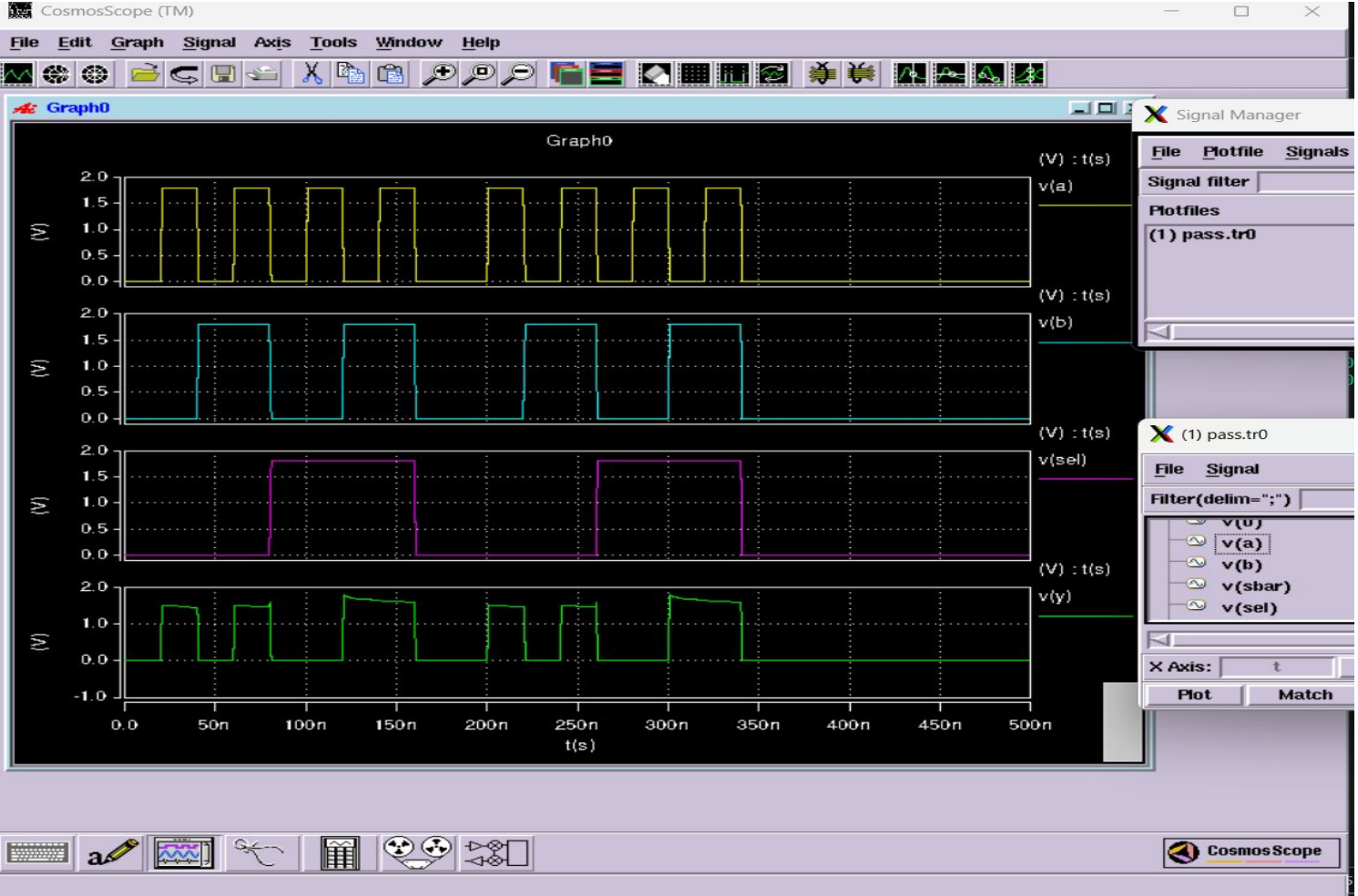
VLSI

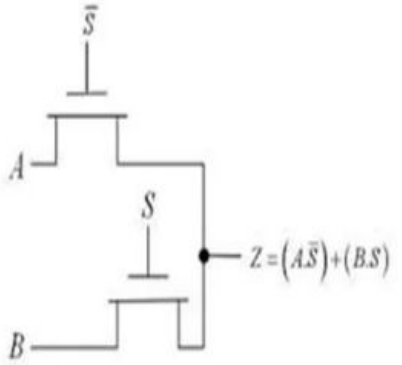
Simulating NMOS and PMOS

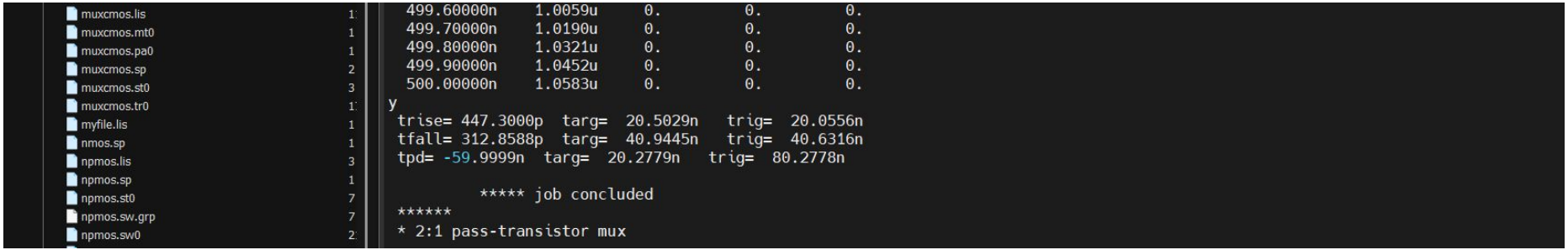


From the DC sweep, the NMOS transistor exhibits a higher maximum drain current (~486 µA) compared to the PMOS transistor (~194 µA), even though both have the same channel length and similar W/L ratios. The ratio of NMOS to PMOS maximum currents is approximately 2.5, which closely matches the ratio of their transconductance parameters ($K_{p,NMOS} / K_{p,PMOS} = 1e\text{-}4 / 4e\text{-}5 = 2.5$). This is expected theoretically because NMOS devices have higher electron mobility than PMOS devices, and the PMOS model has a smaller Kp value. In practical CMOS design, PMOS transistors are usually made wider than NMOS transistors to roughly equalize their drive strengths.

pass transistor based Multiplexer

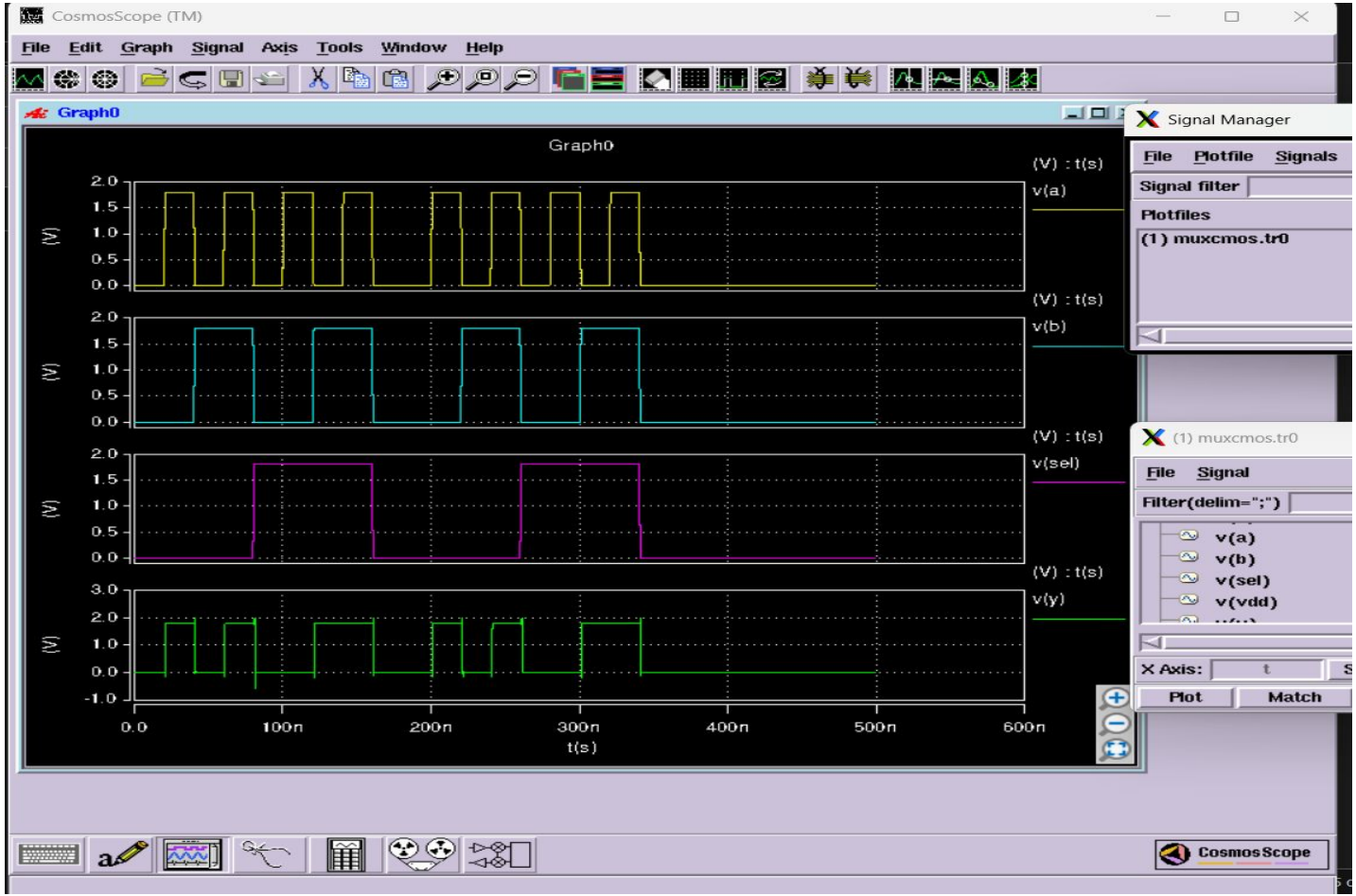


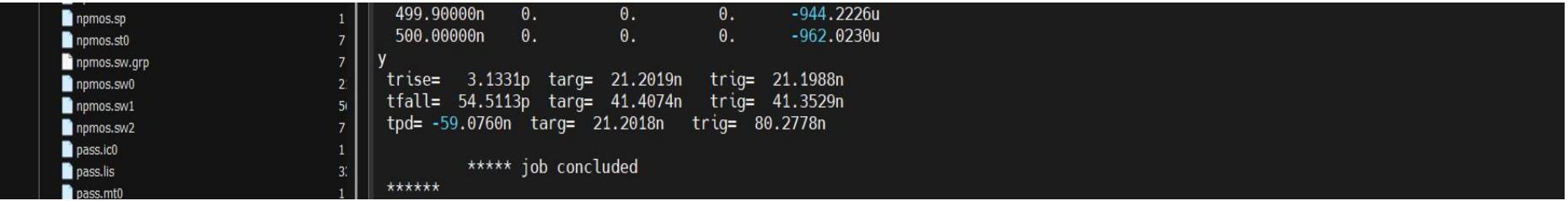




The pass-transistor 2:1 MUX shows very fast output transitions with a rise time of approximately 447 ps and a fall time of approximately 313 ps. The propagation delay measured from the select input to the output shows a negative value (≈ –60 ns), which is an artifact of the measurement definition and early voltage spikes typical in pass-transistor logic. These spikes occur because the output can momentarily respond before the input fully settles, especially when using NMOS pass transistors that pass strong 0 but degraded 1. Overall, the rise and fall times are consistent with expectations for a lightweight pass-transistor MUX, and in practical circuits, outputs are sampled after inputs settle to avoid glitches

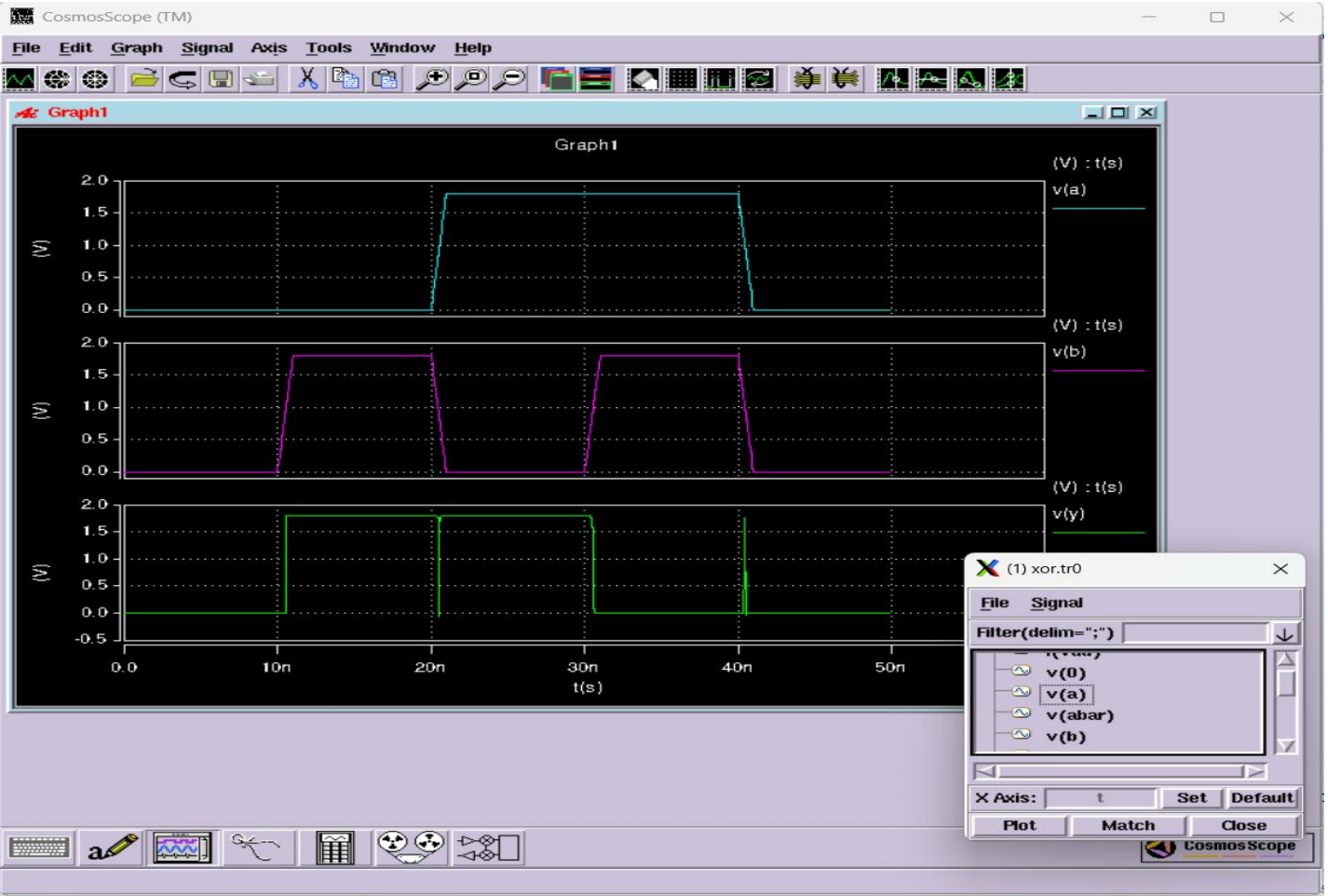
CMOS based Multiplexer

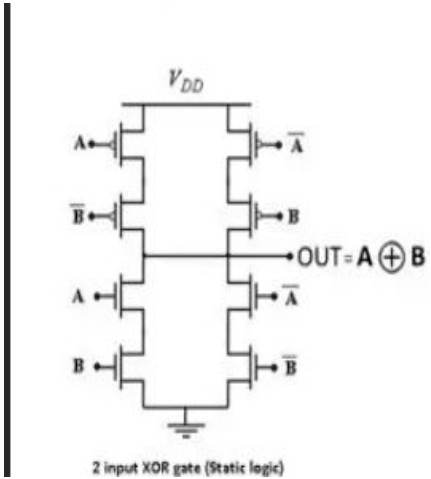




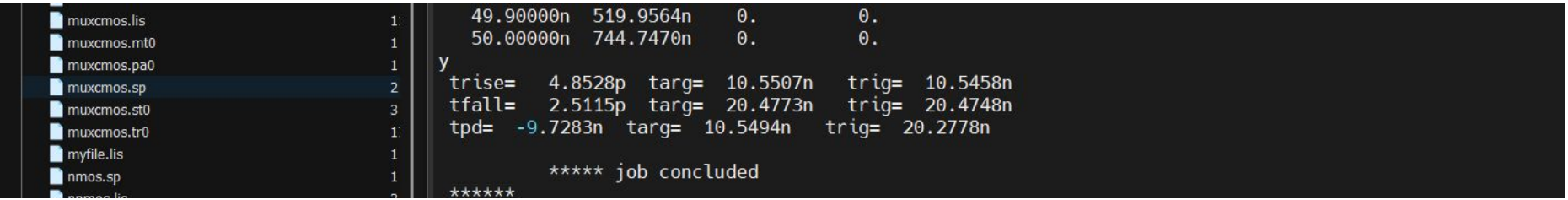
The full CMOS 2:1 MUX exhibits very fast output transitions, with a rise time of ~3 ps and a fall time of ~55 ps, significantly faster than the pass-transistor MUX. The measured propagation delay shows a negative value (~–59 ns), which is an artifact of the HSPICE measurement definition and early transient overshoots typical in CMOS switching. Overall, the CMOS MUX provides strong, sharp output transitions due to its full pull-up and pull-down network, and in practical designs, the outputs are sampled after the input settles to obtain a meaningful delay.

CMOS based XOR gate





2 input XOR gate (Static logic)



The full CMOS XOR gate exhibits very fast output transitions, with a rise time of ~4.85 ps and a fall time of ~2.51 ps. The measured propagation delay shows a negative value (~–9.73 ns), which is an artifact of the measurement definition and small output overshoot. During the transitions of the inputs, the output can exhibit brief voltage spikes, which are typical in CMOS gates due to the simultaneous switching of pull-up and pull-down networks. The rise and fall times are much shorter than those of the 2:1 MUX, consistent with the smaller fanout and reduced transistor network depth. These results align well with theoretical expectations for full CMOS logic