

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Spring

Year : 2013
Full Marks: 100
Pass Marks: 45
Time : 3 hrs

*Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.*

1. a) Explain the assembling and compiling process with suitable examples.
b) Describe an algorithm used for the division of signed numbers. Find the result of $(-9)_{10}$ divided by $(2)_{10}$ using same algorithm.
2. a) Define addressing modes and their purposes. Explain various addressing modes with their advantages and disadvantages.
b) What is micro-programming? Explain how micro-programmed control unit is implemented.
3. a) What is micro-operation? Explain micro-operation for indirect and execute cycle.
b) What may be the problems if input devices are directly connected with bus without modules? What are the functions of I/O module?
4. a) What are the basic problems are with programmed and interrupt driven I/O? How they are overcome by DMA? Explain.
b) Explain cache memory and its uses. Explain set-associative mapping techniques in cache.
5. a) Compare RISC and CISC systems.
b) What is pipelining? Explain with example how pipelining speed up computation time.
6. a) What is cache coherence? Discuss the solution for cache coherence problem.
b) Explain Flynn's classification of computer.
7. Write short notes on: (Any two)
 - a) Virtual memory
 - b) Register organization
 - c) I/O channel.

POKHARA UNIVERSITY

Level: Bachelor
Programme: B.E
Course: Computer Architecture

Semester - Fall

Year : 2013
Full Marks: 100
Pass Marks: 45
Time : 3 hrs

*Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.*

- a) Differentiate between Computer Architecture and Computer Organization. Draw the diagram of extended IAS computer.
- b) Define addressing modes and their purposes. Explain various addressing modes with their advantages and disadvantages.
- c) Draw flowchart for Booth's multiplication algorithm. Perform $(7)_{10} * (-2)_{10}$ using Booth's multiplication algorithm.
- d) Explain how the concept of micro-programming is used to implement a control unit? How the control word of the micro-instructions could be arranged in the control memory?
- e) What are micro instructions? Explain different types of instruction based on number of address.
f) What are the drawbacks of programmed I/O and interrupt driven I/O? Explain how DMA overcomes those drawbacks.
- g) Explain about communication between CPU and I/O processor. Support your answer with the help of suitable example.
- h) Why mapping is needed in cache? Discuss any two mapping strategies used in cache.
- i) Explain the roles of overlapped register window in RISC processor.
- j) What do you mean by pipelining? How pipelining increases the performance of system? Explain in detail.
- k) In certain scientific computations it is necessary to perform the arithmetic operation $(A_i * B_i) + (C_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i = 1 through 6.

b) Explain about interconnection structure in detail also define cache coherence.

7. Write short notes on any two:

- a) Instruction Cycle
- b) Application of Microprogramming
- c) Virtual Memory

POKHARA UNIVERSITY

Semester: Fall

Year : 2014

Full Marks: 100

Pass Marks: 45

Time : 3 hrs.

Level: Bachelor
Degree: BE
Programme: Computer Architecture (New Course)
Course: Computer Architecture

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.

Attempt all the questions.

✓ Differentiate between computer organization and architecture with example. 8

✓ Define RTL . Explain all micro operations with RTL code 7

Define CPU structure and explain each part. 7

✓ Draw internal CPU structure and explain each part. 8

a) What is normalization in floating point operation? How do you

b) What is normalization in floating point operation? 8

normalize the floating point after floating point operation?

मुमान संस्कृती विद्यालय प्राप्ति एकान्तरी महाविद्यालय
वालवासी, ललितपुर १५८७५.८९९९
२०८५ संविधान

POKHARA UNIVERSITY

Semester: Spring

Year : 2014

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

Level: Bachelor
Degree: BE
Programme: Computer Architecture
Course: Computer Architecture

Candidates are required to give their answers in their own words as far as practicable.
As practicable, figures in the margin indicate full marks.

Attempt all the questions.

a) Differentiate between Computer Architecture and Computer Organization. Explain the term SSL, LSI and VLSI. 8

b) Define the term micro-operation. Write down the sequence of microinstructions for fetch and interrupt cycle. 8

c) What is the necessity of Booth's algorithm? Draw the flowchart for floating point division. 7

d) What is microprogramming? Explain the function of micro programmed control unit with figure. 8

e) Draw draft architecture of CPU and show the microinstruction and control signal for the following instruction:

- Load Accumulator
- Store Accumulator
- And to Accumulator
- Jump if AC=0.

f) Why are external devices not connected directly with bus structure of computer system? Draw an internal structure of I/O module. 7

g) Why are different approaches for dealing with condition branches? Define RISC processor and differentiate it with CISC processor. 8

h) What are different approaches for dealing with condition branches? Define RISC processor and differentiate it with CISC processor. 8

i) What are different approaches for dealing with condition branches? Define RISC processor and differentiate it with CISC processor. 8

j) Describe how branch prediction and delayed branch deal with condition branch. 1

b) In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)/(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for $i=1$ through 6.

7. Write short notes on: (Any two)

- a) Multicore organization
- b) VHDL
- c) Flynn's classification of computer

2x5

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Computer Architecture

Semester: Fall

Year : 2015

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between Computer Architecture and Computer Organization. Explain the term ~~SSI~~ and VLSI. 8
2. b) Define RTL. Describe different types of Shift micro-operations. 7
2. a) Define Instruction Set? Explain the basic component used in register organization. 7
3. b) Divide (8) by (3) using 2's complement division. 8
3. a) How floating point arithmetic operations are performed using binary numbers? Give an example. 7
4. b) Differentiate between Hardwired and Micro-programmed control unit. 8
4. a) Explain the logic of Hardwired unit. 8
5. a) Differentiate between direct, associative and set associative mapping technique. 8
5. b) Define cache miss. Describe cache read operation with flowchart. 8
5. a) Compare Programmed I/O and Interrupt Driven I/O. How does DMA overcome the problems of both these techniques? 7
5. b) Which instruction set computers are used in today's world? 8
6. a) Differentiate between RISC and CISC. 8
6. b) How parallelism occurs in uniprocessor system? What are the connections possible for multiprocessor system? 7
6. b) Assume that pipeline has K=6 segment and execute n=120 tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 2x5
7. Write short notes on: (Any two)
 - a) Dual Core and Quad Core Processors.
 - b) BCD Adder.
 - c) Register Windowing and Register Renaming.

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Spring

Year : 2015

Full Marks: 100

Pass Marks: 45

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between Computer Architecture and Computer Organization with example. 8
1. b) What are the different registers used for storage and data transfer in CPU? 7
2. a) Perform 7/3 division using unsigned binary division. 8
2. b) Explain arithmetic pipelining with examples. 7
3. a) Explain how single address, two address and variable format differ from each other? 8
3. b) Define mapping function. Briefly explain the Set-associative mapping technique. 7
4. a) What are the limitations of programmed I/O, how these are improved in interrupt driven I/O, and how the limitations of interrupt driven I/O are improved by DMA. 7
4. b) Instruction pipelining increases system performance without increasing processor number, explain how? 4
4. c) What are Pipelining hazards and how can these be removed? 4
5. a) Assume that pipeline has $K=8$ segment and execute $n=120$ tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 8
5. b) Define parallelism? Draw different interconnection structure of multiprocessor system and describe it with necessary diagram. 7
6. a) Explain different types of hardware performance issues in multicore computers. 8
6. b) What is cache coherency and how can they be removed? 2.5
7. Write short notes on: (Any two) 7
7. a) BCD Adder
7. b) Dual Core and Quad Core Processors
7. c) VHDL

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Computer Architecture

Semester: Fall

Year : 2016
 Full Marks: 100
 Pass Marks: 45
 Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) Define Computer Organization and what are the instruction used in LAS computer explain each in detail. 8
- b) Explain instruction cycle state diagram with interrupt. 3 7
- a) Compute $(7)_{10} \times (-3)_{10}$, where numbers are represented by 2's complement representation (Booth Algorithm) 8
- b) Explain how hardwired control unit is implemented, with appropriate block diagrams. 7
- a) Define cache. Explain set associative mapping with necessary diagrams. 7
- b) Define cache miss. Describe cache read operation with flowchart. 8
- a) Define External Interfaces. Explain how DMA improves the limitations of Interrupt Driven I/O. 8
- b) How Instruction pipelining can increase system performance? A non pipeline system takes 50ns to process a task. The same task can be processed in a six segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? 7
- a) Mention the need of use of large register file in RISC. Explain overlapping register windows in RISC with example? 8
- b) Explain different interconnection structures in multiprocessor systems. 7
- a) What is cache coherence problem? Explain MESI protocol approach for the solution of this problem. 8
- b) Explain different types of hardware and software performance issues in multicore computers. 8

7. Write short notes on: (Any two)

- a) Register Transfer language (RTL)
- b) Dual and Quad Core Processor
- c) Addressing Modes

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Computer Architecture

Semester: Spring

Year : 2016
 Full Marks: 100
 Pass Marks: 45
 Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- (a) Write codes for the operation $Y = (A + B * C) / (E - F)$ using 3 -, 2 -, * 8
 1 – and 0 – address instruction format. 7
- b) Write RTI for fetch, indirect and interrupt cycles. 7
- a) Describe the basic ALU with its functional block diagram and operational truth table. 3
- b) Draw Booth multiplication algorithm and perform multiplication between 5 and -6. 8
- a) Design 2 bit array multiplier using combinational logic 7
- b) Explain the operation of microprogram sequencer used in microprogramming CU with its block diagram. 8
- a) Draw memory hierarchy with their relative characteristics and differentiate between SRAM and DRAM. 7
- b) Describe the principle of associative cache mapping with its merits and demerits. 7
- a) Explain DMA with flowchart and interconnection of DMA controller 7
 with processor, memory and I/O devices. 8
- b) Explain the major characteristics of CJSC with its shortcomings. 8
- c) Describe different interconnection structures in multiprocessor system. 7
- b) Describe hardware performance issues in multicore computer. 10
 2x5
- b) Write short notes on: (Any two) 8
- a) Hardwired CU
 b) Array Processor
 c) Control Hazard in Instruction Pipeline

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2017
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.

Attempt all the questions.

- a) The terms "computer architecture" and "computer organization" are same or different, explain with examples. 7
- b) Define RTL. Describe different types of Shift micro-operations. 8
- a) What is instruction cycle, explain instruction cycle state diagram with interrupt. 7
- b) Multiply using Booth's Algorithm: $(-11)_{10} * (15)_{10}$ 8
- a) Describe an algorithm used for the division of signed numbers. Find the result of $(-9)_{10}$ divided by $(2)_{10}$ using same algorithm. 8
- b) Explain hardwired implementation of control unit. List out advantages of using hardwired control unit. 7
- a) What is micro instruction sequencing? Explain single address field and variable format sequencing techniques used in micro-programmed implementation of control unit. 7
- How can use of cache memory improve performance in any computer system? Explain set-associative and direct mapping in cache. 6
- b) Define locality of reference. Differentiate between Static and Dynamic RAM. 6
- a) Define DMA. Explain DMA transfer modes. 7
- b) Define DMA. Explain DMA transfer modes. 8
- c) Compare RISC and CISC systems. Write the methods used in solving Compare RISC and CISC systems. 8
- a) What is cache coherence problem? 9
- b) What is cache coherence problem? 9
- the problem.
- Write short notes on: (Any two)
- a) Multi-core organization 8
- b) Parallelism in Uniprocessor System 8
- c) Register windows 8

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Spring

Year : 2017
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- a) ~~What is stored program concept, explain with reference to IAS computer.~~ 7
- b) ~~What is register in computer system? Explain different types of registers used in computer system.~~ 3 1+7
- a) ~~Perform multiplication of -5*2.~~ 7
- b) ~~Explain working principle of micro-programmed implementation of control unit. Why it is slower than hardwired implementation of control unit.~~ 5 6+2
- a) ~~Explain single address field and two address field sequencing techniques used in micro-programmed implementation of control unit.~~ 7
- b) ~~What is associative memory? Explain hardware organization of associative memory.~~ 6 2+6
- a) ~~How redundancy is achieved in RAID, explain with any two RAID levels.~~ 6 8
- b) ~~Explain the Input output module in computer system along with its block diagram, also write its importance.~~ 7 5+
- a) ~~Mention the need of use of large register file in RISC. Explain overlapping register windows in RISC with example?~~ 8 7
- b) ~~What is pipelining hazards? Explain structural and data hazard with solutions.~~ 8 9
- a) ~~Explain Flynn's classification, along with its general block diagrams.~~ 9
- b) ~~What is cache coherence? Explain any two methods of solving cache coherence problem.~~ 9

Write short notes on: (Any two)

- a) ~~Memory hierarchy~~
- b) ~~Register Transfer Language (RTL)~~
- c) ~~Dual core and Quad core processors~~

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE

Course: Computer Architecture

Semester: Fall

Year : 2018

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain different stages of computer evolution with reference of generation of computer. 7
- b) Explain instruction cycle state diagram with interrupt. 3
2. a) How overflow be detected in computer? Verify the operation (7) / (-3) using signed 2's complement method. 8
- b) Compare and Contrast between micro-program and hardwired control unit. Explain the micro program sequencer with example. 5
3. a) What is interrupt cycle? Explain how instruction be processed with interrupt in computer along with necessary diagram. 5
- b) What is m-way interleaving? Explain different types of memory interleaving. 7
4. a) Consider a system with main memory (MM) consisting of 8K blocks, a cache memory consisting of 256 blocks and a block size of 16 words- what will be the word field, block filed and Tag field length? How many bits are there in main memory address? If the system uses direct mapping and associative mapping techniques. 8
- b) What are the drawbacks of programmed I/O and interrupt driven I/O? Explain how DMA overcomes those drawbacks. 7
5. a) Assume that pipeline has K=8 segment and execute n=125 tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 8
- b) What type of hardware and software performance issues are seen in multi-core computers? Explain. 10

6. a) Explain different interconnection structures in multiprocessors. 9
b) What is cache coherence problem? Explain MESI protocol for solving cache coherence problem. 9

7. Write short notes on: (Any two)

a) RISC vs. CISC

b) Hardware Description language (HDL)

c) Logic Microoperation

POKHARA UNIVERSITY

Semester: Spring
Year : 2018
Level: Bachelor
Programme: BE
Course: Computer Architecture

Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.

Attempt all the questions.

- ✓ What are the characteristics of computer system? Draw and explain the basic computer organization in detail. 8
- ✓ What is RTL? Explain it when data transfer takes place between one and four bit register. 7
- ✓ How a floating point number is represented in computer system? Verify the operation $(9) \times (-2)$ using signed magnitude data 4. 8
- ✓ What is sequencer? Draw and explain the micro programmed control unit in detail. 5 7
- ✓ What is instruction cycle? Write the necessary micro-operations for fetch, decode, indirect and interrupt cycles 1. 8
- ✓ What is mapping? What are the different cache memory mapping techniques? 6 7
- ✓ What is DMA? Explain why DMA is used instead of interrupt driven and programmed I/O? 7
- ✓ What is instruction pipeline? Explain 3-segment instruction pipelining used in RISC computer. 8 8
- ✓ How a computer system can be classified according to Flynn's classification an arithmetic pipeline to speed up the computer to solve the expression $A_i * C_i + D_i$ for $i=0, 1, 2, 3, 4$. 9 7
- b) What are the functions of ISR? Explain how interrupt are processed in computer system. 7
- a) How floating point number can be added or subtracted using pipelining techniques? 8
- b) What are different interconnection structures when there are multiple 7

CPUs?

7. Write short notes on: (Any two)

~~x~~ Alternative Chip Organization

~~x~~ Types of registers

✓ Control memory organization and mapping logic

2x

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall Year : 2019
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.

Attempt all the questions.

- ✓ Explain the functional view of the computer system with reference to each component. 8 ✓
- ✓ How data can be transferred between registers? Explain in detail. 2 ✓
- ✓ Describe the arithmetic and logic circuit with its appropriate block diagram. 3 ✓
- ✓ Multiply $(14)_{10}$ and $(3)_{10}$ using unsigned binary multiplication method with data flow diagram. 4 ✓
- ✓ Perform $(-5) * (-3)$ using the Booth multiplication algorithm. 4 ✓
- ✓ Compare single and two address field addressing techniques used in micro-programmed implementation of control unit. 5 ✓
- ✓ Does hardwired implementation of Control Unit makes control unit fast or slow explain? Mention disadvantages of Hardwired implementation. 5 ✓
- ✓ What is associative memory? How match logic works for associative memory? 6 ✓
- ✓ Define DMA. Explain DMA controller with different DMA transfer modes. 7 ✓
- ✓ Explain the advantages of pipelining in the multiprocessor system. 8 ✓
- ✓ Explain the instruction pipeline with examples. 8
- ✓ Describe the cache coherency occur in multiprocessor system? What are the various ways to troubleshoot the problem? 9
- ✓ Explain Flynn's classification of computer system. 9
- ✓ Write short notes on: (Any two)
1. Explain RISC vs CISC
2. Optical disk
3. Multi Core Organization

POKHARA UNIVERSITY

Level: Bachelor

Programme: BE

Course: Computer Architecture

Semester: Spring

Year : 2019

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. **9** Explain the different evolutionary milestones in development of computer system. **1** 7✓
2. a) What are the different types of register used in computer system, explain with examples. **3** 8✓
2. a) Write the algorithm and perform multiplication of 9×3 using booth algorithm. **4** 8✓
2. b) Differentiate between micro programmed control and hardwired control unit? What are the techniques used to sequence microinstructions. **5** 7✓
3. a) What is instruction cycle? Explain various sub cycle of instruction cycle with micro-instructions involved in each sub cycle. **3** 8✓
3. b) Define virtual memory. Explain address mapping using pages in virtual memory. **6** 7
4. a) Explain how redundancy is obtained in RAID, with reference to any two RAID levels. What is the application of RAID? **6** 8
4. b) Explain, with an example, how effective address is calculated in Direct, Register indirect, Relative and Index addressing modes. (Assume necessary data if you need) **7** 7
5. a) What is mean by pipelining? Explain in brief about RISC pipelining? **8** 7✓
5. b) What is cache coherence problem? Explain methods of solving cache coherence problem. **9** 8
6. a) What are the various interconnected structure used for multiprocessor system? Explain them. **9** 7
6. b) Briefly explain the different performance issues in Hardware. **10** 8
7. Write short notes on: (Any two) 2×5
 - a) Register Transfer language (HDL) ✓
 - b) Future trends in computer ✓
 - c) Instruction pipelining

POKHARA UNIVERSITY

Level: Bachelor
Programme: B E
Course: Computer Architecture

Year : 2020
Semester: Fall
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- 1) Differentiate Computer Organization and architecture. Explain the various addressing modes. (2) 8 ✓
- 2) Define R TL. Explain about BUS and Memory transfer in R TL. (2) 7 ✓
- 3) Explain different types of registers used in computer system. What is use of register in computer system? (3) 8 ✓
- 4) Perform multiplication - $13 * 7$ using Booth's Algorithm. (4) 8 ✓
- 5) What are the various number representation method in computer system? (4) 7 ✓
- 6) Explain block diagram of micro programmed control organization and write down its advantages. (5) 8 ✓
- 7) Explain associative and set-associative mapping in cache memory? (6) 8 ✓
- 8) Explain interrupt with its classes in detail. Also explain about interrupt driven I/O. (7) 7 ✓
- 9) What is pipelining hazards? Explain structural and data hazard and its solution (8) 8
- 10) What is cache coherence problem? Explain software and hardware solution of cache coherence problem. (9) 7
- 11) Write about parallelism in computer system. Explain about symmetric multiprocessor in detail. (9) 8
- 12) Explain about the various Hardware Performance issues in Multicore Computers. (10) 8

- WYSIC storage devices (any two)
- ✓ Serial Magnetic tape (SMT) ②
 - ✓ Magnetic tape and disk ⑥ ✓
 - ✓ Differentiate between RISC and CISC ③ ✓

7. Write short notes on: (Any two)

- a) Shift Micro operations ②
- b) Magnetic tape and disk ⑥
- c) Differentiate between RISC and CISC. ⑧ ✓

POKHARA UNIVERSITY

Semester Spring

Year 2020

Full Marks 70

Pass Marks 35

Time 2 hrs

Course Bachelor
Program BE
Computer Architecture

Questions are required to answer in their own words as far as practicable.
The figures in the margin indicate full marks

Attempt all the questions.

Section - A: (5*10=50)

Q N 1 As a computer engineer you are studying the subject computer architecture, but the same course is being taught to electronics and communication engineering students as

the same course is being taught to computer architecture, so how do you differentiate between computer architecture?

Q N 2 Explain the roles of overlapped register window in RISC calculations.

Q N 3 What is Register Renaming? Explain the roles of overlapped register windows

Q N 4 Differentiate between Hardwired and Micro programmed Control Unit. Describe the pros and cons of programmed I/O and interrupt driven I/O and explain how DMA overcomes drawbacks of programmed I/O.

Q N 5 It is said that cache memory helps to improve the performance of computer system, in real world computer system big cache memory is of small size only, with different levels. Can we use a single bus based on how cache memory works?

Section - B: (2*10=20)

Q N 6 a) How can you say that "using pipeline to support your answer?" Perform the following signed multiplication (10) * (20) \downarrow

b) What is floating point?

\checkmark

POKHARA UNIVERSITY

Level: Bachelor

Programme: BE

Course: Computer Architecture

Semester: Fall

Year : 2022

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | | |
|-------|--|--------------|
| 1. a) | Discuss the term Computer Architecture. Explain IAS computer architecture with detailed diagram. | 8 |
| b) | Define addressing mode. Explain different addressing modes with appropriate figures and example of each. | 7 |
| 2. a) | Define RTL. How data can be transferred between registers. Explain. | 8 |
| b) | Define Instruction cycle. What are the different states in an instruction cycle? Also explain fetch cycle, decode cycle, execute cycle and indirect cycle. | 8 |
| 3. a) | Draw the flowchart for Booth's Algorithm. Use the algorithm for binary multiplication of (-12) and (-9). | 8 |
| b) | Explain single and two address field sequencing techniques in micro programmed control unit. | 7 |
| 4. a) | Differentiate between Hardwired and Micro-programmed control unit. Explain the logic of Hardwired unit. | 7 |
| b) | What is memory hierarchy? Explain with reason why do we need multilevel memory hierarchy? | 7 |
| 5. a) | Explain various communication techniques for I/O devices. | 8 |
| b) | Differentiate between various mapping techniques when main memory data is to be mapped into cache memory. | 7 |
| 6. a) | What is power efficient processor? Explain dual core processor with respect to quad core processor. | 8 |
| b) | Describe in brief about Flynn's Taxonomy. Also explain how parallelism can be experienced in uniprocessor systems. | 7 |
| 7. | Write short notes on: (Any two) | 2×5 |
| a) | RISC vs. CISC | |
| b) | Vector processors and Array processors | |
| c) | BCD Adder | |