

504

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE

Semester - Fall

Course: Logic Circuits

Year : 2010
Full Marks : 100
Pass Mark : 45
Time : 3 hrs

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

Define analog and digital Systems. Which system do you prefer 5 and why?

User's complement to subtract the following.

i. $(100010)_2 - (10101)_2$

5

ii. $(3857)_{10} - (1250)_{10}$

"Excess-3 code is self complementing code", how? 5

Find the complement of $F = X + YZ$; then show that $F \cdot F' = 0$ and $F + F' = 1$ 7

Simplify the following Boolean function to minimum no of 8 literal $f = AB' + B'C' + A'C'$. Implement the reduced form with basic gates and NAND gate only.

A Boolean function is given: 8

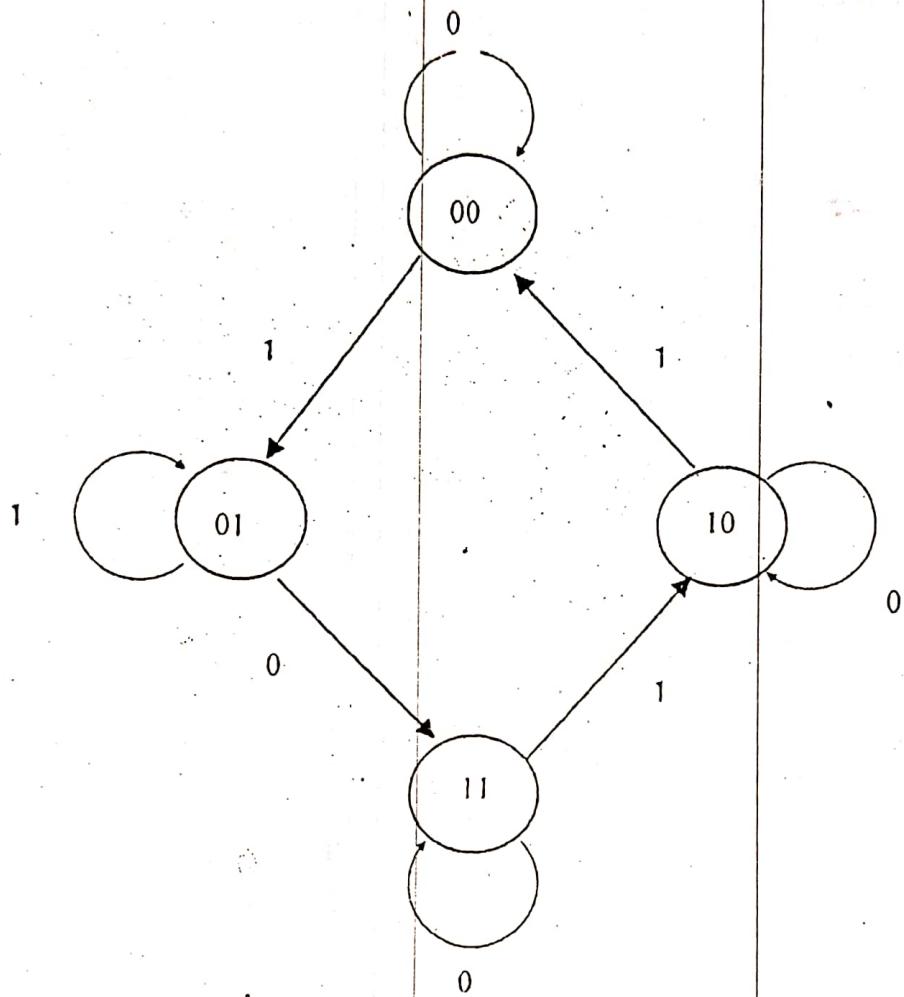
$F(A,B,C,D) = \Sigma(1,4,5,6,12,14,15)$ and don't care condition $d(A,B,C,D) = \Sigma(10,11)$. Simplify it using K-map. Replace all the gates with NAND gate only.

Design a combinational logic whose output is the 2's complement of the input number. 7

Draw the truth table for full adder. Implement full adder using two 4:1 MUX 8

Explain the operation of JK flip-flop with the help of 7 characteristics table. How it can be converted into T-flip-flop?

Realize the following state diagram into a circuit using J-K flip-flop. 10



- b. What is register? What is its use? Briefly explain the operation of - 5
serial-in-serial-out shift register using timing diagram.
6. a. Draw the block diagram of ALU and explain it. 7
b. Design a 4-bit arithmetic circuits which performs eight different 8
arithmetic operations.
7. Write short notes on (Any Two): 2×5
- a. Gray Code
 - b. Output Hazard Race
 - c. Multiplexer

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Attempt all the questions.

1. a. Perform the following operation. 5

i. $(10101)_{gray} = ()_2$

ii. $(756)_8 = ()_{16}$

iii. $(256)_{10} = ()_8$

iv. $(11011.111)_2 = ()_{10}$

v. $(3A.CD)_{16} = ()_{10}$

- b. Perform following subtraction using r's complement method. 5

i. $(2569)_{10} - (4382)_{10}$

ii. $(1010)_2 - (1100)_2$

- c. "Excess-3 code is a self-complementing code". Justify it. 5

2. a. Find the complement of $F=X+YZ$; then show that $F.F'=0$ and $F+F'=1$ 7

- b. Use K-map to simplify the given function and draw the logic diagram $F(w,x,y,z)=\sum(0,1,2,3,7,8,10)$ and the don't care conditions: $d(w,x,y,z)=\sum(5,6,11,15)$. Implement the simplified function using NAND gates only. 8

3. a. Design a code converter circuit which converts 8 4 -2 -1 code to binary. 8

- b. Show how a full adder can be converted to a full subtractor with the addition of one inverter circuit. 7

4. a. Design the 4 bit comparator circuit which compare two no A and B either $A < B$, $A > B$ or $A = B$. 8
- b. What is multiplexer? Describe 4:1 multiplexer with internal

5

7

8

2x5

diagram.

OR

What is Demultiplexer? Explain 8×1 DMUX with its circuit diagram.

5. a. Design a 4-bit synchronous down counter using J-K flip flop. 10
b. Present the truth table, logic diagram and characteristics 5
equation of J-K flip flop.
6. a. What is shift register? Explain different types of shift register. 7
b. Design a 4-bit arithmetic circuit and show its function table. 8
7. Write short notes on any two: 2x5
- a. Digital and Analog System
 - b. De- Morgan's theorem
 - c. State reduction and assignment
 - d. Design of shifter

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Attempt all the questions.

2x5

- a) Compare analog and digital system. Which one is better and why? 5
- b) Use r's complement to subtract the following: 5
 - i. $(100)_2 - (110000)_2$
 - ii. $(7850)_{10} - (7650)_{10}$
- c) What do you mean by alphanumerical code? "Excess- 3 codes are called self complementing code". Explain it. 5
- a) Simplify the Boolean function F and don't care conditions d in (1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given: 7
 - i. $F = A'B'D' + A'CD + A'BC$
 - ii. $d = A'BC'D + ACD + AB'D'$
- b) Design a code converter circuit which converts 8 4 -2 -1 code to binary. 8
- a) Design a circuit that compares two 3 bit numbers A and B to check if they are equal. The circuit has one output 'y' so that $y = 1$ if $A = B$ and $y = 0$ if $A \neq B$. 8

OR

Design a combinational circuit using a ROM. The circuit accepts a 3 bit numbers and generates an output binary number equal to the sum of the input numbers. 3

- b) What is multiplexer? Describe 4:1 multiplexer with internal diagram. 7
- a) Differentiate between combinational and sequential logic circuit. 5
- b) Implement a full adder using 3×8 decoder and OR gates. 5

- c) Give the truth table, logic diagram and characteristics equation of J-K flip flop. 5
5. a) Define shift registers. Explain operation of parallel in parallel out shift register. 8
- b) Design a 3-bit synchronous binary counter using T-flip-flop. 7
6. a) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations. 8
- b) Design a 4-bit combinational logic shifter and explain it. 7
7. Write short notes on any two: 2×5
a) Tristate logic
b) Output Hazard Race
c) Universality of 'NAND' and 'NOR' gate
d) Design of BCD adder

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Attempt all the questions.

- a. Perform the operation as indicated:
 - i. $(1010)_{\text{gray}} = (\dots)_{\text{2}}$
 - ii. $(2EB.7A)_{16} = (\dots)_{10}$
 - iii. $(225.225)_{10} = (\dots)_{\text{2}}$
 - iv. $(237.5)_8 = (\dots)_{16}$
- b. Describe the parity method of error detection with a suitable four bit system example. Also, write down its limitations. 7
- a. Explain the NAND gate as an universal gates. 7
- b. Reduce the expression $F(A, B, C, D) = \sum(0, 6, 8, 13, 14)$, and $d(A, B, C, D) = \sum(2, 4, 10)$. Express the simplified function in sum of minterms. 8
- a. Design a combinational circuit with three inputs and one output. The output is equal to logic 1 when the binary value of the input is less than 3. The output is logic 0 otherwise. 8

OR

Design a binary to gray code converter circuit using the minimum number of logic gates. Use the four variable input and four variable output case. 8

- b. Implement the following function with a multiplexer: 7

$$F = (A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$$

OR

A combinational circuit is defined by the following three functions. 7

$$F_1 = x'y' + xyz'$$

$$F_2 = x' + y$$

$$F_3 = xy + x'y'$$

Design a circuit with decoder and external gates.

4. a. What is the major difference between the synchronous and asynchronous logic. Explain about the JK flip flop with respect to truth table, k-map and characteristic equation. 2+5
- b. What do you mean shift register? Explain about parallel in parallel out shift register. 2+6
5. a. Explain the operation of D flip - flop with the help of the truth table, logic diagram and characteristic equation. 5
- b. Explain briefly about status register. 5
- c. State and prove De-Morgan's theorem. 5
6. a. Design a 4 bit arithmetic circuit. 7
- b. Design a 3 bit up down synchronous counter using JK flip flop which is capable of counting the both up and down sequences as desired by user. 8
7. Write short notes on any two: 2x5
- Analog and digital system
 - PLA
 - Venn diagram

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2+5
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2+6
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5
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Attempt all the questions.*

5
a) User's complement to subtract the following 5

$$\text{i. } (00101101)_2 - (10110101)_2$$

$$\text{ii. } (835701)_{10} - (569812)_{10}$$

8
b) Compare and contrast digital system with analog system. 5

c) Explain the parity method of error detection with a suitable example. 5

2x5
a) Realize all the basic gates using NOR gate only 5

b) Distinguish between minterms and maxterms. 5

c) What is processor unit? Draw it's block diagram. 5

a) Simplify the following Boolean function: 7

$$F(W,X,Y,Z) = \sum(1,6,7,8,11,13) \text{ with don't care condition}$$

$$d(W,X,Y,Z) = \sum(0,2,3,4,10,12) \text{ and then implement the function using NOR gates only}$$

b) Design a code conversion circuit which converts BCD to excess-3 code. 8

OR

Design a code converter circuit to convert 8, 4,-1,-2 code to gray codes. 8

a) Design a full Subtractor using two 4×1 MUX. 7

OR

Implement the following function using 8×1 multiplexer. 7

$$Y(A,B,C,D) = \sum(0,1,2,5,9,11,13,15)$$

b) Explain the following: 8

- | | | |
|----|---|-------|
| | i. Synchronous and asynchronous logic | |
| | ii. Combinational and sequential logic | |
| 5. | a) Explain the operation of a J-K flip flop along with its characteristic table. Write down its characteristic equation and graphic symbol.
What are the drawbacks of R-S flip flop? | 7 |
| | b) Design a 4 bit updown counter using T flip flop. | 8 |
| 6. | a) Describe the operation of a four bit shifter with a neat diagram. | 7 |
| | b) Discuss the purpose of shift register. Explain serial in parallel out and parallel in parallel out shift register. | 2+3=5 |
| 7. | Write short notes on any two:
a) State table and State diagram
b) PLA
c) State diagram and state table | 2×5 |

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Attempt all the questions.

2×5

- a) Compare and contrast analog and digital system.
b) Compute any four of the followings as indicated.

i. $(11101)_{gray} = ()_2$

ii. $(706)_8 = ()_{16}$

iii. $(512)_{10} = ()_8$

iv. $(110110.101)_2 = ()_{10}$

v. $(3FAFE.1BA)_{16} = ()_{10}$

- a) Perform the following operation using BCD method:

i) $689 - 354$

ii) $496 + 825$

- b) Discuss in brief about gray code.

- c) Explain the parity method of error detection with a suitable example.

- a) Discuss the universal property of NAND and realize all the basic gates using NAND gate only.

- b) Use K-map to simplify the given Boolean function in POS and implement the simplified function using NOR gate only.

$$F(A, B, C, D) = \sum(1, 3, 8, 9, 12, 13, 14, 15), \text{ and don't care}$$

$$d(A, B, C, D) = \sum(2, 7, 10)$$

- a) Design a code converter circuit which converts 8 4-2-1 code to binary.

Or

Design a circuit diagram to generate and check the Odd Parity.

- 115
- b) Derive a PLA program table for the combinational circuit that squares, 7
3 bit number.

Or

Implement the following Boolean functions using multiplexer

- $F(w, x, y, z) = \sum(0, 1, 3, 4, 5, 8, 9, 15)$
 - $F(x, y) = \sum(1, 2, 3)$. Also draw the internal circuit of the resulting multiplexer.
5. a) What is a shift register? With the help of timing diagram explain the operation of serial-in-serial-out shift register. 7
8
- b) What are the basic differences between combinational and sequential logic circuits. Explain the operation of a T flip-flop
6. a) Design an arithmetic circuit with two selection variables S_1 and S_0 that generates the following arithmetic operations. 8

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A$	$F = A + 1$
0	1	$F = A - B - 1$	$F = A - B$
1	0	$F = B - A - 1$	$F = B - A$
1	1	$F = A + B$	$F = A + B + 1$

- b) Design a 3-bit synchronous gray code up counter using D flip-flop. 8

Or

Design a 4 bit gray code synchronous counter .Using T flip-flop.

7. Write short notes on: (Any two) 2x5

- Venn diagram.
- Design of Accumulator.
- State reduction and assignment.
- Decoder and encoder.

POKHARA UNIVERSITY

— June

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Semester: Fall

Year : 2013

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Attempt all the questions.

1. a) Define analog and digital systems. Which system do you prefer and why? 7
- b) i) Subtract $(100101)_2$ from $(1111101)_2$ using 2's complement method. 8
- ii) Subtract $(7729)_{10} - (842.4)_{10}$ using 9's complement. 8
2. a) Explain the universal property of NOR gate with appropriate logic gates. 8
- b) Design a logic circuit to implement the Boolean function
 $F(A,B,C,D) = \sum(1,3,7,11,15)$
 $D(A,B,C,D) = \sum(0,2,5)$ in the term of
 - Sum of products
 - Implement with NAND-NAND gate only
3. a) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9'S complement of the input digit. 8

OR

- Design a combinational circuit which takes three input numbers and produces an output equal to square of the input.

- b) A combinational circuit is defined by the following three functions 7

$$F_1 = x'y' + xyz' \quad F_2 = x' + y \quad F_3 = xy + x'y'$$

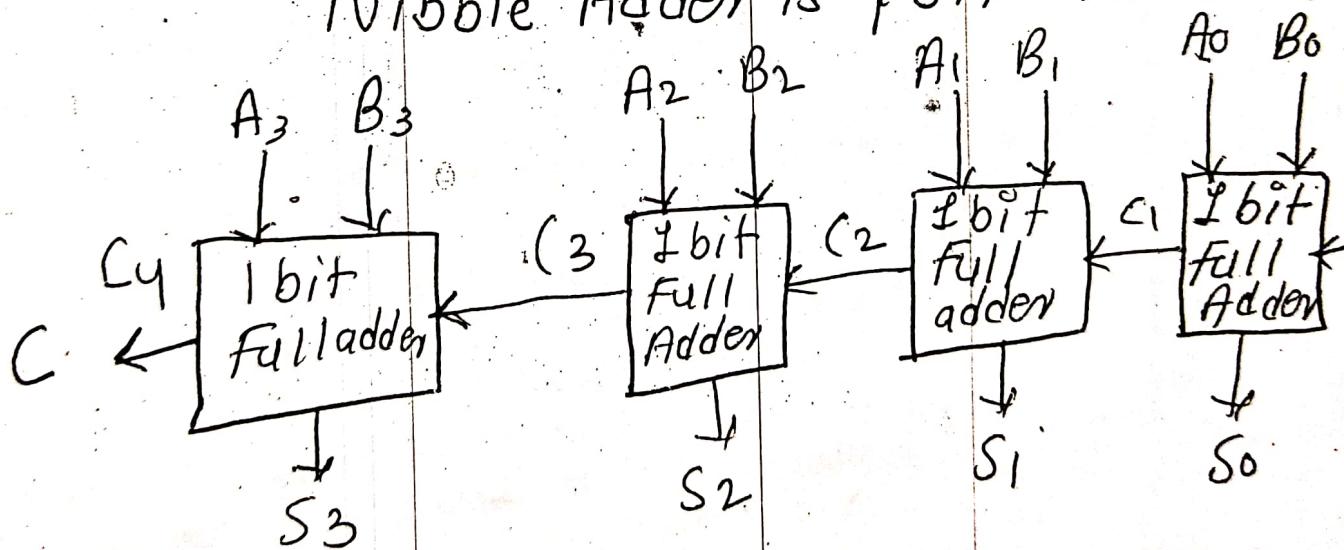
Design the circuit with a decoder and external gates.

- Give the truth table logic circuit and characteristic equation of J-K flip flop. How it can be converted into T flip flop. 7
- Design a counter with the following binary sequence 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use T flip flop. 8

5. a) Design an adder/subtractor circuit with one selection variable S and two inputs A and B. When S=0 the circuit performs A+B when S=1 the circuit performs A-B by taking the 2's complement of B.
- b) What is PLA? Derive the programming table for the combinational circuit that squares a 3-bit input number.
6. a) Explain in brief about:
- Gray code
 - Modulo 2 system.
- b) Differentiate between synchronous and asynchronous logic.
- c) What do you understand by output hazard races?
7. Write short notes on (Any two):
- Nibble Adder
 - Magnitude comparator
 - Master Slave flip-flop

Nibble Adder

Nibble Adder is 4 bit Adder.



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Attempt all the questions.

- a) Describe in brief why most of system in the present days has been converted to digital rather than analog.
- b) "8 4 -2 -1 code is self-complementing code." Justify this statement.
- c)
 - i) Perform the following subtraction $(34)_8 - (27)_8$ convert the given number into binary and perform subtraction using 2's complement.
 - ii) Determine the value of base x if $(321)_x = (57)_8$
- a) Design even parity generator when a 3 bit message contains cyclic code.
- b) Reduce the given expression in minimum number of literals using Boolean algebra and derive the truth table and implement in NAND logic.

$$A+B[AC+B\{AC+(B+C')D\}]$$
- a) A logic circuit implements the following Boolean function $F = A'C + AC'D'$ It is found that the circuit input combination $A=C=1$ can never occur. Using K-map with proper don't care conditions, find a simplified expression and implement it using NAND gates only.
- b) Derive a PLA program table for the combinational circuit that squares 3 bit number minimize the number of product term.
- a) Differentiate between PLA and ROM. Implement the given four Boolean function using 8×4 PLA

$$\checkmark A(x, y, z) = \Sigma(1, 2, 4, 6)$$

$$B(x, y, z) = \Sigma(0, 1, 6, 7)$$

$$C(x, y, z) = \Sigma(2, 6)$$

$$D(x, y, z) = \Sigma(1, 2, 3, 5, 7)$$

- b) Explain in detail about the positive edge triggered J.K flip-flop. Write its advantage over S-R flip-flop. 8
5. a) With suitable example explain about state reduction and assignment. 7
Also, write the advantages of state reduction and assignment.
- b) What is shift register? Explain the operation of serial-In serial out shift register with its circuit diagram and timing diagram. 8
6. a) Design a 3 bit synchronous binary up counter using JK flip-flop. 8
b) Design a 4-bit arithmetic circuits which performs eight different operations. What do you mean by 'Output Hazard Races'? With the help of diagram explain how Read/Write operation is performed in RAM. 7
7. Write short notes on: (Any Two) 2x5
- a) Status Register
 - b) Nibble Adder
 - c) Master Slave f/f.

$$1 + \bar{B} = \bar{B}$$
 complement law.

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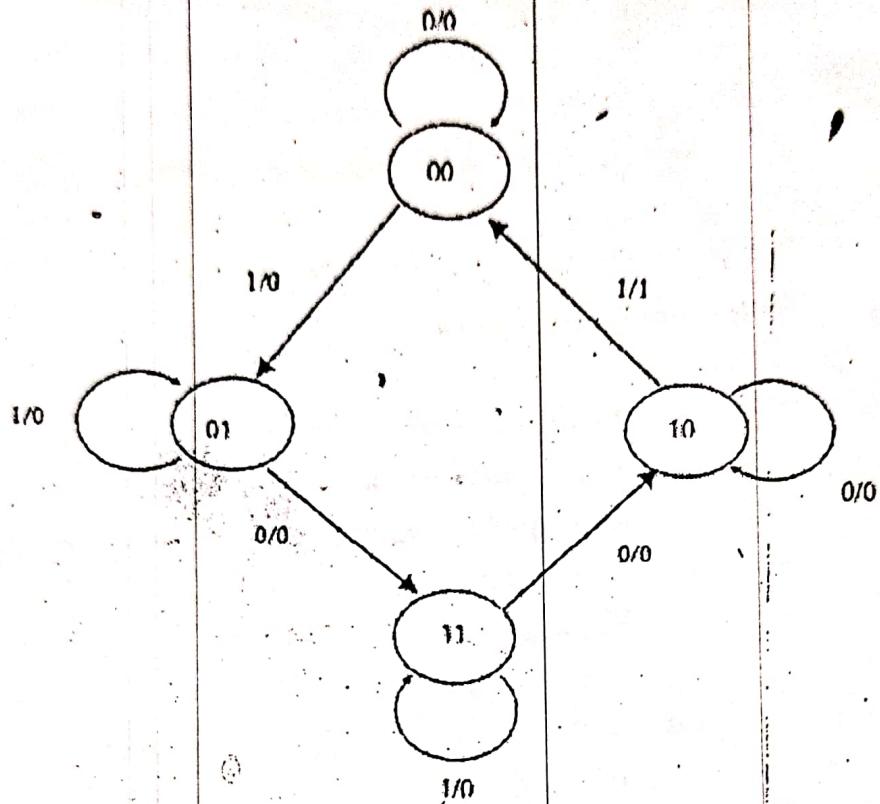
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Attempt all the questions.

1. a) What are the differences between Digital and Analog system. Why digital systems are preferred rather than Analog system. 5
- b) Add and multiply the following number in the given base without converting to decimal.
- $(1230)_4$ and $(23)_4$
 - $(135.4)_6$ and $(43.2)_6$
- c) Perform the following conversion. 5
- $(5849)_{10} = (\quad)_{\text{Excess-3}}$
 - $(8412)_{10} = (\quad)_{2421}$
 - $(10101111)_{\text{GRAY}} = (\quad)_2$
2. a) Simplify the following expression using Boolean algebra 5
- $(AB' + ABC)' + A(B + AB')$
 - $[(BC' + A'D)(AB' + CD')]$
- b) Given the following Boolean function: $F = xy + x'y' + y'z$ 5
- Implement it with OR and NOT Gate
 - Implement it with only AND and NOT Gate
- c) A Boolean function is given by $F(A,B,C,D) = \sum(3,4,5,7,9,13,14,15)$ 5
 and don't care condition $d(A,B,C,D) = \sum(0,2,8)$. Simplify it using K-Map and implement using NAND gate only.
3. a) Design a combinational circuit that converts a decimal digit from the 2421 code to 84-2-1 code to binary. 8
- b) Design a BCD to Excess -3 code converter circuit. 7
4. a) Design a Comparator circuit that compared two 4 bit numbers. The two numbers being A and B. It is required to obtain three possible

outcomes, i.e., $A > B$, $A < B$ and $A = B$.

- b) Implement the following with appropriate MUX:
i. $F(A,B,C) = \sum(1,3,5,6)$
ii. $F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$
5. a) Design a sequential circuit corresponding to the given state diagram using S-R flipflop. 8



- b) Explain operation of J-K Flip-flop with its logic diagram and truth table. 7
6. a) What is counter? Explain its any one of its type in brief. 8
b) Design 4-bit logical circuits which perform eight different logical operations. 7
7. Write short notes on: (Any two) 2x5
- Parity checker
 - Output Hazard Races
 - Status Register

7 Level: Bachelor

Semester: Spring

Year

Full Marks: 2014

Programme: BE

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Course: Logic Circuit

Time

3 hrs.

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Attempt all the questions.

- a) Define positive and negative logic system. "Digital circuits are easier to design than analog circuit." Do you agree with this statement? Give reasons to support your answer.

- b) Find the value of X:

i) $(777)_x = (212)_8$

ii) $(DEC)_H = (0101)_x$

iii) $(563)_7 = (X)_3$

iv) $(100111)_{\text{Gray}} = (X)_{\text{Binary}}$

- a) State and Prove De-Morgan's Theorem. List out the factors to be considered while constructing the Logic Gates.

- b) What is Don't care condition? Simplify given function using K-map with circuit design.

$$F(W, X, Y, Z) = \Sigma(1, 4, 5, 6, 12, 14, 15) \quad \text{and} \quad \text{don't care condition}$$

$$D(W, X, Y, Z) = \Sigma(10, 11)$$

- a) Define universal gate. Design the three bit EX-OR circuit using only Universal gates.

- b) Design a combinational circuit that accepts a 3 bit number as input and generates the output binary number equal to the 2's complement of input number.

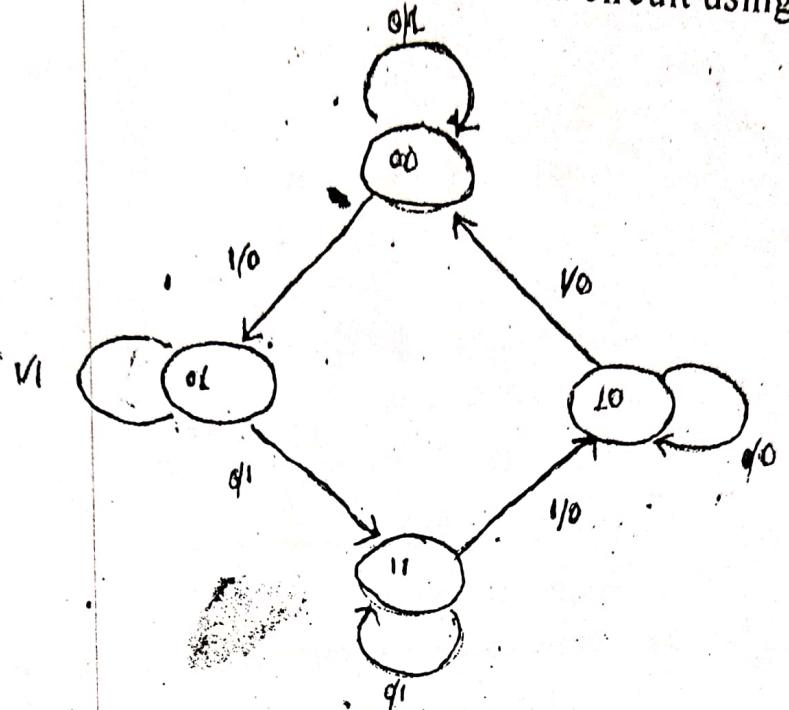
- a) Show how a full adder can be converted to a full subtractor with the addition of one inverter circuit.

- b) Implement the following :

i. $F(A, B, C) = \Sigma(1, 3, 5, 6) \quad (\text{using MUX})$

ii. $F1 = \Sigma(0, 2, 5), F2 = \Sigma(3, 4, 7), F3 = \Sigma(6, 7) \quad (\text{using ROM})$

5. a) Realize the following state diagram into a circuit using j-k flip-flop.



- b) Describe read and write operation in RAM with diagram. Draw a circuit for 6-bit SIPO shift register.
6. a) Design an arithmetic circuit with one selection variable and two data inputs A and B. When $S=0$, the circuit performs the addition operation $F = A+B$ when $S=1$, the circuit performs the increment operation $F = A+1$ (only show the block diagram).
- b) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations.
7. Write short notes on: (Any two)
- Master slave flipflop.
 - Nibble Adder.
 - PLA.

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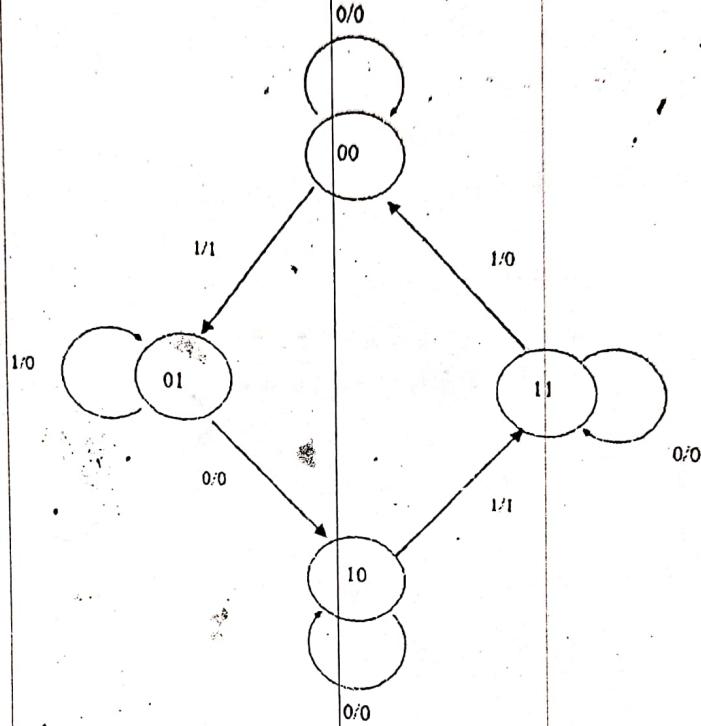
Attempt all the questions.

1. a) Which system is more efficient for logical computation? Differentiate between Digital and Analog system. 5
 - b) Perform the conversion as indicated (any two). 5
 - i. $(243)_6 = ()_{\text{Excess-3}}$
 - ii. $(816)_{10} = ()_{2421}$
 - iii. $(BE)_{16} = ()_2$
 - c) Use 2's complement to subtract the following: 5
 - i. $(101)_2 - (10100)_2$
 - ii. $(3950)_{10} - (876)_2$
 - iii. $(378)_{BCD} - (256)_{BCD}$
2. a) Prove the following Boolean expression. 5
 - i. $\overline{AB} + BC + \overline{ABC} = \overline{A} + BC$
 - ii. $X\overline{Y} + Y\overline{Z} + Z\overline{X} = \overline{XY} + \overline{YZ} + \overline{ZX}$
 - b) Simplify the Boolean function F and don't care conditions d in (1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given: 5

$$F = A'B'D' + A'CD + A'BC$$

$$d = A'BC'D + ACD + AB'D'$$
 - c) A Boolean function is given by $F(A,B,C,D) = \sum(3,4,6,8,10,12,14)$ and don't care condition $d(A,B,C,D) = \sum(0,2,8)$. Simplify it using K-Map and implement using NAND gate only. 5
3. a) Design a single combinational logic circuit that performs the addition of two input bits (a and b) when third input bit c is set to 0 whereas, the same circuit performs the subtraction of same two input bits when c is set to 1. 7

4. a) Design a BCD synchronous up counter using T-flip flop. 8
- a) Implement the following three Boolean function with a PLA 8
- $$F_1 = \sum(0,1,2,4) \quad F_2 = \sum(0,5,6,7) \quad F_3 = \sum(0,3,5,7)$$
- b) What do you mean by Decoder? Implement the following Boolean function $F = \sum(1,3,5,6)$ using $4 * 1$ MUX. 7
5. a) Design a sequential circuit corresponding to the given state diagram using D Flip Flop for the following state diagram. 8



- b) Explain operation of J-K Flip-flop with its logic diagram, truth table, excitation table. 7
6. a) What is counter? Differentiate between serial in serial out register and parallel in serial out register with associated diagrams. 8
- b) Illustrate the process how does binary value of 4 flags in status registers change with necessary diagram. 7
7. Write short notes on: (Any two) 2x5
- a) Random Access Memory.
- b) Self complementing code.
- c) Universal Gates.

Level: Bachelor

Semester: Spring

Year

: 2015

Programme: BE

Full Marks: 100

Course: Logic Circuit

Pass Marks: 45

Time

: 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

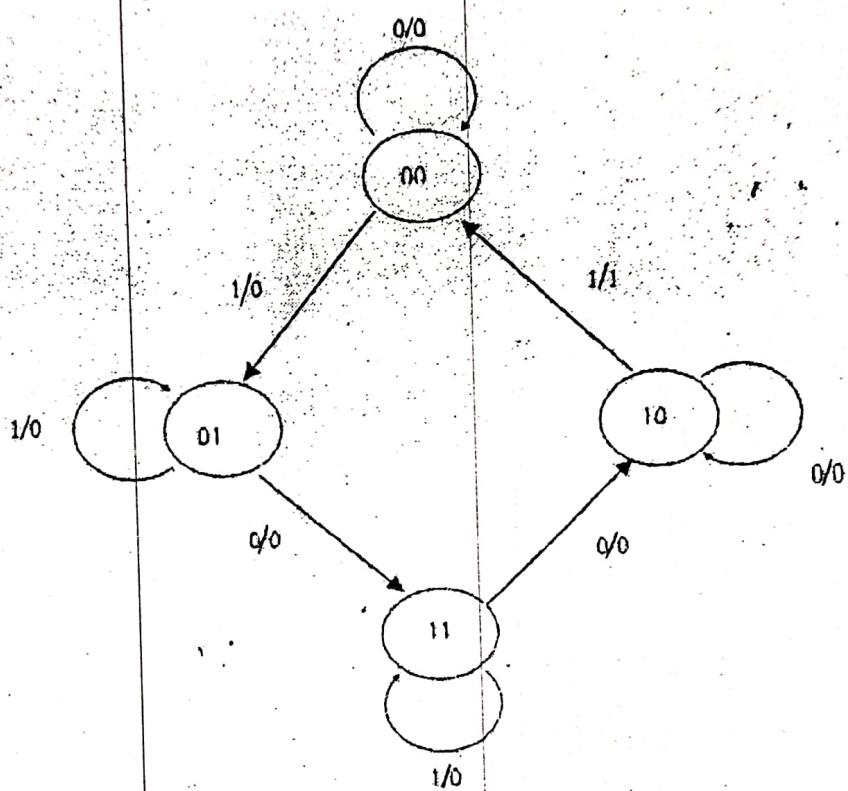
The figures in the margin indicate full marks.

Attempt all the questions.

1. a) How can we represent the information? Differentiate between Digital and Analogue system.
b) Perform the following conversion.
 - i. $(573)_{10} = (?)_{\text{Excess-3}}$
 - ii. $(842)_{10} = (?)_{2421}$
 - iii. $(10101111)_{\text{GRAY}} = (?)_2$
 - iv. $(FAB)_{16} = (?)_2$
2. a) Simplify the following expression using Boolean algebra
 - i. $(AB' + AB'C')' + A(B' + AB')$
 - ii. $[(BC' + A'D)(AB' + C'D')]$b) Simplify the Boolean function F and don't care conditions (1) SOP (2) POS and (3) draw NAND-NAND equivalent logic. Given:
 - i. $F = A'B'D' + A'CD + A'BC$
 - ii. $d = A'BC'D + ACD + AB'D$c) A Boolean function is given by $F(A,B,C,D) = \sum(3,4,6,8,10,12,14)$ and don't care condition $d(A,B,C,D) = \sum(0,2,8)$. Simplify it using K-Map and implement using NAND gate only.
3. a) Design a combinational circuit that converts a decimal digit from the 2421 code to 84-2-1 code to binary.
b) Design a circuit for 4 bit full Subtract adder.
4. a) Design a comparator circuit that compares two 4 bit numbers. The two numbers being A and B. It is required to obtain three possible outcomes. i.e., $A > B$, $A < B$ and $A = B$.

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- b) Implement the following with appropriate MUX:
- $F(A,B,C) = \sum(1,3,5,6)$
 - $F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$
5. a) Design a sequential circuit corresponding to the given state diagram using J-K flip flop.



- b) Design a counter with the following binary sequence 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use T flip flop.
6. a) Design an adder/subtractor circuit with one selection variable S and two inputs A and B. When $S=0$ the circuit performs $A+B$ when $S=1$ the circuit performs $A-B$ by taking the 2's compliment of B.
- b) Design a 4-bit arithmetic circuit which performs eight different arithmetic operations.
7. Write short notes on: (Any two)
- Magnitude comparator
 - Universality of NAND and NOR gates
 - Output Hazard Races

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Logic Circuits

Semester: Fall

Year : 2016
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Attempt all the questions.

What is Digital and Analog systems? Also list out the advantages of digital system over the analog system. 7

Perform the conversion as indicated 8

- i. $(243)_6 = ()_{\text{Excess-3}}$
- ii. $(816)_{10} = ()_{2421}$
- iii. $(BE)_{16} = ()_2$
- iv. $(777)_x = (212)_8$

Implement XNOR gate using only NAND gates and XOR gate using NOR gate only. 7

Define Literal & term. Find Canonical SOP for this expression 8
 $F = \overline{a}\overline{c} + \overline{a}\overline{b} + \overline{b}\overline{c}$.

Design a combinational circuit that converts a decimal digit from the 2421 code to BCD. 8

A Boolean function is given: $F(w,x,y,z) = \Sigma(1,4,5,6,12,14,15)$ and don't care condition $d(w,x,y,z) = \Sigma(1011)$. Simplify it using K-map with logic gate implementation. 7

Design a comparator circuit that compared two 4 bit numbers. The two numbers being A and B. It is required to obtain three possible outcomes. i.e . $A > B$, $A < B$ and $A = B$. 8

Realize the following state diagram into a circuit using T- flip-flop. 7

POKHARA UNIVERSITY

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Attempt all the questions.

1. a) Define Analog and Digital System. Why digital systems are preferred over Analog system. 5
 - b) Convert the following numbers from the given base to the other bases 1+2+2 as indicated
 - i. $(11001.11)_2 = ()_8$
 - ii. $(5FE.DD)_{16} = ()_{10}$
 - iii. $(777)_8 = ()_{16}$
 - c) Perform the subtraction with the following Binary number using 1's Complement
 - i. $1010100 - 1000100$
 - ii. $1000100 - 1010100$
 2. a) State and Prove De-Morgan's Theorem. Briefly explain the factors to be considered while constructing the Logic Gates. 8
 - b) What is don't care condition? Simplify given function using K-map and implement it in a circuit. 7

$F(W,X,Y,Z) = \Sigma(1,4,5,6,12,14,15)$ and don't care condition
 $D(W,X,Y,Z) = \Sigma(11,13)$.
 3. a) Design a combinational circuit that accepts a 4 bit number as input and generates the output binary number equal to the 2's complement of input number. 8
- OR**
- Design a circuit for 3-bit parity generation and 4-bit parity checker using even parity. 7
 - b) Explain in detail about synchronous Up/Down counter. 7
 - a) Define the term LSI and MSI. Design 3:8 decoder with its logic circuit 7

and block diagram.

- b) Implement the following :

i. $F(A,B,C) = \sum(1,3,5,6)$

(using MUX)

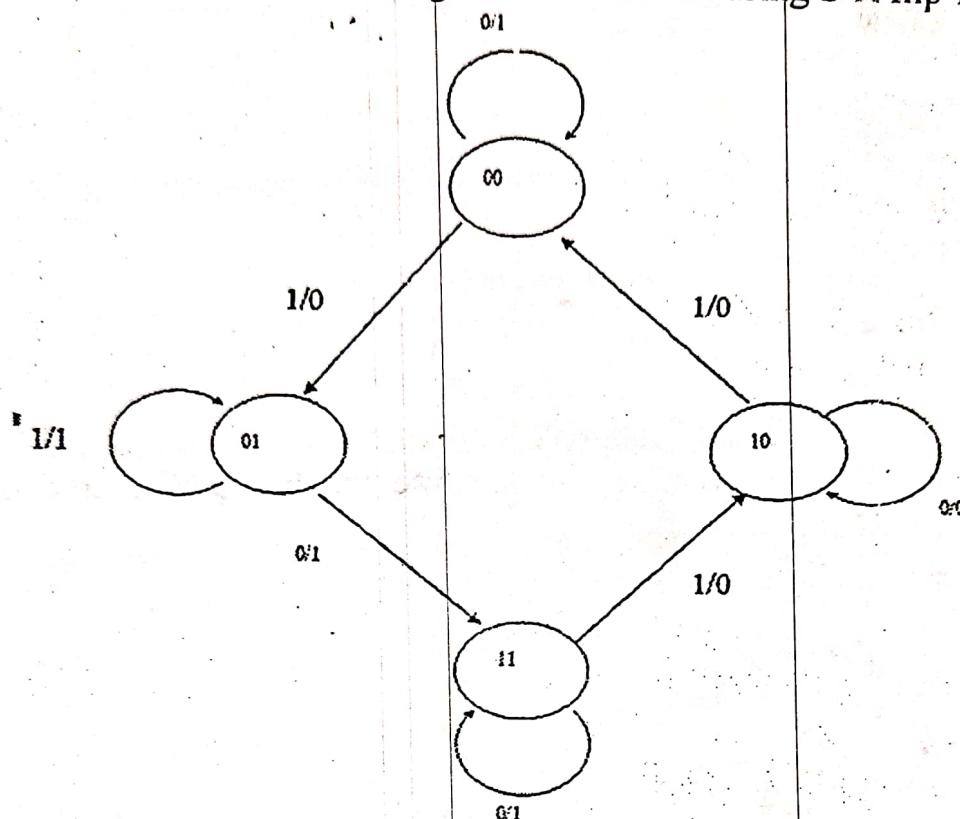
ii. $F1 = \sum(0,2,5)$ $F2 = \sum(3,4,7)$ $F3 = \sum(6,7)$

(using ROM)

8

5. a) Realize the following state diagram into a circuit using S-R flip-flop.

8



- b) Explain operation of J-K Flip-flop with its logic diagram and truth table. 7

- a) Design Arithmetic Logic Unit (ALU) that performs 8 Arithmetic operation and 4 different logical operations. 8

- b) Design a MOD 11 asynchronous counter using J k flip flop and showing with its working, counting sequence and timing diagram. 7

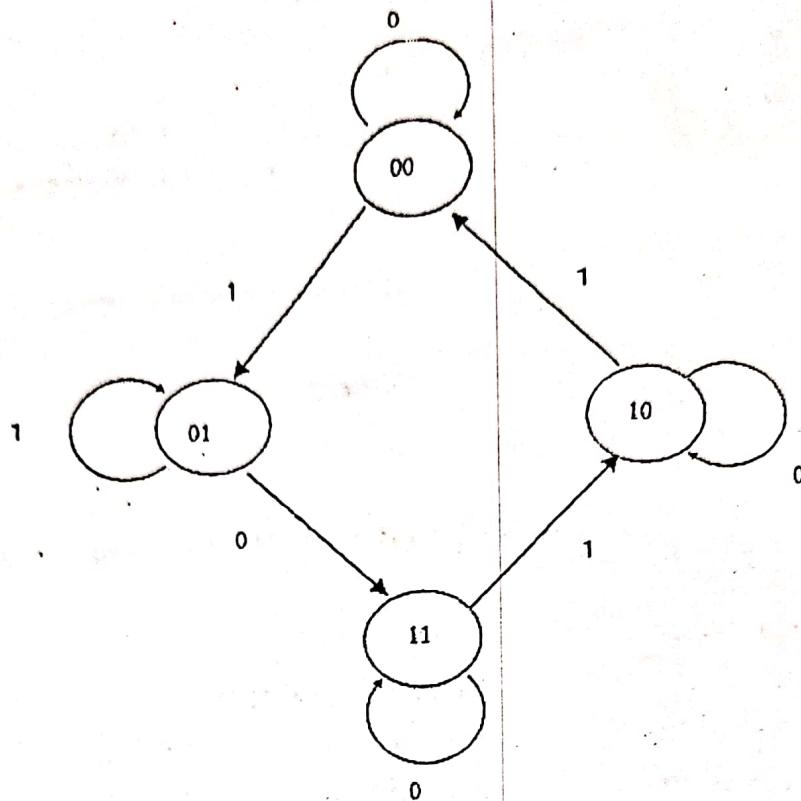
OR

What is shift register? Explain the SISO shift register with circuit diagram.

Write short notes on: (Any two) 2×5

- a) Parity method for error detection
b) SOP and POS
c) PLA
d) Nibble Adder

2



5. a) What are major 5 different between synchronous and asynchronous counters? Design a 4-bit up-down binary counter. 8
- b) What is counter? Differentiate between serial in serial out register and parallel in serial out register with associated diagrams. 7
6. Design an arithmetic circuit with two selection variables, s_1 and s_0 , that generates the following arithmetic operations. Draw the logic diagram of one typical stage. 11

s_1	s_0	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A+B$	$F = A+B+1$
0	1	$F = A$	$F = A+1$
1	0	$F = B'$	$F = B'+1$
1	1	$F = A+B'$	$F = A+B'+1$

7. Write short notes on: (Any two) 2
- a) Shift register
- b) D-flip flop
- c) PLA

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Logic Circuits

Semester: Fall

Year : 2017
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Attempt all the questions.

- a) 'Gray code is also known as reflected code'. Justify your answer with appropriate illustration. 5
- b) Determine the value of base x if $(211)_x = (152)_8$. 5
- c) Realize all the basic gates using NAND gate only. 5
- d) Use K-map to simplify the given Boolean function in SOP form and implement the simplified function using NAND gate only. 7
- F(A, B, C, D) = $\sum(5, 7, 9, 12, 13, 14, 15, \text{don't care})$ and don't care, d(A, B, C, D) = $\sum(3, 6, 8)$ 4+4
- b) Design a circuit of a 3-bit parity generator and the circuit of a 4-bit parity checker for odd parity. 4+4

OR

- Design a combinational circuit that has four inputs and two outputs one of the outputs is high when majority of inputs are high. The second output is high only when all inputs are of same type. 8
- a) With the help of an example, show how you can construct a higher order MUX using two or more number of lower order MUXs. 8
- b) Implement a full adder circuit with the help of two half adder circuit along with the truth table. 7
- a) Explain the operation of clocked R-S flip-flop with the help of its logic diagram, characteristic table and characteristic equation. 8
- b) Differentiate RS and JK flip flop. 7
- b) Design a synchronous 4 bit binary up counter using T flip flop which counts all possible odd numbers. 7

OR

- What is a modulo-7 counter? Design such a counter using JK flip-flop. 2+5

POKHARA UNIVERSITY

Level: Bachelor
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Semester: Fall

Year : 2018
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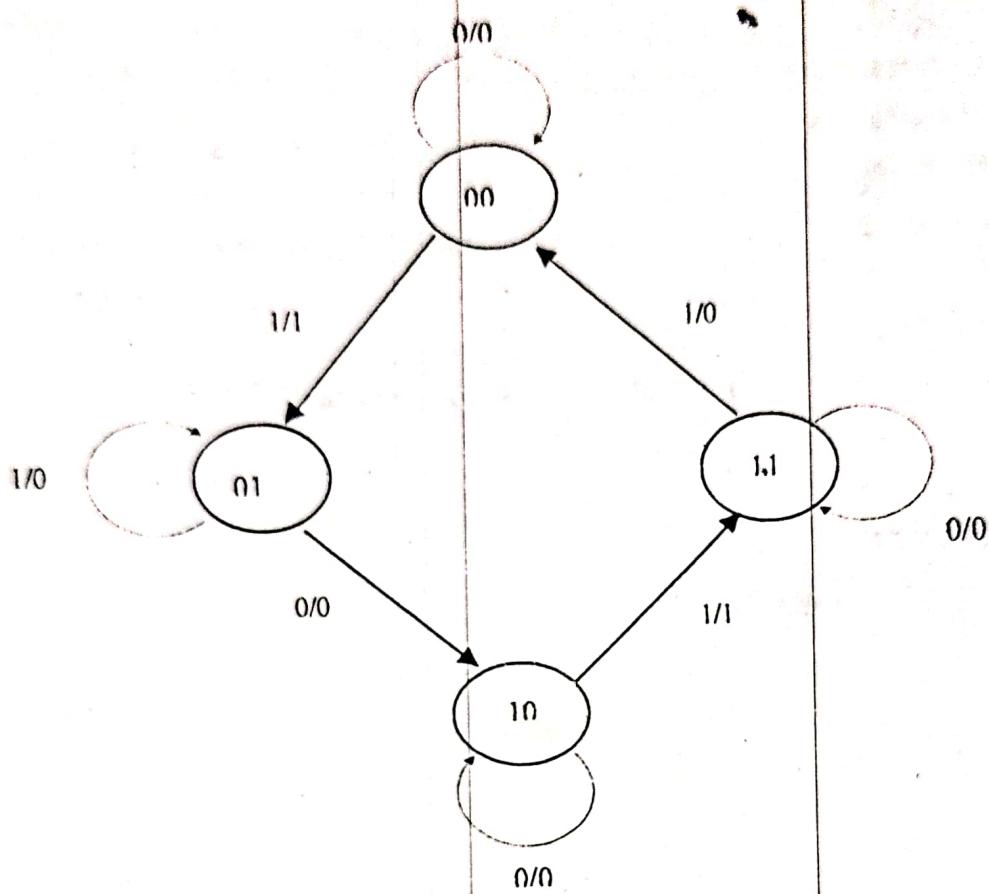
Attempt all the questions.

- | | | |
|----|--|---|
| 1. | a) Define Analog and Digital Signal. Differentiate digital system and Analog system. | 4 |
| | b) Convert the following conversions: | 8 |
| | i. $(101001.101)_2 = (?)_{10}$ | |
| | ii. $(ABD)_{16} = (?)_8$ | |
| | iii. $(10101101)_2 = (?)_{\text{gray}}$ | |
| | iv. $(175.351)_8 = (?)_{16}$ | |
| | c) Define logic gates. Explain the universality of NAND and NOR gates. | 3 |
| 2. | a) Why NOR gate is called universal gate? State and prove De-Morgan's theorem. | 8 |
| | b) Use K-map to simplify the given Boolean function with don't care condition and realize it using basic gates only: $F = \sum(1, 4, 8, 12, 13, 15)$ and $d = \sum(3, 7, 11, 14)$. | 7 |
| 3. | a) Design a combinational logic circuit that has four input and two outputs. One of the outputs is high when majority of inputs are high. The second output is high only when all inputs are of same type. | 8 |
| | b) Design a circuit for 3-bit parity generation and 4-bit parity checker using odd parity. | 7 |
| 4. | a) A combinational circuit is defined by the function, | 8 |
| | $F_1(A, B, C) = \sum(3, 5, 6, 7)$ | |
| | $F_2(A, B, C) = \sum(0, 2, 4, 7)$, implement by using PLA. | |
| | b) What is magnitude comparator? Design a two bit magnit | |

comparator whose outputs are $A > B$, $A < B$ and $A = B$.

5. a) Design a sequential circuit corresponding to the given state diagram using S-R FlipFlop for the following state diagram.

8



- b) With necessary logic diagram, truth table, excitation table, explain the operation of J-K flip flop.

7

6. a) What is shift register? Explain serial in parallel out and parallel in parallel out shift registers.

7

- b) Design a 4-bit arithmetic circuits which performs eight different arithmetic operations.

8

7. Write short notes on: (Any two)

2x5

- a) Counters
- b) Master -slave Flip Flop
- c) Nibble Adder

- 3
5. a) What do you mean by ALU? Design an arithmetic circuit to implement the following function table. A and B are 4 bit binary numbers.

S1	S0	Cin	F
0	0	0	A
0	0	1	$A+1$
0	1	0	$A+B$
0	1	1	$A+B+1$
1	0	0	$A+B'$
1	0	1	$A-B$
1	1	0	$A-1$
1	1	1	A

- b) What is a shift register? Draw the block diagram for shifting the content of register A to register B. Describe the operation.
6. Compare and contrast *any three* of the following:
- Synchronous and asynchronous logic.
 - Decoder and encoder
 - XOR and XNOR gates
 - Analog versus Digital System
7. Write short notes on: (Any two)
- Accumulator
 - Don't care conditions
 - Parity method for error detection
- 7
- 8
- 2x5
- 2

POKHARA UNIVERSITY

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Semester: Spring

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Attempt all the questions.

- a) How does the logic system express data during computation? 5
 Differentiate between Digital and Analog system.
- b) Perform the conversion as indicated (any two). 5
- $(235)_6 = ()_{\text{Excess-3}}$
 - $(369)_{10} = ()_{2421}$
 - $(BCA)_{16} = ()_2$
- c) Use 2's complement to subtract the following: 5
- $(1010)_2 - (10100)_2$
 - $(957)_{10} - (876)_{10}$
 - $(378)_{\text{BCD}} - (256)_{\text{BCD}}$
2. a) Why NAND and NOR are called Universal Gates? Construct $F=AB+CD$ using universal gates. 7
 b) Define K-Map. Simplify the expression mentioned below using K-Map. 8
- $$F(A, B, C, D) = \sum(1, 3, 7, 10, 13, 15)$$
- $$d(A, B, C, D) = \sum(0, 2, 8)$$
- Where d denotes don't care. Also implement the simplified function using NOR gates only.
3. a) Design a combinational circuit that has four inputs and two outputs one of the outputs is high when majority of inputs are high .The second output is high only when all inputs are of same type. 7
 b) Implement the following Boolean function using 16:1 Multiplexer

$$F(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$$
4. a) Design a 4 bit parallel adder subtractor circuit with one selection variables M and two inputs A and B. For $M = 0$, the circuit required to

perform addition i.e. $(A+B)$ and for $M = 1$, the circuit must perform subtraction $(A - B)$ by taking 2'S complement of B.

- b) Explain negative edge triggered S-R flip-flop with necessary logic diagram, characteristic table, characteristic equation and waveform. 8
5. a) Design a synchronous Mod-6 counter using clocked D Flip Flop 8
b) Define shift register. Draw diagram for parallel in serial out shift register and discuss its operation with necessary explanation. 7
6. a) Explain the process how does binary value of 4 flags in status register change with necessary diagram. 8
b) Design a 3-bit Synchronous DOWN Counter using T flip-flop. 7
7. Write short notes on: (Any two) 2x-
- a) State Reduction and State Assignment
 - b) Random Access Memory
 - c) Self-complementing code