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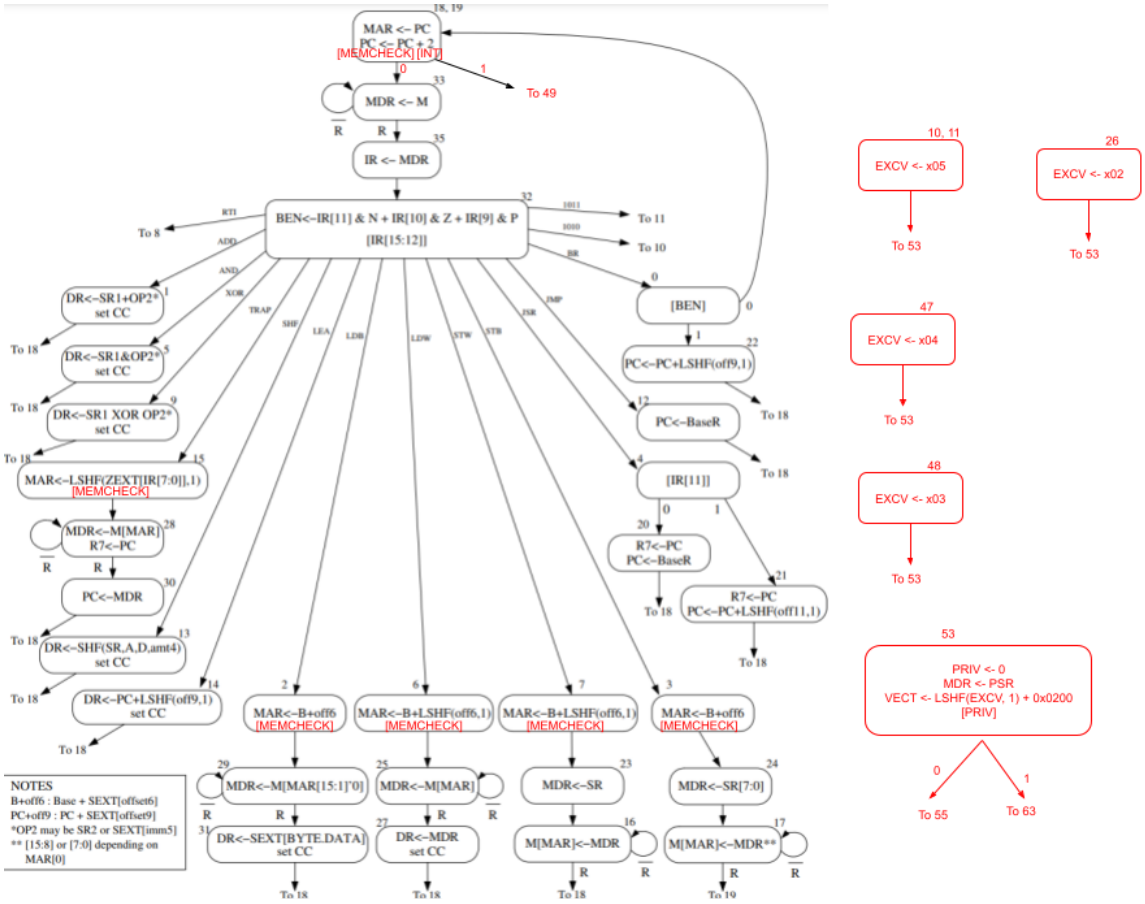
Lab 5 Readme

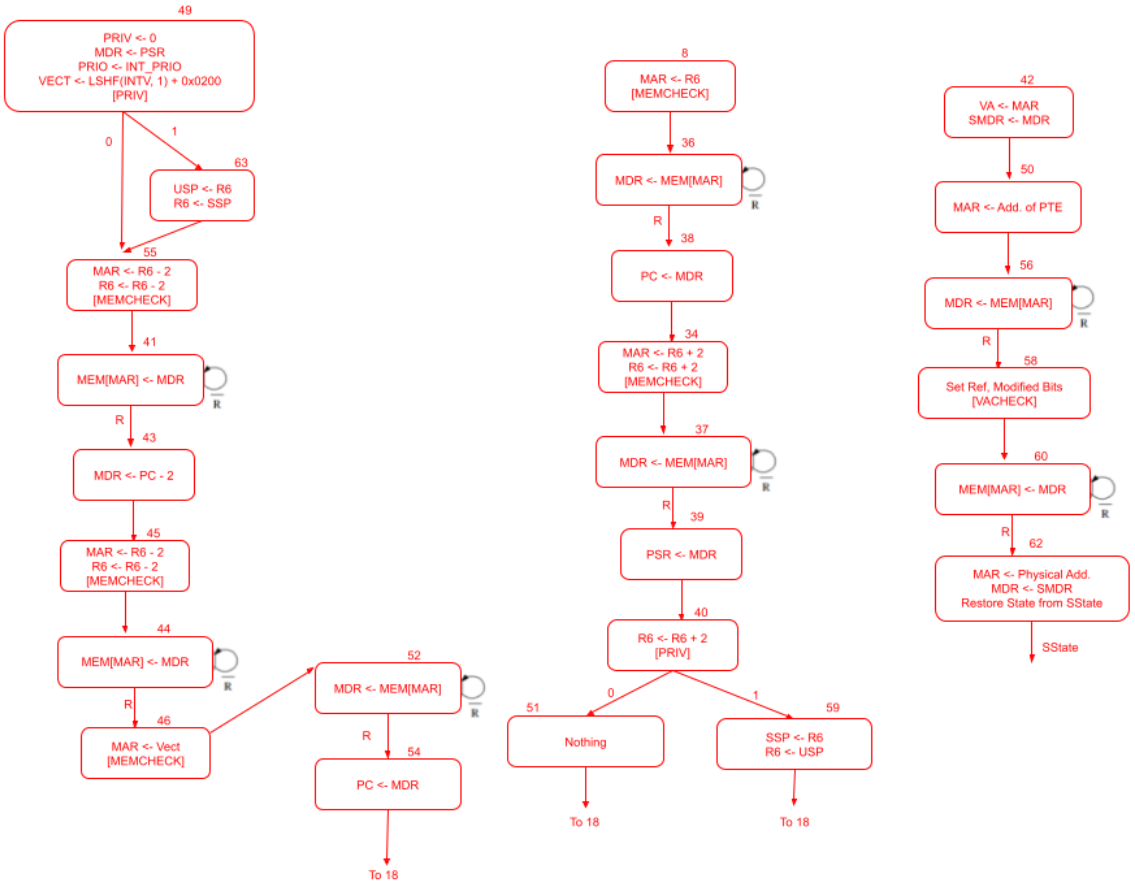
State Diagram

The [MEMCHECK] assertion saves the current state and sends the next state to 42 for virtual address translation.

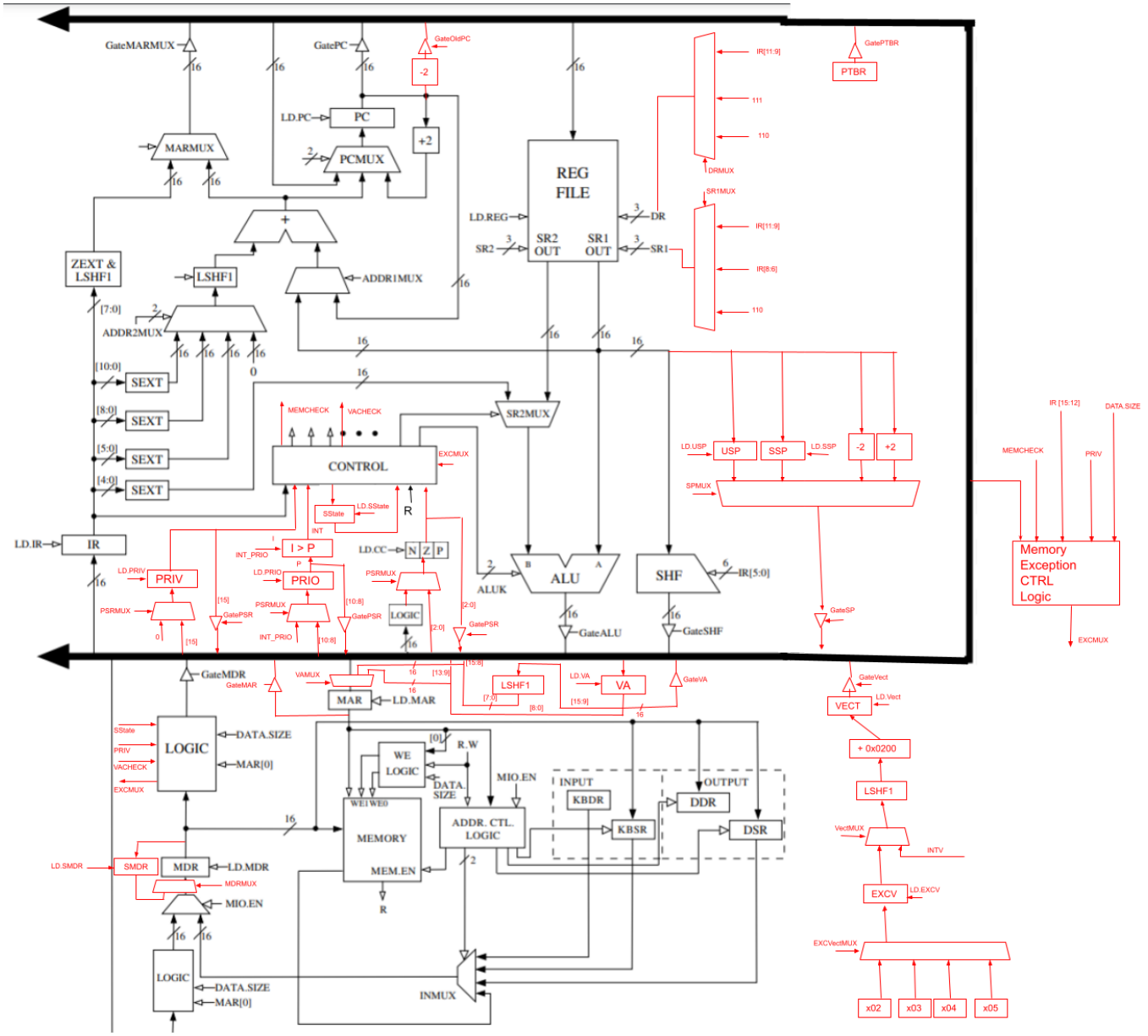
State 42 is the beginning state for the virtual address translation. The saved state is then returned to at the end of translation.

State 26 handles the page fault exception.


18, 19
MAR <- PC
PC <- PC + 2
[MEMCHECK] [INT]
0
1
To 49
33
MDR <- M
R
R
35
IR <- MDR
32
BEN<-IR[11] & N + IR[10] & Z + IR[9] & P
[IR[15:12]]
RTI
To 8
1011
To 11
1010
To 10
BR
ADD
AND
XOR
TRAP
SHF
LEA
LDR
LDW
STW
STB
JSR
JMP
0
[BEN]
0
1
22
PC<-PC+LSHF(off9,1)
To 18
12
PC<-BaseR
To 18
4
[IR[11]]
0
1
20
R7<-PC
PC<-BaseR
To 18
21
R7<-PC
PC<-PC+LSHF(off11,1)
To 18
1
DR<-SR1+OP2*
set CC
To 18
5
DR<-SR1&OP2*
set CC
To 18
9
DR<-SR1 XOR OP2*
set CC
To 18
15
MAR<-LSHF(ZEXT[IR[7:0]],1)
[MEMCHECK]
28
MDR<-M[MAR]
R7<-PC
R
R
30
PC<-MDR
To 18
13
DR<-SHF(SR,A,D,amt4)
set CC
To 18
14
DR<-PC+LSHF(off9,1)
set CC
To 18
2
MAR<-B+off6
[MEMCHECK]
6
MAR<-B+LSHF(off6,1)
[MEMCHECK]
7
MAR<-B+LSHF(off6,1)
[MEMCHECK]
3
MAR<-B+off6
[MEMCHECK]
29
MDR<-M[MAR[15:1]'0]
R
R
31
DR<-SEXT[BYTE.DATA]
set CC
To 18
25
MDR<-M[MAR]
R
R
27
DR<-MDR
set CC
To 18
23
MDR<-SR
16
M[MAR]<-MDR
R
R
To 18
24
MDR<-SR[7:0]
17
M[MAR]<-MDR**
R
R
To 19
NOTES
B+off6 : Base + SEXT[offset6]
PC+off9 : PC + SEXT[offset9]
*OP2 may be SR2 or SEXT[imm5]
** [15:8] or [7:0] depending on
MAR[0]
10, 11
EXCV <- x05
To 53
26
EXCV <- x02
To 53
47
EXCV <- x04
To 53
48
EXCV <- x03
To 53
53
PRIV <- 0
MDR <- PSR
VECT <- LSHF(EXCV, 1) + 0x0200
[PRIV]
0
1
To 55
To 63


49
PRIV <- 0
MDR <- PSR
PRIO <- INT_PRIO
VECT <- LSHF(INTV, 1) + 0x0200
[PRIV]
0
1
63
USP <- R6
R6 <- SSP
55
MAR <- R6 - 2
R6 <- R6 - 2
[MEMCHECK]
41
MEM[MAR] <- MDR
R
43
MDR <- PC - 2
45
MAR <- R6 - 2
R6 <- R6 - 2
[MEMCHECK]
44
MEM[MAR] <- MDR
R
46
MAR <- Vect
[MEMCHECK]
52
MDR <- MEM[MAR]
R
54
PC <- MDR
To 18
8
MAR <- R6
[MEMCHECK]
36
MDR <- MEM[MAR]
R
38
PC <- MDR
34
MAR <- R6 + 2
R6 <- R6 + 2
[MEMCHECK]
37
MDR <- MEM[MAR]
R
39
PSR <- MDR
40
R6 <- R6 + 2
[PRIV]
0
1
51
Nothing
To 18
59
SSP <- R6
R6 <- USP
To 18
42
VA <- MAR
SMDR <- MDR
50
MAR <- Add. of PTE
56
MDR <- MEM[MAR]
R
58
Set Ref, Modified Bits
[VACHECK]
60
MEM[MAR] <- MDR
R
62
MAR <- Physical Add.
MDR <- SMDR
Restore State from SState
SState

Datapath



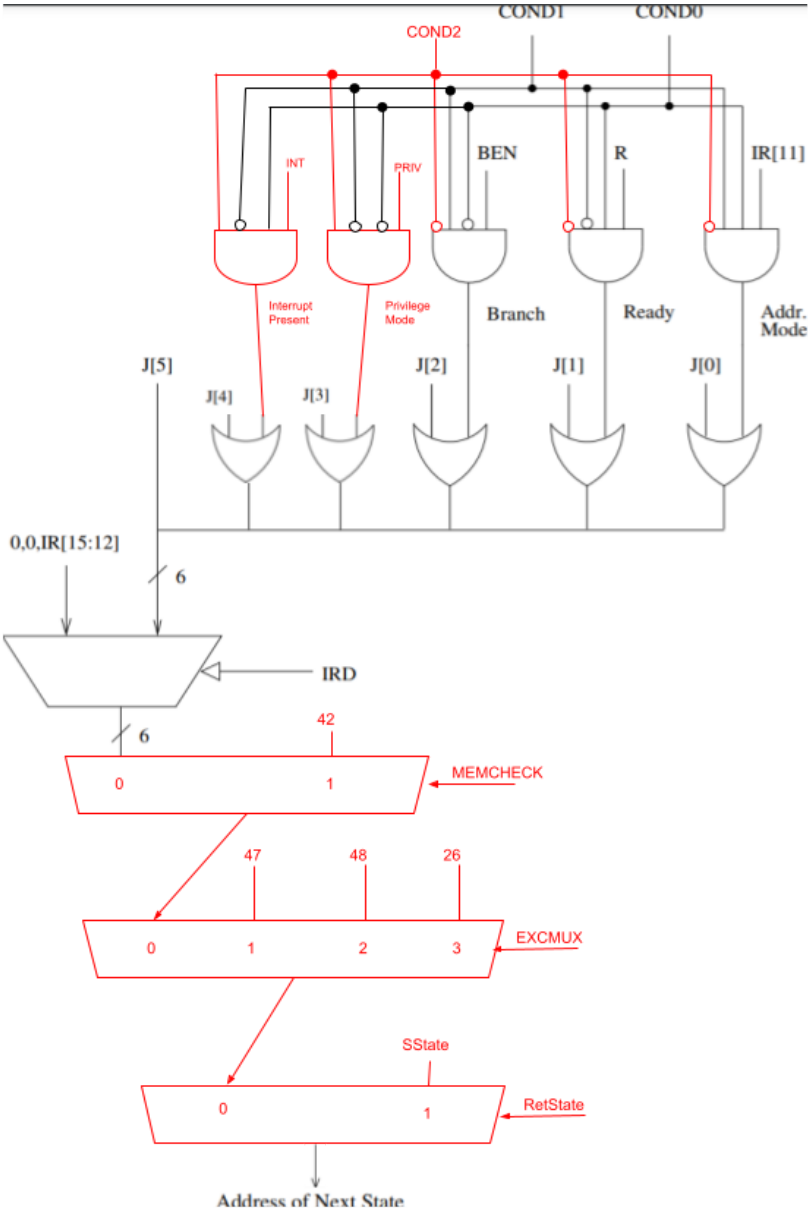
- PTBR register
- SState register to hold next state
- Added a SMDR register to hold saved MDR
- VA register to hold virtual address during translation

Control Signals

- GatePTBR - gate ptbr onto bus

- LD.SState - loads next state into sstate
- GateVA - gate va onto bus
- LD.VA - loads va from bus
- VAMUX - 0 for loading mar from bus, 1 for loading add. of pte, 2 for loading physical add.
- GateMAR - put Mar on bus
- LD.SMDR - load MDR into smdr
- MDRMUX - 0 for loading mdr from bus/memory, 1 for loading from smdr

MicroSequencer



When MEMCHECK is 1 (which happens every time MAR gets loaded), the microsequencer will redirect the machine to state 42 for VA translation. At the end of translation, RetState will be 1 to return to the saved next state after the MAR was originally loaded.

Another exception, microinstruction state 26, has been added for page faults.