Hazards report

1. Data Hazards
    a. Full Forwarding unit: checks on Rdst and Rsrc in ID/EX buffer if they are the same as Rdst in EX/MEM or in MEM/WB and if they are the same and we have a writeRegister signal on we forward this data(Alu output from EX/Mem or data from WB stage are selected instead of Rdst read from decode stage).
    b. Load Use : checks on Rdst and Rsrc in ID/EX buffer if they are the same as Rdst in EX/MEM and that memory read signal is on so we stall for a cycle and complete execution.Stalling is done when the Data hazard signal returned to fetch stage from decode stage is on PC Mux selects no change on pc, so no new instruction is fetched and decode stage outs control signals with zeros(the instruction will not execute this cycle).
2. Control Hazards:
    a. Static branch prediction: assume branch taken until we reach Execution stage then we check if a hazard occurred. If so , instruction in decode is flushed(zero signals outed to buffer) and the Rdst is forwarded to the Fetch stage and the right instruction is Fetched.
3. Structural Hazards : Two Rams are used(Instruction ram and data Ram).