# New Synchronization Method for Thyristor Power Converters to Weak AC-Systems

Richard Weidenbrüg, Francis P. Dawson, *Member, IEEE*, and Richard Bonert

*Abstract*—**This paper presents an improved approach to obtaining good zero voltage crossing signals. These signals are subsequently used as synchronization signals for a phase controlled thyristor power converter. Detection of accurate zero crossings are possible even under the following conditions: large frequency changes, sudden load changes, and large commutation overlap angles. The improved accuracy in the integrity of the zero crossing is obtained by reconstructing a voltage representing the ac source voltage. This voltage is determined from the distorted thyristor converter input voltage, the converter input current, and an online identification of the source impedance using a microcontroller-based adaptive algorithm. The improvement provided by the new zero crossing detection scheme is verified experimentally.**

## I. Introduction

A significant number of industrial installations require the use of a line commutated ac to dc converter. These converters or bridges, as they are commonly referred to, are typically six pulse configurations, as shown in Fig. 1, or in some instances, 12 pulse configurations. The control of these converters can be classified in terms of the following three distinct actions: line synchronization [1]–[13]; phase angle delay; and distribution of gating pulses.

In certain industrial situations, it is common to encounter a weak ac distribution system or stated otherwise, the equivalent short circuit impedance of the system as viewed from the converter terminals becomes large enough to create a significant commutation overlap angle. As a result, the voltage appearing across the input converter terminals has significant superimposed notching. Fig. 2 shows a representative waveform of the input converter terminal voltage and the network voltage $V_{ab}$. Clearly the corrupted signal $V_{AB}$ is not suitable as a synchronization signal, since multiple zero crossings can occur. These multiple zero crossings are known to create control instabilities. The purpose of this paper is threefold: 1) to briefly review the nature of the gating instability; 2) to provide a comparative summary of existing means of improving the integrity of the zero crossing signal; and 3) to propose a new method of obtaining more accurate zero crossings in order to address the gating instability problem as well as additional practical concerns.

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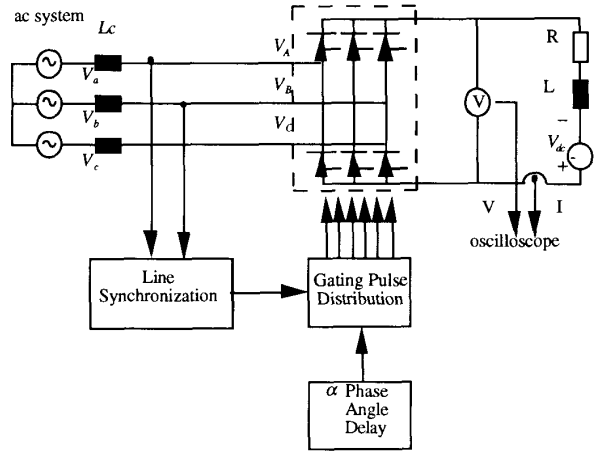


Fig. 1. Equidistant firing circuit for a 6 pulse line commutated bridge: Test conditions: $Vac$ = 55 V, $f$ = 60 Hz, $L_c$ = 6 mH, $L$ = 63 mH, and $R$ = 30 Ω, $Vdc$ = 110 V.

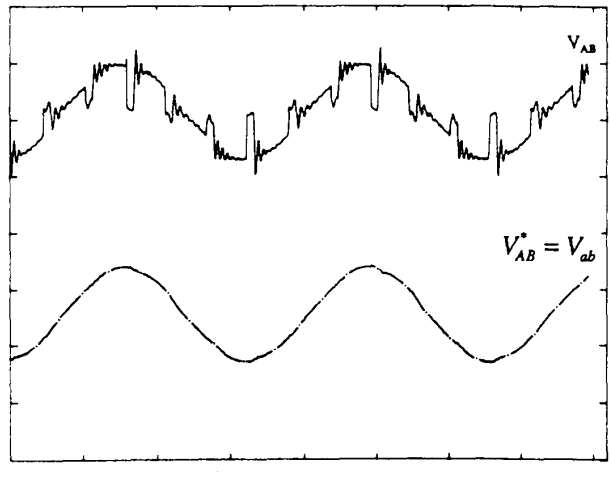


Fig. 2. Input converter terminal voltage. Top trace: Input converter terminal voltage $V_{AB}$ (100 V/div, 5 ms/div). Bottom trace: Network voltage $V_{ab}$ and $V^*_{AB}$ after accurate reconstruction (100 V/div, 5 ms/div): $\alpha = 90°$; $L_c$ = 6 $mH$.

## II. Nature of Gating Instability

Under ideal conditions, the gating signal is referenced with respect to the zero crossing of the voltage $V_{ab}$ of the network. This zero crossing is identified with the mark "synch" in Figs. 3(a)–(c). In the real situation of a con-

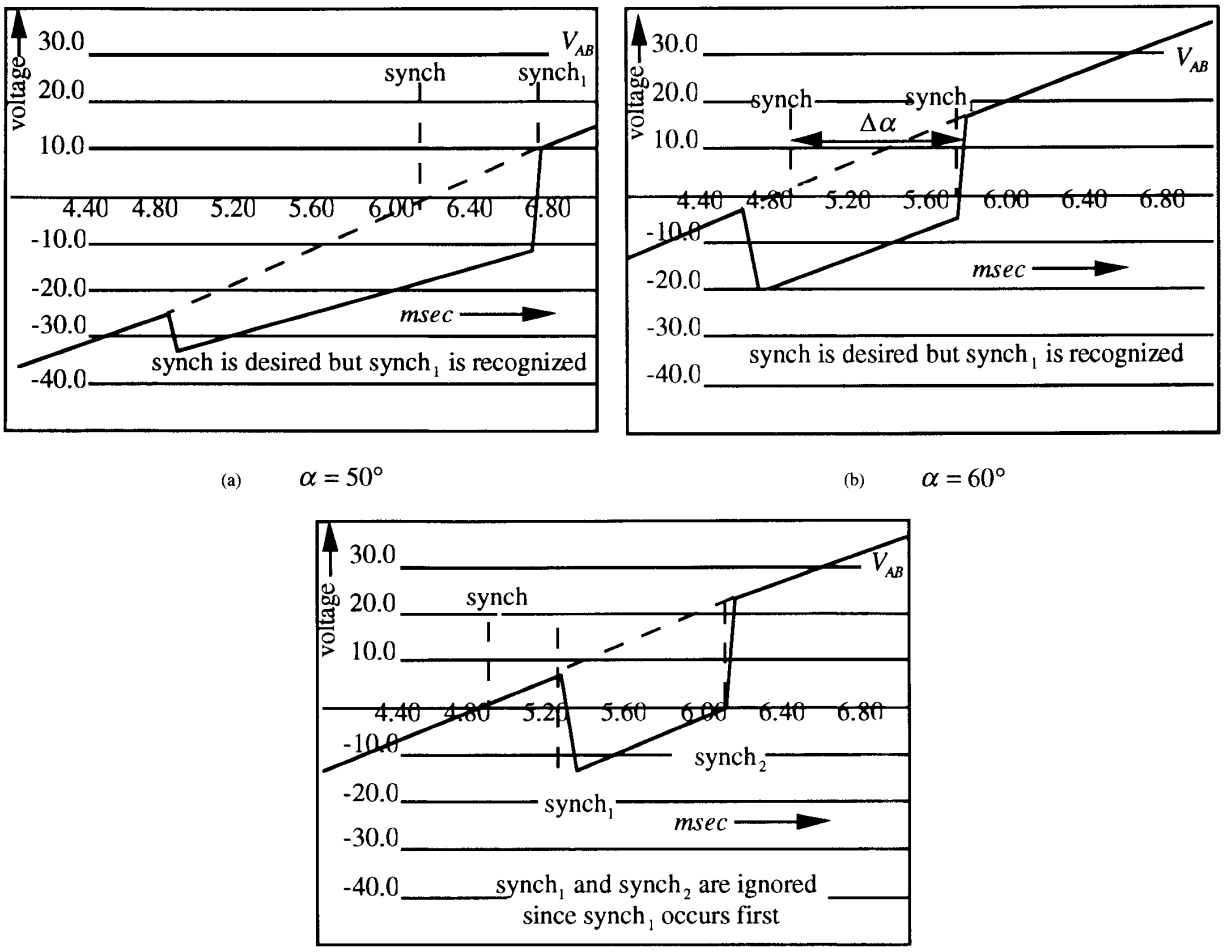


Fig. 3. Reference voltage signal $V_{AB}$.

verter connected to a weak system, the terminal voltage deviates from $V_{ab}$. In practical terms, we observe commutation notches.

If these notches are in the neighborhood of the ideal zero crossings, referred to as "synch" in Figs. 3(a)–(c), a false zero crossing detection "synch$_1$" occurs as shown in Figs. 3(a) and (b).

Of greater concern is the fact that the error $\Delta\alpha$ in the gating signal is not constant. Instead, a nonlinear oscillation in the value of $\alpha$ occurs. With the aid of Figs. 3(a)–(c), this instability can be explained as follows.

The proper gating should take place at the instant "synch" as shown in Fig. 3(a). Instead, it is delayed to "synch$_1$." As a result, the commutation notch for the delayed gating signal will shift towards the right, along with the reference "synch" as shown in Fig. 3(b). Thus "synch$_1$" in Fig. 3(b) is delayed even further. This delay results in the notch moving even further to the right of "synch" as shown in Fig. 3(c).

Notice that in Fig. 3(c), the valid and recognized reference is suddenly "synch" and not the false signal "synch$_1$." Consequently, the reference zero crossing occurs much earlier, and the notch moves, at the next gating instant, to the left of "synch" as shown in Fig. 3(a). This process repeats itself on a cyclical basis.

Of further concern is the fact that the commutation notch not only shifts, but exhibits a change in its width. The degree of shifting and variations in the notch pulse width effects the firing angle $\alpha$. The frequency of the nonlinear oscillation of $\alpha$, due to the nonstationary notches is either 30 Hz or 180 Hz for a six-pulse bridge. The 180 Hz limit cycle applies if the gating references are derived from each phase for the positive and negative voltage zero crossing. This means that six independent references are generated per line period. The 30 Hz-limit cycle occurs, if only one reference signal per period from one phase is used followed by six equally spaced gatings derived from the reference signal. The last scheme is

known as the single phase equidistant synchronization method.

In the event of a gating instability, the dc output as shown in the top trace of Fig. 8 contains a low frequency subharmonic component. The 30 Hz fluctuation in the dc output voltage can readily be observed, and is associated with a single phase equidistant synchronization scheme.

## III. Comparative Summary of Solutions to Zero Crossing Noise Reduction

The problems associated with the poor detection of zero crossings have been addressed in the past by various schemes, for example: choice of voltage sensing location; low pass filtering; bandpass filtering; digital filtering; predictive linearization; and open loop voltage drop compensation. The limitations of each of these approaches is summarized as follows:

### *A. Choice of Voltage Sensing Location*

The synchronization voltage waveform can be obtained at either the converter terminals or on the primary side of the converter transformer. The former approach is not advisable, as shown previously, in that the voltage waveforms will have superimposed commutation notches. Filtering of these notches is necessary in order to reduce the chance of detecting multiple zero crossings. On the other hand, less filtering can be accomplished by obtaining the voltage from the primary side of the converter transformer. Some voltage notching will still be evident in that the voltage drop across the equivalent network impedance has not been compensated for. An additional problem associated with primary voltage sensing is the necessity for specialized instrumentation (i.e., high voltage potential control transformers, protection, and shielding).

### *B. Lowpass Filter*

Low pass filters are designed to operate in a fixed frequency range. The purpose of these filters is to smooth out the notches in the synchronization waveform. This filtering action also has the negative effect of introducing a phase shift to the original signal. An additional phase-shift is introduced by the voltage drop across the commutating reactance upstream from the point of sensing. This voltage drop is influenced by the converter load and converter firing angle. Unstable closed loop control of a converter will occur if voltage sensing is performed at the converter terminal and the ac system is weak [1], [10], [13].

### *C. Bandpass Filter*

Improved zero crossing signals can be obtained by utilizing a bandpass filter rather than a lowpass filter [7], [14]. Typical filters have a low Q and a bandpass frequency range of 45 Hz–120 Hz (i.e., at 60 Hz operation). Subharmonics and harmonics are substantially attenuated under these conditions. An additional advantage of the bandpass filter is the lack of phase shift in the fundamental frequency between the filter input and output. The presumption is that the frequency is constant.

The disadvantage of this method is the restricted operating frequency range caused by the properties of the bandpass filter. In particular the output phase shift variations in high Q bandpass filters are extremely sensitive to variations in the filter parameters.

### *D. Digital Filters*

Phase-locked loops (PLL's) can be used to remove distortion from the incoming signal [5], [9], [12]. The PLL method provides a suitable solution within a wide frequency range as long as the frequency of the reference signal does not change quickly. The dynamic response to a line disturbance is slow (at least two line periods). Another disadvantage of the PLL approach is that the errors in the zero crossings and errors arising as a result of periodic fast load changes are not compensated for.

### *E. Predictive Linearization*

In this method, the distorted reference voltage signal is linearized in the vicinity of a zero crossing region in order to obtain an approximate location of the zero crossing instant [8]. Although large frequency changes can be considered, an upper limit on the commutation overlap angle is fixed, thus making this approach unsuitable for weak AC systems. The calculation time needed to reconstruct the zero crossing of the voltage reference signal represents a delay in the synchronization signal. The firing circuit must therefore compensate for this delay, and also take into account the execution time of the software algorithm.

### *F. Open Loop Voltage Drop Compensation*

The phase shift arising as a result of the commutation reactance can be compensated for in the following way. First, a look-up table containing entries of phase shift as a function of firing angle is generated. It is assumed that the line to line voltage, the load, and the commutation inductance are all known quantities. This tabulated phase-shift is then used to offset a given firing angle [7]. It is presumed that the zero crossing signal is a filtered version of the converter line to line voltage. Additional flexibility can be attained by including information about the load and line in a look up table. The memory requirements for such an effort could become very impractical. An additional drawback of such an approach is that a constant commutation inductance has been implicitly assumed. This is not always true. Finally, it should be noted that the load dependent and firing-angle dependent commutation phase shift are not the same in the steady state or transient state. Predicting the effects of sudden changes in firing angle on closed loop control stability is an additional complexity which should be taken into account.

All of the aforementioned approaches listed above suffer in one or more of the following ways:

1) the zero crossing signal instant is load current and firing angle dependent;
2) the zero-crossing signal is sensitive to load transformer impedance, and frequency variations;
3) the zero-crossing method is valid for a restricted range of commutation overlap angles;
4) the zero-crossing signal cannot be ascertained in real time; and
5) specialized instrumentation is required.

Each of these problems can be addressed by proposing a new method of obtaining a more accurate zero crossing voltage signal. This method is henceforth referred to as adaptive on line waveform reconstruction. In essence, the approach taken is to indirectly obtain a zero crossing of the synchronization signal from an infinite bus, i.e., constant voltage or stiff voltage. Infinite buses do not actually exist in practice. However, to first order, it is sufficient to consider the voltage $V_{ab}$ in Fig. 1, behind the transformer impedance as being relatively stiff.

What makes the proposed approach unique is that the voltage $V_{ab}$ is inferred online from the converter line to line voltage and two of the line currents. Consequently, all instrumentation associated with the measurement of voltages and currents can be grouped together with the converter electronics. This makes the installation process far simpler, and therefore, more attractive.

## IV. Adaptive Online Waveform Reconstruction

An overall view of the approach taken in reconstructing the infinite bus voltage $V_{AB}^*$ is shown in Fig. 4(a). Fig. 4(b) illustrates the two voltages $V_{AB}^*$ and $V_{ab}'$ used in the adaption process. The notch taken corresponds to one of the positive going notches as shown in Fig. 2. The following summary details the importance of each of these voltage values [15].

$V_{AB}^*$ corresponds to the calculated voltage of the network. This voltage can be computed online, by using the following:

$$V_{AB}^* = V_{AB} + L_C \frac{d}{dt}(i_a - i_b) \tag{1}$$

where $V_{AB}$ is the sensed converter line to line voltage and $d/dt$ corresponds to the calculated rate of change of the sensed difference current $(i_a - i_b)$.

If $L_c$ is estimated correctly then $V_{AB}^*$ becomes equal to $V_{ab}$ during the commutation notch where $V_{ab}$ represents the ideal voltage of the network. In order to determine $L_c$, the following adaptive process is used.

The *first step* is to measure $V_{AB}^*$ before and after the notch. From this data, the voltage $V_{ab}'$ during the notch is calculated by interpolation. The *second step* is to measure $V_{AB}^*$ during the notch. The *third step* is to determine the error in estimating $L_c$ which is referred to as $\Delta L_c$. This error is proportional to the area between the measured waveform $V_{AB}^*$ and the interpolated waveform $V_{ab}'$ during the notch interval. The following equation defines the

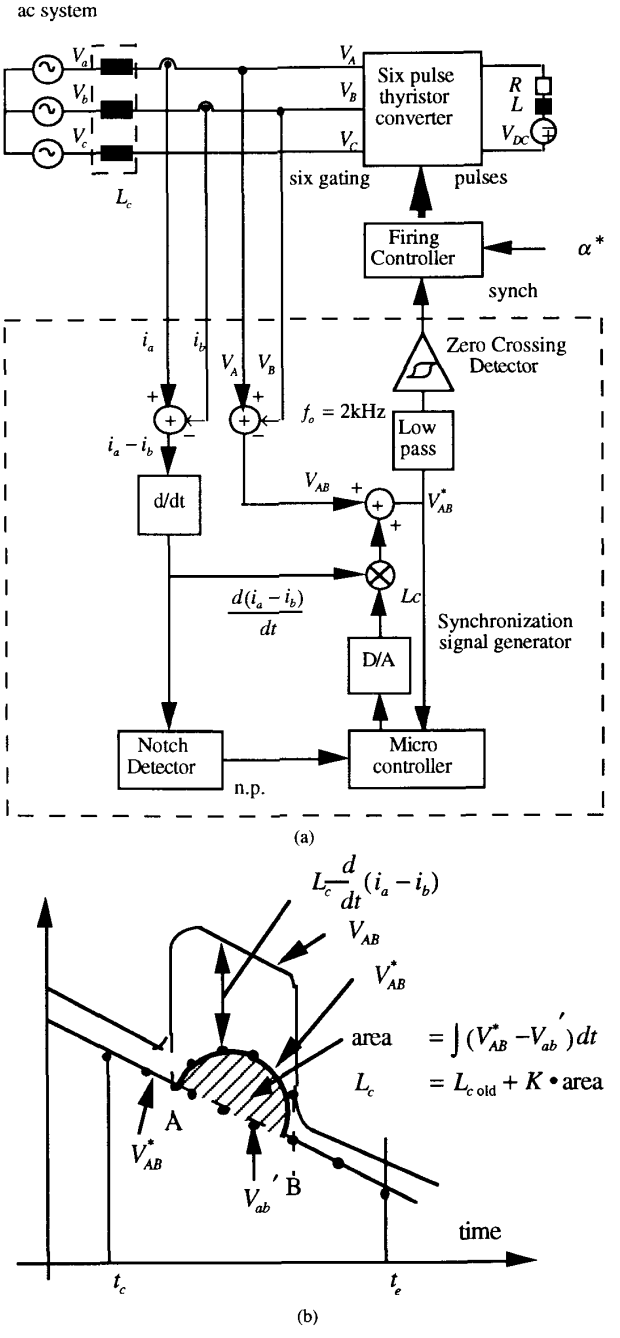


Fig. 4. (a) Adaptive online reconstruction synchronization signal. Test conditions $V_{ac}$ = 55 V, $f$ = 60 Hz, $L_c$ = 6 mH, $L$ = 63 mH, $R$ = 30 Ω, $V_{dc}$ = 110 V. (b) Calculation of the ideal network voltage $V_{ab}$ and the line inductance $L_c$.

error in the inductance value:

$$\Delta L_c = K \int_A^B (V_{AB}^* - V_{ab}')\, dt \tag{2}$$

where the adapted value for $L_{c_{new}}$ is given by

$$L_{c\,new} = L_{c_{old}} + \Delta L_c. \tag{3}$$

As the microcontroller is a discrete system, the measurement of $V_{AB}^{*}$ is carried out at the sample points between the time $t_c$ and $t_e$, as indicated in Fig. 4(b). $V_{ab}'$ is then calculated by interpolation and finally $\Delta L_c$ using (2) and $L_{c_{new}}$ are determined. After several cycles, the volt's second integral in (2) will approach zero. At this point $L_{c_{new}}$ is precisely $L_c$ in (1).

The advantage of the proposed structure is that $V_{AB}^{*}$, as an analog value, is always continuously available. Furthermore, $L_c$ is determined only once per pulse period, thus allowing sufficient time for computation. The approach to determine $L_c$ by an integral, in an adaptive manner, makes the method very robust and independent of single sample errors.

## V. Hardware Implementation

The firing controller uses a single phase equidistant synchronization method and was implemented according to the detailed description in [3]. The principle components of the synchronization signal generator are: a sampled date differentiator for the current signal; voltage signal time delay; voltage notch detector; microcontroller; digital-to-analog converter; high frequency cutoff low pass filter; and zero crossing detector.

Details regarding the former six components are presented in the following summary:

### *A. Sampled Data Differentiator*

The differentiated current signal has to be available at all times to guarantee the on-line capability of the whole system. This therefore precludes the use of a microprocessor. Instead, a hybrid circuit with a bandwidth of 140 kHz is proposed. The block diagram is shown in Fig. 4. The analog signal $(i_a - i_b)$ is sampled by the first sample and hold device $S\&H_1$ with a sample time of 7 $\mu$s. The second sample and hold device samples the difference. $\Delta(i_a - i_b) = i_a - i_b - i'_a + i'_b$ where $i'_a - i'_b$ is the present value for the difference current held by the sample and hold device $S\&H_1$. A time delay $\Delta t = 5$ $\mu$s exists between the two triggering signals CL1 and CL2 of Fig. 5. Finally, the third sample and hold device $S\&H_2$ resamples the output of $S\&H_2$ with a very short sampling time delay ($\Delta t = 2$ $\mu$s) in order to filter out switching transients that can appear during the acquisition of the new sampled value stored by $S\&H_2$. The sample rate of the sampled date differentiator has to be high enough to guarantee a step width compatible with that of the minimum expected firing angle step size and to guarantee the acquisition of a sufficient number of samples of $V_{AB}^{*}$ and $V_{ab}'$ during the commutation notch.

### *B. Voltage Signal Time Delay*

The line to line voltage signal $V_{AB}$ needs to be delayed for the same time that it takes to generate the signal $d/dt$. This is accomplished by passing $V_{AB}$ through two sample and hold devices connected in series. Sychronization is achieved by triggering these devices with the clock signals CL1 and CL2 (Fig. 5).

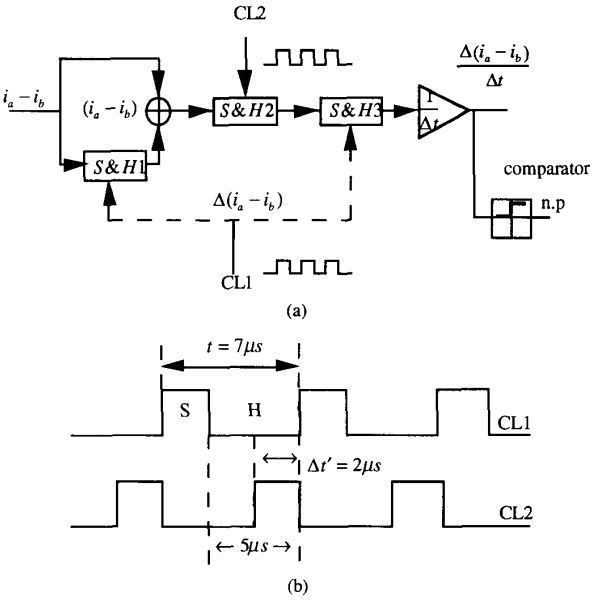


Fig. 5. Sampled data differentiator: (a) Block diagram and (b) triggering signals.

### *C. Voltage Notch Detector*

The adaptive algorithm in the microcontroller needs a digital input signal to indicate the presence of commutation notches in the converter line to line voltage $V_{AB}$ (Fig. 6). The positive half of the differentiated current signal is utilized as a commutation notch indicator. (Referred to in Fig. 4(a), 5, and 6 as n.p.).

A comparator indicates when the differentiated differential current signal exceeds a predetermined level slightly higher than the noise level. Unfortunately, the comparator also generates multiple edges at the commutation notch boundaries due to snubber ringing. However, these events occur at a high frequency. Consequently, the multiple edges can be eliminated by recognizing only transition periods which are longer than half the snubber resonant period.

### *D. Microcontroller*

A single chip Hitachi microcontroller with a 10 MHz internal clock is used in performing the calculations to determine the source inductance $L_c$. This microcontroller was chosen because of its fast 16-b CPU and its on board 10-b analog to digital converter. The algorithm for updating $L_c$ is performed once per sample period (60°) after a commutation pulse (n.p.) has been recognized.

### *E. High Frequency Cutoff Low Pass Filter*

The compensated voltage reference signal $V_{AB}^{*}$ is passed through a 2 kHz low pass filter in order to smoothen the sample and hold nature of the output waveform.

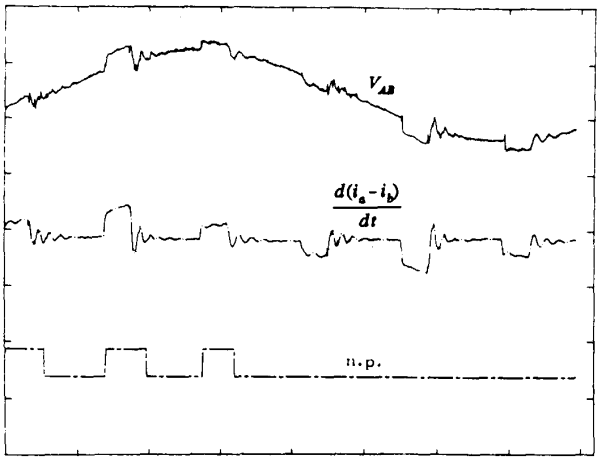


Fig. 6. Commutation related waveform. Top trace: Converter input line to line voltage $V_{AB}$ (50 V/div, $\alpha = 20°$, 2 ms/div). Middle trace: Differentiated line current signal. Bottom trace: Digital signal indicating the presence of positive going voltages notches (+15 V).

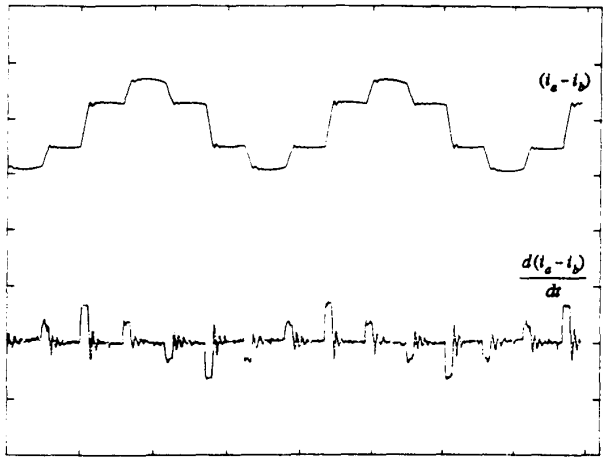


Fig. 7. Current signal and the derivative of the differenced current. Top trace: line current at the converter input (2.5 A/div 5 ms/div). Bottom trace: Derivative of the differenced current signal (10 A/div): $\alpha = 90°$; $Lc = 60$ $mH$.

## VI. Software Implementation

The program of the microcontroller has to handle the following tasks:

1) Sample the voltage $V_{AB}^*$ before the notch, during the notch, and after a notch.
2) Select three samples before and after the notch in order to interpolate, the voltage $V_{ab}$ over the notch interval. The sample times taken in interpolating during the notch are identical to those of $V_{AB}^*$.
3) The program must then calculate from $V_{ab}$ and $V_{AB}^*$ during the notch, the value $\Delta L_c$, and the updated value for $L_c$. After this, the program returns to sampling $V_{AB}^*$ before, during and after the next upcoming notch.

The only additional demanding part of the program is the interpolation of the voltage $V_{ab}$.

### A. Numerical Interpolation

There are different methods by which interpolation can be implemented [16]. The most appropriate interpolation is accomplished using cubic splines. This method calculates one interpolating polynomial between each set of adjacent data. The continuity of first and second derivatives of the interpolating functions guarantees a smooth reconstructed waveform even if the data is widely spaced. Three sampled voltage values are needed on each side of the commutation notch as illustrated in Fig. 4(b). Operating conditions guarantee that the sampled voltage values are undistorted immediately before the commutation notch. Therefore, the last three voltage values before the notch are taken as future interpolating points. Immediately after the commutation notch, it is necessary to eliminate all readings related to snubber ringing. The approach taken is to first add the sampled values over one period of the snubber ringing waveform and then average them. The averaged voltage is then taken as one of the interpolating points subsequent to the commutation notch. Note the sampling frequency is many times greater than the snubber ringing frequency. Once the interpolation polynomial is found, five evenly distributed values for $V_{AB}^*$ are calculated and then stored in memory for future calculation of $L_c$. A memory block of 220 bytes is used as a storage ring to store up to 110 consecutive values of $V_{AB}^*$. This number of stored values for $V_{AB}^*$ provided sufficient accuracy for the calculation of (2).

## VII. Experimental Results

Fig. 7 shows the line current $(i_a - i_b)$ and its derivative under dynamic operating conditions. Fig. 2 shows the notching voltage $V_{AB}$ on the thyristor converter input side and the properly adapted reconstructed voltage reference signal $V_{AB}^*$. Notice that the adapted value for $V_{AB}^*$ is virtually undisturbed and faithfully represents the infinite bus voltage. The nondistorted signal $V_{AB}^*$ is subsequently used to accurately generate the synchronization signal for the firing circuit.

Several experiments were performed to compare the dynamic behavior of the power converter using both the new zero-crossing detection approach and conventional low-pass filtering of the converter voltage. Fig. 8 voltage shows the output dc voltage of the power converter for the two aforementioned approaches with a constant phase angle control signal. The results show clearly that in the case of significant line distortion, the new adaptive synchronization process provides stable output performance with a minimum amount of distortion.

## VIII. Conclusions

The performance of a new zero-crossing detection method has been presented. This method has been experimentally shown to eliminate the gating instability which occurs with at least one other commonly used zero-crossing detection method. The new method is based on a microcontroller aided adaptive compensation of the dis-

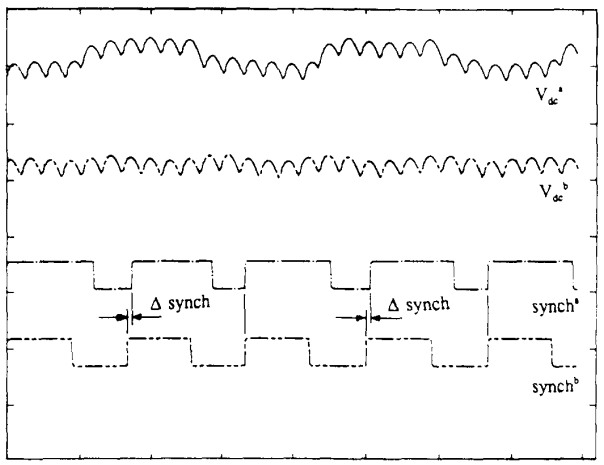


Fig. 8. Comparison between low pass filtered zero crossing voltage signal and the adaptively reconstructed zero crossing voltage signal ($\alpha = 100°$). $Vdc^a$: output dc-voltage $Vdc$ of the power converter for a low-pass filtered line to line voltage zero crossing signal (45 V/div, 10 ms/div). $Vdc^b$: output dc-voltage $Vdc$ of the power converter for the adaptively reconstructed zero crossing signal (45 V/div, 10 ms/div). synch$^a$: synchronization signal obtained using a low pass filtered line to line voltage signal. synch$^b$: synchronization signal obtained using the adaptively reconstructed synchronization waveform $V_{AB}^*$.

torted reference line voltage. A reliable and precise synchronization signal is generated by taking into account the commutation notch distortion of the line voltage. This makes the new scheme suitable in applications where the ac system is weak or where the frequency of the line may vary.

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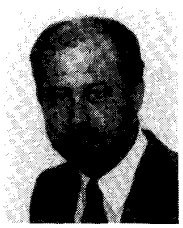

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