//Proposed headline: what you need to know about RISC-V

//Proposed intro:

Can you believe that it has been a little over a decade since the start of the RISC-V project!

Well, believe it or not, but last year the RISC-V project celebrated its 10th anniversary. If you have no idea what I'm talking about, then this article is perfect for you.

**What is RISCV?**

RISC-V is an open standard instruction set architecture (ISA) based on established reduced instruction set computer (RISC) principles.

**Why RISCV?**

As obvious as it is, the most famous two instruction set Architectures are the X86 and the ARM, both of them have very different fields of application.

The X86 ISA is mostly used in desktops, laptops, and servers. While ARM ISA is mostly used in mobile phones and tablets. On the other hand, the RISC-V ISA is most suitable for use in some specific applications like edge computing, Storage, and AI applications.

RISC-V is an open-source ISA, thus there are no fees required to use the IP, it has a small standard base ISA, with multiple standard extensions, it is simple as it's far smaller than other commercial ISAs, and stable because the Base and first standard extensions are already frozen, so there is no need to worry about major updates.

**History**

In 2010, the RISC-V instruction set was developed at the University of California, Berkeley. Unlike any other academic designs, the RISCV ISA was designed to be used in practical microprocessors.

The RISC-V community is supervised by RISC-V International - a global non-profit association that was founded in 2015 as the RISC-V Foundation with 29 members, RISC-V is now a global organization with over 750 members in more than 50 countries.

The RISC-V project was initially created in the US, but the association decided to move out of the US to avoid any future uncertainty with the export restrictions on RISC-V. So, in March 2020, the RISC-V international association was incorporated in Switzerland.

**Microarchitectures based on RISC-V ISA**

In 2018, SiFive -one of the most active members of the RISC-V Foundation- released a board called HiFive that was capable of running Linux. There have been other microarchitectures like PicoRV32 that implements the RISC-V RV32IMC Instruction Set, NV-RISCV which is supplied by Nvidia and it implements RV64I Instruction Set and many others.

//Proposed conclusion:

It is mind-blowing to see that for only 10 years, RISC-V has achieved so much and it’s still growing fast. Also, having different application fields makes it possible for RISC-V to compete with ARM and X86 very soon.

**Links and references**

• Volume 1, Unprivileged Spec v. 20191213: https://riscv.org/wp-content/uploads/2019/12/riscv-spec-20191213.pdf

• Volume 2, Privileged Spec v. 20190608: https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-161.pdf

• https://riscv.org/

• https://www.power-and-beyond.com/risc-v-what-is-it-all-about-a-994876/

• https://www.seeedstudio.com/blog/2020/06/01/10-things-you-should-know-about-risc-v-in2020-m/