TSL 0.18 micron, 1.8 volt

Dual-Port Synchronous RAM

TSL18RD130

Version 3.1

November 2003

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Table of Contents

Preface

About This Guide vii
Overview of Contents vii
Associated Guides and Documentation vii
Conventions viii

Introduction

Description 1-2
Memory Organization 1-6
Abutment Box with Connector Names and Relative Positions 1-6
Connector Width and Description 1-7
Parameter Names 1-8
Timing Specifications 1-11
Leakage Power 1-12
Output Buffers 1-12
Timing Dependencies 1-12
Timing Diagrams 1-14
Read Cycle 1-14
Write Cycle (IO separate) 1-15
Write Cycle (IO common) 1-16
Write Cycle with optional select bit write 1-17
Chip selection waveforms 1-18
Bank address waveforms 1-18
Read / Write (address match) conflict between two ports 1-19
Characterization Conditions 1-21
Internal Power Specifications 1-22
Internal Power Calculation 1-22
Simulation conditions 1-23
Leakage Current Specifications 1-24
Applications 1-25
Expansion of Word Width 1-25
Expansion of Word Depth 1-25

Characteristics

Word Width 8 2-3
Word Width 16 2-6
Word Width 24 2-9
Word Width 32 2-12
Word Width 48 2-15
Word Width 64 2-18
Word Width 72 2-21

Derating Information

Derating Equations 3-2
Power Dissipation 3-4
Derating 3-5

Preface

This guide is intended for use with TSL enhanced process, 1.8volt, Dual-Port Synchronous RAM (TSL18RD130).

About This Guide

Overview of Contents

This guide contains the following chapters:

Chapter 1, Introduction
Gives a general description of the functions and characteristics of the Dual-Port Synchronous RAM.

Chapter 2, Characteristics
Includes the detailed characteristics tables for some possible word depths and widths.

Chapter 3, Derating Information
Describes the derating factors you should use to estimate delays under different operating conditions.

Associated Guides and Documentation

Other publications you can consult for related information are:

TSL18CIO150, 0.18 micron, 1.8 Volt, Super Core Limited I/O Pad Library

TSL18CIO250, 0.18 micron, 3.3 Volt, Super Core Limited I/O Pad Library

TSL18CIO210, 0.18 micron, 3.3 Volt, Core Limited NAND I/O Pad Library

TSL18CIO310, 0.18 micron, 5.0 Volt, Core Limited HOST I/O Pad Library

TSL18CPC250, 0.18 micron, 3.3/5 Volt, Core Limited PCI I/O Pad Library

TSL18FS120, 0.18 micron, 1.8 Volt, Fast Silicon SC Library

TSL18CIO220, 0.18 micron, 3.3 Volt, Core Limited I/O Pad Library

TSL18SIO220, 0.18 micron, 3.3 Volt, Staggered I/O Pad Library

TSL18ASIO220, 0.18 micron, 3.3 Volt, Analog Staggered I/O Pad Library

TSL18SPC220, 0.18 micron, 3.3 Volt, PCI Staggered I/O Pad Library

TSL18PC220, 0.18 micron, 3.3 Volt, PCI Inline I/O Pad Library

TSL18IO231, 0.18 micron, 1.8/3.3 Volt, Inline Custom I/O Pad Library

TSL18IO210, 0.18 micron, 3.3 Volt, Inline Custom I/O Pad Library

TSL18IO310, 0.18 micron, 3.3/5 Volt, Inline Custom I/O Pad Library

TSL18RS160, 0.18 micron, 1.8 Volt, High Density Synchronous RAM Compiler

TSL18RO160, 0.18 micron, 1.8 Volt, Synchronous Via ROM Compiler

TSL18RD130, 0.18 micron, 1.8 Volt, Dual-Port Synchronous RAM Compiler (this datasheet)

Conventions

The following syntax conventions are used in this guide:

bold text	Is used for emphasis.
italic text	Indicates new terms and references to other sources of information.
italic text in blue	Indicates cross references that are also hypertext links.
`courier text`	Indicates commands that you enter directly, system responses, and file examples.
`bold courier text`	Indicates user input in examples of terminal sessions.
Helvetica italic text	Is used in syntax descriptions to indicate arguments where you should substitute a real value

Chapter 1
Introduction

Topics covered in this chapter include:

Description, page 1-2

Memory Organization, page 1-6

Connector Width and Description, page 1-7

Parameter Names, page 1-8

Timing Specifications, page 1-11

Timing Diagrams, page 1-14

Characterization Conditions, page 1-21

Internal Power Specifications, page 1-22

Simulation conditions, page 1-23

Leakage Current Specifications, page 1-24

Applications, page 1-25

Description

The TSL18RD130 is a Dual-Port Synchronous RAM implemented in the 0.18 micron, 1.8 volt TSL18L6 technology.

Each port (labelled 1 or 2) is completely independent, and there are no constraints on the timing of the ports relative to each other except in the case of address contention. Because ports 1 and 2 are completely symmetrical, the descriptions in this manual apply to both ports; to differentiate the ports, the term PINp is used to reference PIN of port “p” where p is either 1 or 2.

The dual-port RAM has four control signals: an inverting or non inverting clock (CEBp or CEp), a three-state output enable (OEBp) active-low, a chip select (CSBp) active-low, a write enable (WEBp) active-low, and optional control signal select bit write (WENBp[n]) active-low.

The dual-port RAM size is define by the following parameters:

WORD_WIDTH: number of bits per word.

WORD_DEPTH: number of words.

The inputs and outputs can either be bidirectional 3-state data input/outputs (IOp[n]) or separate data inputs (Ip[n]) and 3-state data outputs (Op[n]).

The addresses, the data inputs, WEB and WENB[n] are internally latched.

Dual-port RAM operation is only sensitive to the falling edge of CEBp or rising edge of CEp.

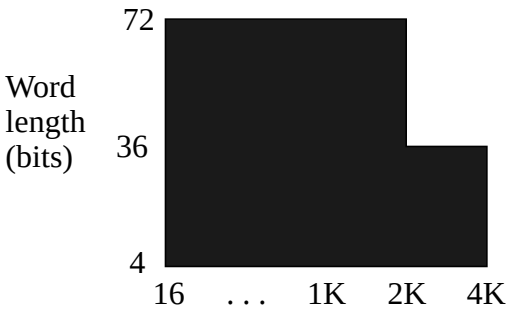
Read and write operations initiates by rising/falling edge of clock signal CE/CEB, providing that CSB signal is low and (in the case of multi-bank configuration) RAM bank is selected.

3-state data outputs are active when OEB signal is low, RAM bank is selected (in the case of multi-bank configuration) and WEBp is high (in case of bidirectional 3-state data input/outputs (IOp[n])). When IO_SEPARATE is true the WEBp signal is not control by the output 3-state.

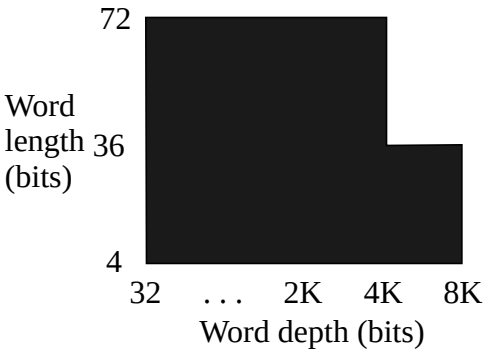
The minimum size for the RAM is 16 by 4 (WORD_DEPTH by WORD_WIDTH). The maximum RAM size is 144K bits: 2k by 72 or 4K by 36.

The TSL18RD130 Dual-Port Synchronous RAM compiler offers a bank interleave or multi-bank option. This option allows a compiled synchronous dual-port RAM to be generated as one of two, three, or four RAM banks. This memory architecture is used to expand word depth or word width (through multiplexing) by using smaller, faster and less power consuming RAM configurations. It is also a flexible way to adjust the shape of the overall RAM for an efficient routing. No external logic is required. By using this scheme the maximum RAM size is extended to 576K bits.

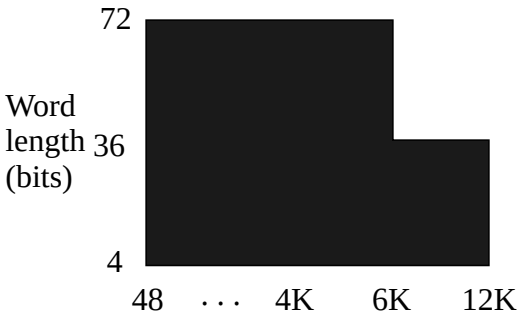
Available RAM configurations for one bank



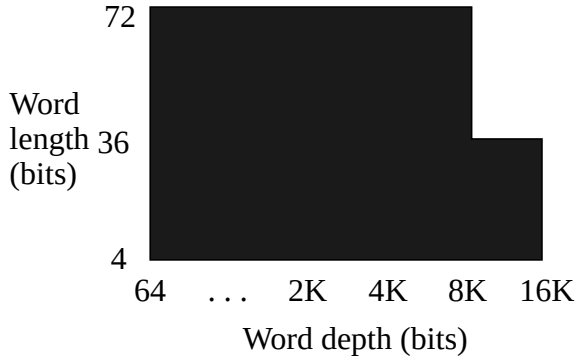
Available RAM configurations with two banks



Available RAM configurations with three banks



Available RAM configurations with four banks



To access this library, you must run RapidCompiler tool and type the following command:

> `RapidCompile tsl18rd130d`

or

> `RapidCompile tsl18rd130h`

or

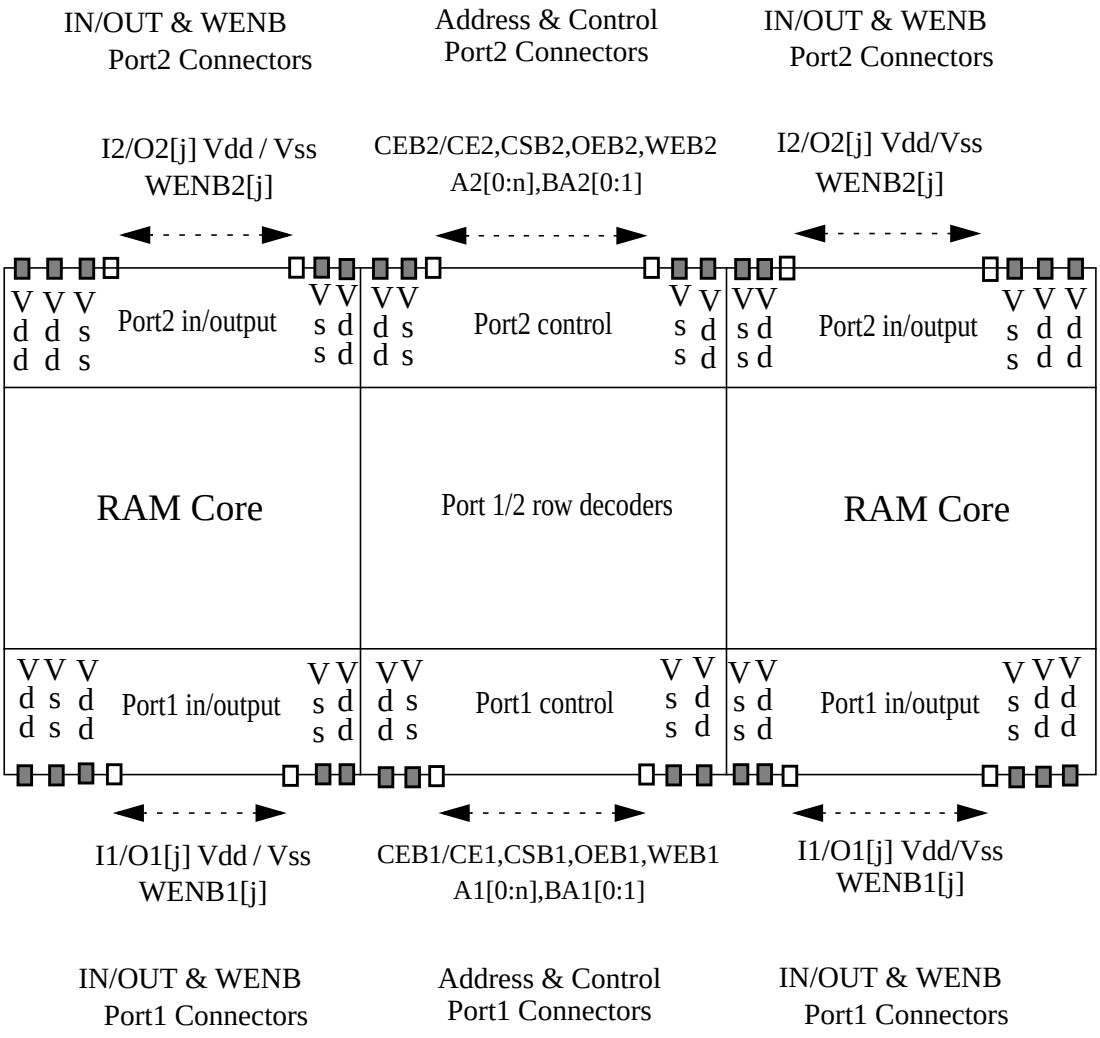
> `RapidCompile tsl18rd130m`

The design rol name is tsl18rd130d. The layout rol name is tsl18rd130h. The model rol name is tsl18rd130m. The parameter template file name is rd3.tpl.

Please see documentation under $LIBRA_HOME_DIR/RapidCompiler/v3.0/doc.

Memory Organization

Abutment Box with Connector Names and Relative Positions



Note ALL VDD & VSS CONNECTORS MUST BE CONNECTED

Connector Width and Description

Conn. Name	Description
VDD*	Power bus
VSS*	Ground bus,
Ip[n]	*n*th input,
Op[n]	*n*th output
IOp[n]	*n*th input/output
Ap[n] *	*n*th address line,
CSBp	Chip select,
CEBp/CEp	RAM clock sensitive on falling or rising edge
OEBp	3-state output enable
WEBp	Write enable
WENBp[n]	*n*th local write enable
BAp[0:1] *	additional address input in case of multiple banks

* Connectors for unused addresses are not brought out.

Parameter Names

These are the parameters for the synchronous Dual-Port RAM compiler cell.

Parameter Name	Description/Type	Default value	Range Min/Max
WORD_DEPTH	Number of bits per output	32	16/4K
WORD_WIDTH	Number of bits per word	4	4/72
IO_SEPARATE	Boolean	False	False/True
MULTI_BANK	Boolean	False	False/True
NUMBER_OF_BANKS	Integer	2	2 to 4
BANK_NUMBER	Integer	1	1 to 4
CLOCK_POLARITY	Boolean	False	False/True
OUTPUT_DRIVE	String	2X	2X/4X/8X
SELECT_BIT_WRITE	Boolean	false	False/True
TOP_METAL_LAYER	String	Metal6	Metal4/Metal5/ Metal6
LAST_FILLING_LAYER	String	OFF	OFF/Metal5/ Metal6
CALMA_LAYER_FILE	String	tsl18l6_10std.clf	tsl18l4_10std.clf / tsl18l5_10std.clf / tsl18l6_10std.clf
MAP_RANGE	Memory Map address range definition	False	False/True
MAP_FIRST_ADDR	First address for Memory Map generation	0	0-8192
MAP_LAST_ADDR	Last address for Memory Map generation	64	0-8192

The total number of bits in the RAM is calculated by using the following formula:
RAM Bits = `WORD_WIDTH` X `WORD_DEPTH`

An example is:

WORD_WIDTH = 8
WORD_DEPTH = 512
RAM Bits = 512 X 8 = 4K bits

Note The maximum number of RAM bits is 147456. Any attempt to make a cell with more than 147456 bits results in an error.

The individual parameters are defined as follows:

`WORD_DEPTH`
: The number of bits per output (words) of the RAM. Fractional RAM cores may be specified to reduce area. Fractional means a number between powers of two. Not all fractional core RAMs can be generated. The compiler will give you the nearest possible size available. Note that when addressing RAM with the fractional core beyond the physical space, the outputs will be indeterminate.

`WORD_WIDTH`
: Specifies the number of RAM outputs. The number of outputs is also referred to as the word length of the RAM, and can vary from a minimum of 4 to a maximum of 72.

`IO_SEPARATE`
: Allows the selection of separate input and output connectors for a specific range of configurations.

`MULTI_BANK`
: Allows the compilation of RAMs with additional selection ports (Pins BAp[0:1]). See the note at the end of this document

`NUMBER_OF_BANKS`
: Only visible if `MULTI_BANK` is true. It defines the number of banks that will be generated. If `NUMBER_OF_BANK` is 2, the only pin defined is BAp[0]. If `NUMBER_OF_BANK` is 3 or 4, both pins BAp[0] and BAp[1] are defined.

`BANK_NUMBER`
: Only visible if `MULTI_BANK` is true. It specifies the RAM's slice. The corresponding decoder will be hard-coded in all design and physical views.

`CLOCK_POLARITY`
: Controls the clock polarity of the memory. If false the memory will be sensitive on the falling edge of the clock and the clock pin will be called CEBp. If true the memory will be sensitive on the rising edge of the clock and the clock pin will be called CEp.

`TOP_METAL_LAYER`
: Specifies the top metal layer used in the chip.

`LAST_FILLING_LAYER`

If set to OFF, no filling will be added on the layers specified in the list. If defined as Metal5, metal filling will be added and no metal filling will be added on above layer. This metal filling will be made by squares of metal to allow rotation of the instances and always provide routing tracks in the preferred routing direction If LAST_FILLING_LAYER is set to the same layer as the TOP_METAL_LAYER, top metal rules will be used for implementing the metal fill. The LAST_FILLING_LAYER parameter will never have a metal layer bigger than the TOP_METAL_LAYER. This will issue an error.

`SELECT_BIT_WRITE`

This option provides the possibility to write just a certain number of bits of a word (multibyte write).

If the option is set to ‘true’, each data input Ip[i] has an additional write enable input WENBp[i], which enables in combination with the global WEBp the writing of the particular bit.

If the option is set to ‘false’, nothing changes in respect to the classical approach, i.e. only the whole word can be written at a time.

`OUTPUT_DRIVE`

Different strength of the output drivers can be chosen (2X, 4X, 8X) to avoid additional buffer insertion by synthesis.

`MAP_RANGE`

Allow to generate memory map for different range. If the option is set to false address range is the range for the first addresses with unique placement. If the option is set to true address range defined by MAP_FIRST_ADDRESS and MAP_LAST_ADDRESS.

`MAP_FIRST_ADDRESS`

Allow to define starting address for Memory Map generation.

`MAP_LAST_ADDRESS`

Allow to define last address for Memory Map generation. For this compiler,it has a settled value WORD_DEPTH-1.

Timing Specifications

Symbol	Description	Delay (ns)	Notes
t_{CYC}	Clock cycle time	2.809	Min
t_{ACC}	Access time	2.294	Max[a]
t_{OUTU}	Time until outputs become unknown	1.027	Max
t_{HCE}	Minimum clock high time	0.198	Min
t_{LCE}	Minimum clock low time	0.363	Min
t_{AS}	Address setup time	0.	Min
t_{AH}	Address hold time	0.406	Min
t_{WS}	Write Enable Bar (WEBp) setup time	0.	Min
t_{WH}	Write Enable Bar (WEBp) hold time	0.333	Min
t_{IS}	Data input setup time	0.053	Min
t_{IH}	Data input hold time	0.408	Min
t_{CS}	Chip select setup time	0.324	Min
t_{CH}	Chip select hold time	0.052	Min
t_{WENBS}	Select bit write setup time	0.079	Min
t_{WENBH}	Select bit write hold time	0.408	Min
t_{BAS}	Bank Address setup time	0.507	Min
t_{BAH}	Bank Address hold time	0.	Min
t_{HOE}	Output Disable time: OEBp rising	0.784	Max
t_{LOE}	Output Enable time: OEBp falling	0.744	Max[a]
t_{HBA}	Output Disable time: BAp[0,1] deasserting	0.835	Max
t_{LBA}	Output Enable time: BAp[0,1] asserting	0.802	Max[a]
t_{HW}	Output Disable time: WEBp falling	0.767	Max
t_{LW}	Output Enable time: WEBp rising	0.682	Max[a]
t_{RWC}	Min time between R/W operations from different ports to the same location (to avoid conflict)	1.676	Min

a. The timing is output load dependent: given with a load of 0pF and drive 2X

Refer to the timing waveforms following this section for the timing specifications in the above table. (Above data correspond to 36 bits by 4096 addresses, typical conditions)

All the timings vary with the RAM size. See the tables in the annexe for specific RAM sizes. The numbers given here are for the maximum RAM size.

All input waveforms have rise and fall times of 0.2ns. All timing measurements are from the 50% of the clock to 50% of the output.

Addresses, control signals WEBp, CSBp, BAp,WENBp[n] and data Inputs are latched on the falling edge of CEBp (rising edge of CEp), control signal OEBp is not latched.

Leakage Power

(The following data correspond to 1024 words by 16 bits, typical condition)

Symbol	Description	Energy (pW)
PLW	Leakage Power	1375720

Output Buffers

The ramp factors and additional delay of the output buffers are given in the following table.

Output Drive	Ramp (ns/pF)	t_{DRIVE} (ns)
2X	0.75	0
4X	0.38	0.01
8X	0.2	0.05

Timing Dependencies

The following equation describes the relation between t_{ACC}, output drive and capacitive load at the output (Cload). Please note, that all timings given in the timing tables are measured with output drive 2x and Cload = 0.0 pF.

$$t_{ACC}^{(drive, Cload)} = t_{ACC} \text{ (from timing table)} + t_{DRIVE}^{(drive)} + Ramp^{(drive)} * Cload$$

For t_{OE} and t_{BA} a similar equation needs to be evaluated:

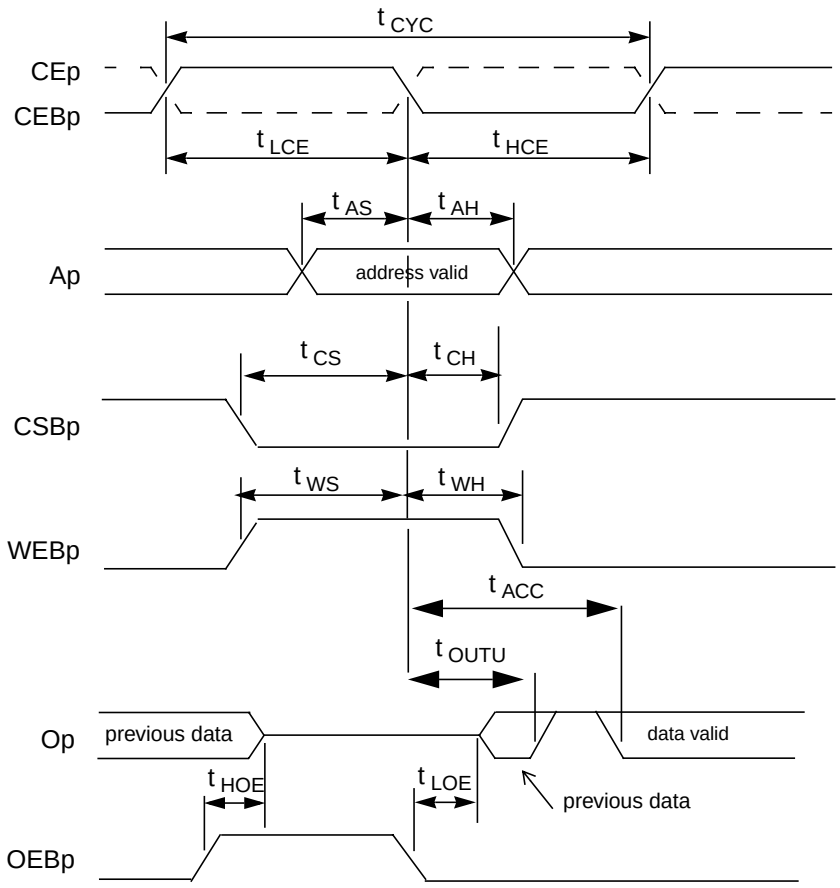
$$t_{OE}^{(drive, Cload)} = t_{OE} \text{ (from timing table)} + t_{DRIVE}^{(drive)} + Ramp^{(drive)} * Cload$$

$$t_{BA}^{(drive, Cload)} = t_{BA} \text{ (from timing table)} + t_{DRIVE}^{(drive)} + Ramp^{(drive)} * Cload$$

Timing Diagrams

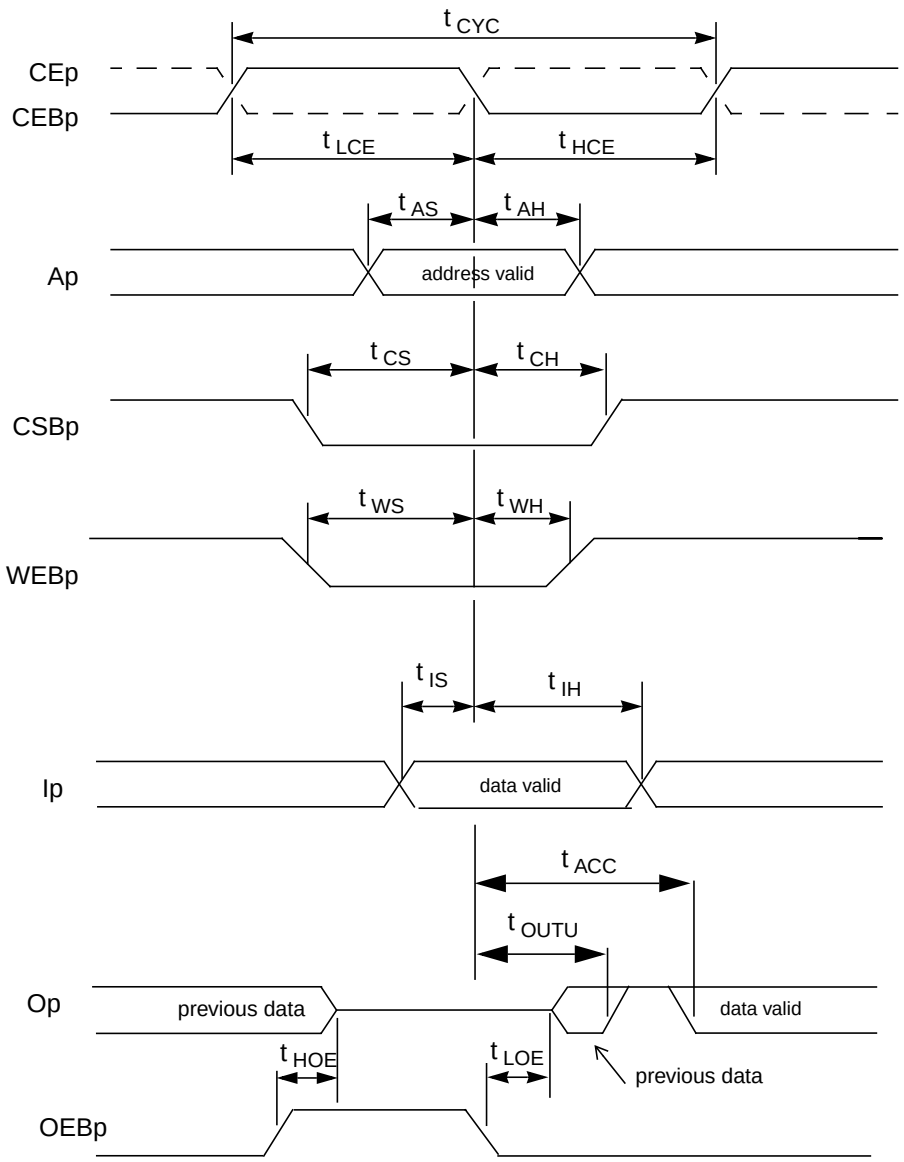
Read Cycle

Outputs are valid an access time (t_{ACC}) after CEBp goes Low (CEp goes High) and are latched until output precharge of the next cycle.



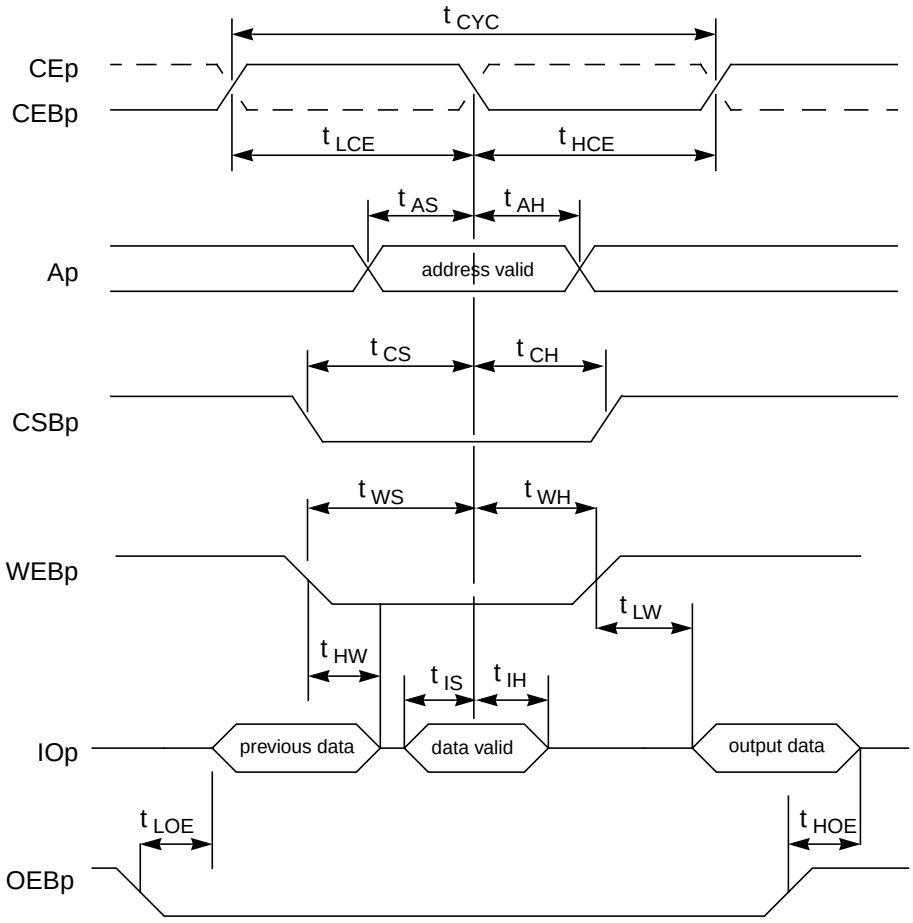
Write Cycle (IO separate)

During write operation the input data are available on output at access time (t_{ACC}) after CEBp goes Low (CEp goes High).



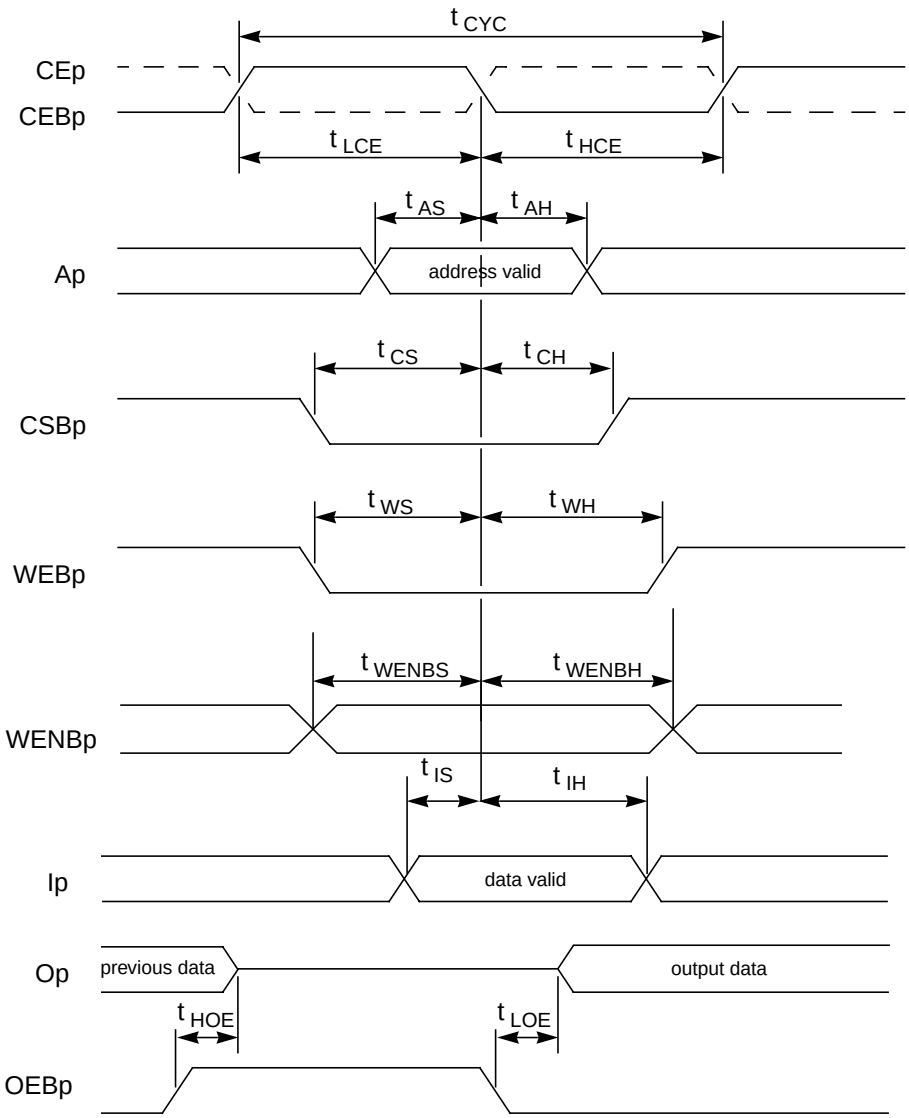
Write Cycle (IO common)

.

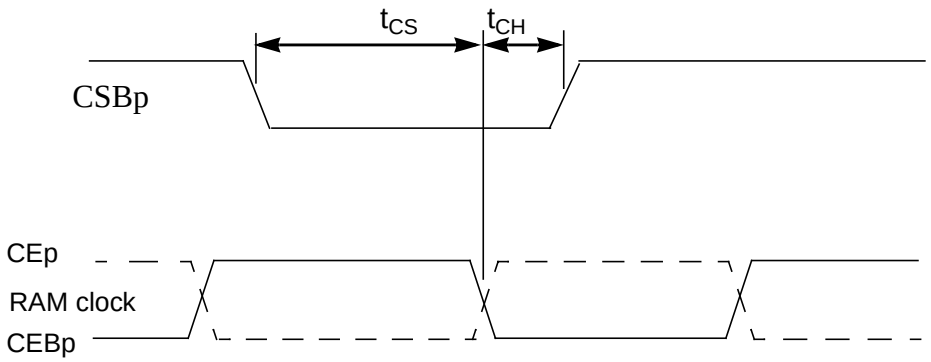


Write Cycle with optional select bit write

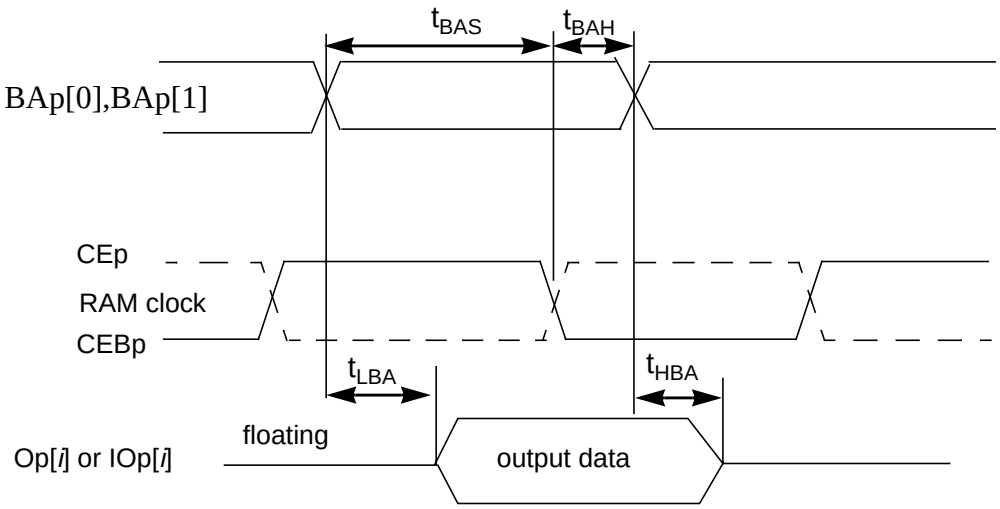
.



Chip selection waveforms

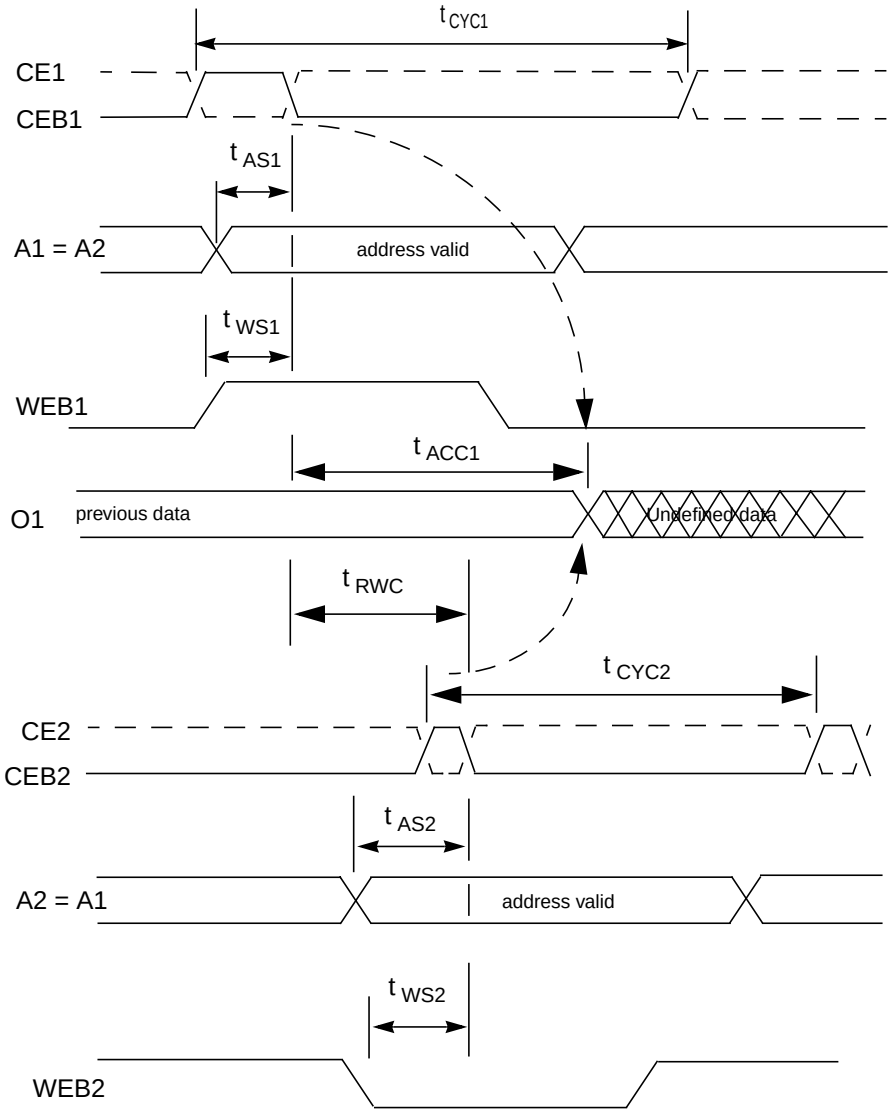


Bank address waveforms

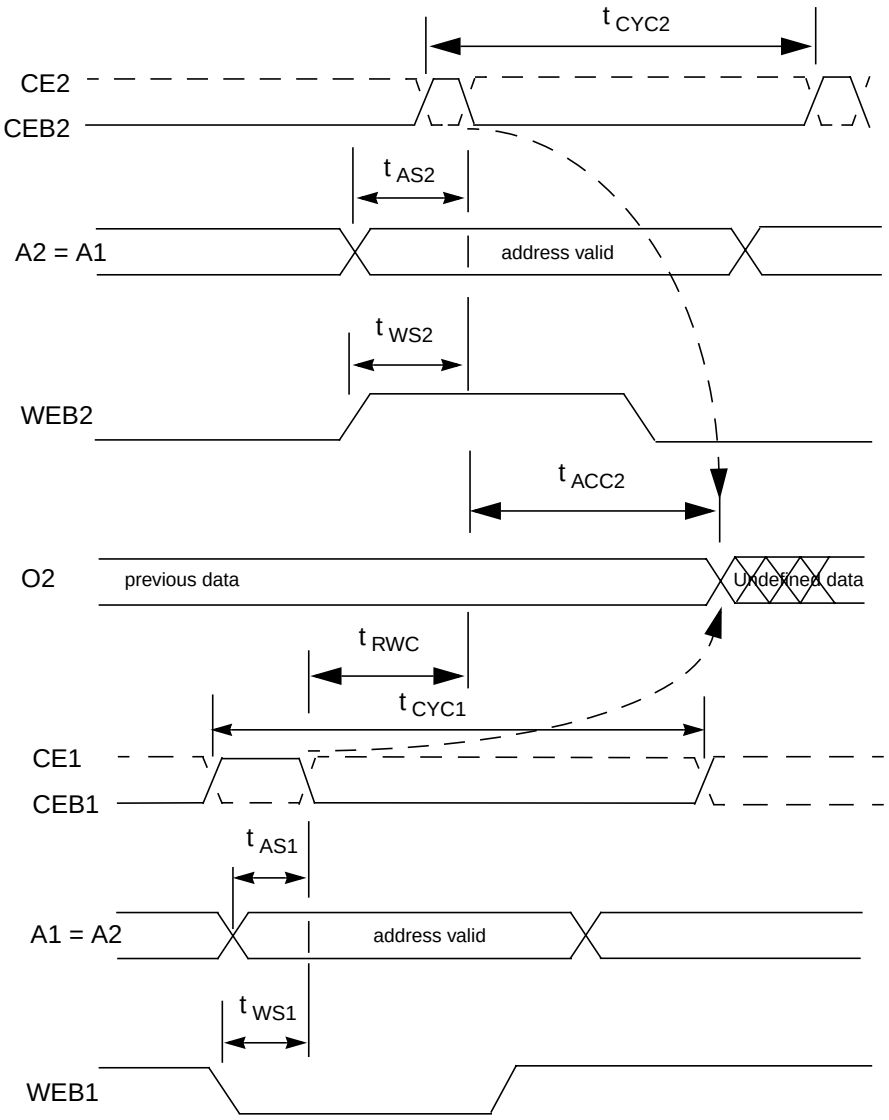


Read / Write (address match) conflict between two ports

Read (port1) and Write (port2) operation to one memory location be away from each other less than t_{RWC} time results to the undefined read operation output. The written data are always correctly stored in memory location.



Write (port1) is followed by the Read (port2)



Characterization Conditions

All timing and power models characterized for min/typ/max conditions:

Parameter Name	Typ	Max	Min
Temperature	25^{o}C	125^{o}C	-40^{o}C
VDD	1.8V	1.62V	1.98V
VSS	0V	0V	0V
process	Typ-P, Typ-N	Slow_P, Slow-N	Fast-P, Fast-N

All datasheet values are for typical conditions.

Technology files used for product development

Type	File Name	Version
STAR-RCXT	tsl18_30	3.0.1.3
Hercules DRC	tsl18_30drc.ev	3.0.1.8
HSPICE Models	tsl18_30	3.0.1.0

Internal Power Specifications

All these energies are given for one port

Following data correspond to 1024 words by 16 bits

Symbol	Description	Energy (μW/MHz)
E_W	Write operation energy	79.48
E_R	Read operation energy	70.16
E_A	Address change operation energy	0.17
E_S	Standby cycle energy	0.33

E_W is the energy during a write operation: CSB is low, active clock CE/CEB edge and no address change.

E_R is the energy during a read operation: CSB is low, active clock CE/CEB edge and no address change.

E_A is the energy during an address change operation, when the memory is selected: CSB is low, all addresses are changing.

E_S is the energy during a standby cycle, when the memory is not selected (CSB is high or, in the case of multi-banks, the bank is not selected).

Internal Power Calculation:

The internal power P (μW) can be calculated like follows:

E(μW/MHz) is either $E_{W,}E_R$, E_A, or E_S

$$P(\mu W) = E(\mu W/MHz) \times F(MHz)$$

where F - clock frequency

Simulation conditions

Following data correspond to typical simulation conditions:

Process	typical
Temperature	$25^{o}C$
Voltage	1.8V
Input transition time	0.2 ns
Output load capacitance	0 pF
Output drive	2X

Leakage Current Specifications

Following data correspond to 1024 words by 16 bits

Symbol	Description	Current (μA)
I_L	leakage current	0.76

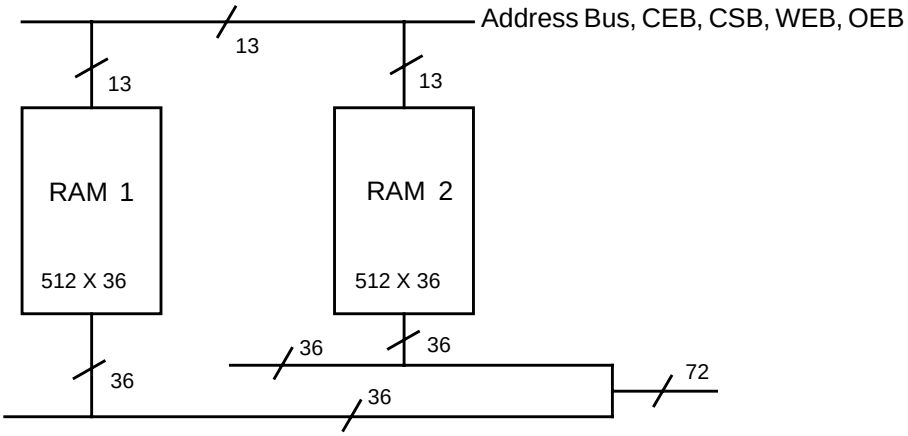
Simulation conditions:

Process	typ
Temperature	25^oC
Voltage	1.8V
Output drive	2X

I_L is the leakage current during a standby cycle:no clock toggle or address change.

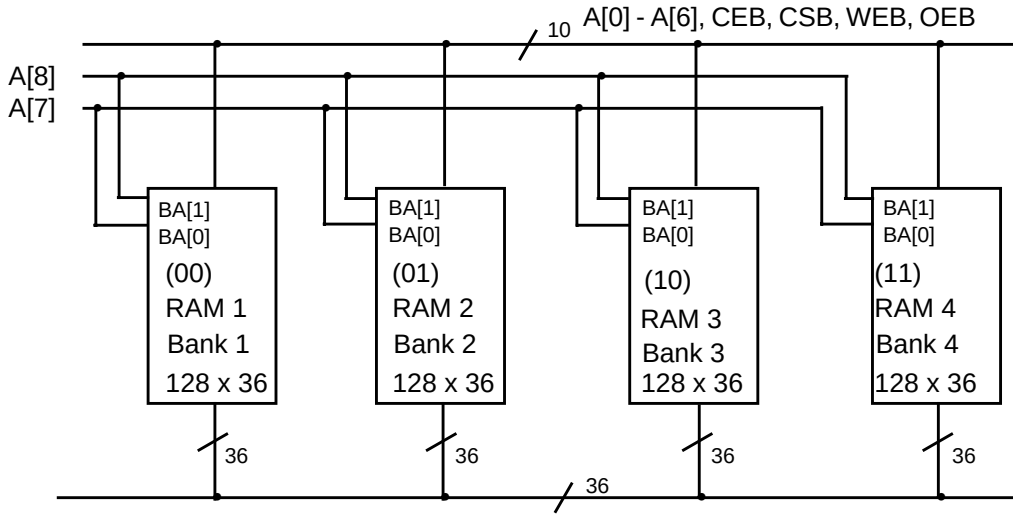
Applications

Expansion of Word Width



In the above figure, two RAMs are used in parallel to double the word width.

Expansion of Word Depth



In the above figure, high-speed 128 x 32 blocks are used to obtain a fast, low-power 512 x 32 memory. Using banks is a clever way to adjust the aspect ratio of the compiler.

Bank selection is determined by the BAp[0] and BAp[1] address inputs according to the following table:

BAp[1] (Ap[8])	**BAp[0] (Ap[7])**	**Bank Selected**
0	0	Bank 1
0	1	Bank 2
1	0	Bank 3
1	1	Bank 4

Chapter 2
Characteristics

This chapter includes the characteristics tables for the following word widths:

Word Width 8, page -3
Word Width 16, page -6
Word Width 24, page -9
Word Width 32, page -12
Word Width 48, page -15
Word Width 64, page -18
Word Width 72, page -21

Each table includes characteristics for different word depths. All the parameters correspond to typical conditions.

For a detailed description of each parameter, refer to *Chapter 1, Introduction*.

Word Width 8

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{CYC} (ns)	1.87	1.88	1.9	1.93	1.99	2.02	2.14	2.36	2.62
t_{ACC} (ns)[a]	1.36	1.37	1.39	1.42	1.49	1.51	1.64	1.79	2.05
width (µm)	156.1	156.1	156.1	156.1	156.1	264.3	264.3	499.3	499.3
height (µm)	94	106.5	131.4	181.1	280.6	280.6	479.7	481.6	879.7
E_W(µW/MHz)[b]	26.05	26.31	26.82	27.85	29.9	39.4	47.61	79.63	104.53
E_R(µW/MHz)[b]	23.93	24.11	24.49	25.23	26.73	36.55	42.52	72.77	76.1
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.3	0.31	0.33	0.34	0.36
E_{ADDR} (µW/MHz)[b,c]	0.07	0.08	0.1	0.12	0.13	0.15	0.17	0.17	0.19
I_L(µA)	0.16	0.17	0.18	0.21	0.27	0.38	0.61	1.38	2.59
t_{OUTU} (ns)	0.91	0.91	0.91	0.91	0.91	0.89	0.89	0.96	0.96
t_{HCE} (ns)	0.16	0.16	0.16	0.16	0.16	0.17	0.17	0.17	0.17
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.33	0.33
t_{IS} (ns)	0.09	0.09	0.09	0.09	0.09	0.09	0.09	0.11	0.11
t_{IH} (ns)	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.08	0.08	0.08	0.08	0.08	0.1	0.1	0.13	0.13
t_{WENBH} (ns)	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{BAS} (ns)	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.51	0.51
t_{BAH} (ns)	0	0	0	0	0	0	0	0	0

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{LOE}(ns)	0.51	0.51	0.51	0.51	0.51	0.53	0.53	0.61	0.61
t_{HOE} (ns)[a]	0.58	0.58	0.58	0.58	0.58	0.6	0.6	0.66	0.66
t_{LBA} (ns)	0.57	0.57	0.57	0.57	0.57	0.59	0.59	0.67	0.67
t_{HBA} (ns)[a]	0.63	0.63	0.63	0.63	0.63	0.65	0.65	0.63	0.71
t_{LW} (ns)	0.45	0.45	0.45	0.45	0.45	0.47	0.47	0.55	0.55
t_{HW} (ns)[a]	0.56	0.56	0.56	0.56	0.56	0.58	0.58	0.64	0.64
t_{RWC} (ns)	0.89	0.9	0.91	0.93	0.98	1.01	1.13	1.26	1.54

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
C_A (pF)	0.009	0.009	0.009	0.009	0.009	0.009	0.009	0.007	0.007
C_{WEB} (pF)	0.009	0.009	0.009	0.009	0.009	0.009	0.009	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.024	0.024	0.024	0.024	0.024	0.024	0.024	0.023	0.023
C_{OEB} (pF)	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.003	0.003	0.003	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.009	0.009	0.009	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.003	0.003	0.003	0.003

a. C_O given with drive 2X

Word Width 16

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{CYC} (ns)	1.91	1.92	1.93	1.96	2.03	2.08	2.2	2.42	2.69
t_{ACC} (ns)[a]	1.39	1.4	1.42	1.45	1.52	1.57	1.7	1.86	2.13
width (µm)	264.3	264.3	264.3	264.3	264.3	480.6	480.6	931.9	931.9
height (µm)	94	106.5	131.4	181.1	280.6	280.6	479.7	481.6	879.7
E_W(µW/MHz)[b]	44.18	44.57	45.35	46.9	50.02	67.02	79.48	149.67	204.9
E_R(µW/MHz)[b]	40.43	40.68	41.19	42.21	44.26	62	70.16	145.79	168.47
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.3	0.31	0.32	0.34	0.36
E_{ADDR} (µW/MHz)[b,c]	0.07	0.08	0.1	0.12	0.13	0.15	0.16	0.17	0.19
I_L(µA)	0.22	0.23	0.25	0.28	0.35	0.49	0.76	1.6	2.98
t_{OUTU} (ns)	0.94	0.94	0.94	0.94	0.94	0.92	0.92	0.99	0.99
t_{HCE} (ns)	0.18	0.18	0.18	0.18	0.18	0.19	0.19	0.18	0.18
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.33	0.33
t_{IS} (ns)	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.09	0.09
t_{IH} (ns)	0.31	0.31	0.31	0.31	0.31	0.32	0.32	0.32	0.32
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.06	0.06	0.06	0.06	0.06	0.07	0.07	0.11	0.11
t_{WENBH} (ns)	0.31	0.31	0.31	0.31	0.31	0.32	0.32	0.32	0.32
t_{BAS} (ns)	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.51	0.51
t_{BAH} (ns)	0	0	0	0	0	0	0	0	0

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{LOE}(ns)	0.53	0.53	0.53	0.53	0.53	0.56	0.56	0.65	0.65
t_{HOE} (ns)[a]	0.6	0.6	0.6	0.6	0.6	0.63	0.63	0.69	0.69
t_{LBA} (ns)	0.59	0.59	0.59	0.59	0.59	0.63	0.63	0.71	0.71
t_{HBA} (ns)[a]	0.65	0.65	0.65	0.65	0.65	0.68	0.68	0.74	0.74
t_{LW} (ns)	0.47	0.47	0.47	0.47	0.47	0.5	0.5	0.59	0.59
t_{HW} (ns)[a]	0.58	0.58	0.58	0.58	0.58	0.61	0.61	0.68	0.68
t_{RWC} (ns)	0.91	0.91	0.92	0.95	1	1.05	1.17	1.31	1.59

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
C_A (pF)	0.009	0.009	0.009	0.009	0.009	0.009	0.009	0.007	0.007
C_{WEB} (pF)	0.009	0.009	0.009	0.009	0.009	0.009	0.009	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.024	0.024	0.024	0.024	0.024	0.024	0.024	0.023	0.023
C_{OEB} (pF)	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.003	0.003	0.003	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.009	0.009	0.009	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.003	0.003	0.003	0.003

a. C_O given with drive 2X

Word Width 24

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{CYC} (ns)	1.94	1.95	1.97	2	2.07	2.36	2.62	2.66	2.74
t_{ACC} (ns)[a]	1.43	1.44	1.45	1.49	1.56	1.77	2.03	2.07	2.2
width (µm)	372.4	372.4	372.4	372.4	372.4	391.1	391.1	715.6	1364.6
height (µm)	94	106.5	131.4	181.1	280.6	481.6	879.7	879.7	879.7
E_W(µW/MHz)[b]	62.3	62.82	63.87	65.96	70.14	88.21	109.6	168.09	305.28
E_R(µW/MHz)[b]	56.93	57.25	57.9	59.2	61.78	73.74	84.25	136.54	260.85
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.3	0.31	0.32	0.34	0.36
E_{ADDR} (µW/MHz)[b,c]	0.07	0.08	0.1	0.12	0.13	0.14	0.16	0.17	0.19
I_L(µA)	0.28	0.29	0.31	0.35	0.43	0.68	1.06	1.83	3.36
t_{OUTU} (ns)	0.97	0.97	0.97	0.97	0.97	1	1	0.97	1.01
t_{HCE} (ns)	0.19	0.19	0.19	0.19	0.19	0.17	0.17	0.18	0.19
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.32	0.32	0.32	0.32	0.32	0.33	0.33	0.33	0.33
t_{IS} (ns)	0.05	0.05	0.05	0.05	0.05	0.08	0.08	0.08	0.07
t_{IH} (ns)	0.33	0.33	0.33	0.33	0.33	0.31	0.31	0.32	0.36
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.05	0.05	0.05	0.05	0.04	0.07	0.07	0.08	0.1
t_{WENBH} (ns)	0.33	0.33	0.33	0.33	0.33	0.31	0.31	0.32	0.36
t_{BAS} (ns)	0.49	0.49	0.49	0.49	0.49	0.51	0.51	0.51	0.51
t_{BAH} (ns)	0	0	0	0	0	0	0	0	0

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{LOE}(ns)	0.55	0.55	0.55	0.55	0.55	0.62	0.62	0.65	0.69
t_{HOE} (ns)[a]	0.62	0.62	0.62	0.62	0.62	0.67	0.67	0.7	0.73
t_{LBA} (ns)	0.61	0.61	0.61	0.61	0.61	0.68	0.68	0.71	0.74
t_{HBA} (ns)[a]	0.67	0.67	0.67	0.67	0.67	0.72	0.72	0.75	0.78
t_{LW} (ns)	0.49	0.49	0.49	0.49	0.49	0.56	0.56	0.59	0.62
t_{HW} (ns)[a]	0.6	0.6	0.6	0.6	0.6	0.65	0.65	0.68	0.71
t_{RWC} (ns)	0.92	0.93	0.94	0.97	1.02	1.25	1.53	1.56	1.63

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
C_A (pF)	0.009	0.009	0.009	0.009	0.009	0.007	0.007	0.007	0.007
C_{WEB} (pF)	0.009	0.009	0.009	0.009	0.009	0.007	0.007	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.024	0.024	0.024	0.024	0.024	0.023	0.023	0.023	0.023
C_{OEB} (pF)	0.005	0.005	0.005	0.005	0.005	0.006	0.006	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.009	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003	0.003

a. C_O given with drive 2X

Word Width 32

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{CYC} (ns)	1.98	1.98	2	2.04	2.1	2.38	2.64	2.69	2.79
t_{ACC} (ns)[a]	1.46	1.47	1.49	1.52	1.6	1.79	2.05	2.11	2.26
width (µm)	480.6	480.6	480.6	480.6	480.6	499.3	499.3	931.9	1797.2
height (µm)	94	106.5	131.4	181.1	280.6	481.6	879.7	879.7	879.7
E_W(µW/MHz)[b]	80.43	81.08	82.39	85.01	90.25	113.05	142.03	220.92	405.65
E_R(µW/MHz)[b]	73.43	73.82	74.61	76.18	79.31	94.4	109.75	182.14	353.22
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.3	0.31	0.32	0.34	0.36
E_{ADDR} (µW/MHz)[b,c]	0.07	0.08	0.1	0.12	0.13	0.14	0.16	0.17	0.19
I_L(µA)	0.34	0.35	0.38	0.42	0.52	0.78	1.2	2.05	3.75
t_{OUTU} (ns)	0.99	0.99	0.99	0.99	0.99	1.01	1.01	0.98	1.02
t_{HCE} (ns)	0.2	0.2	0.2	0.2	0.2	0.18	0.18	0.18	0.19
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.32	0.32	0.32	0.32	0.32	0.33	0.33	0.33	0.33
t_{IS} (ns)	0.03	0.03	0.03	0.03	0.03	0.07	0.07	0.07	0.06
t_{IH} (ns)	0.35	0.35	0.35	0.35	0.35	0.32	0.32	0.33	0.39
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.03	0.03	0.03	0.03	0.03	0.06	0.06	0.08	0.09
t_{WENBH} (ns)	0.35	0.35	0.35	0.35	0.35	0.32	0.32	0.33	0.39
t_{BAS} (ns)	0.49	0.49	0.49	0.49	0.49	0.51	0.51	0.51	0.51
t_{BAH} (ns)	0	0	0	0	0	0	0	0	0

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
t_{LOE}(ns)	0.57	0.57	0.57	0.57	0.57	0.63	0.63	0.68	0.72
t_{HOE} (ns)[a]	0.64	0.64	0.64	0.64	0.64	0.68	0.68	0.72	0.77
t_{LBA} (ns)	0.63	0.63	0.63	0.63	0.63	0.69	0.69	0.73	0.78
t_{HBA} (ns)[a]	0.69	0.69	0.69	0.69	0.69	0.73	0.73	0.77	0.82
t_{LW} (ns)	0.51	0.51	0.51	0.51	0.51	0.57	0.57	0.61	0.66
t_{HW} (ns)[a]	0.62	0.62	0.62	0.62	0.62	0.66	0.66	0.7	0.75
t_{RWC} (ns)	0.94	0.95	0.96	0.99	1.04	1.27	1.54	1.58	1.66

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth								
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**
C_A (pF)	0.009	0.009	0.009	0.009	0.009	0.007	0.007	0.007	0.007
C_{WEB} (pF)	0.009	0.009	0.009	0.009	0.009	0.007	0.007	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.024	0.024	0.024	0.024	0.024	0.023	0.023	0.023	0.023
C_{OEB} (pF)	0.005	0.005	0.005	0.005	0.005	0.006	0.006	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.009	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003	0.003

a. C_O given with drive 2X

Word Width 48

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
t_{CYC} (ns)	2.12	2.12	2.13	2.16	2.21	2.41	2.68	2.74
t_{ACC} (ns)[a]	1.53	1.54	1.55	1.58	1.63	1.84	2.1	2.18
width (µm)	715.6	715.6	715.6	715.6	715.6	715.6	715.6	1364.6
height (µm)	96	108.4	133.3	183.1	282.6	481.6	879.7	879.7
E_W(µW/MHz)[b]	119.98	121.36	124.12	129.64	140.67	162.74	206.89	326.58
E_R(µW/MHz)[b]	111.49	112.27	113.84	116.97	123.22	135.73	160.74	273.35
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.29	0.31	0.32	0.34
E_{ADDR} (µW/MHz)[b,c]	0.06	0.08	0.09	0.11	0.13	0.14	0.16	0.17
I_L(µA)	0.49	0.5	0.53	0.6	0.72	0.98	1.49	2.5
t_{OUTU} (ns)	1.04	1.04	1.04	1.04	1.04	1.03	1.03	1
t_{HCE} (ns)	0.19	0.19	0.19	0.19	0.19	0.19	0.19	0.19
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33
t_{IS} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{IH} (ns)	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.37
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.06
t_{WENBH} (ns)	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.37
t_{BAS} (ns)	0.51	0.51	0.51	0.51	0.51	0.51	0.51	0.51
t_{BAH} (ns)	0	0	0	0	0	0	0	0

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
t_{LOE}(ns)	0.66	0.66	0.66	0.66	0.66	0.66	0.66	0.72
t_{HOE} (ns)[a]	0.71	0.71	0.71	0.71	0.71	0.71	0.71	0.76
t_{LBA} (ns)	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.78
t_{HBA} (ns)[a]	0.76	0.76	0.76	0.76	0.76	0.76	0.76	0.81
t_{LW} (ns)	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.66
t_{HW} (ns)[a]	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.75
t_{RWC} (ns)	1	1.01	1.02	1.04	1.08	1.29	1.56	1.62

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
C_A (pF)	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
C_{WEB} (pF)	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.023	0.023	0.023	0.023	0.023	0.023	0.023	0.023
C_{OEB} (pF)	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003

a. C_O given with drive 2X

Word Width 64

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
t_{CYC} (ns)	2.14	2.15	2.16	2.19	2.24	2.45	2.71	2.79
t_{ACC} (ns)[a]	1.57	1.57	1.59	1.61	1.67	1.88	2.14	2.25
width (µm)	931.9	931.9	931.9	931.9	931.9	931.9	931.9	1797.2
height (µm)	96	108.4	133.3	183.1	282.6	481.6	879.7	879.7
E_W(µW/MHz)[b]	154.98	156.83	160.54	167.95	182.78	212.43	271.75	432.24
E_R(µW/MHz)[b]	143.45	144.53	146.7	151.04	159.71	177.05	211.74	364.55
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.29	0.31	0.32	0.34
E_{ADDR} (µW/MHz)[b,c]	0.06	0.08	0.09	0.11	0.13	0.14	0.16	0.17
I_L(µA)	0.61	0.63	0.66	0.74	0.88	1.18	1.77	2.95
t_{OUTU} (ns)	1.06	1.06	1.06	1.06	1.06	1.06	1.06	1.02
t_{HCE} (ns)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33
t_{IS} (ns)	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.04
t_{IH} (ns)	0.37	0.37	0.37	0.37	0.37	0.37	0.37	0.41
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.04
t_{WENBH} (ns)	0.37	0.37	0.37	0.37	0.37	0.37	0.37	0.41
t_{BAS} (ns)	0.51	0.51	0.51	0.51	0.51	0.51	0.51	0.51

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
t_{BAH} (ns)	0	0	0	0	0	0	0	0
t_{LOE}(ns)	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.77
t_{HOE} (ns)[a]	0.73	0.73	0.73	0.73	0.73	0.73	0.73	0.81
t_{LBA} (ns)	0.74	0.74	0.74	0.74	0.74	0.74	0.74	0.83
t_{HBA} (ns)[a]	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.86
t_{LW} (ns)	0.62	0.62	0.62	0.62	0.62	0.62	0.62	0.71
t_{HW} (ns)[a]	0.71	0.71	0.71	0.71	0.71	0.71	0.71	0.79
t_{RWC} (ns)	1.02	1.02	1.03	1.05	1.1	1.31	1.59	1.65

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
C_A (pF)	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
C_{WEB} (pF)	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.023	0.023	0.023	0.023	0.023	0.023	0.023	0.023
C_{OEB} (pF)	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003

a. C_O given with drive 2X

Word Width 72

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
t_{CYC} (ns)	2.16	2.16	2.18	2.2	2.26	2.47	2.73	2.82
t_{ACC} (ns)[a]	1.58	1.59	1.61	1.63	1.69	1.9	2.17	2.29
width (µm)	1040.1	1040.1	1040.1	1040.1	1040.1	1040.1	1040.1	2013.5
height (µm)	96	108.4	133.3	183.1	282.6	481.6	879.7	879.7
E_W(µW/MHz)[b]	172.47	174.56	178.75	187.11	203.83	237.28	304.18	485.07
E_R(µW/MHz)[b]	159.42	160.66	163.13	168.07	177.95	197.72	237.24	410.15
E_S(µW/MHz)[b]	0.23	0.25	0.26	0.28	0.29	0.31	0.32	0.34
E_{ADDR} (µW/MHz)[b,c]	0.06	0.08	0.09	0.11	0.13	0.14	0.16	0.17
I_L(µA)	0.67	0.69	0.73	0.81	0.96	1.28	1.91	3.17
t_{OUTU} (ns)	1.07	1.07	1.07	1.07	1.07	1.07	1.07	1.03
t_{HCE} (ns)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.21
t_{LCE} (ns)	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{AS} (ns)	0	0	0	0	0	0	0	0
t_{AH} (ns)	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{WS} (ns)	0	0	0	0	0	0	0	0
t_{WH}(ns)	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33
t_{IS} (ns)	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03
t_{IH} (ns)	0.38	0.38	0.38	0.38	0.38	0.38	0.38	0.43
t_{CS} (ns)	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{CH} (ns)	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
t_{WENBS} (ns)	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.03
t_{WENBH} (ns)	0.38	0.38	0.38	0.38	0.38	0.38	0.38	0.43
t_{BAS} (ns)	0.51	0.51	0.51	0.51	0.51	0.51	0.51	0.51
t_{BAH} (ns)	0	0	0	0	0	0	0	0

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
t_{LOE}(ns)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.79
t_{HOE} (ns)[a]	0.74	0.74	0.74	0.74	0.74	0.74	0.74	0.83
t_{LBA} (ns)	0.76	0.76	0.76	0.76	0.76	0.76	0.76	0.85
t_{HBA} (ns)[a]	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.88
t_{LW} (ns)	0.64	0.64	0.64	0.64	0.64	0.64	0.64	0.73
t_{HW} (ns)[a]	0.73	0.73	0.73	0.73	0.73	0.73	0.73	0.81
t_{RWC} (ns)	1.03	1.03	1.04	1.06	1.1	1.32	1.6	1.67

a. The timing is output load dependent: given with a load of 0pF and drive 2X
b. All the energies are given with an output load capacitance equal to zero. All input transition times are equal to 0.5ns. The simulation conditions are typical.
c. E_S and E_{ADDR} are given for half address bits changing.

Parameters	Word Depth							
	16	**32**	**64**	**128**	**256**	**512**	**1024**	**2048**
C_A (pF)	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
C_{WEB} (pF)	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
C_{CSB} (pF)	0.008	0.008	0.008	0.008	0.008	0.008	0.008	0.008
C_{CEB}/C_{CE} (pF)	0.023	0.023	0.023	0.023	0.023	0.023	0.023	0.023
C_{OEB} (pF)	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_I (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003
C_O(pF)[a]	0.006	0.006	0.006	0.006	0.006	0.006	0.006	0.006
C_{IO} (pF)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.009
C_{BA} (pF)	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
C_{WENB} (pF)	0.004	0.004	0.004	0.004	0.004	0.004	0.004	0.003

a. C_O given with drive 2X

Chapter 3
Derating Information

The propagation delay values apply only to the specified operating conditions of a VDD level of 1.8 volts, a junction temperature of 25 degrees C, and a Typ-Typ process. You can estimate the delay under different conditions by using the graphs and tables in this chapter. The sections in this chapter provide information on the following:

- *Derating Equations, page 3-2*
- *Power Dissipation, page 3-4*

Derating Equations

Delays can be estimated in the case of different voltage, temperature and process conditions than the characterized ones by using the following equations:

Typical process case:

$t_{DELAY\_DERATED\_TYP}=t_{DELAY\_TYP}*(1+K_{Vtyp}*[VDD-VDD_{TYP}])*(1+K_{Ttyp}*[T-T_{TYP}])$

Fast process case:

$t_{DELAY\_DERATED\_MIN}=t_{DELAY\_TYP}*K_{Pmin}*(1+K_{Vmin}*[VDD-VDD_{TYP}])*(1+K_{Tmin}*[T-T_{TYP}])$

Slow process case:

$t_{DELAY\_DERATED\_MAX}=t_{DELAY\_TYP}*K_{Pmax}*(1+K_{Vmax}*[VDD-VDD_{TYP}])*(1+K_{Tmax}*[T-T_{TYP}])$

where:

$t_{DELAY\_DERATED\_TYP}$ is the wished voltage-temperature derated timing with a *typical process* (typical N and typical P model transistors),

$t_{DELAY\_DERATED\_MIN}$ is the wished voltage-temperature derated timing with a *fast process* (fast N and fast P model transistors),

$t_{DELAY\_DERATED\_MAX}$ is the wished voltage-temperature derated timing with a *slow process* (slow N and slow P model transistors),

t_{DELAY_TYP} is the typical delay timing from datasheet,

t_{TYP} is the typical temperature used in datasheet: t_{TYP} = 25 degreesC,

VDD_{TYP} is the typical voltage used in datasheet: VDD_{TYP} = 1.8 volts,

The min condition used : VDD_{MIN} =1.98volts, T_{MIN} =-40 degreesC,

The max condition used : VDD_{MAX} =1.62volts, T_{MAX} =125 degreesC,

T is the junction temperature over the operating temperature range of -40 degreesC to +125 degreesC,

VDD is the voltage over the operating voltage range of 1.62 volts to 1.98 volts,

$K_{P(typ, min, max)}$ is the process derated factor,

$K_{V(typ, min, max)}$ is the voltage derated factor for each process,

$K_{T(typ, min, max)}$ is the temperature derated factor for each process.

The derating factors for TSL18RD130 are shown in the following table:

Process	Min	Typ	Max
K_P	0.8	1.0	1.2
K_V	-0.5652	-0.6052	-0.5871
K_T	0.0015	0.0014	0.0012

Example

Conditions:

Junction Temperature: T = 125 degC,

Voltage: VDD = 1.62 Volts,

Fast N and Fast P model transistors.

t_{DELAY_TYP} = 1.36 ns (Chapter 2 table rd16x8).

We are in the case of a *fast process*, so the following equation is used:

$$t_{DELAY\_DERATED\_MIN} = t_{DELAY\_TYP} * K_{Pmin} * (1 + K_{Vmin} * [VDD - VDD_{TYP}]) * (1 + K_{Tmin} * [T - T_{TYP}])$$

With the above conditions, the derated timing is:

$t_{DELAY\_DERATED\_MIN}$= 1.36*0.8*(1-0.5652*[1.62 - 1.8])*(1+0.0015*[125 - 25])

$t_{DELAY\_DERATED\_MIN}$= 1.38 ns.

Power Dissipation

The majority of power dissipation in a CMOS circuit is the AC element that results from the charging and discharging of capacitors. Some power dissipation can be attributed to crossover currents, but this factor is usually less than 20% of the AC power dissipation. The VDD voltage is responsible for the greatest variation in power dissipation.
The following equation can be used to calculate the total power dissipation of RAM:
If output is active (OEB =’0’ and BA matching)

m = number of switching outputs i.e. outputs with programmed ’0’.
Cout(i) = load capacitance in F for i switching output.
Pt = total internal power in W.
F = output switching frequency in Hz.

$$PowerDissipation(W) \leq Pt + \left[\langle VDD^2 \times \sum_{i=1}^{m} Cout(i) \rangle \right] \times F$$

Maximum power dissipation occurs when m = word width

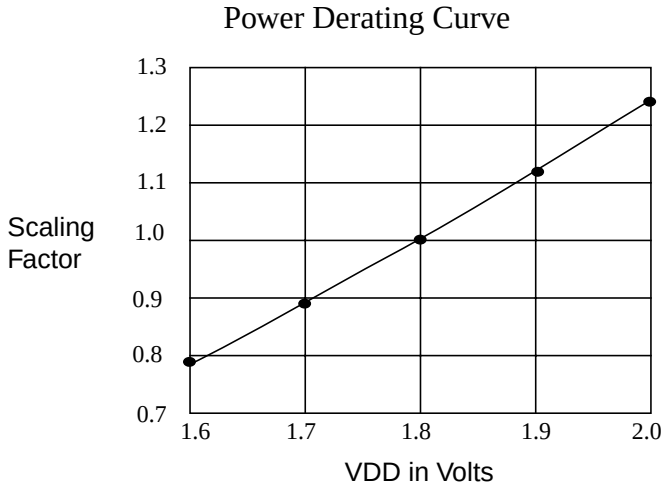
If output is inactive (OEB =’1’ or BA not matching), the above equation is reduced to the part of the internal power

$$PowerDissipation(W) \leq Pt$$

Derating

The equation assumes a source voltage (VDD) of 1.8 volts, typical N and typical P model parameters, and a junction temperature of 25 degrees C.

To estimate the power dissipation at a voltage other than 1.8 volts, first calculate the total power dissipation, then multiply by the scaling factor from the following graph:



For example, if the estimated power with VDD at 1.8V is 2 watts, then with VDD at 1.6 volts, the power decreases to 0.79* 2watts = 1.58 watts.