Single electron and hole quantum dot transistors operating above 110 K

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Both single electron and hole quantum dot transistors in silicon-on-insulator were fabricated and characterized. The quantum dots were formed using electron-beam nanolithography and reactive ion etching. The single electron quantum dot transistors show the oscillation of the drain current as a function of the gate voltage at temperatures up to 170 K and drain biases up to 80 mV. The oscillation is due to electron tunneling through the discrete energy levels inside the quantum dot. The average energy level spacing is ~60 meV. Data analysis shows that the discrete energy levels are caused by Coulomb interaction as well as quantum size effects. The single hole quantum dot transistors show similar oscillations up to 110 K and drain biases up to 50 mV. The average energy level spacing is ~36 meV. © *1995 American Vacuum Society.*

I. INTRODUCTION

Until recently, quantum dot transistors (QDTs) have been primarily based on GaAs–AlGaAs heterojunction and the electric field-induced confinement.[1] However, the electric field-induced confinement cannot create a quantum dot small enough to permit high operation temperatures. With the recent advancement in silicon-on-insulator (SOI) wafers, particularly separation by implanted oxygen (SIMOX) wafer technology, it is now possible to use silicon dioxide to form very small quantum dots with excellent confinement.[2–4]

We have developed a new method of fabricating QDTs on SIMOX using electron-beam lithography (EBL) and reactive ion etching (RIE). By using EBL instead of the stress-dependent oxidation rate to define the quantum dots[3] the sizes and shapes of the quantum dots could be better controlled. Using this method, we have fabricated single electron and single hole silicon QDTs that can operate above 110 K. The possibility of single hole QDTs have been speculated for some time;[5] however, they were not demonstrated in any three terminal devices except for some studies on hole Coulomb blockades in Si–SiGe two terminal diodes.[6,7] In this paper, we present the fabrication process of both single electron and single hole QDTs in silicon and compare their characteristics.

II. DEVICE STRUCTURE

As shown in Fig. 1, the silicon QDT consists of a quantum dot separated from the source and the drain by two constrictions. The quantum dot is surrounded by thermal oxide and has a gate on top that can change the charge concentration inside the dot. Since the quantum dot is small, discrete energy levels will be formed. The constrictions with a size smaller than that of the quantum dot create the tunneling barriers: one is between the quantum dot and the source and the other is between the quantum dot and the drain. The source and the drain were doped *n*-type for electron QDTs and *p*-type for hole QDTs. For single electron QDTs, the gate and drain voltage are positive to induce electrons in the quantum dot and to drive the electrons from the source to the drain. For hole QDTs, the two biases are reversed. When one of the discrete energy levels inside the dot is aligned with the Fermi level at the source, charge can tunnel through the barriers, giving resonant tunneling current. The resonance and off-resonance in the tunneling lead to the drain current oscillating with the charge population in the quantum dot, and therefore with the gate voltage.

III. FABRICATION

The starting SIMOX wafer has a 360-nm-thick buried oxide and 60-nm-thick top silicon layer. A 30-nm-thick sacrificial oxide was grown first and optical lithography was used to pattern the oxide for the active area as shown in Fig. 2. EBL was used to pattern the quantum dot with polymethymethacrylate (PMMA) resist. The pattern on PMMA was then transferred to the sacrificial oxide layer which in turn was transferred to the top silicon layer using RIE as shown in Fig. 2. After the removal of the sacrificial oxide mask, the gate oxidation was performed followed by the deposition and patterning of undoped polysilicon to cover the whole quantum dot. This was followed by self-aligned source drain implantation. For the electron QDTs, phosphorus implantation with dose of 2×10^{15} cm^{-2} and energy of 40 keV was used, while BF_2^+ implantation with dose of 2×10^{15} cm^{-2} and energy of 70 keV was used for the hole QDTs. The final anneal to activate the dopant was done at 950 °C in a regular fur-

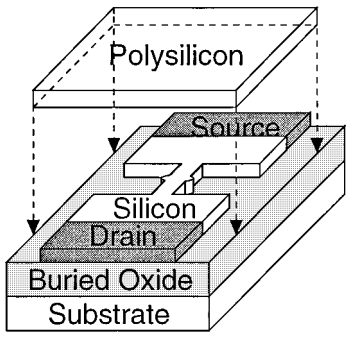


FIG. 1. Schematic of a silicon quantum dot transistor with quantum dot separated from the source and drain by the two constrictions. For clear illustration, the gate is lifted and the gate oxide is not shown.

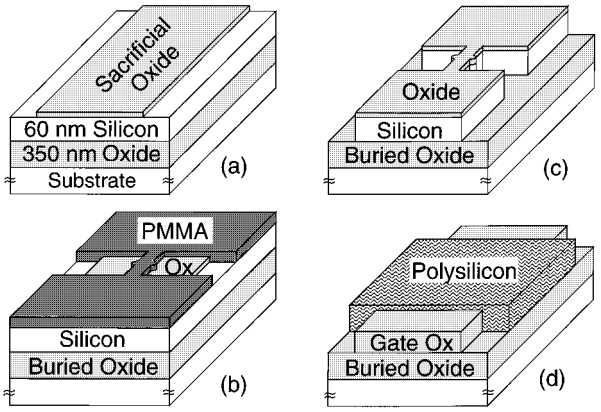


FIG. 2. The simplified fabrication steps of the silicon QDTs. (a) Definition of active area by optical lithography. (b) Patterning of PMMA with EBL. (c) Etching of sacrificial oxide with PMMA mask and silicon with sacrificial oxide mask. (d) Gate oxide growth and polysilicon gate definition.

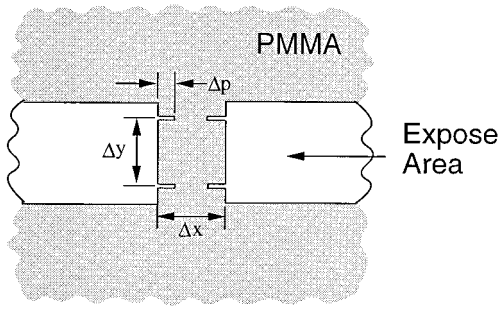


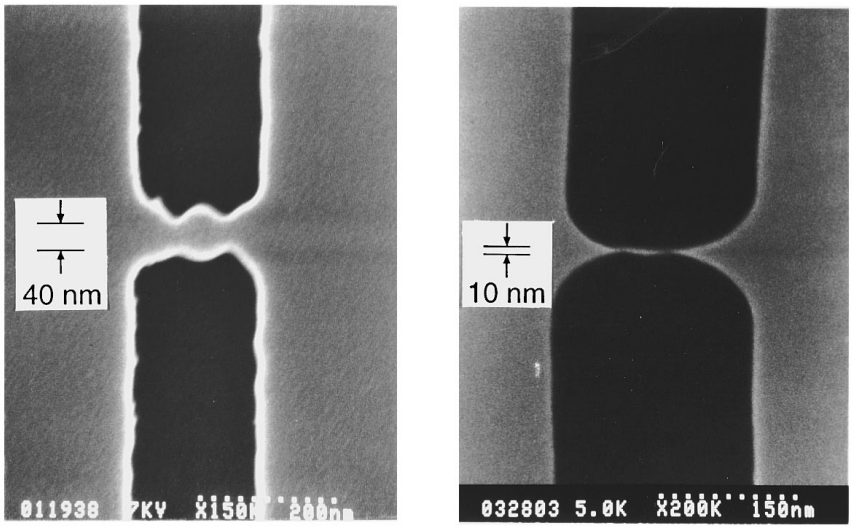
FIG. 3. The e-beam lithography patterns used in exposing the quantum dot. The gap (Δx) and the width (Δy) are 50–75 nm. The Δp is 16–24 nm.

nace. Aluminum was used for final metalization with titanium as a barrier metal. Finally, the devices were sintered in forming gas to reduce the interface states.

As shown in Fig. 3, the EBL pattern used to define the quantum dots consists of two boxes, similar to those of the split gate pattern,[1] and four lines. The size of the quantum dot was defined by the gap between the split gates (Δx) and by the distance between the two constrictions (Δy), which were designed to be around 50–75 nm. The actual defined dots sizes were smaller due to the proximity effect in EBL and silicon consumption during gate oxidation. The constrictions were formed by the four lines extending outside the boxes. The typical extension (Δp) was 16 nm on each side. However, the actual extension was smaller due to proximity effect. The exposed PMMA was developed in cellosolve:methanol solution.

In the quantum dot definition, the PMMA was used as an etch mask for the sacrificial oxide layer. RIE with CHF_3 gas was used to etch the oxide with a selectivity better than 1:1 between the oxide and PMMA. The patterned sacrificial oxide was then used as an etch mask for the top silicon layer. Chlorine-based RIE was used for etching the silicon. Afterwards the top sacrificial oxide was etched away using HF. In the process, some of the buried oxide under the quantum dot was also etched away. This turned out to be advantageous because it exposed the bottom surface of the quantum dot for oxidation during the gate oxidation step. Figure 4(a) shows a quantum dot after the silicon RIE.

Gate oxidation was done at 1000 °C to form a gate oxide thickness of 42 nm. The high temperature oxidation step would anneal any damages caused by RIE. The oxidation consumed the silicon and hence reduced the initial size of the quantum dots by about 35 nm. Figure 4(b) shows a quantum dot after gate oxidation and with the gate oxide removed. It looks like an ellipsoid instead of a sphere. Its size is about 10 nm×30 nm×30 nm. To fabricate a more spherical quantum



(a) (b)

FIG. 4. (a) SEM micrograph of the silicon quantum dot after the silicon RIE. (b) SEM micrograph of the silicon quantum dot transistor after the gate oxidation and removal of the gate oxide.

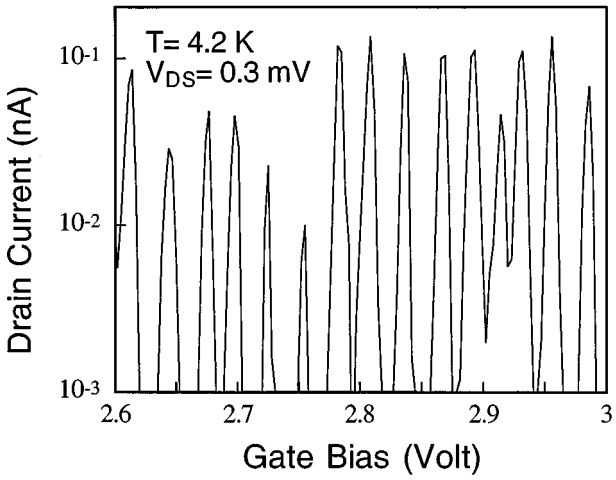


FIG. 5. The drain current vs gate voltage of the electron QDT at 4.2 K and 0.3 mV drain bias.

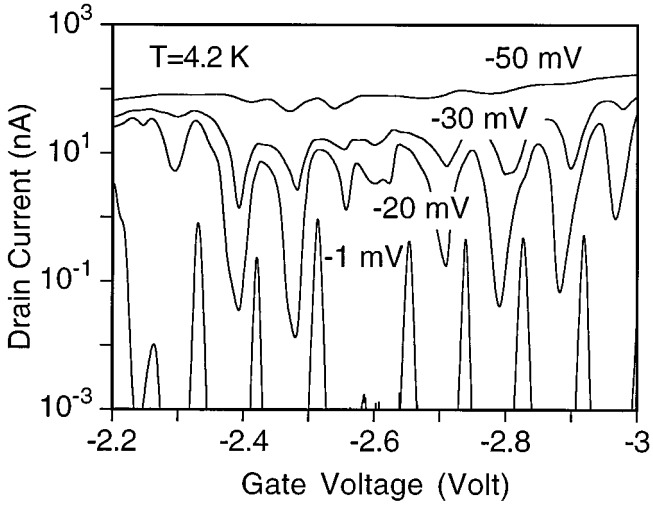


FIG. 7. The drain current vs gate voltage of the hole QDT for various drain biases.

dots, the distance between constrictions (Δy) should be reduced.

The fabrication processes of the electron and hole QDTs are very compatible. The only difference is in the source and drain implantation step. Both devices were fabricated on the same top silicon layer with boron doping concentration of approximately 3×10^{15} cm^{-3}. However, for the given dot size, the average number of dopants inside a dot was only $\sim$0.03; therefore the dot was virtually undoped.

IV. DEVICE CHARACTERISTICS

The QDTs were measured using a HP-4145B and in a variable temperature chamber. For the single electron QDTs, the gate was *positively* biased to induce electrons under the gate. As the electrons were induced in the quantum dot one by one, the drain current oscillated as a function of the gate bias as shown in Fig. 5. Each oscillation peak corresponds to the tunneling of electrons through one discrete single electron energy level inside the quantum dot. At 4.2 K, the peak current is at least two orders of magnitude higher than the valley current. In the measurement, the drain voltage was kept at 0.3 mV to prevent heating effects.

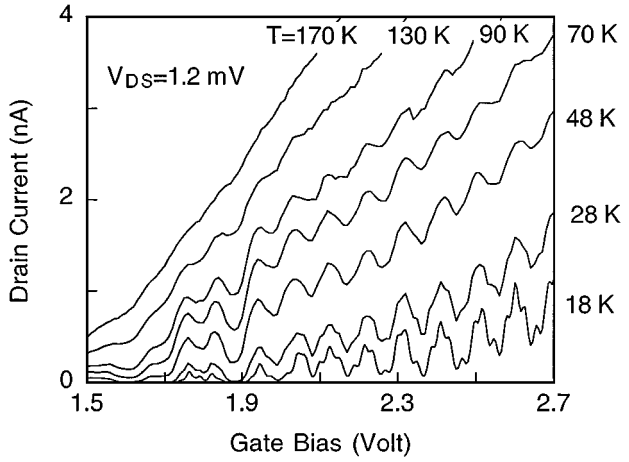


FIG. 6. The drain current vs gate voltage of the electron QDT at various temperatures.

Figure 6 shows the effects of temperature that varies from 18 to 170 K. As the temperature increased, the peaks broadened because of thermal broadening of the energy levels. However, some oscillation peaks persisted over 170 K indicating a large energy level spacing inside the quantum dot.

For single hole QDTs, the gate was biased *negatively* in order to induce holes in the quantum dot. The drain bias was also biased *negatively* to drive holes from the source into the drain. As the holes were induced in the quantum dot, the drain current oscillated (Fig. 7). The peak-to-valley current ratio is well above 1000 at a 1 mV drain voltage. When a higher drain bias was applied, the separation between source Fermi level and drain Fermi level increased which introduced a larger energy window for tunneling to occur. Consequently, the oscillation peaks in the drain current were broadened just as if the temperature was increased.

The temperature dependence for the hole QDTs is shown in Fig. 8. At 81 K, the oscillation peaks can still be clearly seen. In fact, we have experimentally observed that the oscillation peaks persisted to 110 K.

The average energy level spacing inside the QDTs can be estimated from the temperature or the drain bias dependencies of the current-voltage (I-V) characteristics. The energy level spacing (ΔE) is approximately equal to $4kT_m$, where T_m is the maximum temperature at which we can still observe the drain current oscillation and k is the Boltzman constant. By measuring the T_m the average energy level spacing was estimated to be 60 meV for the electron QDTs, and 36 meV for the hole QDTs. The drain bios dependent study for hole QDTs also confirms the energy level spacing estimation.[8]

To study the origin of the large energy spacing, we estimated the quantum size energy and Coulomb charging energy. This analysis indicates both the quantum size effect and the Coulomb blockade effect are significant. By assuming

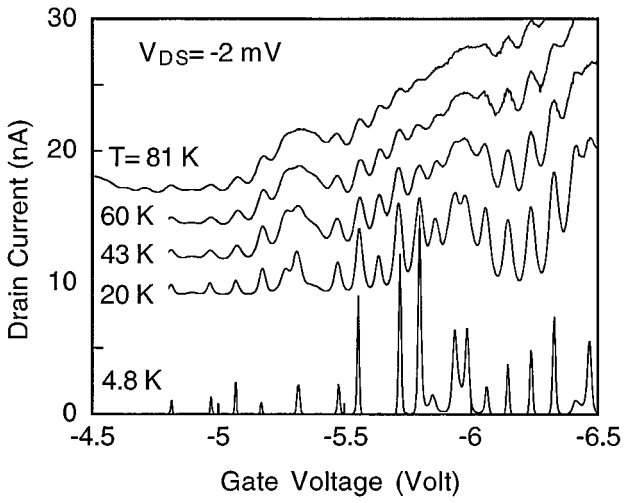


FIG. 8. The drain current vs gate voltage of the hole QDT for various temperatures. The curves have been displaced for clarity.

the quantum dot to be a box, the quantum energy level spacing in the electron and hole QDTs were estimated to be 30 and 10 meV, respectively. The Coulomb energy spacing for the electron and hole QDTs were estimated to be 30 and 25 meV, respectively.

V. CONCLUSION

We have developed a controllable method to fabricate single electron QDTs on SOI that show oscillation at 170 K and have energy level spacing of ~60 meV. We have also fabricated single hole QDTs that show oscillation at 110 K and have energy level spacing of ~36 meV. Each oscillation peak corresponds to the resonant tunneling of charges through the discrete energy levels inside the quantum dot. The large energy level spacing is due to contribution of both Coulomb interaction and quantum size effects. As to our knowledge, this is the first fabrication of three terminals hole QDTs, which opens the possibilities of using them to complement the electron QDTs in logic circuits.[8]

ACKNOWLEDGMENTS

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