Verification Report

Verification Environment for RISC-V-IMC Core

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# Introduction to the Device-Under-Test (DUT)

The DUT is a RISC-V core with IMC extension. The design has 25 input/output signals which connect the DUT with a Compressed Decoder module, Clint module and a Top module. The RISC-V core has the capability to run 32-bit Integer Instructions, 32-bit Multiply Instructions and 16-bit Compressed Instructions on a 3 stage pipeline. It has a clock and an active low reset signal. Other signals include interrupt handling, connection with Instruction Memory, Data Memory & Compressed Decoder.

# Verification Plan

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| **No.** | **Feature** | **Test Description** | **Ref.** | **Type** | **Result** | **Comments** | **Stimulus** |
| 1 | R-Type Compressed Instructions | Checking if the read from register and write to the register is working or not. Moreover, accuracy of the specified arithematic operation will also be checked. |  | Transaction |  |  | Random |
| 2 | I-Type Compressed Instructions | Checking if the read from register and write to the register is working or not. Moreover, accuracy of the specified arithematic operation will also be checked.  In case of Load instruction, reading from memory will also be tested. |  | Transaction |  |  | Random |
| 3 | S-Type Compressed Instructions | Writing into memory will be tested. |  | Transaction |  |  | Random |
| 4 | J-Type Compressed Instructions | Checking if the Program Counter works properly or not in case of an unconditional jump. |  | Transaction |  |  | Directed or Random |
| 5 | B-Type Compressed Instructions | Checking if the Program Counter works properly or not in case of an conditional jump. |  | Transaction |  |  | Directed or Random |
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## Explanation of Different Fields

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| --- | --- |
| **No.** | The serial number of the test. |
| **Feature** | The feature which the current test is verifying in full or partially.  The feature is usually on the abstraction level of a user. |
| **Test Description** | A detailed description of the test case being performed.  You can be as verbose as you want. |
| **Ref.** | Reference to the section in the related standard document.  The section number as well as page numbers should be described here. |
| **Type** | Type of the test. Whether the test is an assertion (A) or a transaction (T) type. |
| **Result** | Pass (P) or Fail (F). |
| **Comments** | Any other comments about the test or its results that you want to mention. |
| **Coverage** | Code or Functional |
| **Stimulus** | Mention the kind of stimulus given. i.e directed system verilog |