Paper Title

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Abstract—Insert abstract text here

Index Terms—Insert keywords here

I. Introduction

The result of the astronomical impact of the very large scale integration (VLSI) industry on the global economy and the extreme widespread use of electronic devices and equipment in various fields across the globe have led to the exponential increase in demand and sophistication of electronic devices. This, of course, goes along with Moore's law which refers to Gordon Moore's projection in 1965 that the number of transistors crammed in integrated circuits (ICs) doubles every two years, though their cost is halved. This increase in the number of transistors put in an IC comes at a cost which are the problems that arise during both the design process and the fabrication process of such intricate devices. This paper addresses the role of placement in the physical design process. Placement tools are used mainly for two things, the first is to place cells in a suitable way for the consequent routing process, and the second is to guide both synthesis and floorplanning processes. Over the years, placement has no longer become a fine-tunning tool used in physical design, but for that matter, it has become a notable contributor to the timing closure process results as well as being an overall major step in physical design. Conventionally, placement is divided into two subprocesses, global placement and detailed placement, however, the scope of this paper will focus exclusively on the former. Global placement aims to evenly and legally distribute the cells over the available placement region putting in mind cells relative positions to each other globally regardless of local problems that may arise, hence the name. This goal is achieved in favour of certain cost metrics such as overall wirelength and the time taken to achieve such a goal. The placement problem is to place the cells in such a way to achieve the best possible cost metrics. Much like the well-known travelling salesman problem and most, if not all, physical design problems, it is an NP-complete problem in combinatorial optimization. Most of the attempts at solving this problem use heuristic algorithms instead of the ineffective brute force trivial approach. Among those metaheuristics are simulated annealing which is popularly used in the optimization of this particular problem, and genetic algorithm which is used for optimization problems in general. In this paper, we implemented the best of both worlds to achieve overall better optimization in terms of wirelength and time.

II. Related Work

As already stated, the placement problem is an NP-complete problem where its optimum solution can be found by trying all possible cells configurations, but due to the tremendous number of cells that exist in almost all VLSI designs which range from millions to billions of cells, it would be utterly impractical to compute every possible configuration in order to find the fittest one. Because of this nature, previous literature made significant improvements in terms of solution fitness and the amount of time consumed through using heuristic techniques such as simulated annealing used in [7], [10], [11], [12], [13] and [14], min-cut placement algorithm used in [1] and [15] and genetic algorithms used in [2], [3] and [7]. However, optimizing placement algorithms isn't limited to heuristic approaches only as others have used different approaches to achieve solid results. For instance, Natarajan et al [8] used an analytical placement algorithm that is based on the quadratic placement approach.

A. Simulated Annealing

Simulated annealing is one of the popular and most effective algorithms among all placement algorithms, in fact, it is generally used as an optimization technique for combinatorial problems. The basic idea of this method comes from the annealing treatment in metallurgy. Annealing in metallurgy is used to accomplish a crystalline lattice structure of the particles of solid metal as it reflects a minimum energy state for the solid. This is achieved by heating the metal in a heat bath until it reaches a temperature named the initial temperature of the annealing process at which all particles are randomly arranged, then whenever the metal reaches thermal equilibrium the temperature is reduced gradually according to a cooling schedule otherwise the resulting crystal will not mirror a minimum energy state. This analogy applies to the simulated annealing metaheuristic where an initial value of temperature T is set and at each iteration, the positions of the cells get scrambled around legal regions then the cost function C is measured, a result is accepted whenever it leads to a decreasing cost function, however, if a result leads to an increasing cost function, it is accepted if and only if the move has a probability greater than a random value between 0 and 1. The probability function is defined as follows:

$$P = e^{\frac{-\Delta C}{T}} \qquad (1)$$

At the end of each iteration, the temperature value decreases by multiplying it by a cooling factor which is less than 1. This process iterates until the temperature goes below 1. It is clear that the performance of this algorithm is based upon four parameters/steps:

1) Initial Configuration: In this step, the individual cells are extracted from the circuit and for each cell, the inputs and outputs are determined. The following diagram and table show the circuit is decomposed.
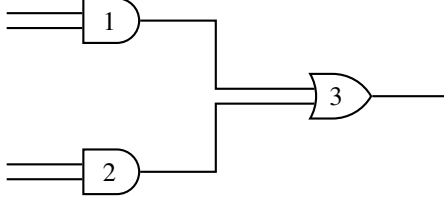

Fig. 1. Sample circuit diagram

TABLE I
SAMPLE CELLS DATA

Cell	Input	Output
1	-	3
2	-	3
3	2	-

At this step, the total wirelength of cells interconnections will most likely be large due to them being placed randomly. Hence the presence of the rest of the subsequent procedures which aim to achieve the optimal placement of the cells.

2) Move Generation Function: At each iteration, cells are rearranged to generate a new placement configuration of the cells. To do so, there are two possible strategies used:

- Move cells randomly to new legal positions
- Swap the positions of each two cells

3) Cost Function: The cost function consists of two terms as follows:

$$C = C_1 + C_2 \qquad (2)$$

Where C_1 is the measure of the total wirelength and C_2 is the measure of total overlap of the chip which is sometimes neglected as in our case but it is used in other papers [16] nevertheless.

Let d_h^{ij} d_v^{ij} be the horizontal and the vertical distance between cell i and its jth out cell respectively, the total wire length of the chip can be expressed as the following equation

$$C_1 = \sum_{i=cell}^{n} \sum_{j=outcell}^{n} (d_h^{ij} + d_v^{ij}) \qquad (3)$$

Where n is the total number of cells in the chip In case of the second term C_2, whenever two cells are swapped, they might overlap, therefore, O_{ij} indicates the overlap between cell i and cell j, this overlap is undesirable and it negatively affects the cost function by increasing its value by the term C_2 which is the summation of each overlap value squared.

$$C_2 = \sum_{i!=j} (O_{ij}^2) \qquad (4)$$

The cost function is calculated at each iteration after generating a new cells layout.

4) Annealing Schedule:

III. PROPOSED APPROACH

Insert proposed approach here

IV. EXPERIMENTAL ANALYSIS

A. Assumptions

Insert assumptions here

B. Experimental Scheme

Insert I/O here

C. Performance Metrics

Insert performance metrics here
Insert simulation output here

D. Performance Comparisons

Insert experiments comparisons here

E. Observation

Insert observation here

V. CONCLUSION AND FUTURE WORK

Insert conclusion and future work here

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