

bits

First Structure:

4

4

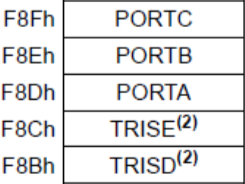
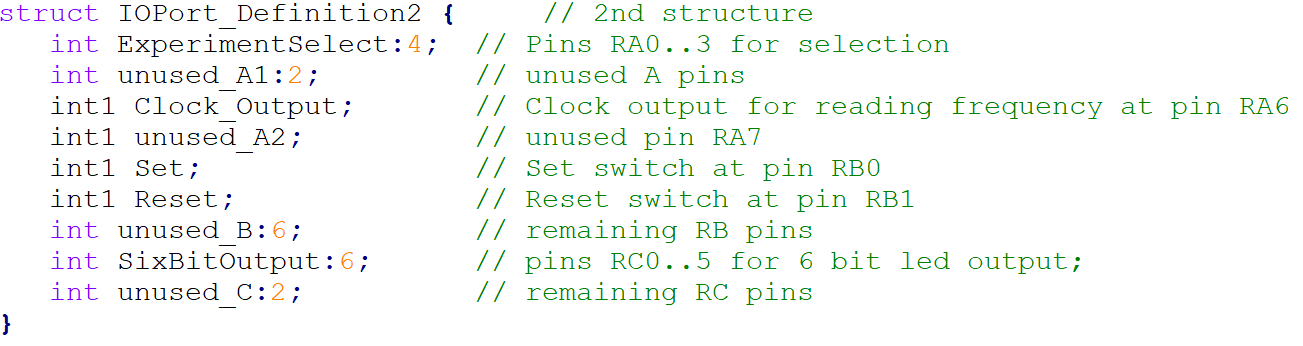
4

4

4

4

Second Structure:



6

2

bits

6

1

1

2

1

1

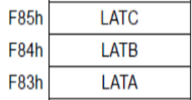
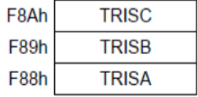
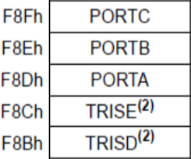
4



Example of second Structure:



Example of First Structure:





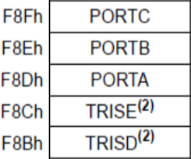


1

2

END

3



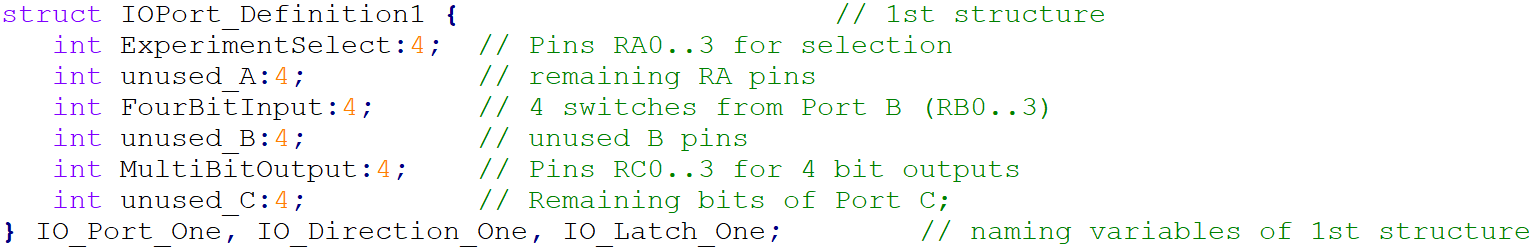
1

2

33

END



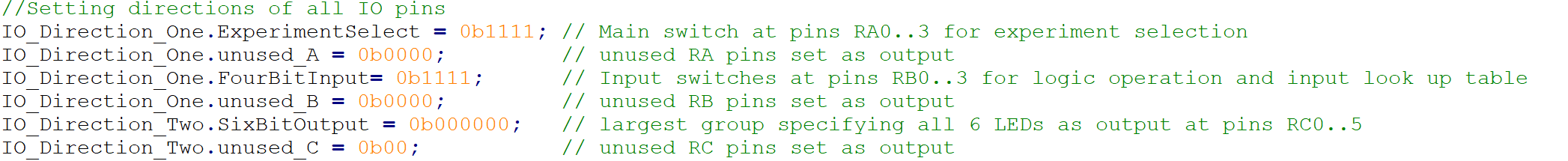


1

2

END

3



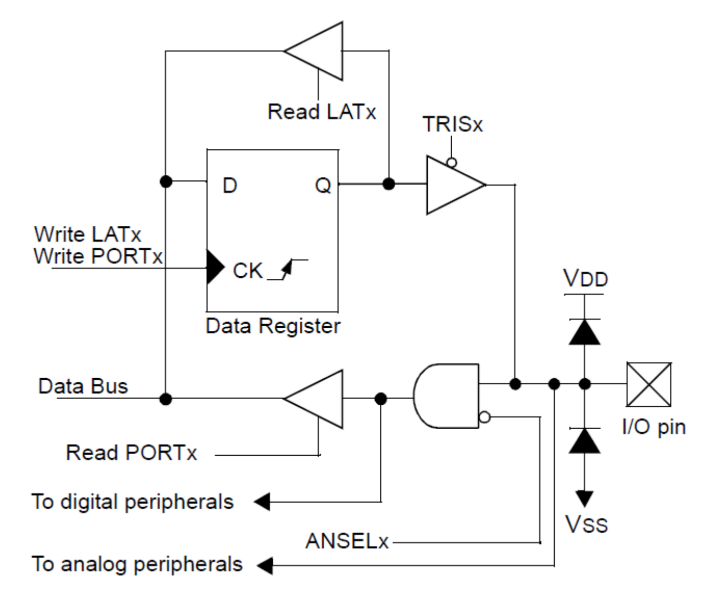
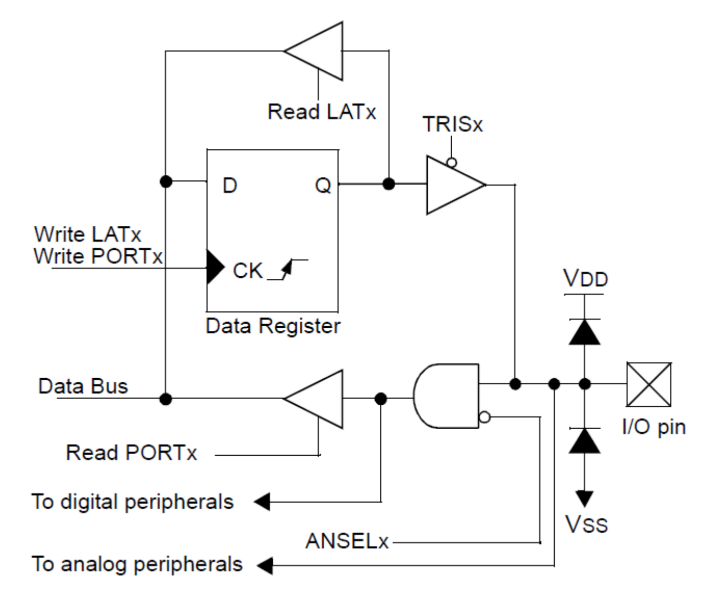
Pins RA0, RA1, RA2, RA3

1

2

END

3

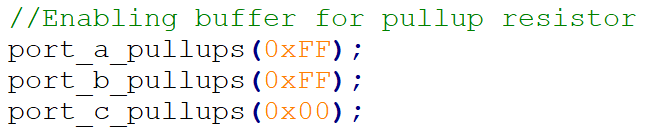
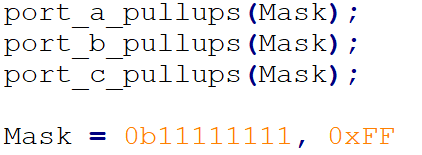


**OUTPUT:**

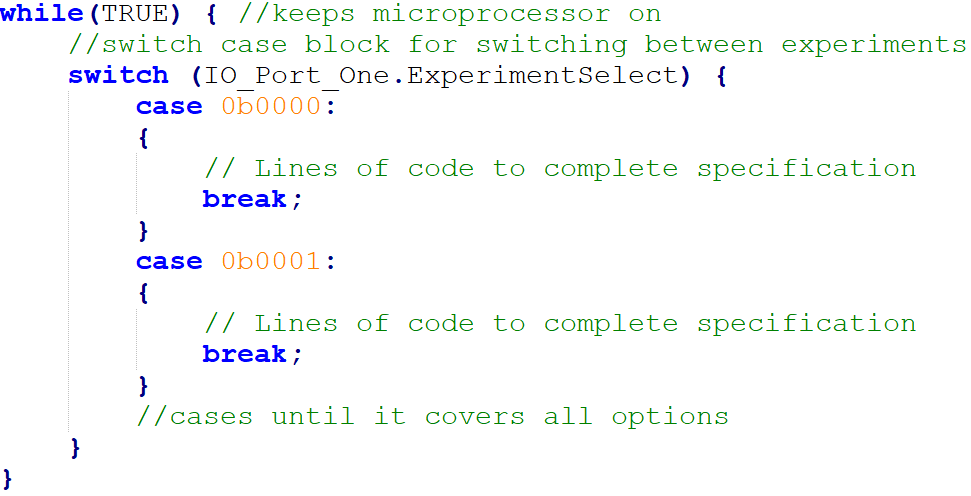
**INPUT:**

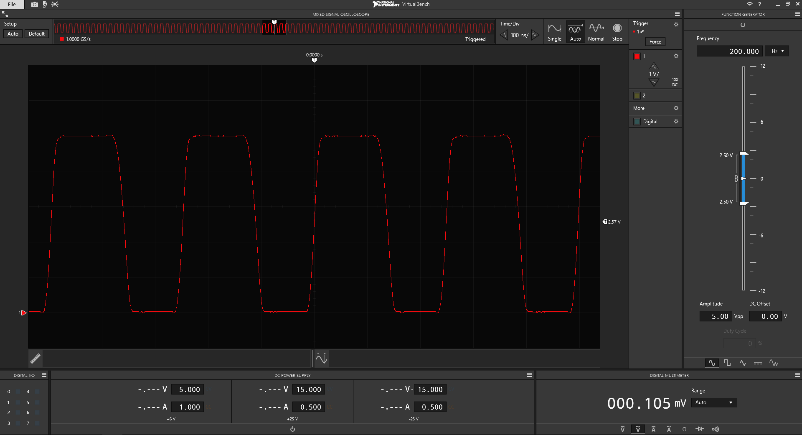
**= 0b1**

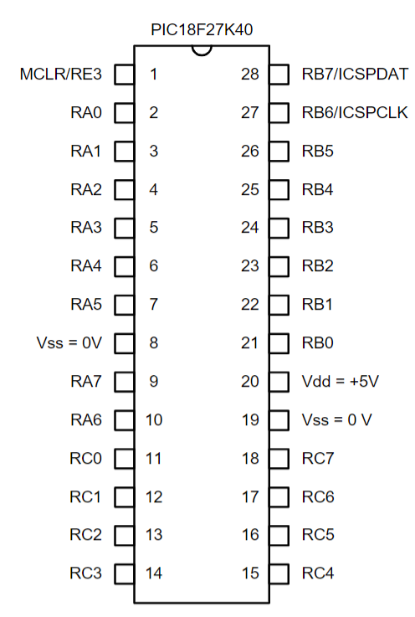
**= 0b0**

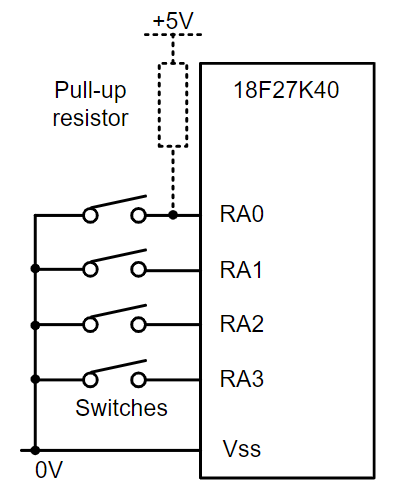
g

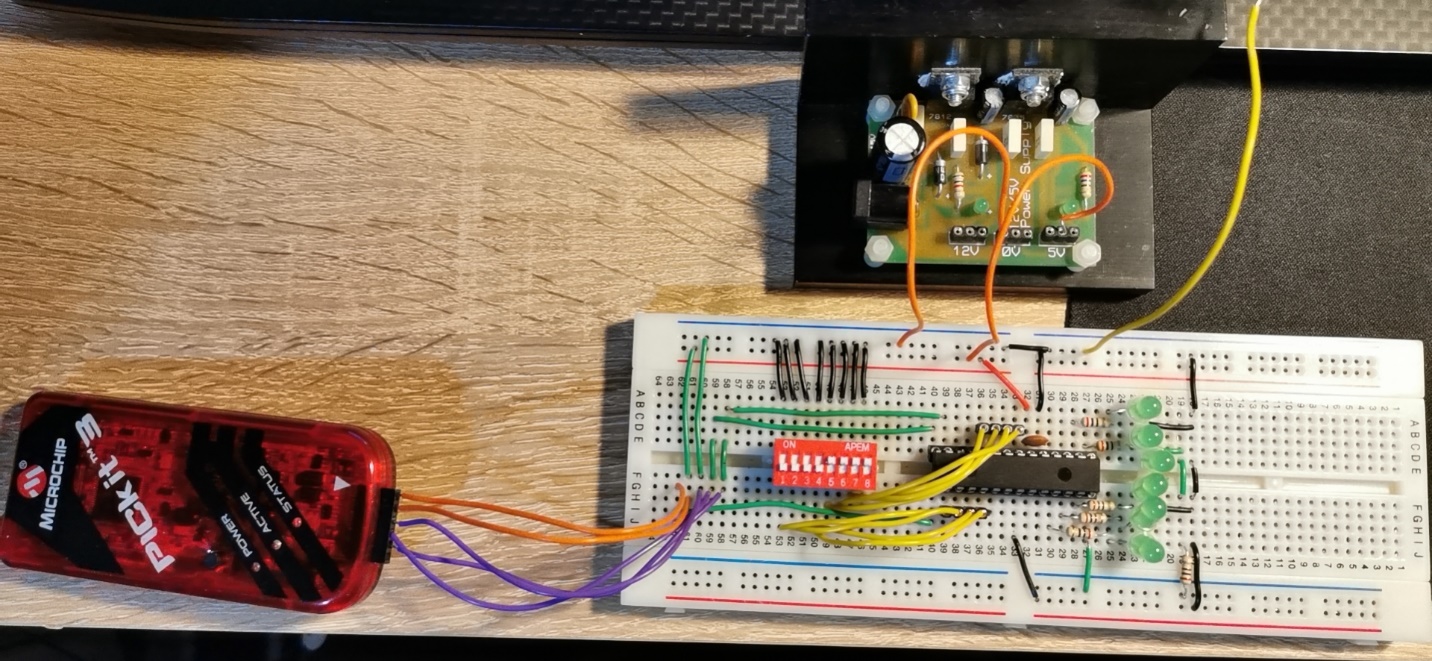
**=>**

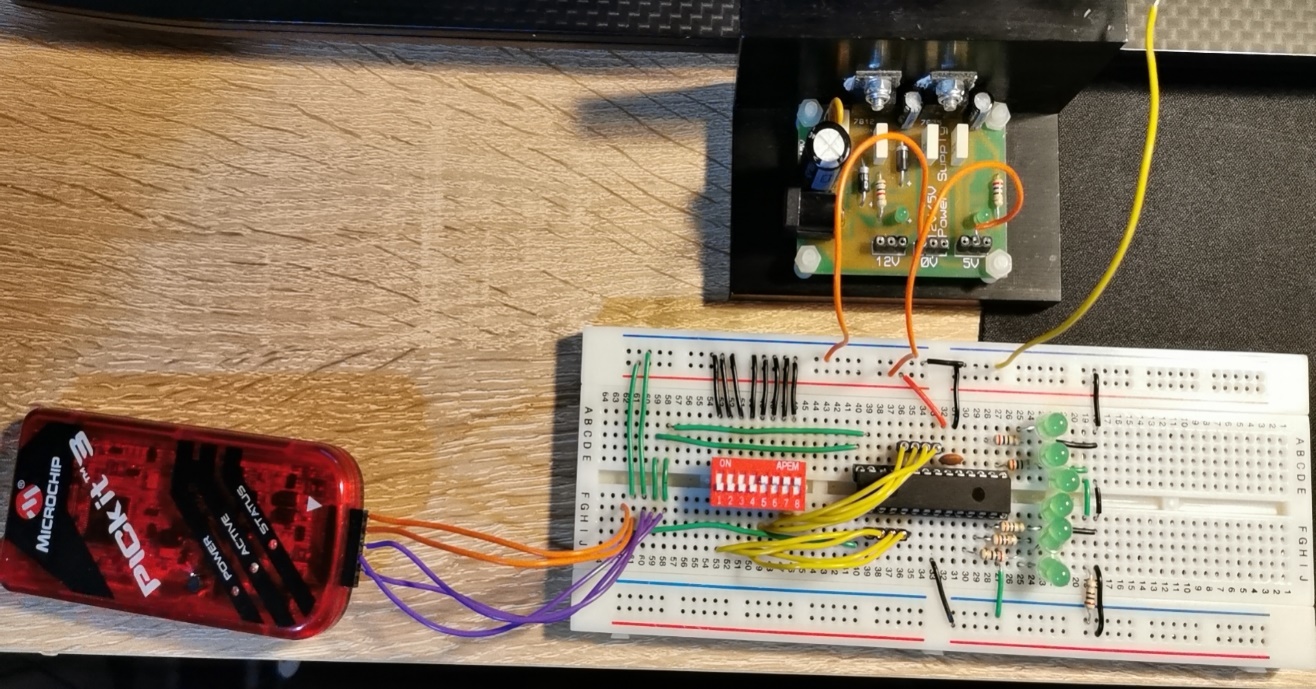




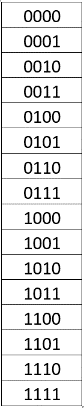


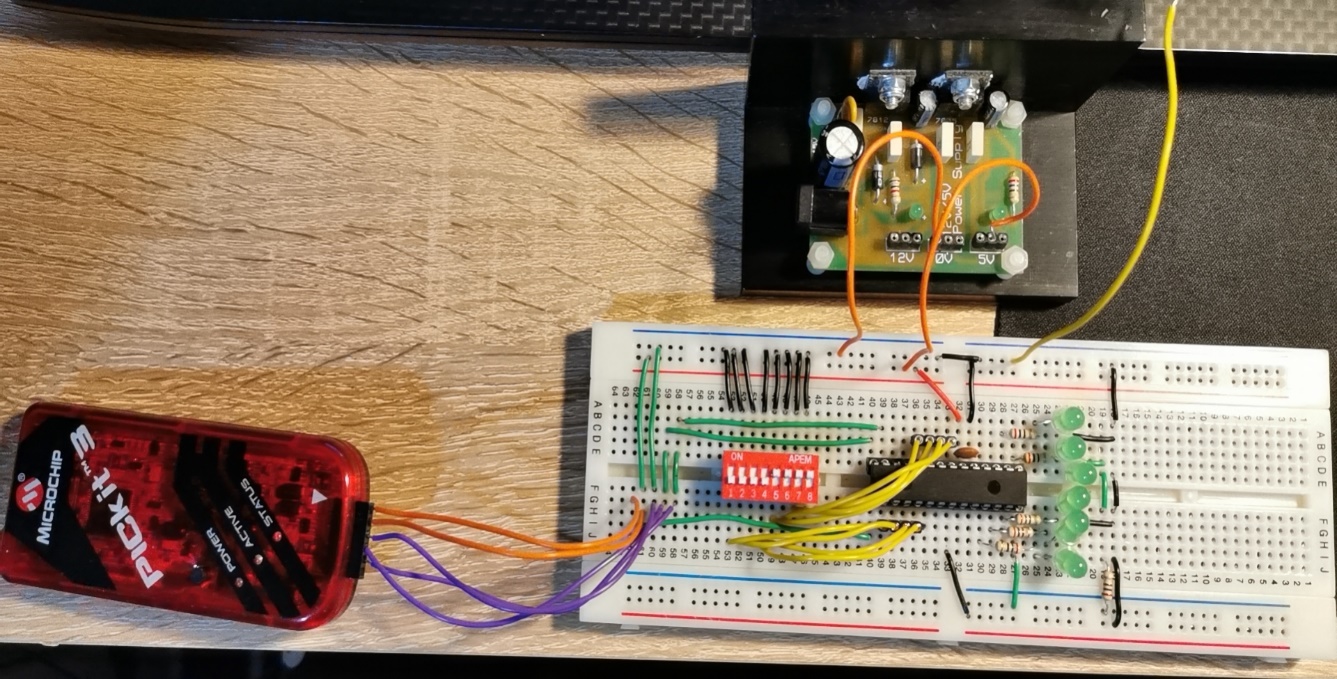
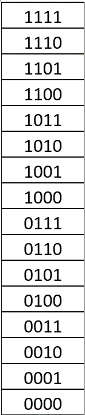




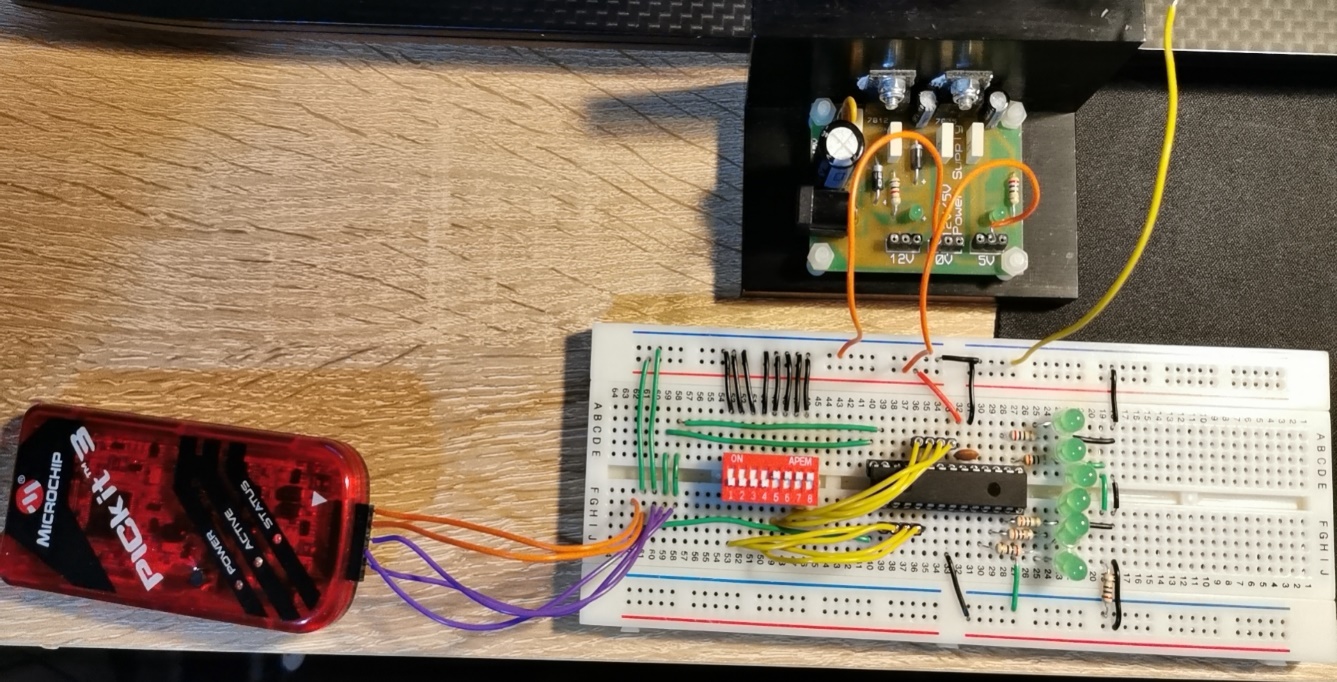


0000 | Clock microprocessor is running at 16MHz, pin RA6 produces 4 MHz.

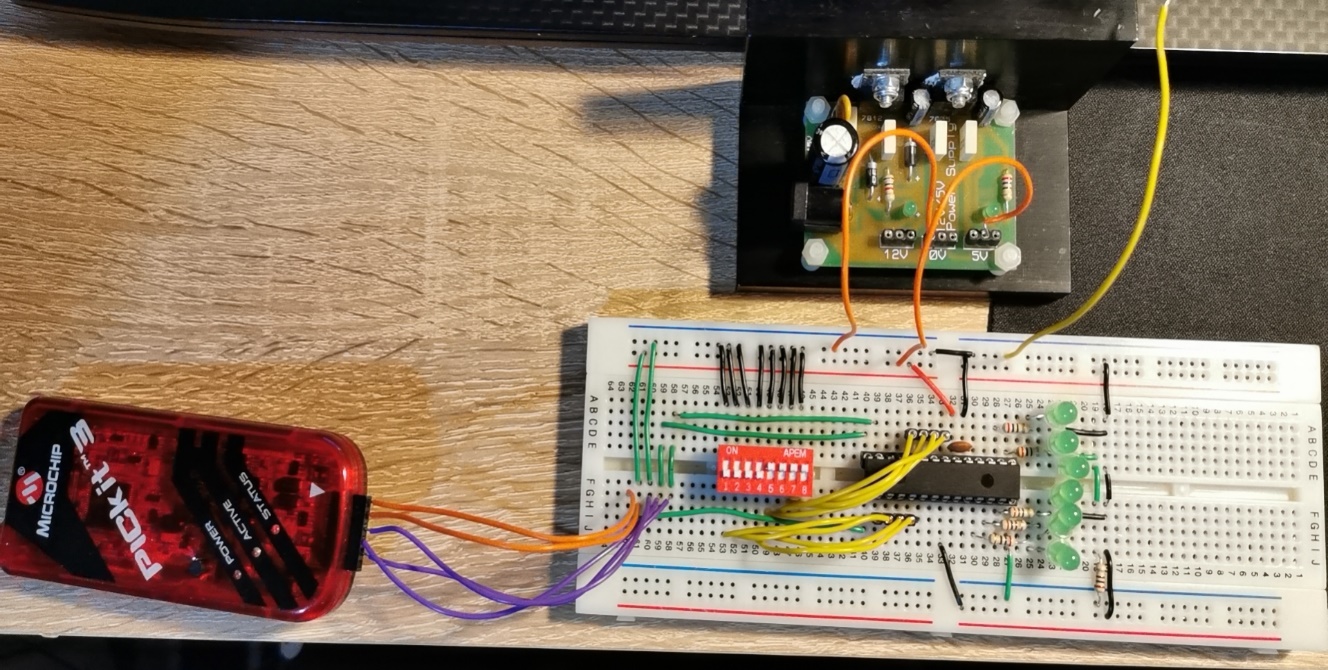




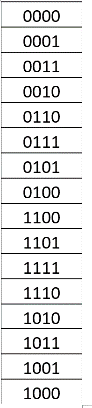
0100 | 4-bit pure-binary down-counter

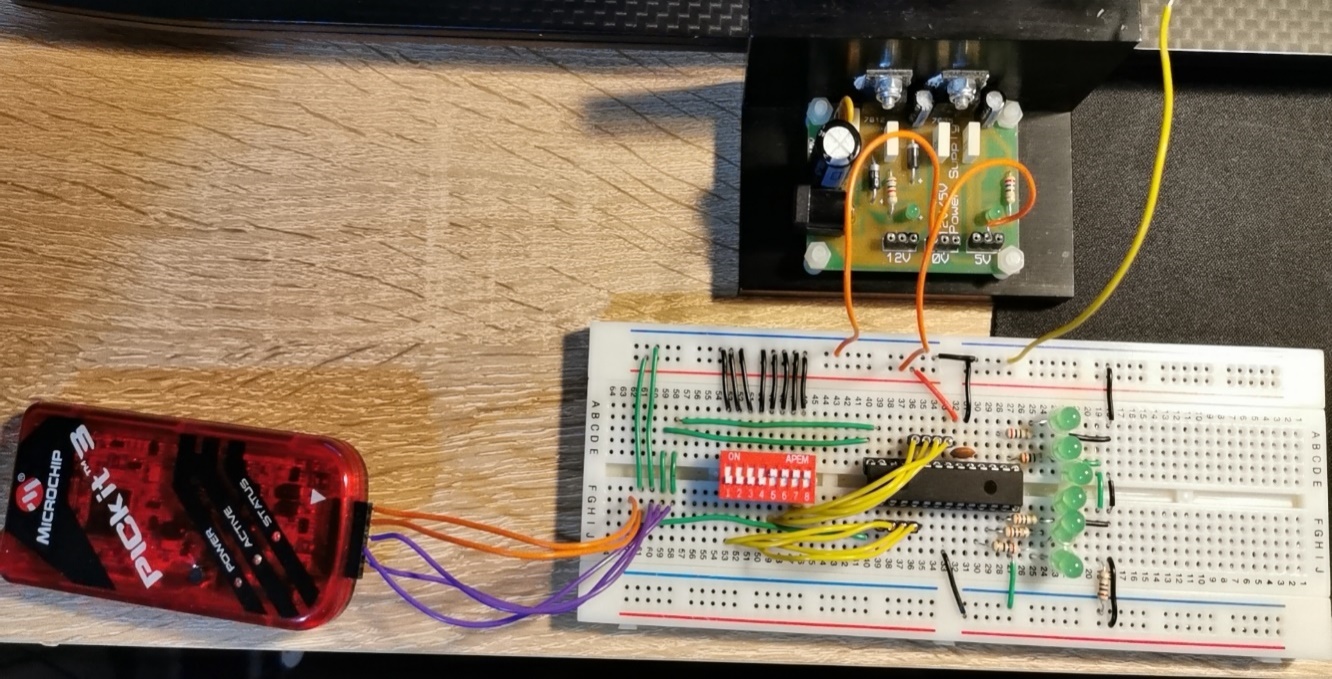


0011 | 4-bit pure-binary up-counter

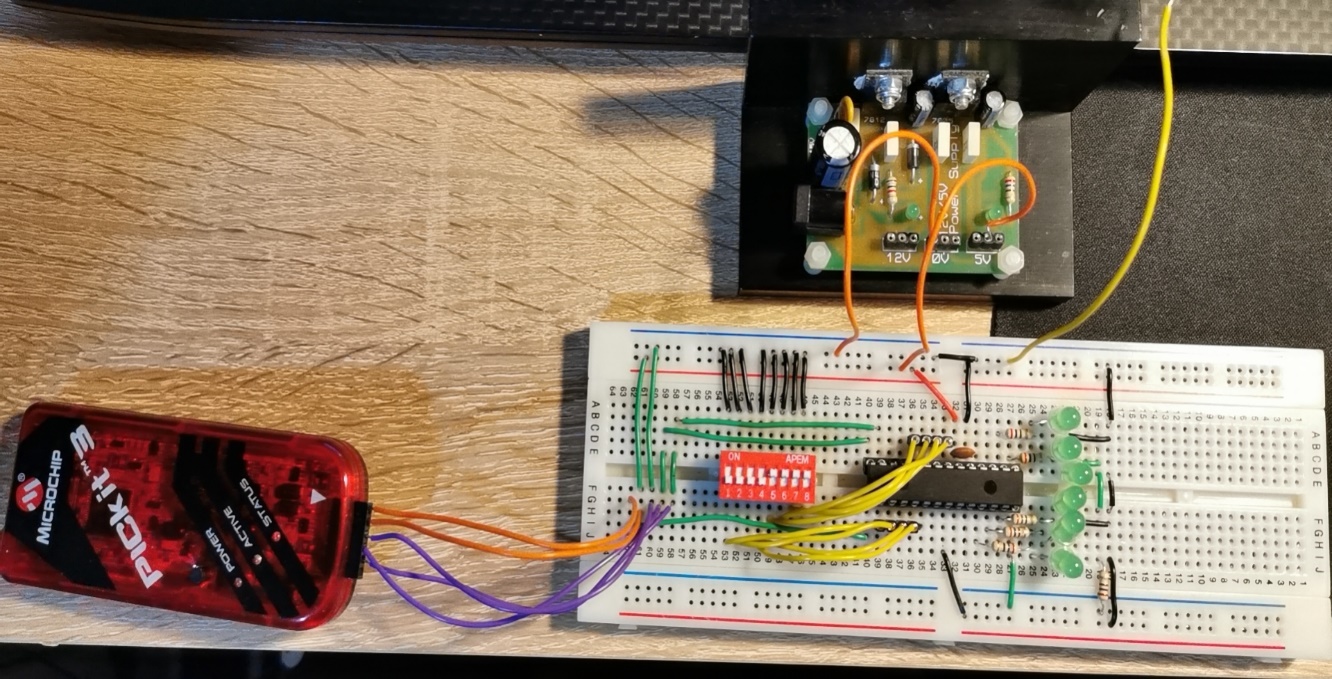
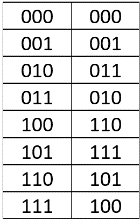


0001 | T-type flip flop in toggle mode. Pin RC0 produces 1Hz.

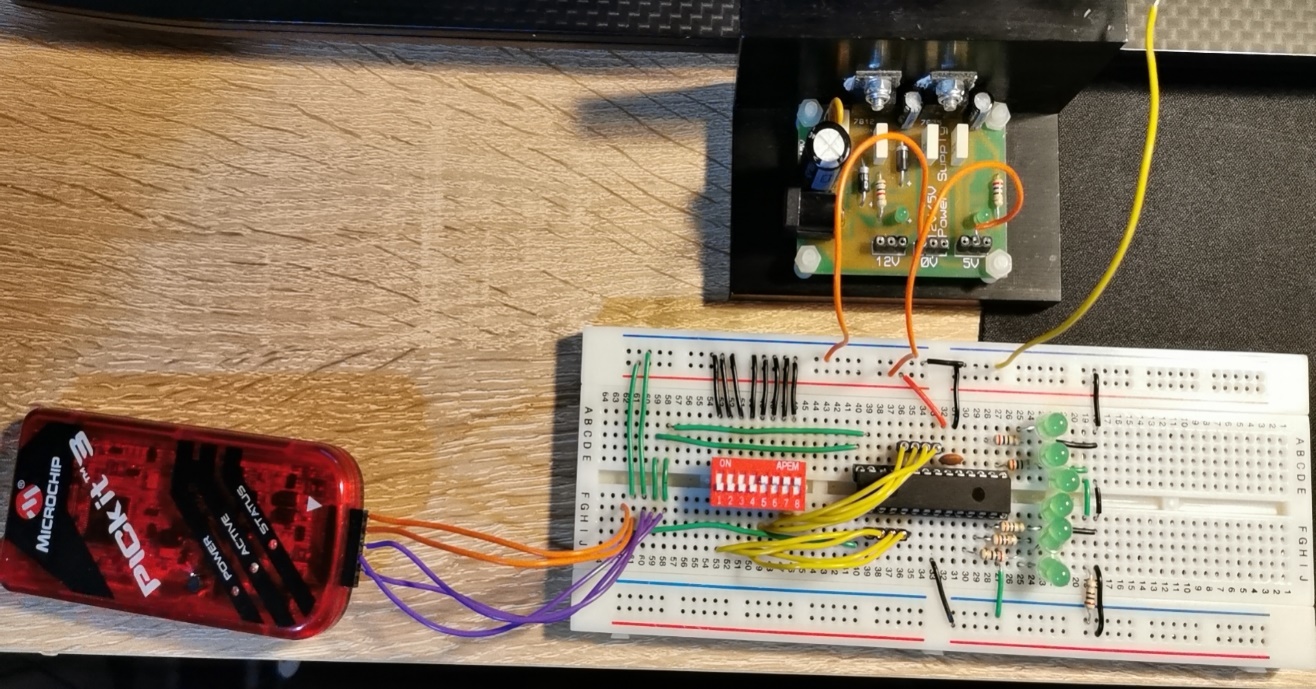




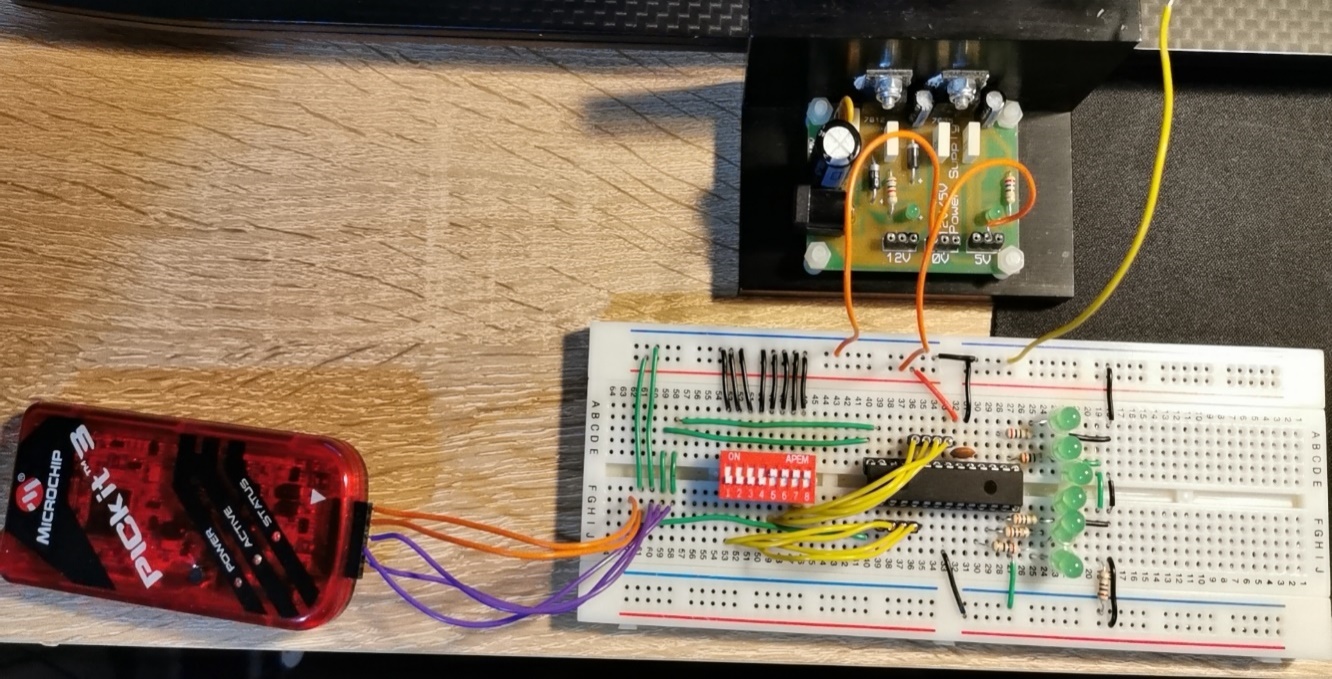
0111| bitwise AND operation



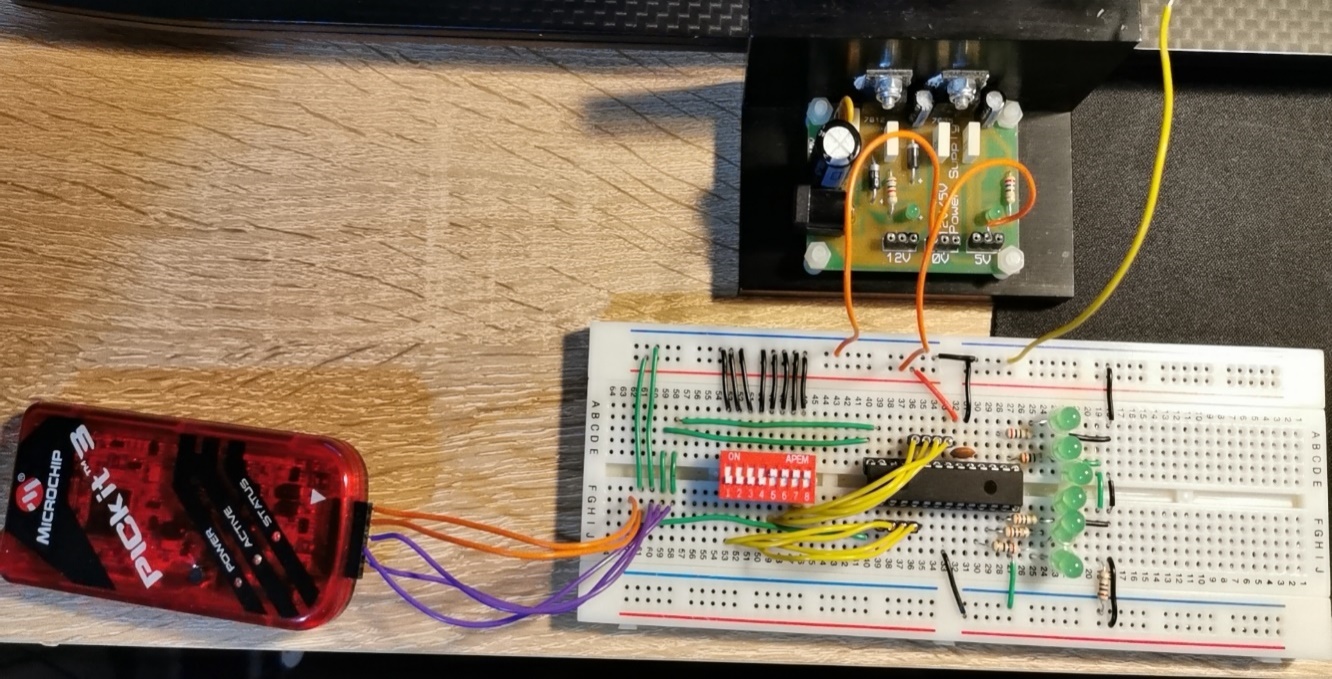
0110 | 3-bit pure-binary up-counter with 3-bit Gray-code up-counter



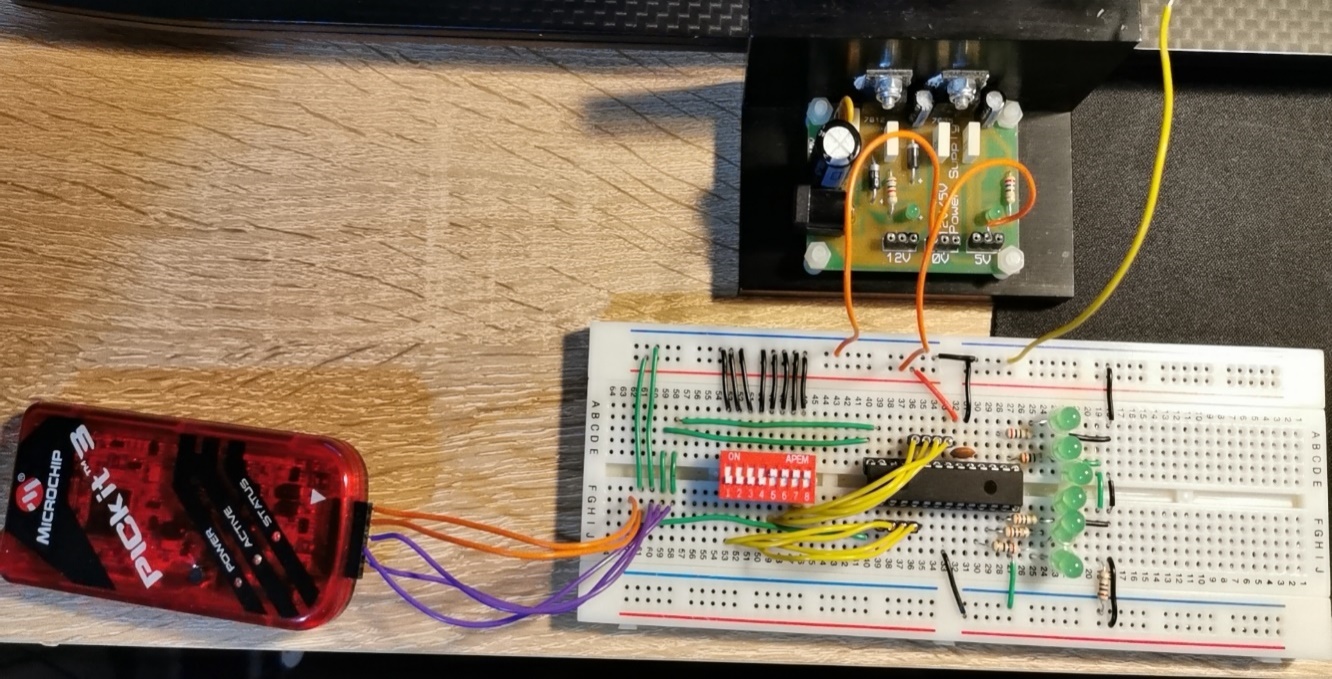
0101 | 4-bit Gray-code up-counter using look-up table



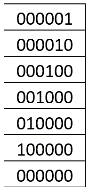
1000 | bitwise OR operation

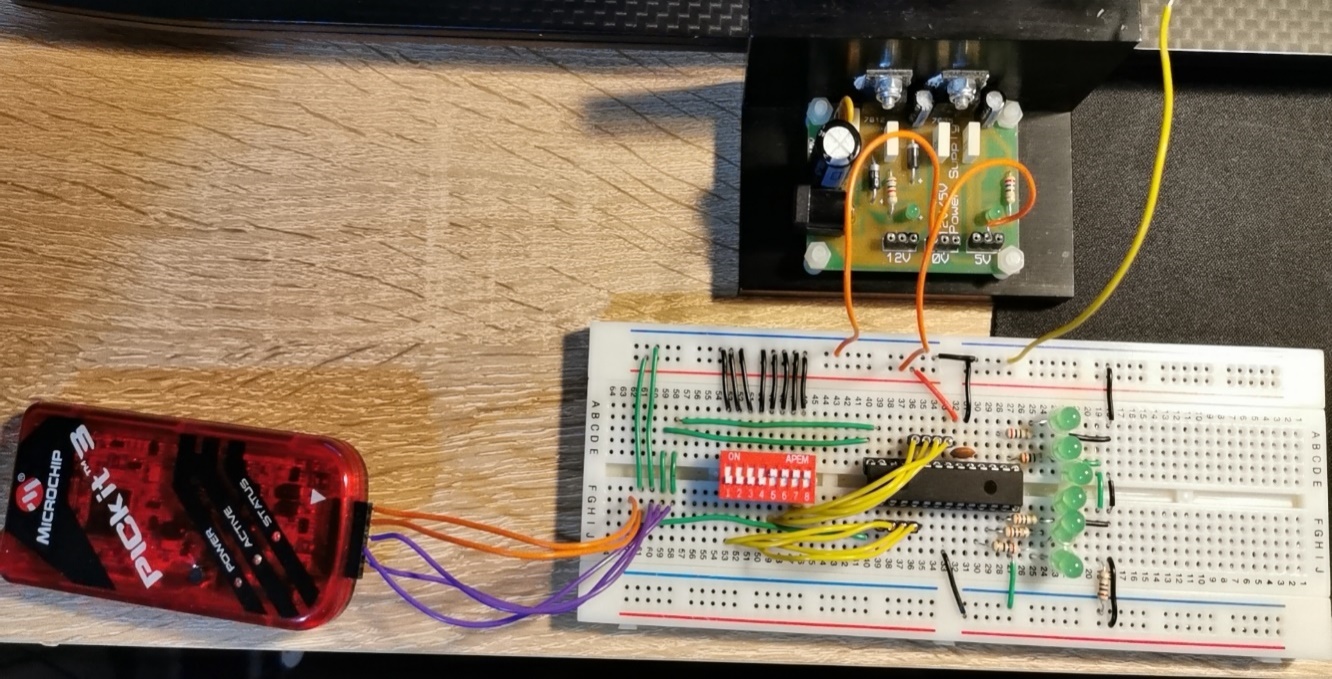


1001 | bitwise NOT operation

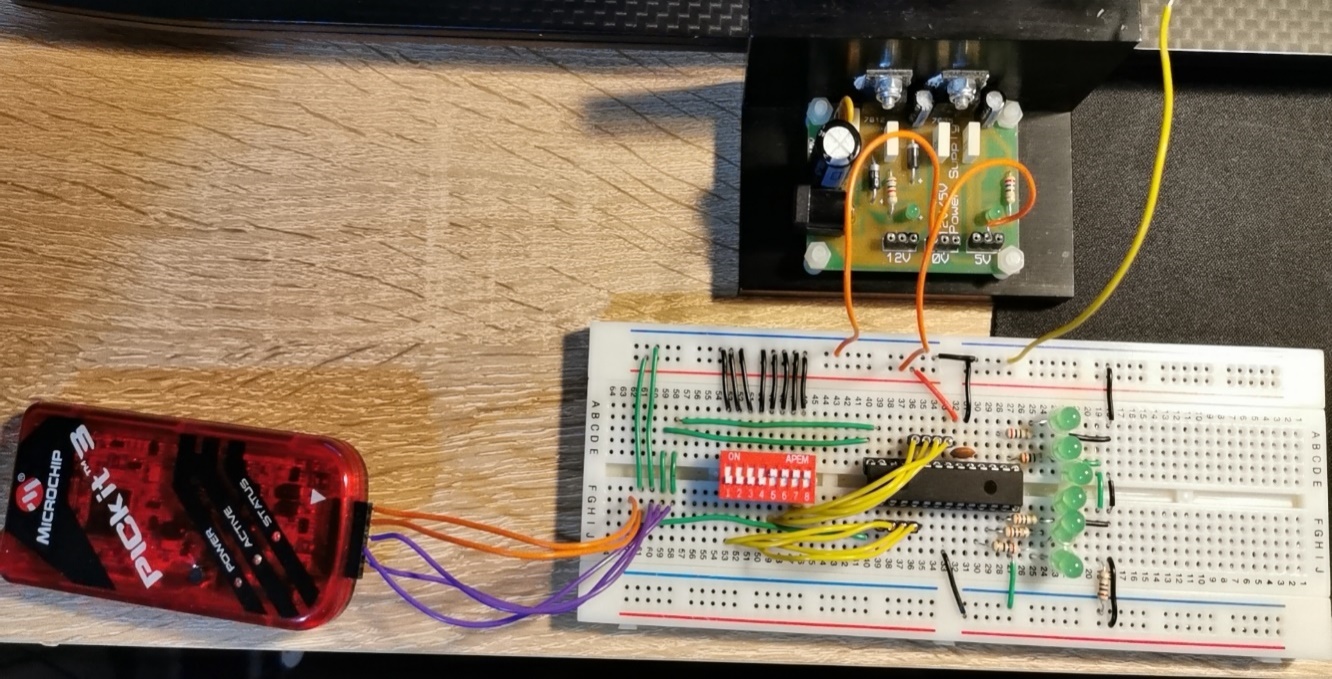


1001 | bitwise Exclusive-OR operation

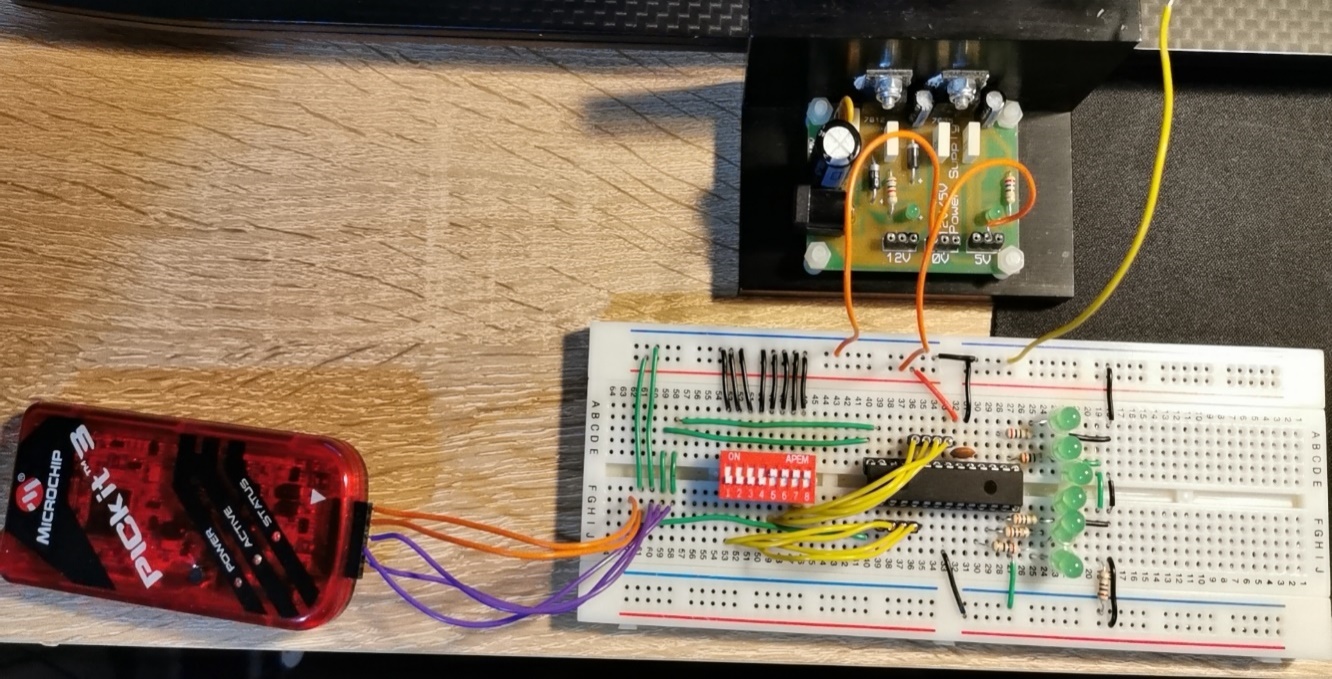




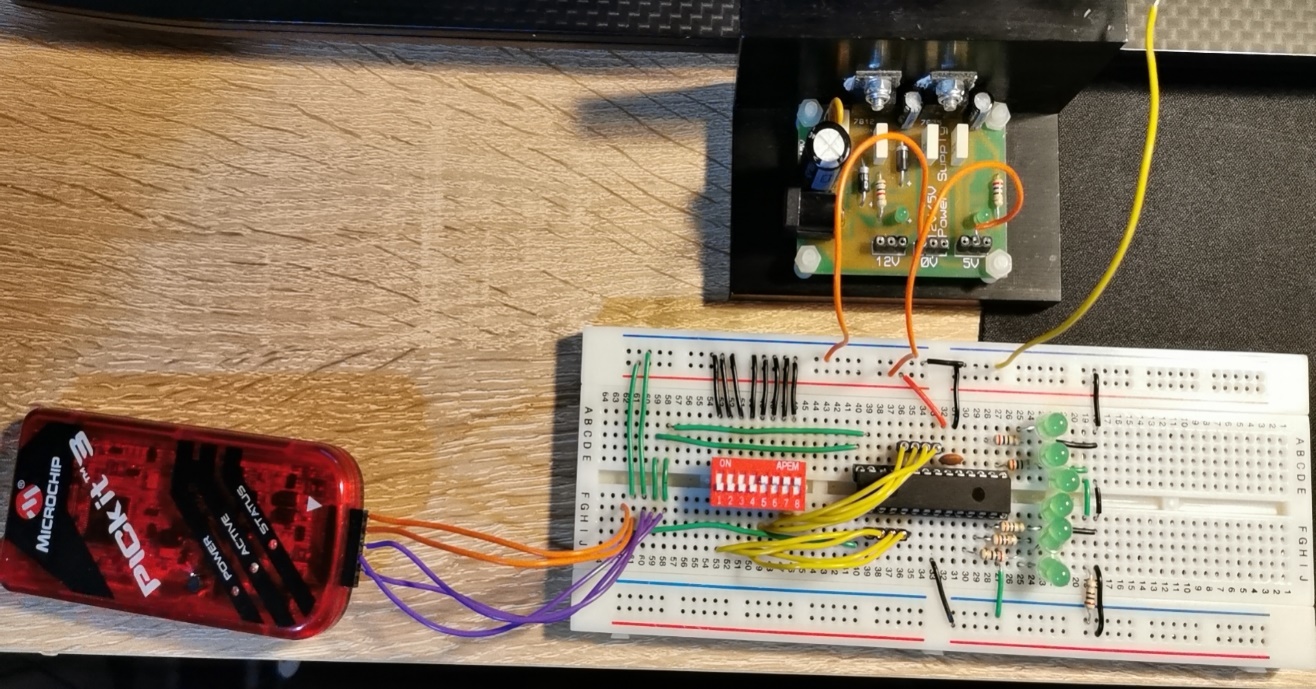
1101 | Lab 1 FSM using Look up Table



1100 | Input Look-up Table



1011 | set-reset flip-flop synthesis



1110 and 1111 | Appropriate action, turn every light off