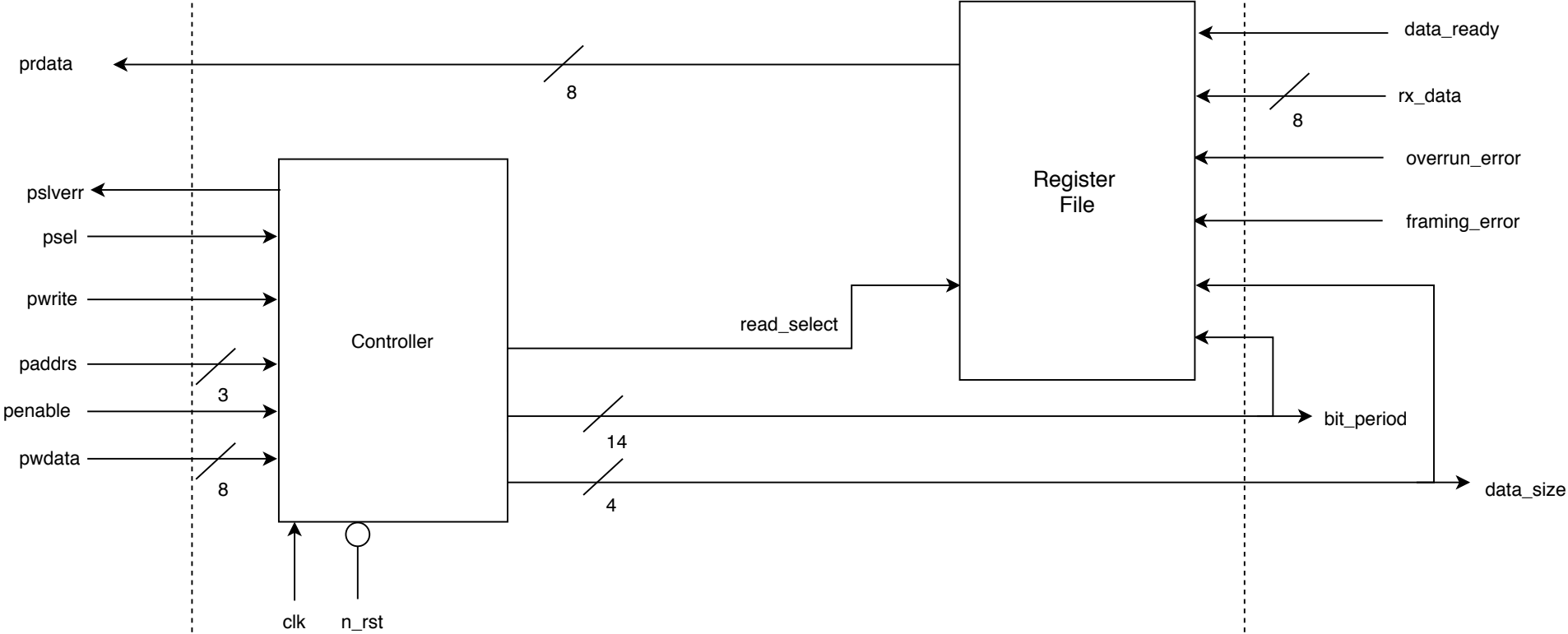


# TOP LEVEL DIAGRAM

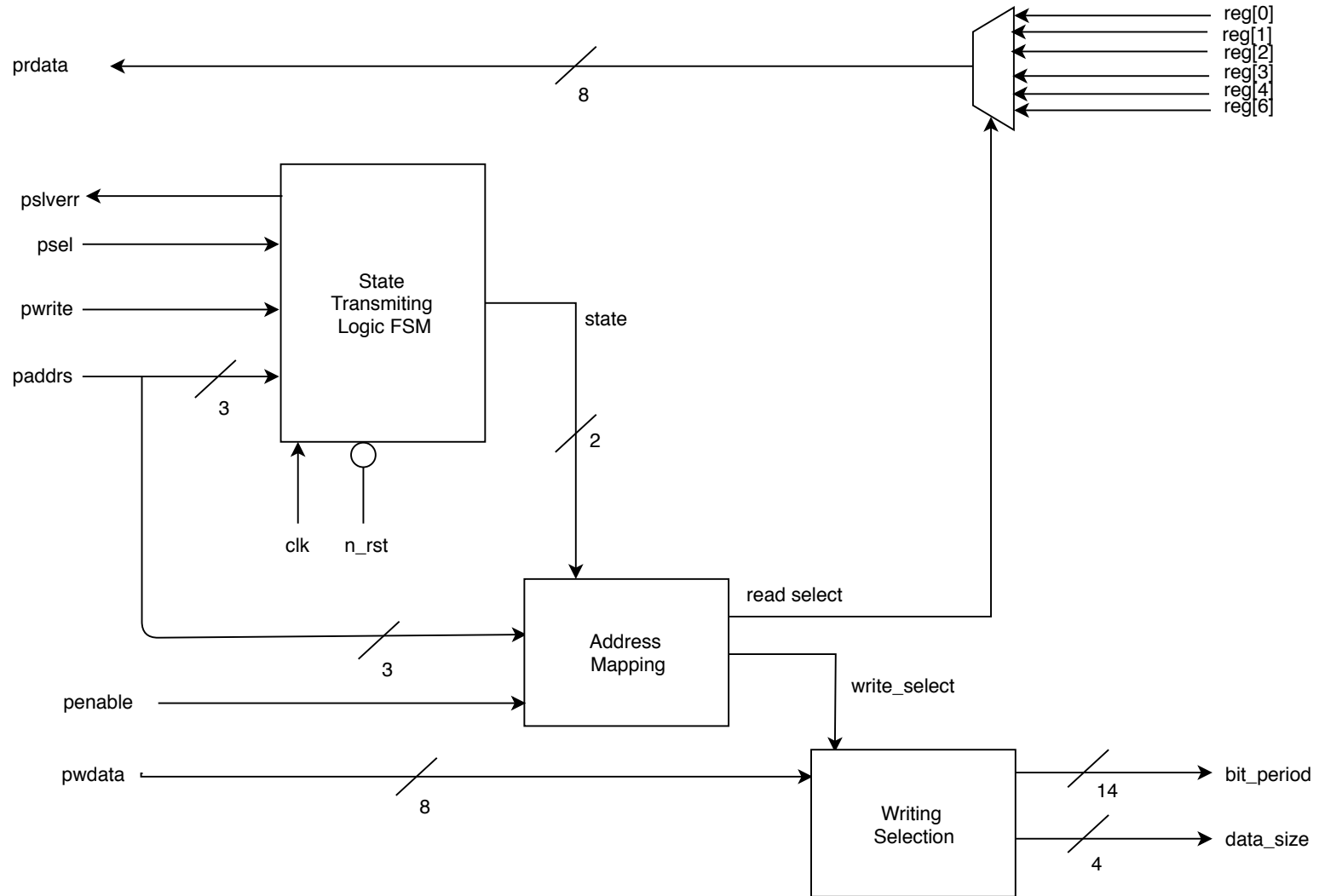
From Master

From UART

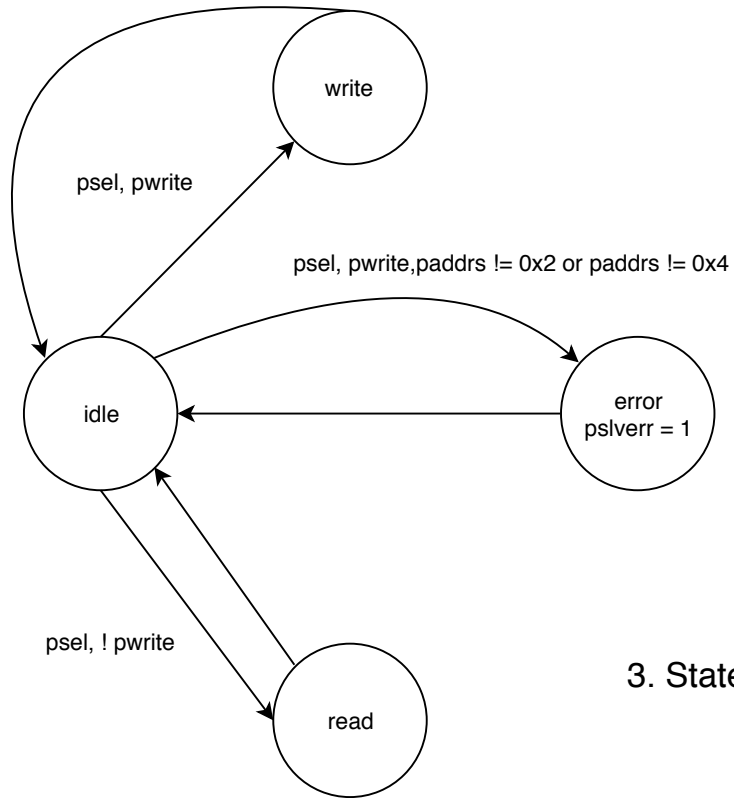


## SUPPORTING DIAGRAMS

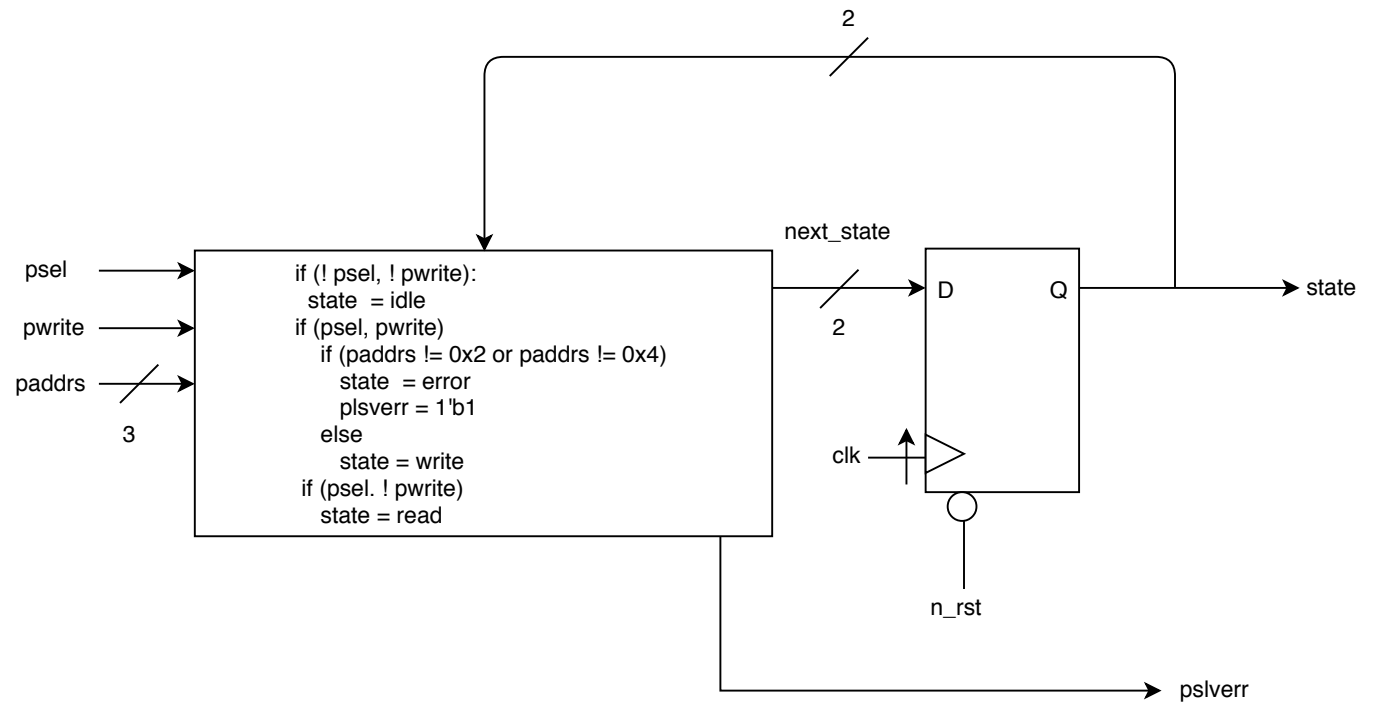
### 1. Controller



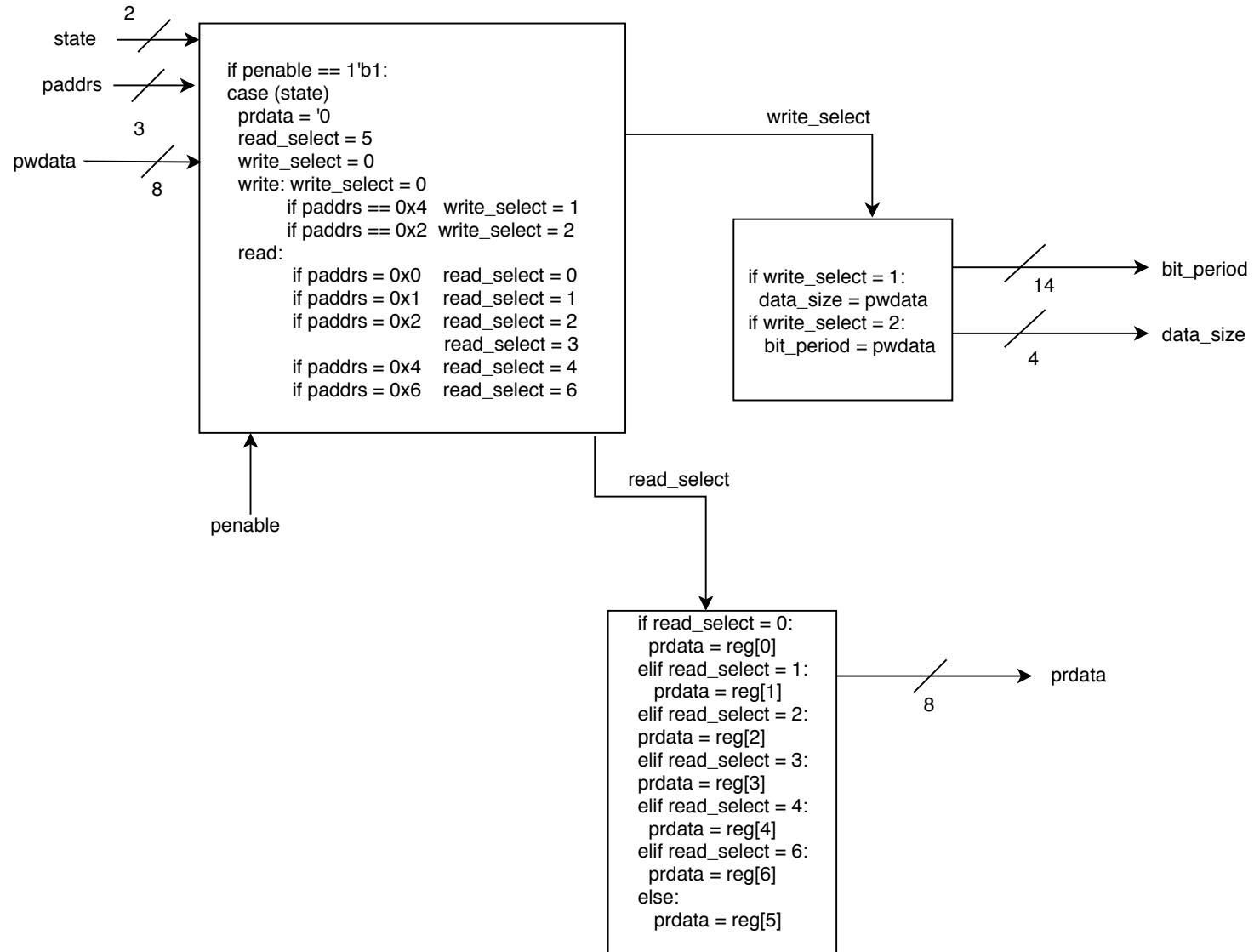
## 2. State Transition Diagram for Controller



## 3. State Transmitting Logic FSM



#### 4. Address Mapping Logic (combinational)



## 5. Register File

