Lab 6 Rubric

1 General Rules

- Partial Credit is done as penalties from full points except where explicitly stated
- Points for any part/item cannot be negative (clamped to 0)
- Sections/Items not attempted receive 0 points

2 Preparation Phase (Full Points: 10)

2.1 Completed Waveform Diagram for the Timer (Perfect Score: 2 points)

2.1.1 Solution

There are a few ways to doing the timing waveforms for the timer, depending on if the timer generates a shift strobe at a cycle count of 3 or 4. Only cycle counts of 3 or 4 are acceptable as any other timing value will generate double sampling of the one of the bits. Additionally it is expected that they will be directly reusing their flex_counters for their timers in a similar way as they were used for the UART lab. Since cycle counts must be cleared based d_edge, their timers will fundamentally need separate cycle and bit counters, but since these waveforms focus on the cycle timing, only the cycle counter is shown in the waveforms (timer).

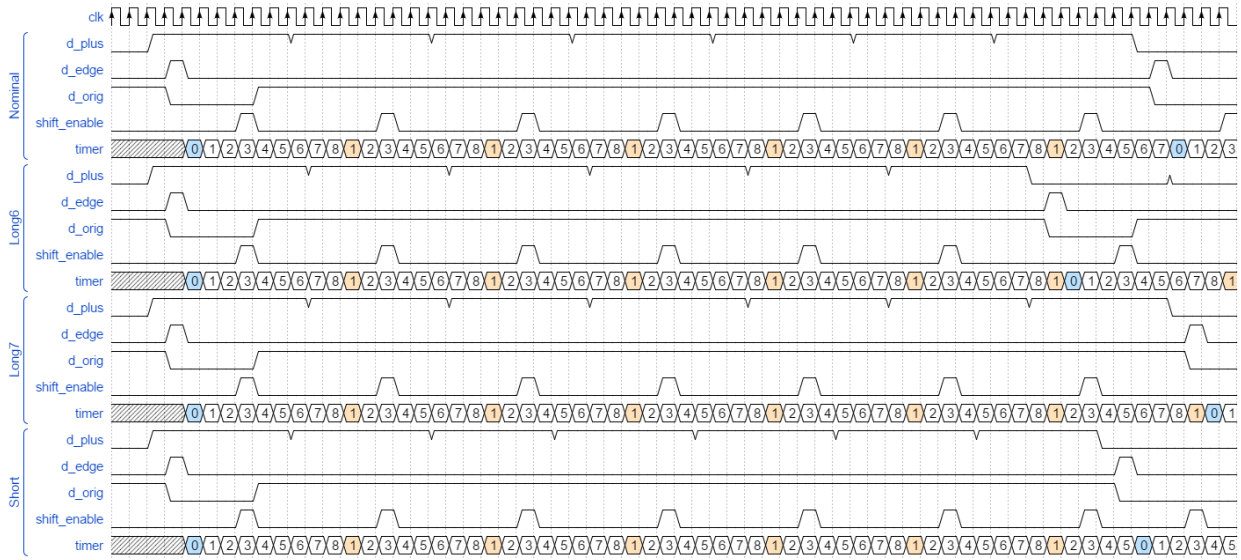

Figure 1: Completed Timer Waveform Diagram based on strobes at a count of 3 cycles

2.1.2 Partial Credit/Penalties

- -0.5 pts per incorrect signal waveform

2.2 Completed State Diagram for the RCU (Perfect Score: 2 points)

2.2.1 Solution

There are many ways to diagram this, but they should all be functionally equivalent to the following diagram. An alternate form would be to remove the CHK_SYNC state and merged the rcv_data condition into the byte_recieved check in the RCV_SYNC state. Also, since the students were told their design would always get at least one good byte after a valid sync byte, they don't need to distinguish between good and bad eop signals until after the first byte of data following a valid sync byte.

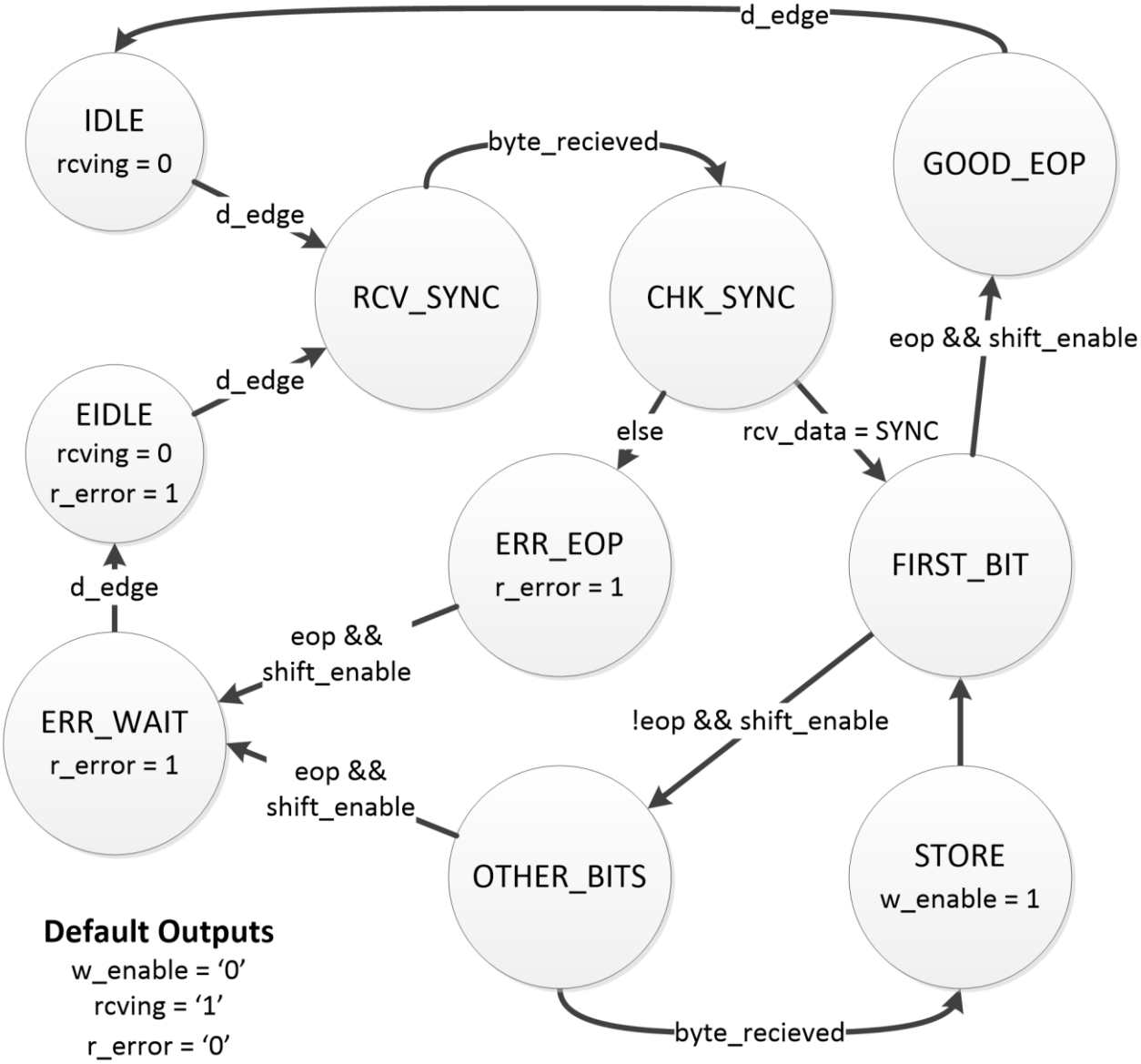

Figure 2: State Transition Diagram for the RCU block w/ state based timer enable delay

2.2.2 Partial Credit/Penalties

- -0.5 per incorrect state's output set
- -0.1 per incorrect state

2.3 Completed RTL Diagram for the RCU (Perfect Score: 1 point)

2.3.1 Solution

There are many ways to diagram this, but they should all be functionally equivalent to the following diagram. Also, state size should be based on their RCU state diagram.

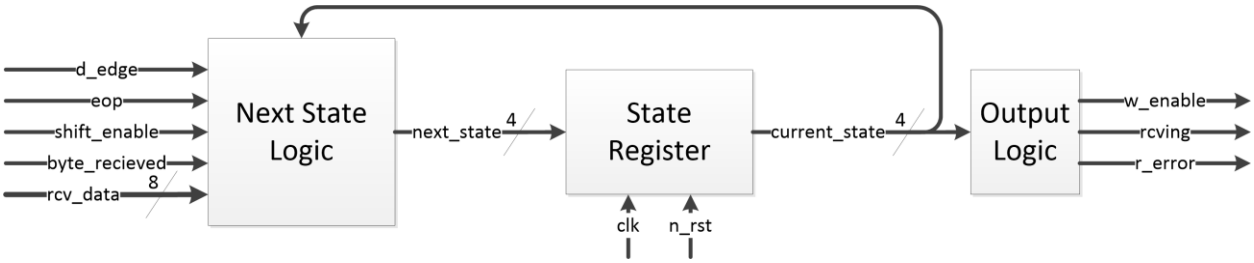

Figure 3: RTL Diagram for the RCU block

2.3.2 Partial Credit/Penalties

- -0.25 points per missing/incorrect input or output signal
- -0.25 points per missing/incorrect signal size

2.4 Completed RTL Diagram for the Decode (Perfect Score: 1 points)

2.4.1 Solution

There are a few ways to diagram this, but they should all be functionally equivalent to one of the two following diagrams. The next_hist value logic could also be collapsed into a single 3-way mux or just general combinational logic block.

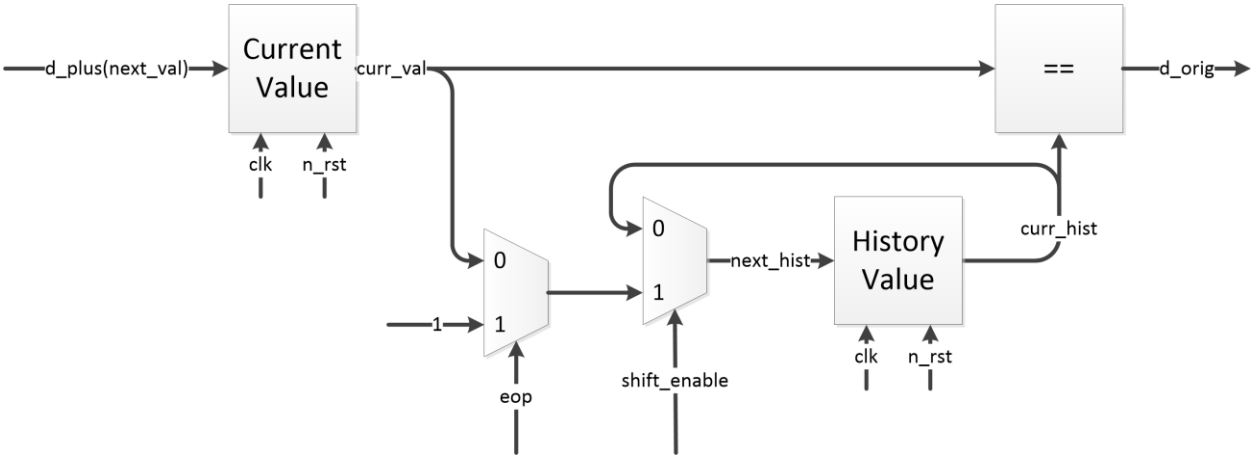

Figure 4: Block Diagram for the Timer Block

2.4.2 Partial Credit/Penalties

- -0.25 points per missing/incorrect input or output signal
- -0.5 points per logic error
- -0.25 points per missing/incorrect signal size

2.5 Completed Block Diagram for the Timer (Perfect Score: 2 points)

2.5.1 Solution

There are a few ways to diagram this, but they should all be functionally equivalent to one of the two following diagrams. However, because of needing to clear the cycle counter based on d_edge, this timer fundamentally requires separate cycle and bit counters.

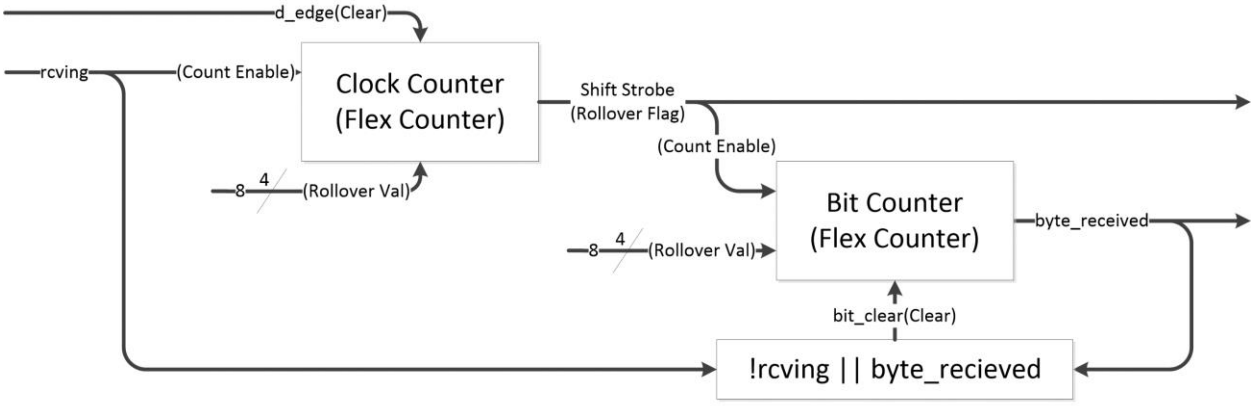

Figure 5: Block Diagram for the Timer Block

2.5.2 Partial Credit/Penalties

- -0.5 points per missing/incorrect input or output signal
- -1 points per logical error
- -0.25 points per missing/incorrect signal size

2.6 Completed Schematic Diagram for the Edge Detector (Perfect Score: 1 points)

2.6.1 Solution

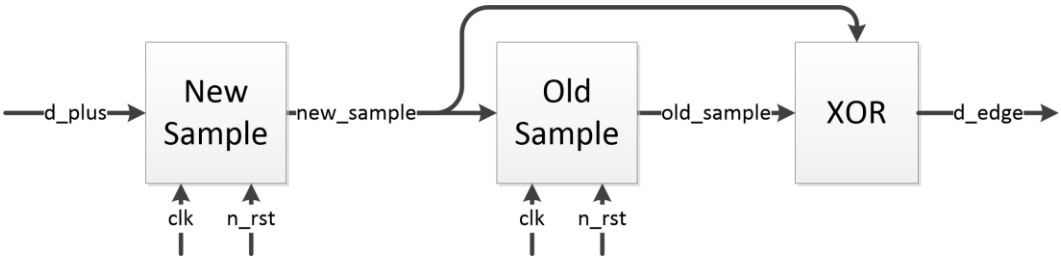

Figure 6: Edge Detector Schematic

2.6.2 Partial Credit/Penalties

- All or nothing

2.7 Completed Schematic Diagram for the EOP Detector (Perfect Score: 1 points)

2.7.1 Solution

Figure 7: EOP Detector Schematic

2.7.2 Partial Credit/Penalties

- All or nothing