Ain Shams University
Faculty of Engineering
Discipline Programs

EDA Verification Plan Report

Computer Engineering and Software Systems (CESS)

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Table of Contents

1.0 Verification Plan 3

2.0 Verification Plan Simulation 5

2.1 Case 1 5

2.2 Case 2 6

2.3 Case 3 6

2.4 Case 4 7

2.5 Case 5 7

1.0 Verification Plan

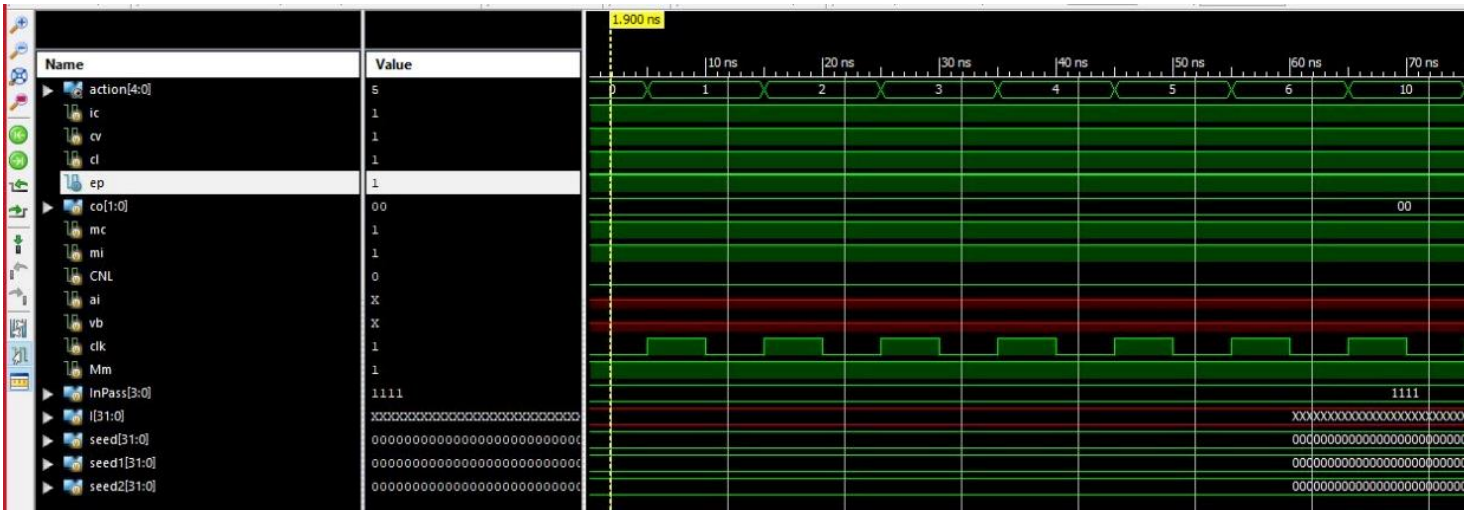
Case Number	State Inputs	Expected Output	Simulation Output	Pass/Fail
CASE 1	IC=1 CNL=0 CV=1 CL=1 InPass=1111 EP=1 MM=1 CO=00 MI=1 MC=1	Action=1 Action=2 Action=3 Action=4 Action=5 Action=6 Action=10	Action=1 Action=2 Action=3 Action=4 Action=5 Action=6 Action=10	Pass
CASE 2	IC=1 CV=1 CL=1 CNL=0 InPass=1111 EP=1	Action=1 Action=2 Action=3 Action=4 Action=5 Action=7	Action=1 Action=2 Action=3 Action=4 Action=5 Action=7	Pass

	CO=01 AI=1 VB=1 MM=1	Action=12 Action=13	Action=12 Action=13	
CASE 3	IC=1 CV=1 CL=1 CNL=0 InPass=1111 EP=1 CO=10 MM=1	Action=1 Action=2 Action=3 Action=4 Action=5 Action=8	Action=1 Action=2 Action=3 Action=4 Action=5 Action=8	Pass
CASE 4	IC=1 CV=1 CL=1 CNL=0 InPass=1111 EP=1	Action=1 Action=2 Action=3 Action=4 Action=5 Action=9	Action=1 Action=2 Action=3 Action=4 Action=5 Action=9	Pass

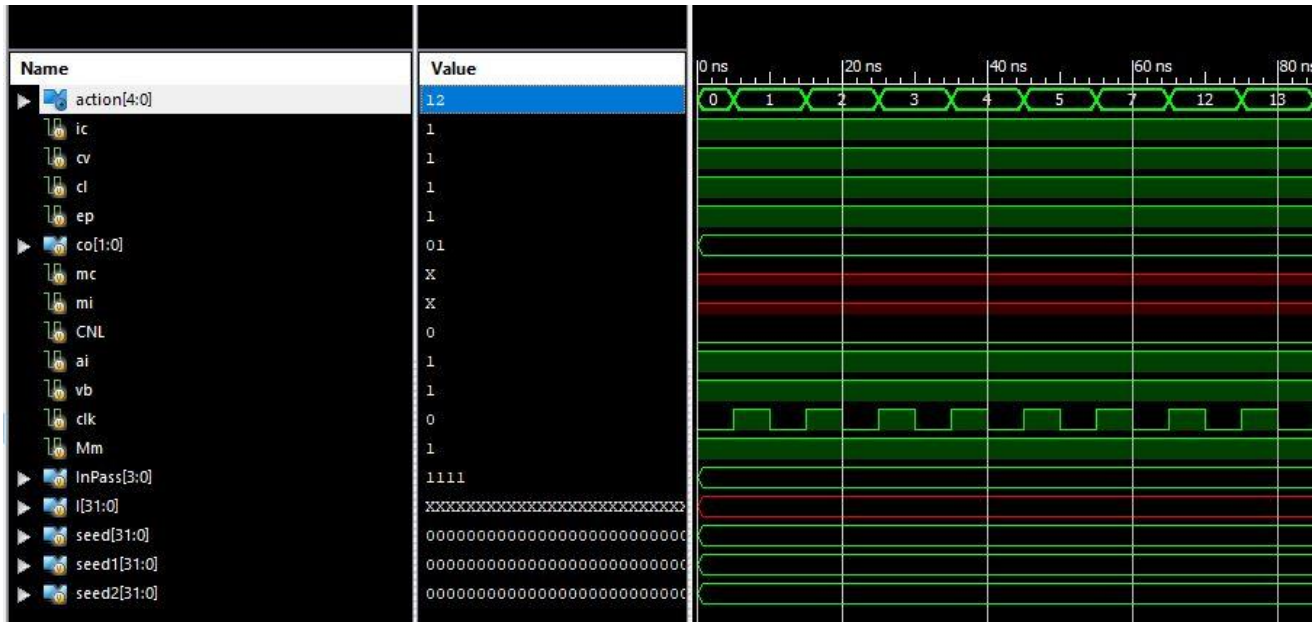
	CO=11 MM=1			
CASE 5	IC=1 CV=1 CL=1 CNL=0 EP=1 InPass=1100	Action=1 Action=2 Action=3 Action=4 Action=3	Action=1 Action=2 Action=3 Action=4 Action=3	Pass

2.0 Verification Plan Simulation

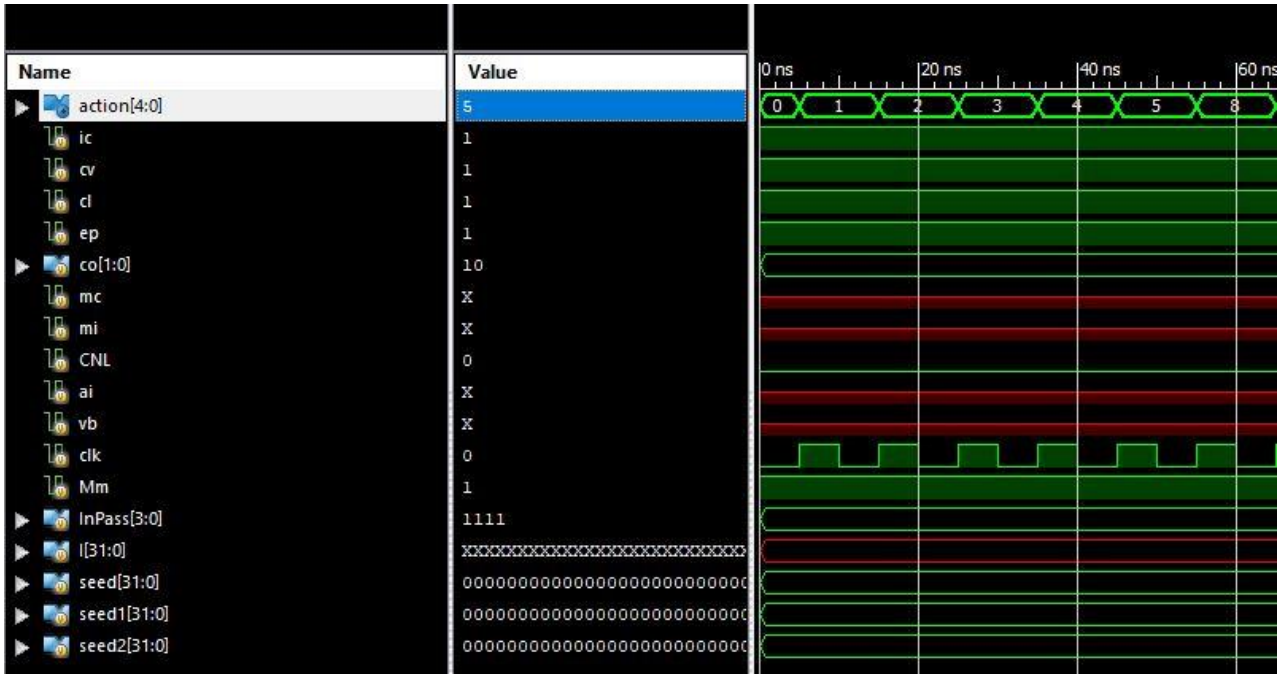
2.1 Case 1



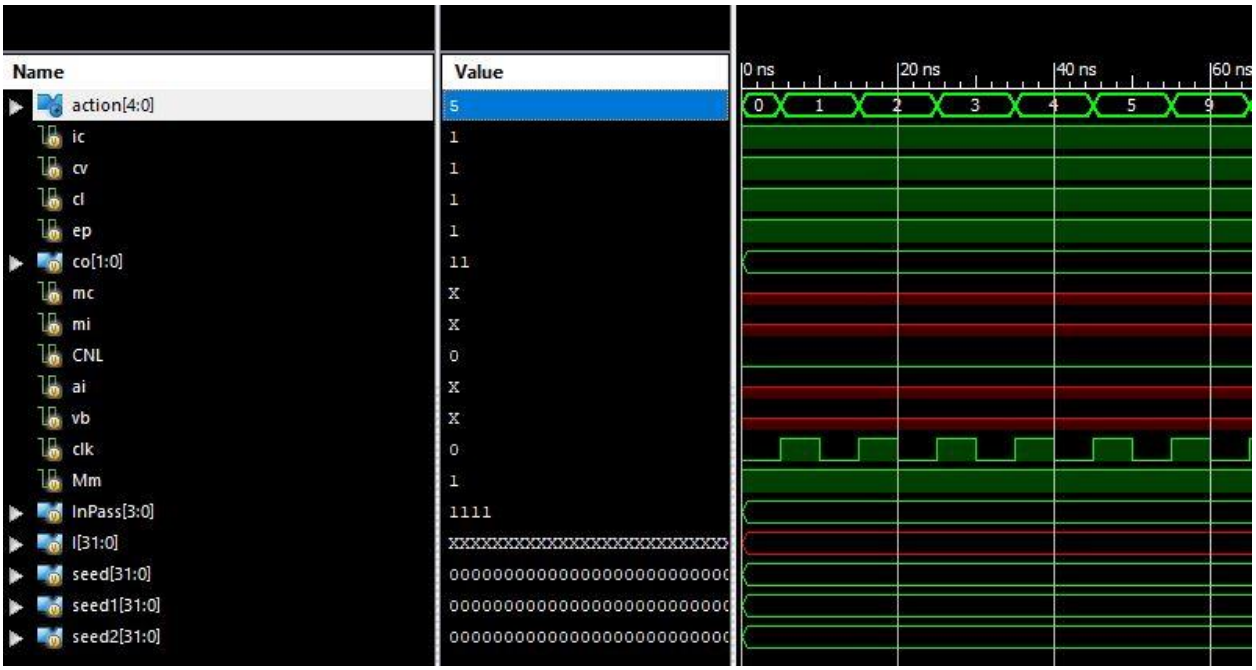
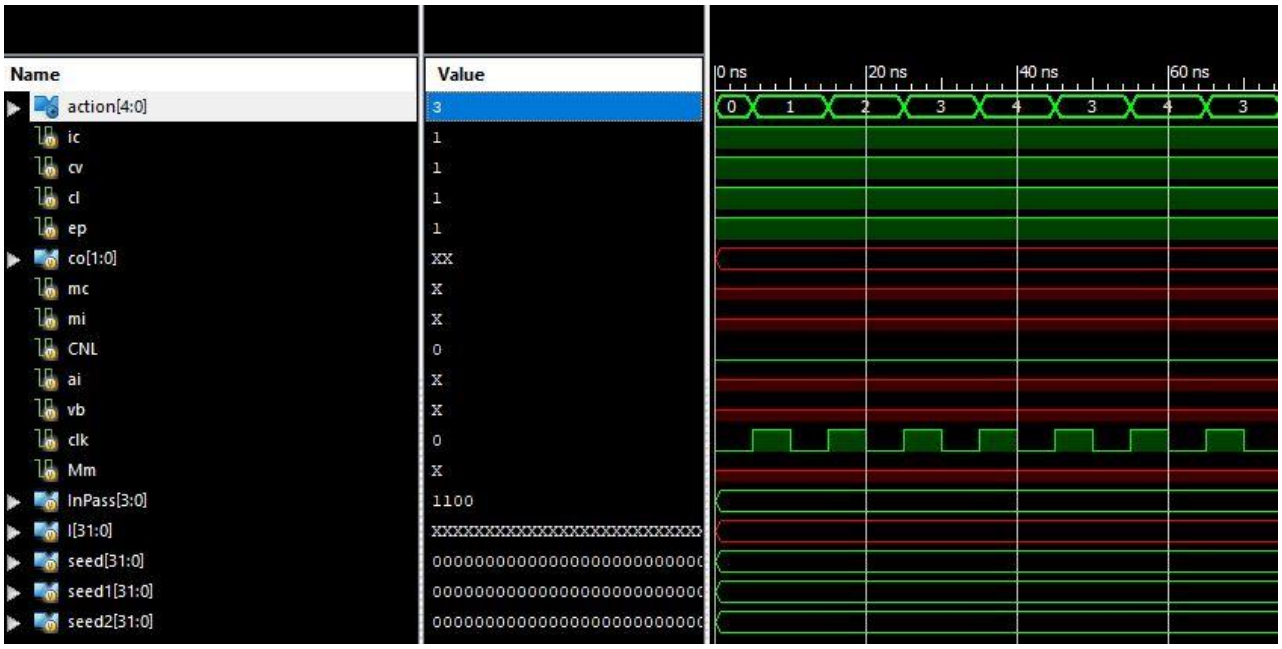
2.2 Case 2



2.3 Case 3



2.4 Case 4



2.5 Case 5