AM2: QDG-FET Based SRAM
Revised

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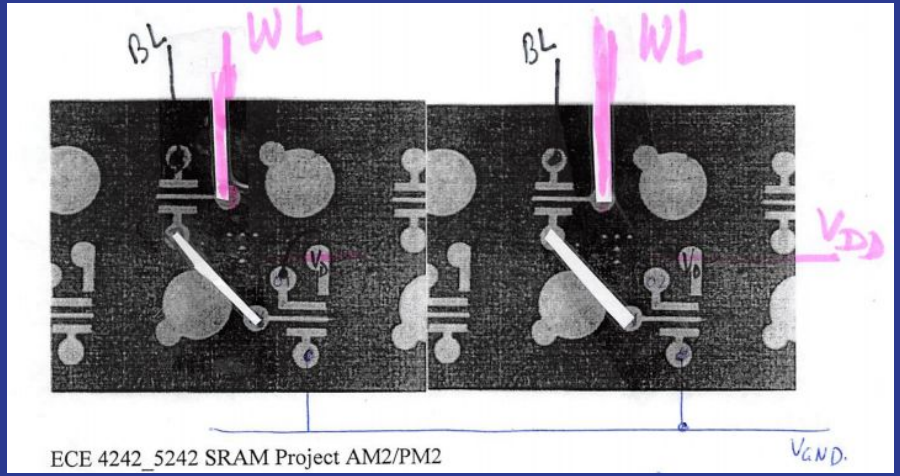
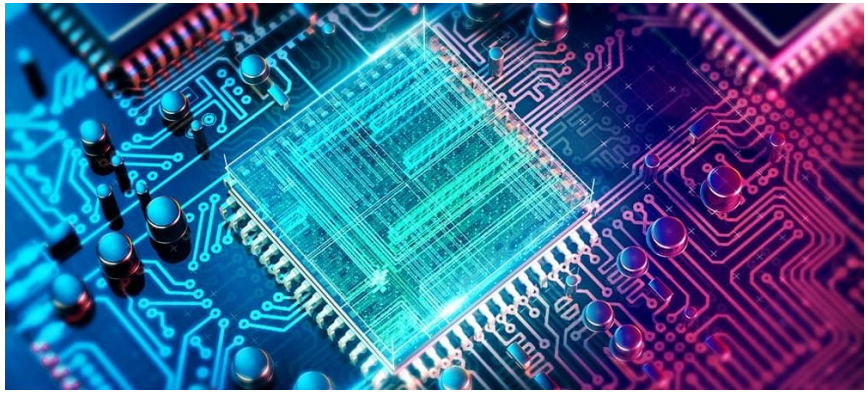


Motivation

- Importance of looking at QDG-FETs
- Fundamental Benefits & Changes
- Applications
- Relevance in Constant Field Scaling

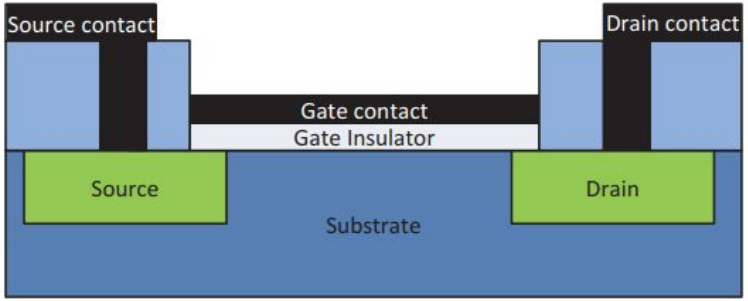


Background

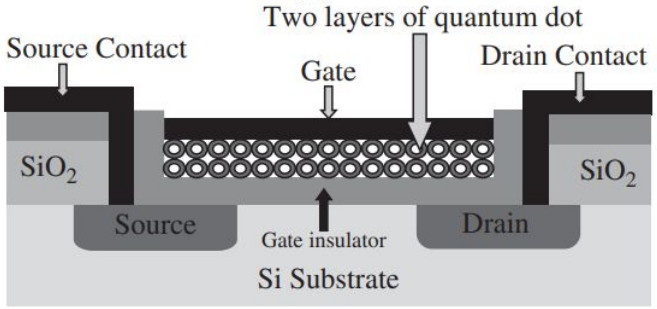
- Additional States in Transfer Characteristic
- What is a Quantum Dot?
- Ability to have > 2 Logic States
- Conventional CMOS SRAM

Transistor Structure

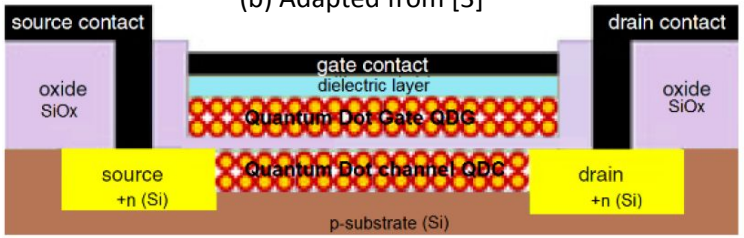
- Standard MOSFET (a)
- QDG-FET (b)
  - This and the standard MOSFET are the types of FET we will be working with.
  - The channel is the same as (b) but with 4 layers of QDs instead of the two displayed here.
- QDG/QDC-FET (c)
- Our concern is the QDG-FET



(a) Adapted from [3]



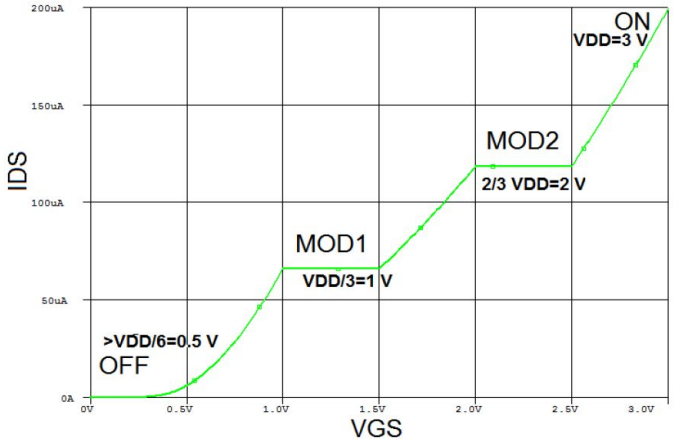
(b) Adapted from [3]



(c) Adapted from [3]

Theory

- Similarities to MOSFET Design Theory
  - Relation between Leakage Current and Threshold Voltage
  - Desire to Minimize Leakage Current and Maximize “ON” Current
- Significant Differences to MOSFET Design
  - Changes in Governing Equations
  - Changes in the characteristic of the FET



Adapted from [1]

$$V_{TH-EFF} = V_{TH} + \Delta V_{TH}$$

$$\Delta V_{TH} = \begin{cases} 0, V_{GS} \leq Vg1, \text{State OFF} \\ \alpha 1(V_{GS} + Vg1), Vg1 < V_{GS} \leq Vg2, \text{State i} \\ 1(Vg2 + Vg1), V_{GS} > Vg2, \text{State ON} \end{cases}$$

$$I_{DS} = \left(\frac{W}{L}\right) C_{OX} \mu_n \left((V_{GS} - V_{TH-EFF}) V_{DS} - \frac{{V_{DS}}^2}{2} \right)$$

Adapted from [1]

$$\Delta V_{TH} = \begin{cases} 0, V_{GS} \leq Vg1, \text{OFF} \\ \alpha 1(V_{GS} + Vg1), Vg1 < V_{GS} \leq Vg2, \text{MOD1} \\ \alpha 1(Vg2 + Vg1), Vg2 < V_{GS} \leq Vg3 \\ \alpha 1(Vg2 + Vg1) + \alpha 2(V_{GS} + Vg3), Vg3 < V_{GS} \leq Vg4, \text{MOD2} \\ \alpha 1(Vg2 + Vg1) + \alpha 2(Vg4 + Vg3), V_{GS} \geq Vg4, \text{ON} \end{cases}$$

Adapted from [1]

Theoretical basis

- Drain Current Calculations for a MOSFET
  - Simply uses a threshold voltage instead of an effective threshold voltage for different states.
- Resulting Characteristic Plots for a normal MOSFET
  - Lack of intermediate states and a smooth curve is formed. Not pictured is a point of saturation past the point of Vg = 3V.

$$I_{DS} = \left(\frac{W}{L}\right) C_{OX}\mu_n \left((V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2} \right)$$

Adapted from [1]

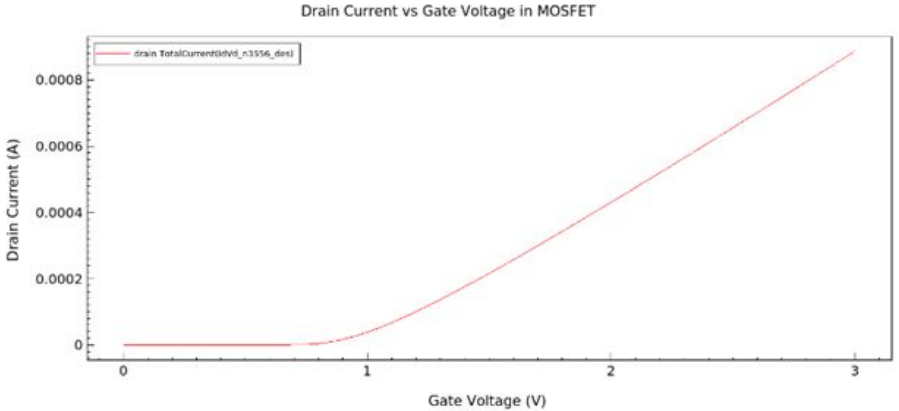


Figure 1: MOSFET Designed in TCAD Sentaurus

Truth Table Structure Comparison

- Additional Bit is possible because 1/3Vdd and 2/3Vdd represent additional logic states due to four layers of Quantum Dots present (two rows for each state).

Table 2. CMOS 1 bit SRAM truth table.

Write signal	Data signal	Stored Data
0	0	Same State
0	1	Same State
1	0	0
1	1	1

Adapted from [1]

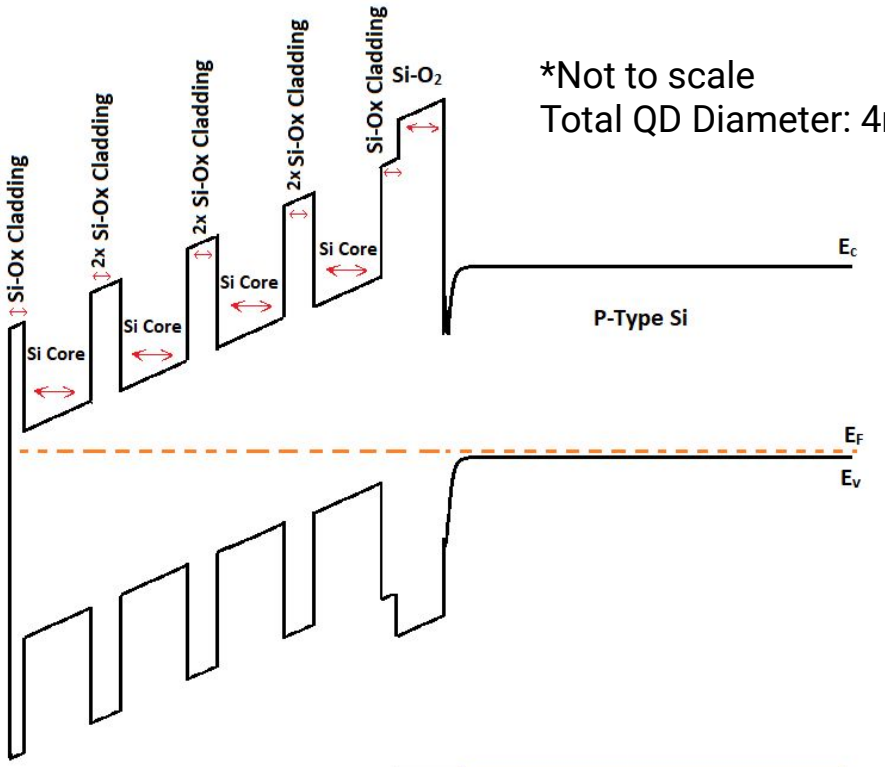
Table 4. The truth table of 2 bit SRAM.

Write signal	Data signal	Stored Data
0	0 V = Logic 0 (00)	Same State
0	⅓ V_{DD} = Logic 1 (01)	Same State
0	⅔ V_{DD} = Logic 2 (10)	Same State
0	V_{DD}= Logic 3 (11)	Same State
1	Logic 0 (00)	> ⅙ V_{DD} = Logic 0 (00)
1	Logic 1 (01)	⅓ V_{DD} = Logic 1 (01)
1	Logic 2 (10)	⅔ V_{DD} = Logic 2 (10)
1	Logic 3 (11)	V_{DD}= Logic 3 (11)

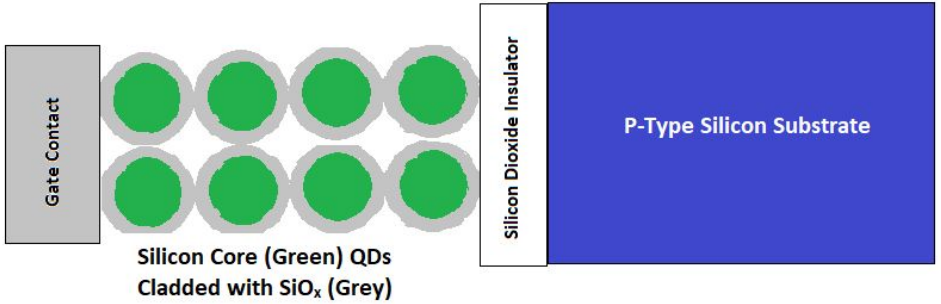
Adapted from [1]

Energy Band Diagram

Material	Band Gap	Thickness
QD Si Core	1.1 eV	2nm
QD Si-Ox Cladding Layer	8.9 eV	1nm
Si-O2 Oxide Layer	9 eV	2nm
P-Type Silicon Substrate	1.1 eV	~140nm

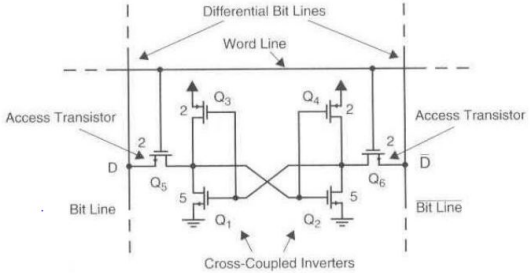


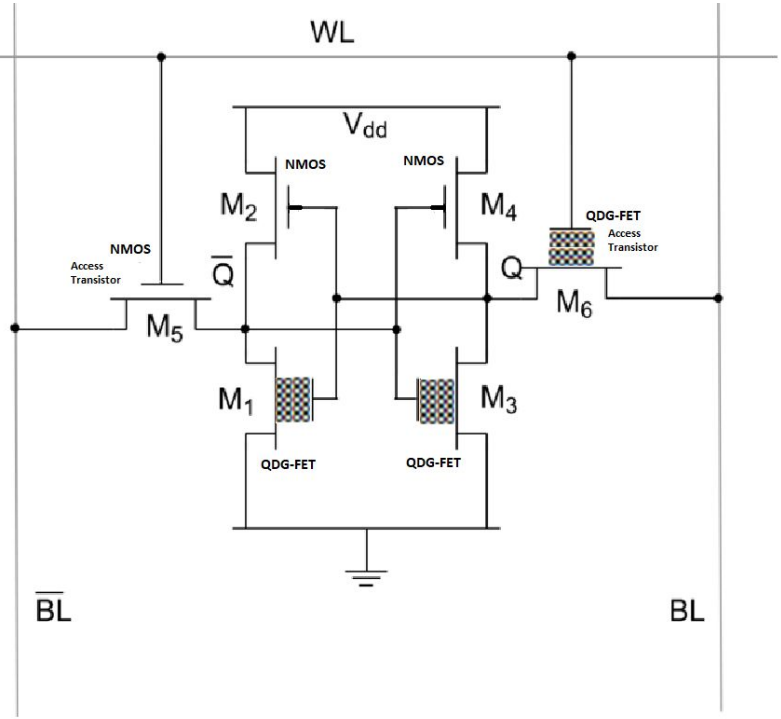
*Not to scale
Total QD Diameter: 4nm



SRAM Structure and Information

- Two cross-coupled and two single FETs (access transistors)
- The Word Line of the SRAM cell allows the auxiliary transistors to access the Bit Lines
- Bit Lines are what transports information regarding the Read/Write of the Cell
- Data is deposited into the cross-coupled Inverters
- Adding Transistors can separate the transistors used for read/write process.
- Adding QD Transistors with the proper software can allow for additional bits to be read/write without needing additional hardware.
- This is relevant because additional hardware density would not be necessary to accomplish the same speed increase per clock cycle.





Adapted from [1]

General Processing Overview

1. Cleaning/Wet Oxidation for ~1500A
2. Source Drain Diffusion Mask
3. Gate Mask, Oxidation, Etching, Si QD Deposition w/ Annealing
4. Source - Drain Contacts & SiO2 Removal with BOE
5. Al Contact & Interconnect Application

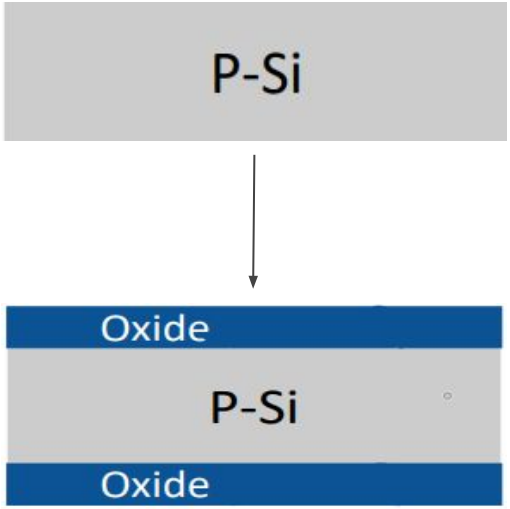
Processing: Wafer Cleaning and Wet-Oxidation

Cleaning Wafer

On Hot Plate at 115°C
Place Wafer in TCE - 2-5 min
Place in Acetone - 2-5 min
Place in Methanol - 2-5 min
Rinse in Deionized Water
Place in a 5% HF solution
Rinse in Deionized Water
Place in Piranha Solution (1H2SO4 :1H2O2) - 5 min
Rinse in Deionized Water
Place in Boiling Propanol - 5 min

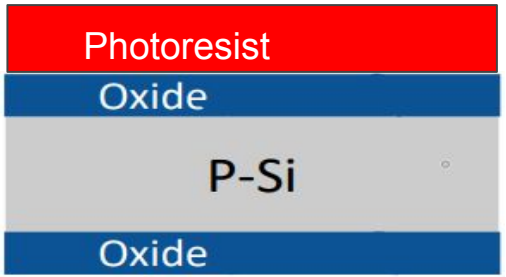
Wet-Oxidation (1400 Å)

Place clean wafer inside the wet-oxidation furnace
2 min at the mouth - 500°C ~ 700°C
10 min inside furnace - 1000° C
2 min at the mouth - 500°C ~ 700°C



Processing: Drain and Source Masks 1

Applying Photoresist



On Hot Plate at 115°C
Place wafer and mounting wafer in TCE - 2-5 min
Place both wafers in Acetone - 2-5 min
Place both wafers in Methanol - 2-5 min
Rinse both wafers in Deionized Water
Blow both wafers dry with N2
Bake both wafers at 115°C on hot plate for 3 min
Cool both wafers for 1 min
Mount the mounting wafer on the spinner using vacuum pressure
Apply S1813 Photoresist on mounting wafer then (Spin at 1000 RPM for 10 sec)
Place the wafer on the surface of the mounting wafer push sides of wafer to mount the wafer on the surface of the mounting wafer using the adhesion of the photoresist
Bake at 115°C for 10-12 min
Cool for 6 min under funnel
Blow dry with N2
Apply Photoresist on wafer (Spin at 5000 RPM for 30 sec) creates ~1.2um of photoresist layer
Bake at 115°C for 2 min
Cool for 2 min

Processing: Drain and Source Masks 2

UV Exposure

Mount the Drain & Source Opening mask in the mask aligner in such a way that the chromium side will be in contact with the wafer using vacuum pressure

Mount the mounting wafer and the sample at the center of the circular holding using vacuum pressure

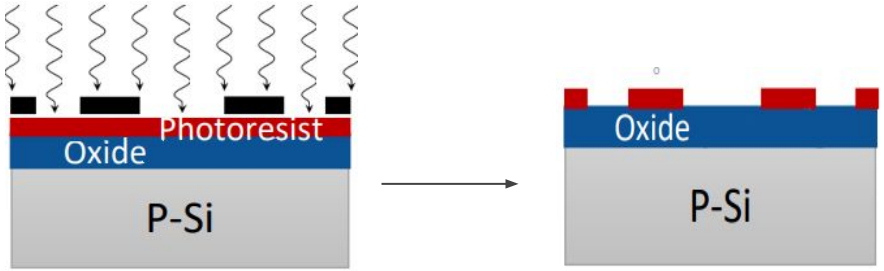
Press the cycle button to see the microscopic view

Align the mask and the sample for UV exposure

Press cycle again to sine UV ipon the sample for 30 sec.

Bake the sample for 1 minute

Cool the wafer for 1 minute



Developer

Prepare 351 developer solution with (1 developer : 3.5 H2O)

Dip the sample in the DI water

Then immerse the wafer in the Developer solution for 12 seconds, while moving the wafer gently while in the solution

Rinse in DI water

Blow dry wafer with N2

Post-bake for 10 minutes

Cool the sample for 2 minutes

Check the sample under microscope after developing for verification

(Avoid white light when the sample has photoresist and over exposing and developing)

Processing: Drain and Source Masks 3

Etching using Buffered Oxide Etch

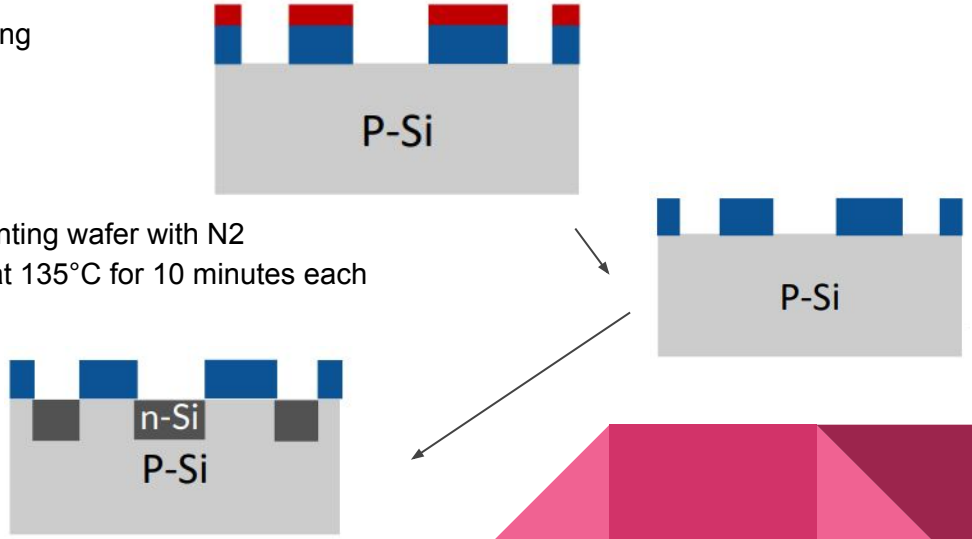
Rinse sample in DI water
(Place wafer in BOE solution for 12 seconds (etch rate of 10Å per second) to etch the oxide for total of 120Å
Rinse with DI water and blow dry with N2
Check sample under microscope in order to verify etching

Removal of mounting wafer and photoresist

Rinse wafer and mounting wafer with acetone
Place both in acetone beaker at 135°C
Separate wafer and mounting wafer then blow dry mounting wafer with N2
Immerse wafer in three separate hot acetone beakers at 135°C for 10 minutes each
Immerse sample in propanal

Diffusion

Place in furnace with a wafer of Phosphorus
2 min at the mouth - 500°C ~ 700°C
15 min inside furnace - 1000° C
2 min at the mouth - 500°C ~ 700°C



Processing: Gate Mask & Oxidation 1

Applying Photoresist

On Hot Plate at 115°C
Place wafer and mounting wafer in TCE - 2-5 min
Place both wafers in Acetone - 2-5 min
Place both wafers in Methanol - 2-5 min
Rinse both wafers in Deionized Water
Blow both wafers dry with N2
Bake both wafers at 115°C on hot plate for 3 min
Cool both wafers for 1 min

Mount the mounting wafer on the spinner using vacuum pressure
Apply S1813 Photoresist on mounting wafer then (Spin at 1000 RPM for 10 sec)
Place the wafer on the surface of the mounting wafer push sides of wafer to mount the wafer on the surface of the mounting wafer using the adhesion of the photoresist
Bake at 115°C for 10-12 min
Cool for 6 min under funnel
Blow dry with N2
Apply Photoresist on wafer (Spin at 5000 RPM for 30 sec) creates ~1.2um of photoresist layer
Bake at 115°C for 2 min
Cool for 2 min

Processing: Gate Mask & Oxidation 2

UV Exposure

Mount the open gate mask in the mask aligner in such a way that the chromium side will be in contact with the wafer using vacuum pressure (This opens all the gates)

Mount the mounting wafer and the sample at the center of the circular holding using vacuum pressure

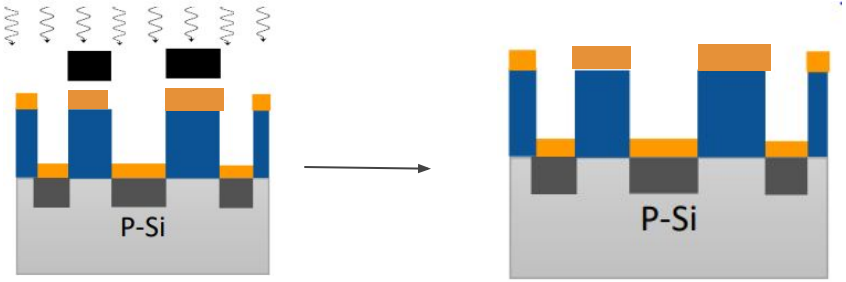
Press the cycle button to see the microscopic view

Align the mask and the sample for UV exposure

Press cycle again to sine UV ipon the sample for 30 sec.

Bake the sample for 1 minute

Cool the wafer for 1 minute



Developer

Prepare 351 developer solution with (1 developer : 3.5 H2O)

Dip the sample in the DI water

Then immerse the wafer in the Developer solution for 12 seconds, while moving the wafer gently while in the solution

Rinse in DI water

Blow dry wafer with N2

Post-bake for 10 minutes

Cool the sample for 2 minutes

Check the sample under microscope after developing for verification

(Avoid white light when the sample has photoresist and over exposing and developing)

Processing: Gate Mask & Oxidation 3

Etching using Buffered Oxide Etch

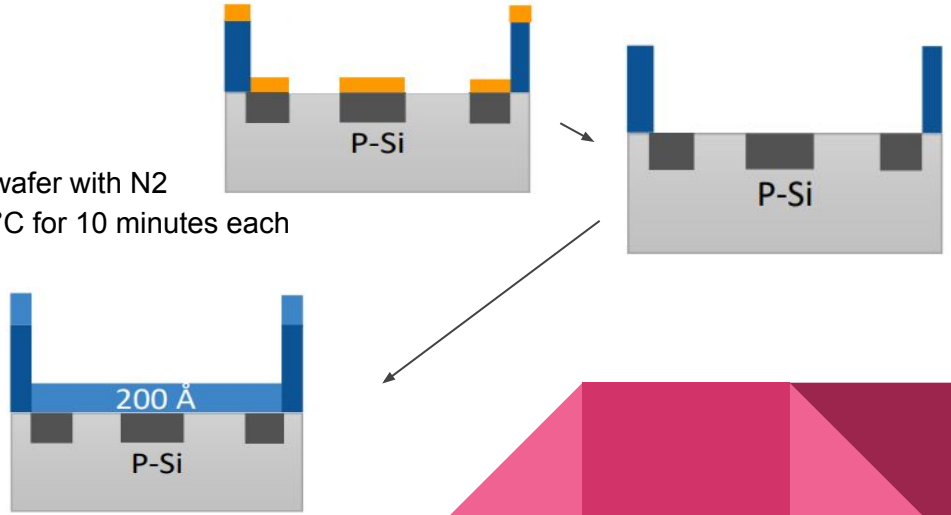
Rinse sample in DI water
(Place wafer in BOE solution for 12 seconds (etch rate of 10Å per second) to etch the oxide for total of 120Å
Rinse with DI water and blow dry with N2
Check sample under microscope in order to verify etching

Removal of mounting wafer and photoresist

Rinse wafer and mounting wafer with acetone
Place both in acetone beaker at 135°C
Separate wafer and mounting wafer then blow dry mounting wafer with N2
Immerse wafer in three separate hot acetone beakers at 135°C for 10 minutes each
Immerse sample in propanal

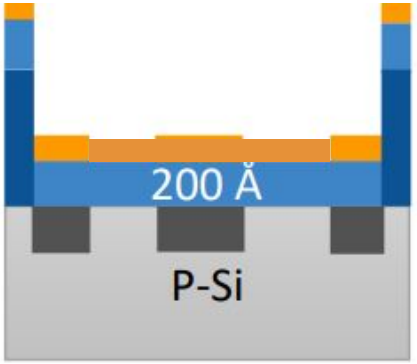
Dry-Oxidation (250 Å)

Place clean wafer inside the wet-oxidation furnace
2 min at the mouth - 500°C ~ 700°C
2 min 9 seconds inside furnace - 1000° C
2 min at the mouth - 500°C ~ 700°C



Processing: Gate Mask & Oxidation 4

Applying Photoresist



On Hot Plate at 115°C
Place wafer and mounting wafer in TCE - 2-5 min
Place both wafers in Acetone - 2-5 min
Place both wafers in Methanol - 2-5 min
Rinse both wafers in Deionized Water
Blow both wafers dry with N2
Bake both wafers at 115°C on hot plate for 3 min
Cool both wafers for 1 min
Mount the mounting wafer on the spinner using vacuum pressure
Apply S1813 Photoresist on mounting wafer then (Spin at 1000 RPM for 10 sec)
Place the wafer on the surface of the mounting wafer push sides of wafer to mount the wafer on the surface of the mounting wafer using the adhesion of the photoresist
Bake at 115°C for 10-12 min
Cool for 6 min under funnel
Blow dry with N2
Apply Photoresist on wafer (Spin at 5000 RPM for 30 sec) creates ~1.2um of photoresist layer
Bake at 115°C for 2 min
Cool for 2 min

Processing: Gate Mask & Oxidation 5

UV Exposure

Mount the second gate mask in the mask aligner in such a way that the chromium side will be in contact with the wafer using vacuum pressure (opens select gates for Quantum dots)

Mount the mounting wafer and the sample at the center of the circular holding using vacuum pressure

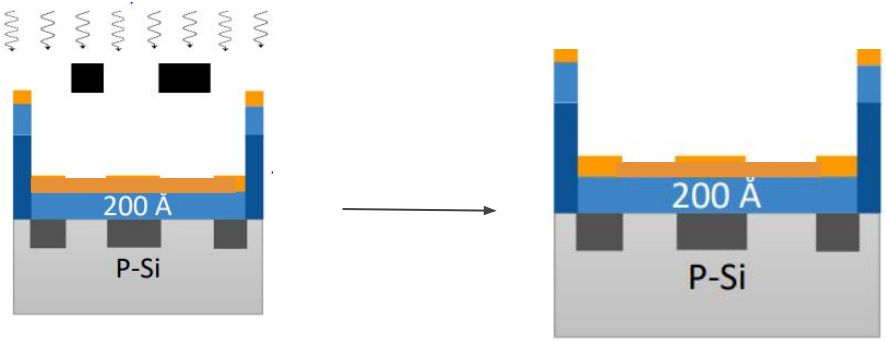
Press the cycle button to see the microscopic view

Align the mask and the sample for UV exposure

Press cycle again to sine UV upon the sample for 30 sec.

Bake the sample for 1 minute

Cool the wafer for 1 minute



Developer

Prepare 351 developer solution with (1 developer : 3.5 H2O)

Dip the sample in the DI water

Then immerse the wafer in the Developer solution for 12 seconds, while moving the wafer gently while in the solution

Rinse in DI water

Blow dry wafer with N2

Post-bake for 10 minutes

Cool the sample for 2 minutes

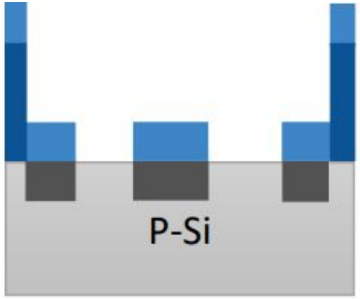
Check the sample under microscope after developing for verification

(Avoid white light when the sample has photoresist and over exposing and developing)

Processing: Gate Mask & Oxidation 6

Etching using Buffered Oxide Etch

Rinse sample in DI water
(Place wafer in BOE solution for 20 seconds (etch rate of 10Å per second) to etch the oxide for total of 200Å
Rinse with DI water and blow dry with N2
Check sample under microscope in order to verify etching

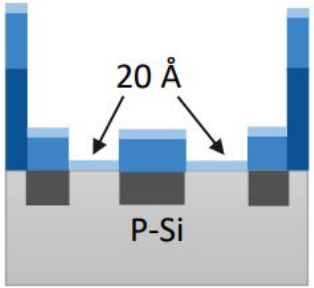


Removal of mounting wafer and photoresist

Rinse wafer and mounting wafer with acetone
Place both in acetone beaker at 135°C
Separate wafer and mounting wafer then blow dry mounting wafer with N2
Immerse wafer in three separate hot acetone beakers at 135°C for 10 minutes each
Immerse sample in propanal

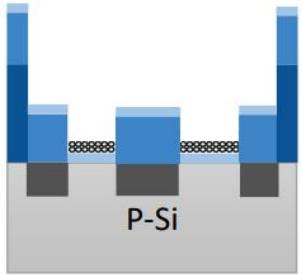
Dry-Oxidation (20 Å)

Place clean wafer inside the wet-oxidation furnace
2 min at the mouth - 500°C ~ 700°C
9 seconds inside furnace - 1000° C
2 min at the mouth - 500°C ~ 700°C



Processing: Quantum Dots 1

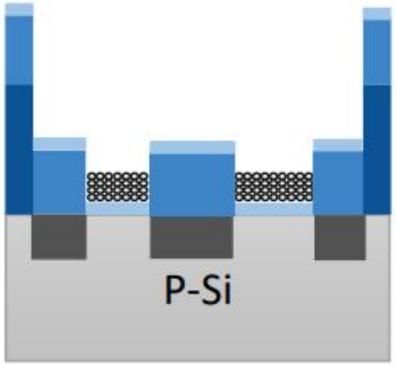
The centrifuged solution. Note the black and clear portions.



Processing/annealing QD

Place silicon or germanium powder in a jar with nickel balls
Place jar in glove box and purge box of oxygen
Place jar in the miller
Run the miller for 99 mins, 99 sec three times
Place jar in glove box and purge box of oxygen
Empty the jar, scrape particulate off the sides and place the particulate in a glass vial
Mix the ethanol and benzoyl peroxide into the glass vile (grows oxide and reduces dot size)
Place glass vial into the sonicator and shake the solution
Place vial into centrifuge and run at 4 speeds (3k, 6k, 9k, and 13k RPM) for 30 minutes each (will separate into a black solution and clear solution)
Remove the clear solution and put into a new glass vial
Add a solution of HF, ethanol, and benzoyl peroxide to the glass vial.
Put solution in a glass petri dish and submerge the wafer in the solution
2 min at the mouth
Anneal QD in 800°C oxygen for 5 minutes
2 min at the mouth

Processing: Quantum Dots 2



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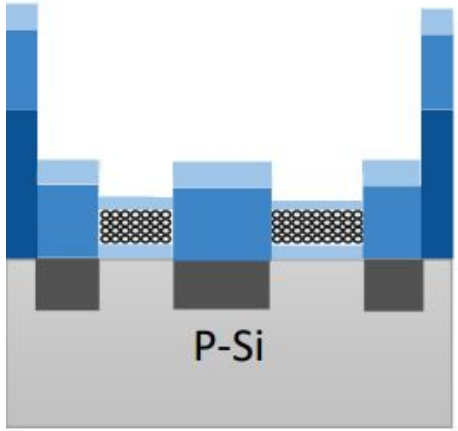
Place vial into centrifuge and run at 4 speeds (3k, 6k, 9k, and 13k RPM) for 30 minutes each (will separate into a black solution and clear solution)
Remove the clear solution and put into a new glass vial
Add a solution of HF, ethanol, and benzoyl peroxide to the glass vial.
Put solution in a glass petri dish and submerge the wafer in the solution
2 min at the mouth
Anneal QD in 300°C argon for 5 minutes
2 min at the mouth

Processing: Source & Drain Contact Mask 1

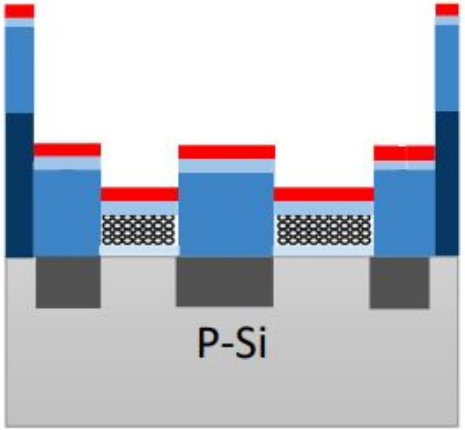
Dry-Oxidation (20 Å)

Place clean wafer inside the wet-oxidation furnace
2 min at the mouth - 500°C ~ 700°C
9 seconds inside furnace - 1000° C
2 min at the mouth - 500°C ~ 700°C



Processing: Source & Drain Contact Mask 2

Applying Photoresist



On Hot Plate at 115°C
Place wafer and mounting wafer in TCE - 2-5 min
Place both wafers in Acetone - 2-5 min
Place both wafers in Methanol - 2-5 min
Rinse both wafers in Deionized Water
Blow both wafers dry with N2
Bake both wafers at 115°C on hot plate for 3 min
Cool both wafers for 1 min
Mount the mounting wafer on the spinner using vacuum pressure
Apply S1813 Photoresist on mounting wafer then (Spin at 1000 RPM for 10 sec)
Place the wafer on the surface of the mounting wafer push sides of wafer to mount the wafer on the surface of the mounting wafer using the adhesion of the photoresist
Bake at 115°C for 10-12 min
Cool for 6 min under funnel
Blow dry with N2
Apply Photoresist on wafer (Spin at 5000 RPM for 30 sec) creates ~1.2um of photoresist layer
Bake at 115°C for 2 min
Cool for 2 min

Processing: Source & Drain Contact Mask 3

UV Exposure

Mount the Open source and drain contacts mask in the mask aligner in such a way that the chromium side will be in contact with the wafer using vacuum pressure

Mount the mounting wafer and the sample at the center of the circular holding using vacuum pressure

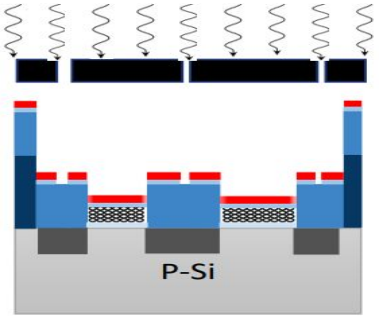
Press the cycle button to see the microscopic view

Align the mask and the sample for UV exposure

Press cycle again to sine UV ipon the sample for 30 sec.

Bake the sample for 1 minute

Cool the wafer for 1 minute



Developer

Prepare 351 developer solution with (1 developer : 3.5 H2O)

Dip the sample in the DI water

Then immerse the wafer in the Developer solution for 12 seconds, while moving the wafer gently while in the solution

Rinse in DI water

Blow dry wafer with N2

Post-bake for 10 minutes

Cool the sample for 2 minutes

Check the sample under microscope after developing for verification

(Avoid white light when the sample has photoresist and over exposing and developing)

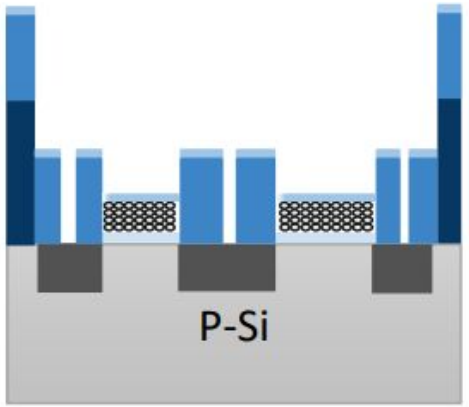
Processing: Source & Drain Contact Mask 4

Etching using Buffered Oxide Etch

Rinse sample in DI water
(Place wafer in BOE solution for 29 seconds (etch rate of 10Å per second) to etch the oxide for total of 290Å
Rinse with DI water and blow dry with N2
Check sample under microscope in order to verify etching

Removal of mounting wafer and photoresist

Rinse wafer and mounting wafer with acetone
Place both in acetone beaker at 135°C
Separate wafer and mounting wafer then blow dry mounting wafer with N2
Immerse wafer in three separate hot acetone beakers at 135°C for 10 minutes each
Immerse sample in propanal

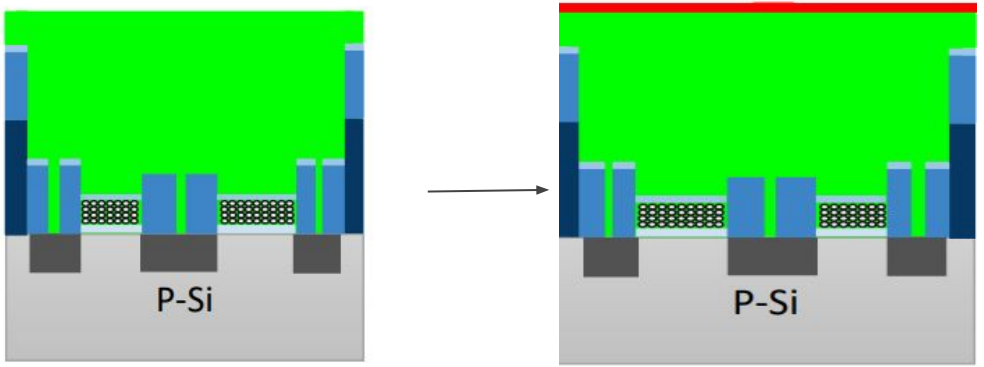


Processing: Al Metallization & Interconnect Mask 1

Metalize device

Place wafer in Aluminum evaporation machine for 9 minutes and 30 seconds in order to add 1500Å of aluminum

Applying Photoresist



On Hot Plate at 115°C
Place wafer and mounting wafer in TCE - 2-5 min
Place both wafers in Acetone - 2-5 min
Place both wafers in Methanol - 2-5 min
Rinse both wafers in Deionized Water
Blow both wafers dry with N2
Bake both wafers at 115°C on hot plate for 3 min
Cool both wafers for 1 min
Mount the mounting wafer on the spinner using vacuum pressure
Apply S1813 Photoresist on mounting wafer then (Spin at 1000 RPM for 10 sec)
Place the wafer on the surface of the mounting wafer push sides of wafer to mount the wafer on the surface of the mounting wafer using the adhesion of the photoresist
Bake at 115°C for 10-12 min
Cool for 6 min under funnel
Blow dry with N2
Apply Photoresist on wafer (Spin at 5000 RPM for 30 sec) creates ~1.2um of photoresist layer
Bake at 115°C for 2 min
Cool for 2 min

Processing: Al Metallization & Interconnect Mask 2

UV Exposure

Mount the Patterns for interconnects mask in the mask aligner in such a way that the chromium side will be in contact with the wafer using vacuum pressure

Mount the mounting wafer and the sample at the center of the circular holding using vacuum pressure

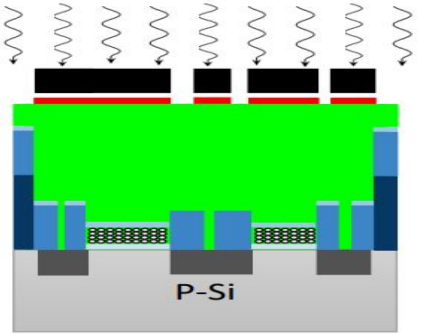
Press the cycle button to see the microscopic view

Align the mask and the sample for UV exposure

Press cycle again to sine UV ipon the sample for 30 sec.

Bake the sample for 1 minute

Cool the wafer for 1 minute



Developer

Prepare 351 developer solution with (1 developer : 3.5 H2O)

Dip the sample in the DI water

Then immerse the wafer in the Developer solution for 12 seconds, while moving the wafer gently while in the solution

Rinse in DI water

Blow dry wafer with N2

Post-bake for 10 minutes

Cool the sample for 2 minutes

Check the sample under microscope after developing for verification

(Avoid white light when the sample has photoresist and over exposing and developing)

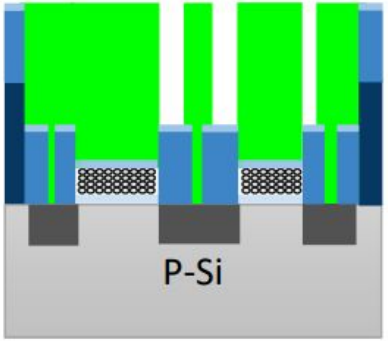
Processing: Al Metallization & Interconnect Mask 3

Etch Aluminum

Rinse sample in DI water
(Place wafer in Aluminum solution for 2 minutes and 6 seconds or until all aluminum not covered is removed
Rinse with DI water and blow dry with N2
Check sample under microscope in order to verify etching

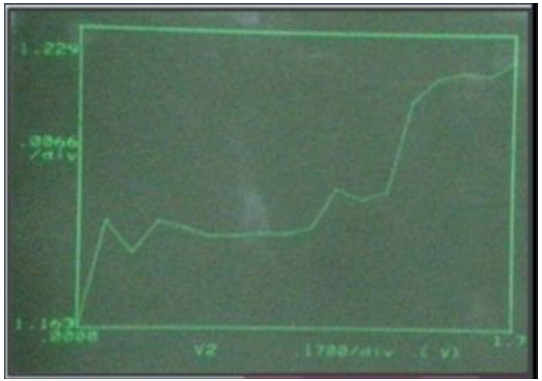
Removal of mounting wafer and photoresist

Rinse wafer and mounting wafer with acetone
Place both in acetone beaker at 135°C
Separate wafer and mounting wafer then blow dry mounting wafer with N2
Immerse wafer in three separate hot acetone beakers at 135°C for 10 minutes each
Immerse sample in propanal



Id-Vg Plot Characteristics

- The characteristic is fairly accurate to the predicted result, with deviations mostly due to noise.
- The effect of the additional voltage states are seen in both the predicted and experimental characteristics as the multiple states due to the presence of QDs is visible.
- QDs do this because as they are insulated semiconductor material, charge carriers tunnel as a further gate voltage is applied, but only at a significant point, causing the intermediate states.
- Important to note that intermediate states are mainly the plateaus in the characteristic, not the significant positive slope.



(a)

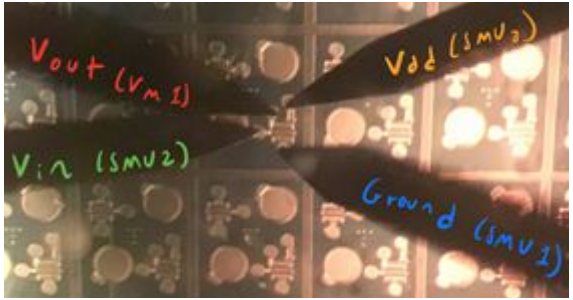
(b)

ID vs. Vg Characteristics

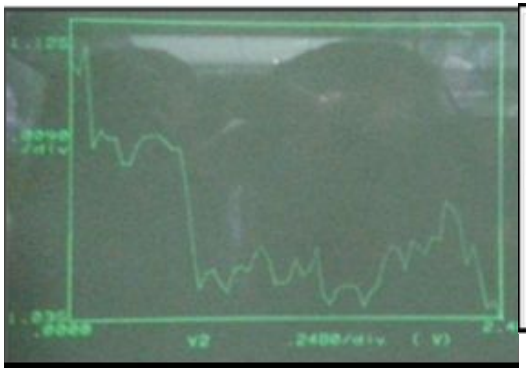
(a) Experimental Curve

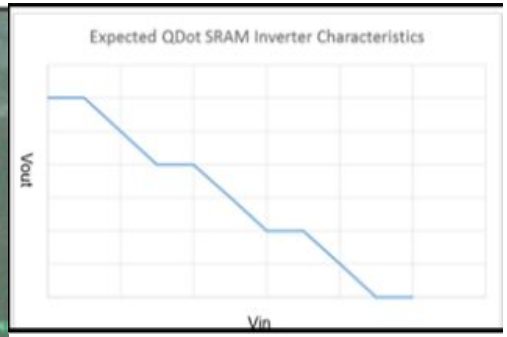
(b) Theoretical Curve

Vin vs Vout Plot Characteristics



- The two intermediate states can also be seen in this characteristic as well.
- Reminiscent of the transfer characteristics of a CMOS inverter, as the NMOS transistor would start off conducting while the PMOS is cutoff and as the input current increases the NMOS eventually becomes cutoff as the PMOS transistor conducts, allowing for an inversion curve.
- Process is changed slightly through the presence of QDs.
- The trend of the inversion can only continue once the previously referenced Gate Voltage requirement for the QDs has been surpassed.





(b)

(a) Vin vs. Vout Characteristics

(a) Experimental Curve
(b) Theoretical Curve

Conclusion & Future Work

- Moore's Law nearing the atomic limit
  - Si atoms have ~0.2 nm diameter, meaning even advanced GAA-FETs will eventually hit a limit the same way Planar FETs and FinFETs have. Adding additional Logic Bits tackles the problem a different way!
- Benefit of logic beyond Binary
  - More information communicated leading to less interconnections necessary.
  - Higher amount of information leading to less dense circuits necessary.
  - Information communicated faster per clock cycle leading to faster processing.
  - A less dense circuit requires less fabrication steps and processing precision which also brings economic benefits.

References

[1] B. Saman, J. Kondo, J. Chandy, and F. C. Jain, “Circuits and Simulation of Quaternary SRAM Using Quantum Dot Channel Field Effect Transistors (QDC-FETs),” *International Journal of High Speed Electronics and Systems*, vol. 27, no. 01n02, p. 1840004, 2018.

[2] F. Hetsch, N. Zhao, S. V. Kershaw, and A. L. Rogach, “Quantum dot field effect transistors,” *Materials Today*, vol. 16, no. 9, pp. 312–325, 2013.

[3] S. Karmakar, J.A. Chandy,M. Gogna, and F.C. Jain, Fabrication and Circuit Modeling of NMOS Inverter Based on Quantum Dot Gate Field-Effect Transistors, Journal of ELECTRONIC MATERIALS, Vol. 41, No. 8, 2012

[4] J. A. Elias, “Class 16: Memories,” in *UK College of engineering*.

[5] Butterfield, Nathan, "Fabrication, Testing and Theoretical Background of a Quantum Dot Floating Gate Flash Non-Volatile Memory (QDG NVM)" (2020). Master's Theses. 1530.

[6] S. Karmakar and F. C. Jain, “Ternary static random access memory using quantum dot gate

field-effect transistor,” Micro & Nano Letters , vol. 10, no. 11, pp. 621–624, 2015.