COMP4300 Fall 2018
Lab Assignment 1

Objective
This lab is aimed at getting you familiar with using the ModelSim simulator.

Instructions
Write a VHDL program consisting of a single entity whose architecture is a single process that implements the following logic gate with 3 inputs and 1 output

inputs			output
a_in	b_in	c_in	result
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	0
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	1

Use exactly the names given above for the signals. All your signals should be of type bit (NOT integer).

Deliverables
Please turn in the following things for this lab:
- o A printout of your VHDL code.
- o A screen shot of your exhaustive simulation.
- o A screen shot of a successful compilation of your code.

Due Date
Sunday, Sept 9, 11:59pm