

MINI-PROJECT 3

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Part 1

From MP 2, we have established the value for β for 2N2222A transistor is 167. Below, I have used the $\frac{1}{4}$ rule to calculate resistor values required to bias the circuit

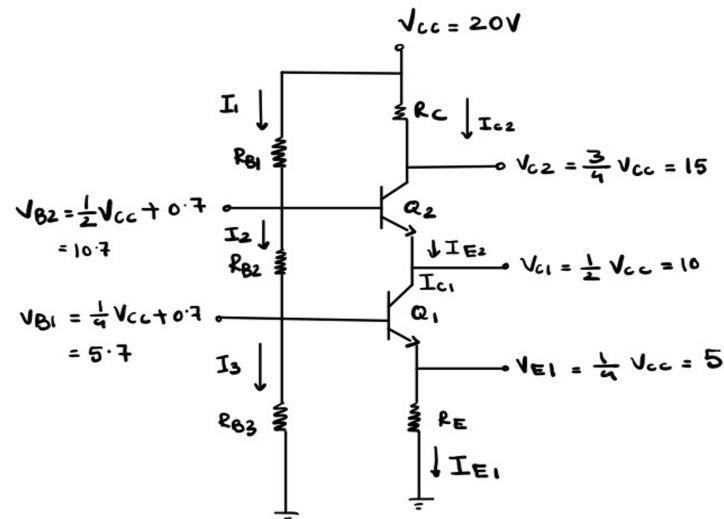


Figure 1.1: Biassed Biased circuit

Currents

$$I_{C2} = \frac{V_{CC} - \frac{3}{4}V_{CC}}{R_C} = 2.0833 \times 10^{-3} A$$

$$I_{B2} = \frac{I_{C2}}{\beta} = 1.2475 \times 10^{-3} A$$

$$I_{B1} = \frac{I_{C1}}{\beta} = 1.2550 \times 10^{-5} A$$

$$I_{E1} = (1 + \beta)(I_{B1}) = 2.1084 \times 10^{-3} A$$

$$I_1 = \frac{I_{E1}}{\sqrt{\beta}} = 1.6315 \times 10^{-4} A$$

$$I_2 = I_1 - I_{B2} = 1.5067 \times 10^{-4} A$$

$$I_3 = I_2 - I_{B1} = 1.3812 \times 10^{-4} A$$

Resistors

$$R_{B1} = \frac{V_{CC} - V_{B2}}{I_1} = 57.0029 k\Omega$$

Standard = 56 k Ω

$$R_{B2} = \frac{V_{B2} - V_{B1}}{I_2} = 30.6467 k\Omega$$

Standard = 30 k Ω

$$R_E = \frac{V_{E1}}{I_{E1}} = 2.3715 k\Omega$$

Standard = 2.4 k Ω

$$R_{B3} = \frac{V_{B1}}{I_3} = 41.2670 k\Omega$$

$$= 43 k\Omega$$

We use the standard value for R_{out} since $R_{out} = R_c$.

Now, we use the calculated values above to find the small signal parameters.

$$g_{m1} = \frac{I_{c1}}{\sqrt{\tau}} = 8.3823 \times 10^{-3}$$

$$r_{\pi 1} = \frac{B}{g_{m1}} = 1.9921 \text{ k}\Omega$$

$$g_{m2} = \frac{I_{c2}}{\sqrt{\tau}} = 8.3333 \times 10^{-3}$$

$$r_{\pi 2} = \frac{B}{g_{m2}} = 2.0040 \text{ k}\Omega$$

We know R_{in} need to be at least 3.5 kilohms and $R_{in} = R_{B2}||R_{B3}||r_{\pi 1}$. Via calculating the R_{in} value, we realiserealize that $R_{in} = 1.7894$ kilohm. Thus, we add a resistor R_x of 1.7106 kilohm at the input in order to meet the design specifications at [2]. Using standard resistor value provided at [2], we take R_x to be 1.8 kilohm.

R_{B1}	R_{B2}	R_{B3}	R_E and R_C	R_X
56 kilohm	30 kilohm	43 kilohm	2.4 kilohm	1.8 kilohm

Table 1.1: Values of all standard resistors for part 1

We can set g_{m1} and g_{m2} to be equal as well as $r_{\pi 1}$ and $r_{\pi 2}$ to be equal. This is because both Q_1 and Q_2 are the same 2N2222A transistor. So, $r_{\pi 1} = r_{\pi 2} = 2.0$ kilohms.

Now, we can use the values of resistors we have found and our small signal model to calculate the values of all the required capacitors to simulate our circuit in LTspice. As demonstrated in [3], we know that a cost efficient circuit would be the one where C_{c1} shorts first. Thus, we use open circuit time constant for C_{c1} and short circuit time constant for C_E . Upon calculating the time constant for them, whichever time constant has the higher value, we declare it to be the dominant pole and use it to calculate the thevalues of the capacitors using the W_{L3dB} value provided in [2]. Below, I have shown the mentioned calculations.

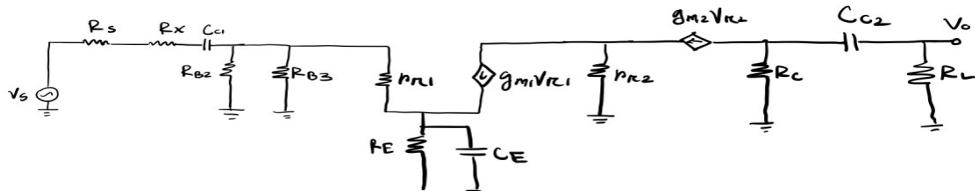


Figure 1.2: Small signal low frequency model

$$\tau_{oc}^{C_{c1}} = (C_{c1}) ((R_s + R_x) + R_{B2} || R_{B3} || (r_{\pi 1} + (1 + \beta) R_E)) \\ = C_{c1} \times 18.7828 \text{ }\mu\text{s}$$

$$\tau_{sc}^{C_E} = C_E \left(R_E \parallel \frac{(R_s + R_x) || R_{B2} || R_{B3}}{1 + \beta} + r_{\pi 1} \right) \\ = C_E \times 21.6755 \text{ }\mu\text{s} \xrightarrow{\text{Dominant pole}}$$

$$W_{L2} = \frac{1}{R_E C_E} = \frac{1}{2.9 \times 10^3 C_E}$$

$$W_{L3dB} = 1200 = \sqrt{\left(\frac{1}{\tau_{sc}^{C_E}}\right)^2 - 2(W_{L2})^2}$$

$$C_E = 38.4427 \text{ }\mu\text{F}$$

standard capacitor: $47 \text{ }\mu\text{F}$

$$\text{so, } C_{c1} = C_{c2} = C_E$$

A)

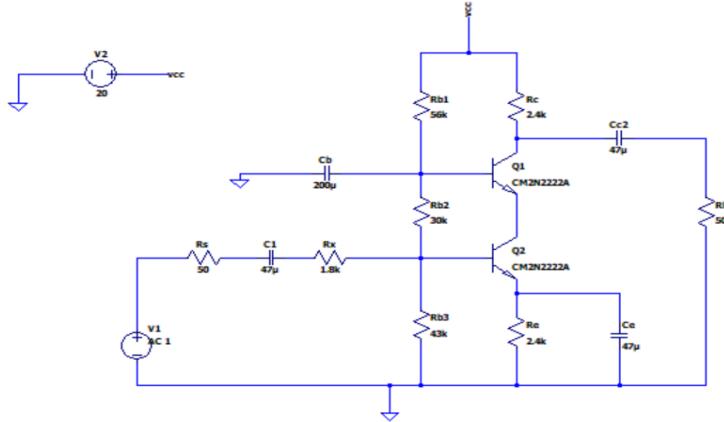


Figure 1.3: Simulated circuit to obtain DC operating points

The above circuit was simulated to obtain the DC operating point for the cascode amplifier.

V _{B1}	V _{B2}	V _{C1}	V _{E1}	V _{C2}	I _{C1} =I _{E2}	I _{C2}	I _{E1}	I _{B1}	I _{B2}
5.42 V	10.45 V	10.00 V	5.07 V	15.55 V	2.02 mA	2.04 mA	2.07 mA	11.04 μA	11.09 μA

Table 1.2: DC operating points

B) The calculations for W_{L3dB} and W_{H3dB} are shown below.

Calculating high frequency poles :

$$C_{n1} = C_{n2} = C_n$$

$$C_n = (2)(C_JE) + (TF) g_m \\ = 92.0832 \text{ pF}$$

$$C_{u1} = C_{u2} = C_u$$

$$C_u = \frac{C_JC}{\left(1 + \frac{V_{ce}}{\sqrt{JC}}\right)^{MJC}} = 4.0078 \times 10^{-11} \text{ F}$$

$$\omega_{HP1} = \frac{1}{(C_{n1} + 2C_{u1})(R_n || R_{B2} || R_{B3} || (R_s + R_x))}$$

$$= 10131890.8652 \text{ rad/s}$$

$$\omega_{HP2} = \frac{1}{(C_u)(R_C || R_L)} = 2520328719.09 \text{ rad/s}$$

$$\omega_{HP3} = \frac{1}{(C_n + 2C_u)(\frac{R_{B2}}{1 + \beta})} = 7757322.05694 \text{ rad/s}$$

Using the poles, the W_{H3dB} value becomes:

$$\omega_{H3dB} = \sqrt{\frac{1}{(\frac{1}{\omega_{HP1}})^2 + (\frac{1}{\omega_{HP2}})^2 + (\frac{1}{\omega_{L2}})^2}}$$

$$= 10.1309 \text{ Mrad/s}$$

Using the poles, the W_{L3dB} value becomes:

$$\omega_{L3dB} = \sqrt{\left(\frac{1}{T_{CE}^{sc}}\right)^2 - 2\omega_{L2}^2}$$

$$= 981.5165 \text{ rad/s}$$

The magnitude and phase plot (plot with the dotted line) is shown in the next page. The W_{H3dB} value and W_{L3dB} value is marked on the magnitude plot as shown.

W_{L3dB} simulated = 1053.2679 rad/s

W_{H3dB} simulated = 10.6893 Mrad/s

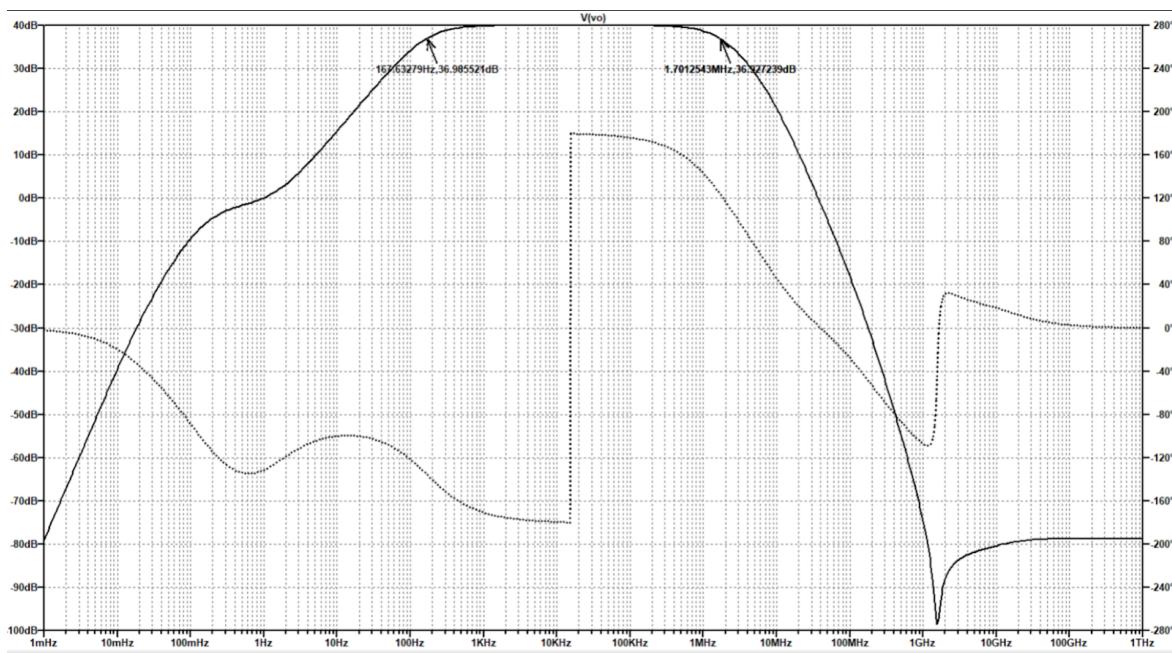


Figure 1.4: magnitude and phase plot for the cascode amplifier

C)

The chosen midband frequency was found via the following calculation. Then using this midband frequency, the voltage transfer curve was obtained in figure 1.5. In order to obtain the graph we conducted a transient analysis applying a sinusoidal input with varying amplitude.

$$\text{midband (frequency)} = \sqrt{f_{H3dB} \times f_{L3dB}}$$

$$= 16.8875 \text{ kHz}$$

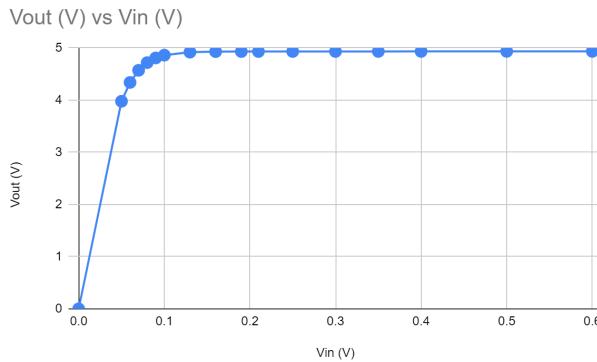


Figure 1.5: voltage transfer curve

Looking at the graph above it is clear that the graph is non linear around 60 mV.

D)

The measured and calculated R_{in} and R_{out} are shown in table 1.3 and the error is calculated in order to see how far off they are from each other. As we know the equation to calculate $R_{in} = (R_{B2} \parallel R_{B3} \parallel R_{pi}) + R_x$ and $R_{out} = R_C$

	Measured	Calculated
R_{in}	3.7908 kiloohm	3.5966 kiloohm
R_{out}	2.49957 kiloohms	2.4 kiloohms

Figure 1.3: Calculated and measured R_{in} and R_{out} value

Discussion:

In part 1, an examination was conducted on the cascode amplifier. Commencing with the application of the 1/4th rule, we biassed the circuit utilising the beta value obtained in MP2, which stood at 167. The DC operating points were measured and computed, revealing their close proximity. In order to fulfil the prerequisite of attaining a desirable input impedance, a resistor was introduced in series with the C_B to the base, measuring at 1.8 kiloohms. To adhere to the specified W_{L3dB} of 1200 rad/s, we employed the open circuit and short circuit time constant method, determining a standard capacitor value of 47 microfarads. In the subsequent part (Part C), we systematically varied the amplitude of the input signal to obtain a voltage transfer curve. The graph displayed a nonlinear output emerging around 60mV. As for the calculation versus measurement of input impedance, the calculated and simulated value proved to be relatively close to each other, validating the accuracy of the employed calculation method. In summary, the LTSPice simulations were utilised to align closely with our calculated values for the Cascode Amplifier circuit.

Part 2

A)

From the question, we know that V_{cc} is 12 V, $V_{E1}=V_{CC}/3$, $I_1 = 0.1I_{E1}$ and that at midband R_i and R_o both equal to $50\pm5\Omega$. We also know that the low frequency cut-off occurs at or below

1000Hz. From MP2, we have established beta to be 118 V/V. Below are the calculations shown to find the design values R_{E1} , R_{C1} , R_{B1} , R_{B2} , R_{E2} , C_{C1} , C_B and C_{C2} .

$$V_{E1} = \frac{V_{CC}}{3} = 4V \quad V_{B1} = V_{E1} + V_{BE} = 4.7V \quad V_{C2} = V_{CC} = 12V$$

$$V_{C1} = V_{B2} = \frac{2}{3}V_{CC} \quad V_{E2} = V_{B2} - V_{BE} = 7.3V \\ = 8V$$

$$R_{in} = \frac{R_{n1}}{1+\beta} \parallel R_{E1}, \quad R_{out} = \frac{R_{c1} + R_{n2}}{1+\beta} \parallel R_{E2}, \quad r_{n1} = \frac{B V_T}{I_{C1}}, \quad I_{C1} = \frac{I_{E1}}{1+\frac{1}{\beta}} \\ = 50 \Omega \quad = 50 \Omega$$

Solving for I_{E1} , we get:

$$50 = \frac{\left(\frac{R_{n1}}{1+\beta}\right) R_{E1}}{\left(\frac{R_{n1}}{1+\beta}\right) + R_{E1}} \quad \left. \begin{array}{l} \text{So, } 50 = \frac{\left(\frac{B V_T}{I_{C1}}\right) \left(\frac{V_{E1}}{I_{E1}}\right)}{1+\beta} \\ \frac{B V_T}{I_{C1}} + \frac{V_{E1}}{I_{E1}} \end{array} \right\}$$

$$R_{E1} = \frac{V_{E1}}{I_{E1}}$$

$$\left(\frac{B V_T}{I_{C1}}\right) \left(\frac{V_{E1}}{I_{E1}}\right)$$

$$\frac{B V_T}{I_{C1}} + \frac{V_{E1}}{I_{E1}}$$

$$I_{E1} = 0.4969 mA$$

Solving for R_{E1} :

$$R_{E1} = \frac{V_{CC}/3}{I_{E1}} \\ = 8.050 k\Omega$$

Solving for r_{B1} :

$$r_{B1} = \frac{V_{CC} - V_{B1}}{0.1 I_{E1}} = 146.9125 k\Omega$$

Solving for r_{B2}

$$r_{B2} = \frac{V_{B1}}{0.1 I_{E1} - I_{B1}} = 103.2653 k\Omega$$

$$\therefore I_{B1} = \frac{I_{E1}}{1+\beta}$$

Solving for R_{E2} and R_{C1}

$$R_{out} = \frac{R_{c1} + R_{n2}}{1+\beta} \parallel R_{E2} \quad R_{n2} = \frac{B V_T}{I_{C2}} \quad R_{C1} = \frac{V_{CC} - V_{B2}}{I_{C1} + I_{B2}} \\ = 50 \Omega$$

$$I_{C2} = \beta I_{B2} \quad I_{C1} = \frac{I_{E1}}{1+\frac{1}{\beta}} \quad I_{B2} = \frac{\left(\frac{V_{E2}}{R_{E2}}\right)}{\beta + 1}$$

$$R_{E2} = 0.4800 k\Omega \quad R_{C1} = 6.4462 k\Omega$$

Now that we have the value of all the resistors, we can use them to draw the low frequency circuit.

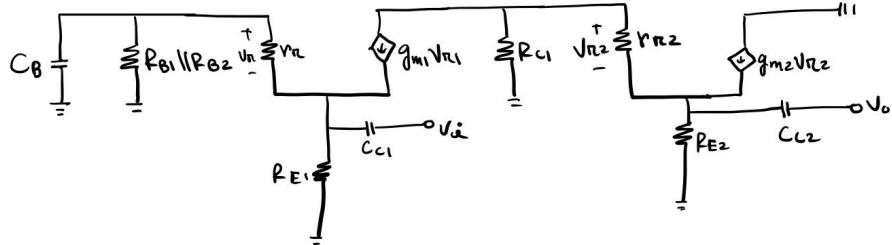


Figure 2.1: Low frequency circuit

As mentioned in the question and as seen from above, the resistance seen by the C_{c1} and C_{c2} capacitors are equal. Because of the locations of C_{c1} and C_{c2} , we realise that the calculation for the resistance seen by C_{c1} and C_{c2} are identical to the calculation used to find the input and output impedance which has to be 50 ohms. Thus, we can say, $C_{c1} = C_{c2}$. Since the resistance seen by these two capacitors are relatively low, they contribute to the dominant pole. Thus, we can use the following equation to find the value of the capacitor.

$$1000 \times 2\pi = \sqrt{\left(\frac{1}{50 \times C_{c1}}\right)^2 + \left(\frac{1}{50 \times C_{c2}}\right)^2}$$

$$C_{c1} = C_{c2} = C$$

$$\text{So, } 1000 \times 2\pi = \sqrt{\left(\frac{1}{50 \times C}\right)^2 + \left(\frac{1}{50 \times C}\right)^2}$$

$$C = 4.5016 \mu F$$

To find C_B , we set the pole associated with C_B at least one decade below so that it does not contribute.

$$T_{CB} = (C_B) \left(R_{BB} || r_{n1} + (1+B) R_{E1} \right)$$

$$444 = \frac{1}{C_B \times 57051.6096 \Omega}$$

$$\text{So, } C_B = 39.4774 \text{ nF}$$

B)

Name	C_{c1}	C_{c2}	C_B	R_{B1}	R_{B2}	R_{E1}	R_{E2}	R_{C1}
Calculated value	4.5 μF	4.5 μF	39.48 nF	146.91 K Ω	103.26 K Ω	8.05 K Ω	0.48 K Ω	6.44 K Ω
Standard value	4.7 μF	4.7 μF	.039 μF	150 K Ω	100 K Ω	8.2 K Ω	470 Ω	6.2 K Ω

Table 2.1: part 2 circuit with standard value of resistors and capacitors

In order to find the midband frequency to measure R_{in} and R_o , the circuit in figure 2.2 was simulated and a bode plot was obtained. The value for low frequency was found to be 1.2606 kHz and the value for high frequency is 5.9192MHz. As we do a geometric mean, we find the midband frequency to be 86.3819 kHz.

We put $V_{test} = 1V$ in the input of the circuit in figure 2.2 and plot V_{test}/ I_{test} and measure the resistance R_{in} at the obtained midband frequency. Doing so give us a R_{in} of 56.7813Ω .

Similarly, for output resistance, we put a V_{test} at the output obtainting a value of 52.7732Ω for R_{out} .

As we can see that the R_{in} value exceeds the design specifications. Thus, we need to modify the resistor values to meet the design specifications. Let $RE1 = 7.5 K\Omega$. Now our R_{in} is 52.4425Ω and $R_{out} = 52.1059 K\Omega$ which meets the design specification.

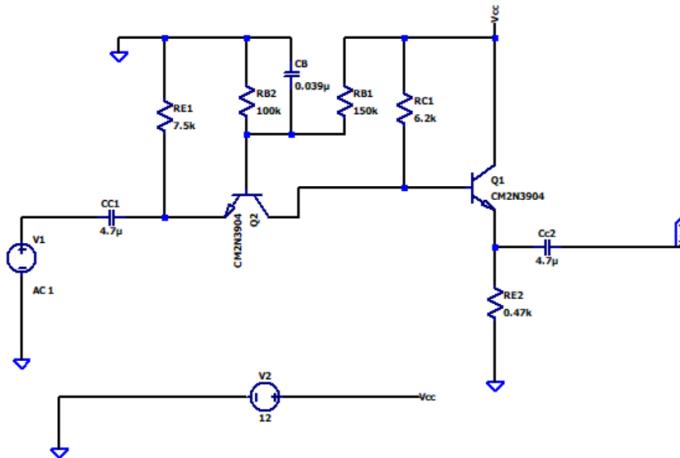


Figure 2.2: Simulated circuit for obtaining midband

We measure the voltage gain by conducting a transient analysis and measuring the output voltage while the input input voltage stay at 1 mV. Doing so, we obtain a A_m of 102 V/V.

C)

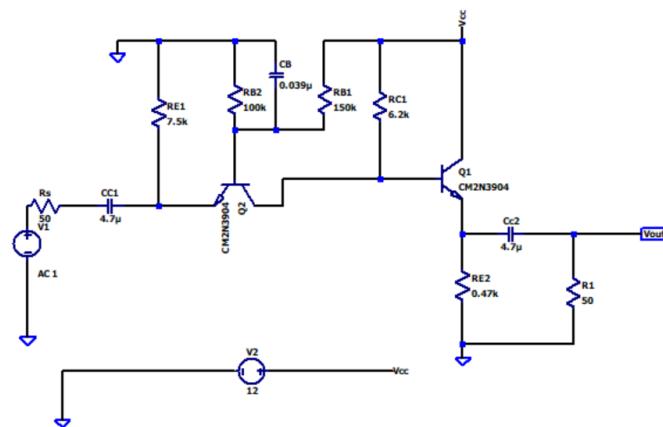


Figure 2.2: Simulated circuit to obtain magnitude and phase plots

The low frequency and high frequency cutoff points are marked on the graph below. The W_{L3dB} point is 670.7947 Hz and W_{H3dB} is 4.6057 MHz. Since the W_{L3dB} point is well below 1000 Hz, the design specifications are met as the input and out resistance would stay the

same after the adjusted R_c and R_{E1} value in part B. Thus, we do not need to adjust any low frequency capacitor values.

The midband gain for the circuit is 55.5831 kHz with the load attached which was found by taking the geometric mean of W_{L3dB} an W_{H3dB} .

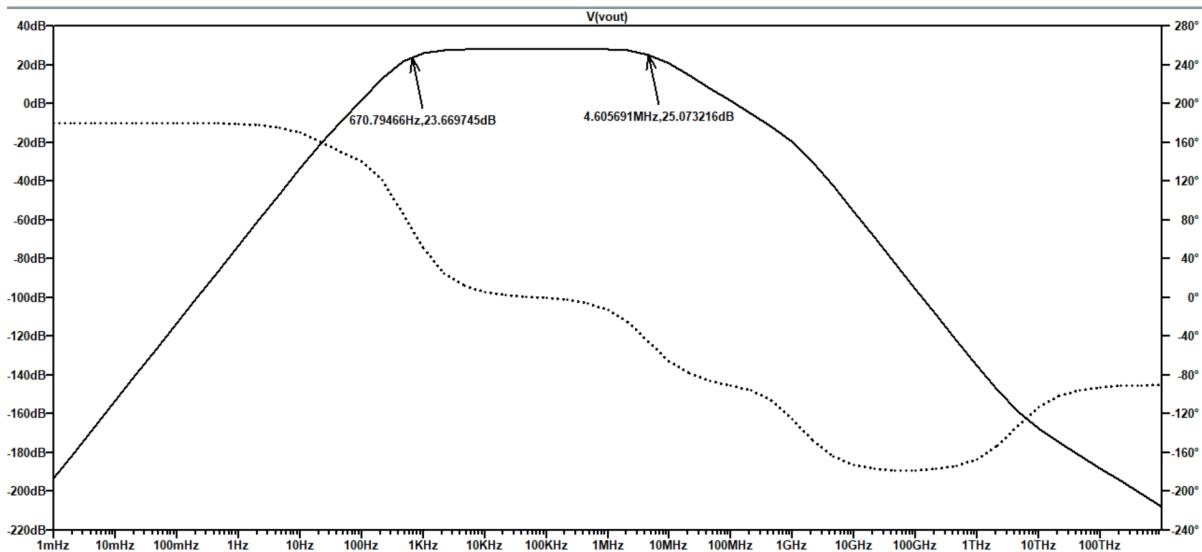


Figure 2.3: Simulated magnitude and phase plot

Discussion:

The simulated outcomes of the cascaded amplifier demonstrate compliance with the specified criteria. The input and output resistances at midband, denoted as R_{in} and R_{out} , respectively, fall within the range of $50\Omega \pm 5\Omega$. Additionally, the low-frequency cut-in is observed to be below 1kHz. These results affirm that the cascaded amplifier successfully meets the required specifications, ensuring the desired performance characteristics within the designated parameters.

Part 3

- A) i) The following circuit with a symmetric differential small signal was applied and probed at V_{out} to obtain the bode plot as asked in the question.
- ii) We measure the gain of the circuit by plotting $V_{out}/(V_a - V_b)$ and use the cursor in LtSpice to measure the gain at 1Khz. Following this process provides us with a value of 11.8141×10^3 V/V which results in a gain of 81.4480 dB.

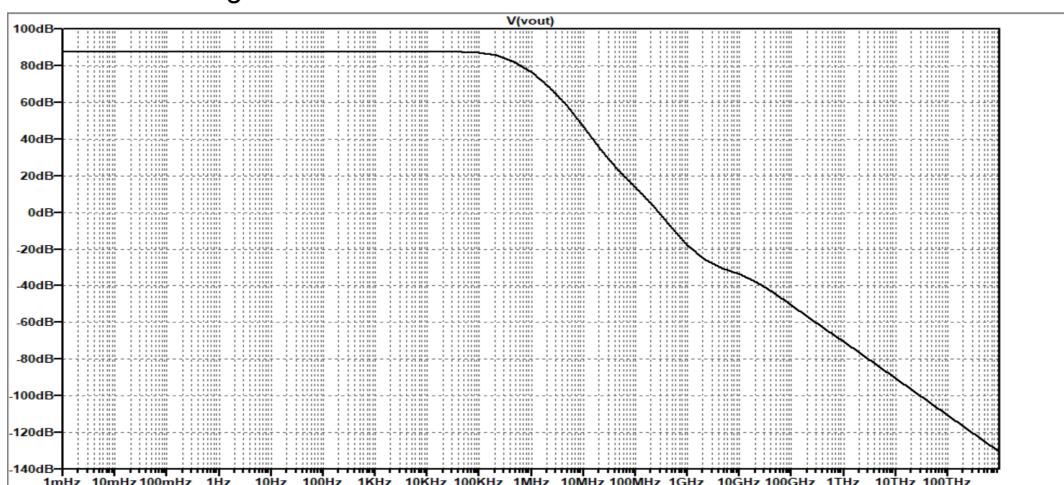


Figure 3.2: Magnitude plot for part A-i

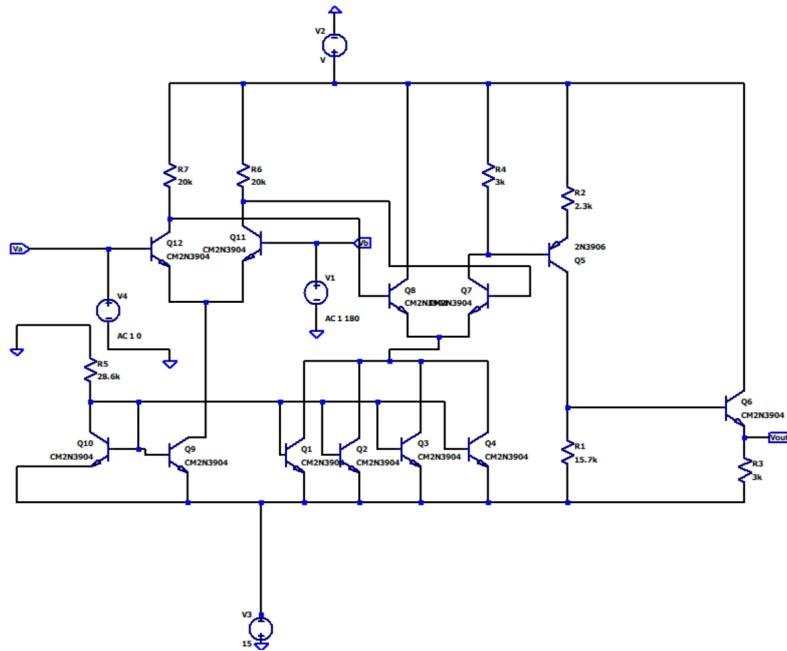


Figure 3.1: Simulated circuit for part A-i

B)

- i) In order to obtain the differential input impedance in time dalmatian, the input sources in figure 3.1 was replace by a sinusoidal signal with amplitude of 1 mV with frequency of 1 kilohertz as mentioned in the question. Then as we take the peak to peak value, we get a value of 4mV for differential voltage. Dividing this 4 mV with the simulated $I_{\text{test(peak-to-peak)}}$ give us a value of $R_{\text{in}} = 23.8162 \text{ k}\Omega$.
- ii) In order to find the R_{out} , I have shorted the input terminals of figure 3.1 and have applied a test voltage source at the output and have plotted $V_{\text{test(peak-to-peak)}}/I_{\text{test(peak-to-peak)}}$ in Ltspice and measured the impedance at 1kHz. Doing so gave me the a R_{out} of 152.4705Ω .

C) i) The magnitude response below was obtained after applying a common mode small signal to the input in figure 3.1 and probing it at Vout.

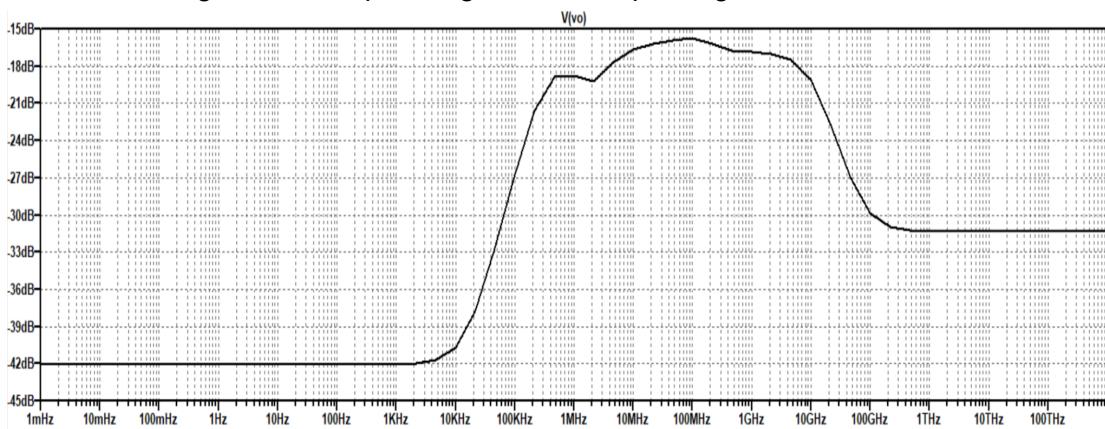


Figure 3.2: Magnitude response for C-i

- ii) The A_d value gained from the simulation was 123.49423 at 1 kHz and the A_{cm} value gained from the simulation was 7.9012×10^{-3} . The equation for $\text{CMMR} = 20 \log_{10}(|A_d|/|A_{\text{cm}}|)$. Carrying out the calculation, we get a value of 123.4942 dB for CMMR.

D)

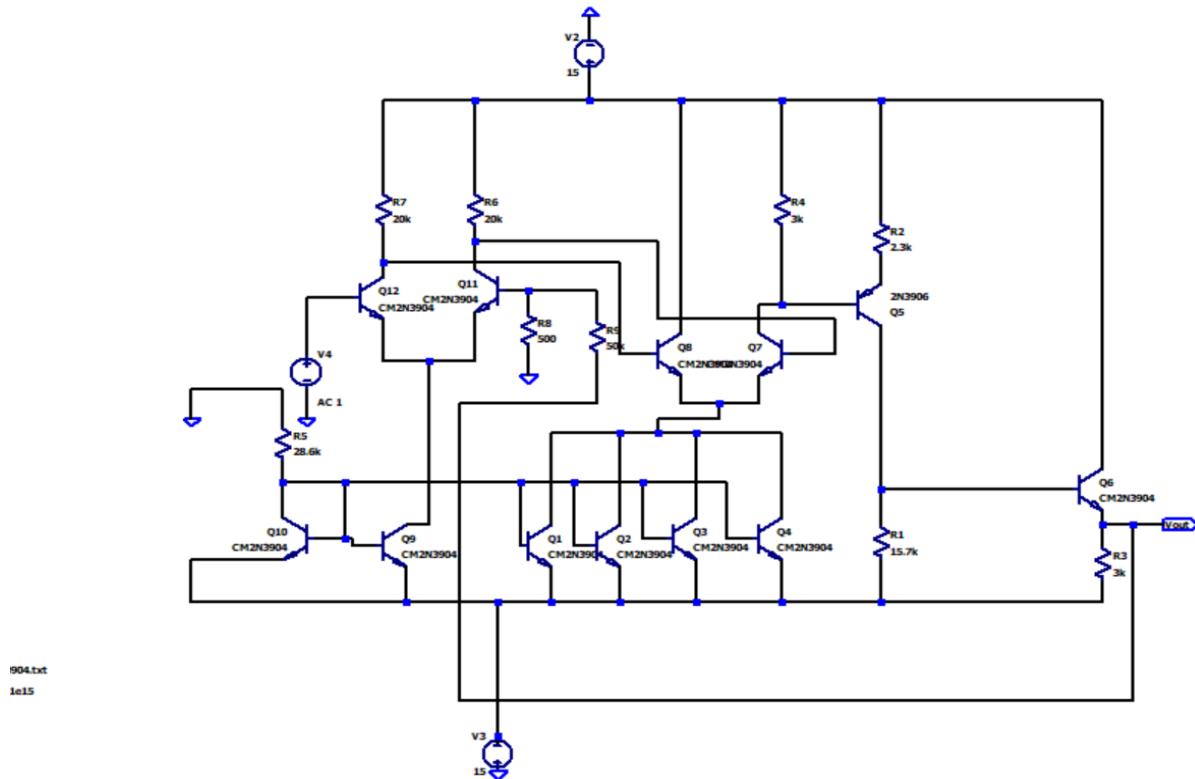


Figure 3.3: Circuit for Non-inverting op amp

The following bode plot was obtained after simulating the noninverting amplifier after attaching a $50\text{k}\Omega$ resistor between the output and the (-) input terminal of your op-amp and one 500Ω resistor between the (-) input terminal and ground

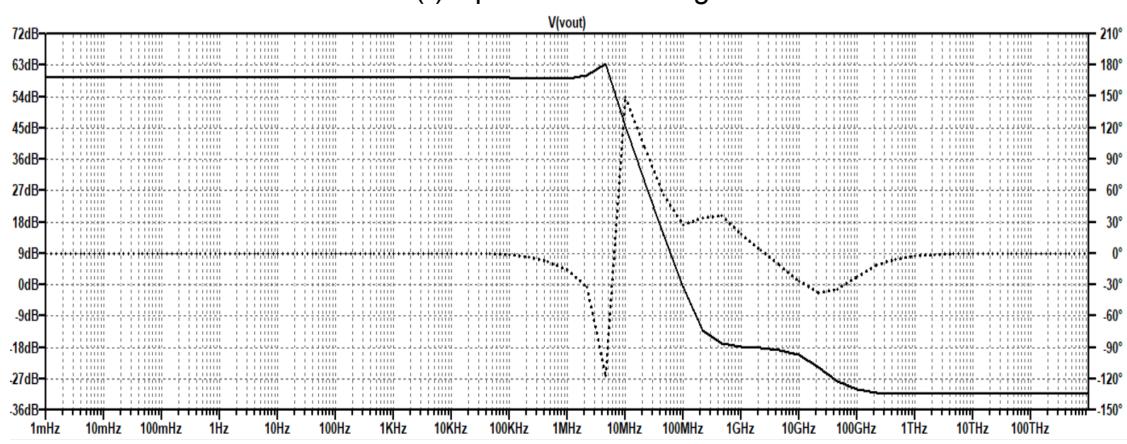
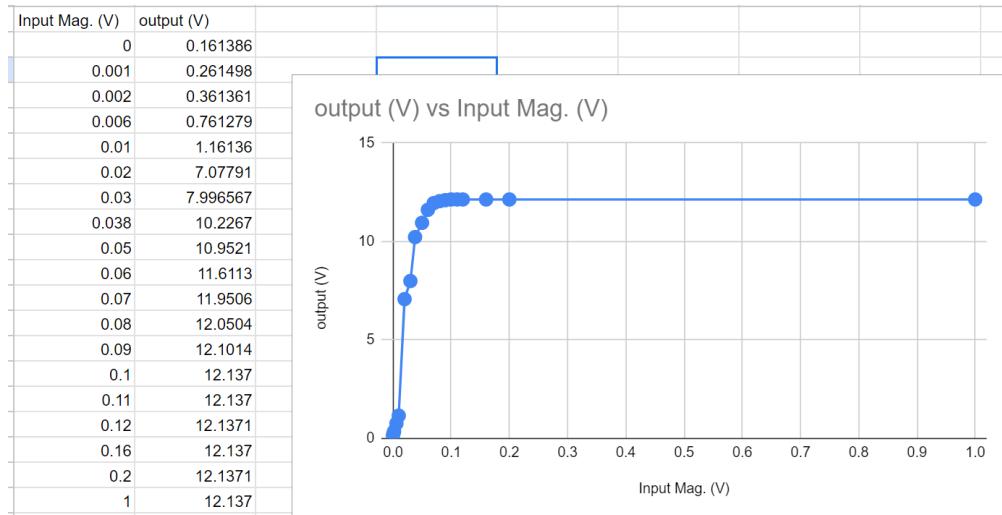


Figure 3.3: Bode plot for D

To determine the voltage gain at 1 kHz in the time domain, introduce a $\pm 1 \text{ mV}$ input signal. Measure the peak-to-peak output voltage of the amplifier and then divide it by the peak-to-peak input voltage, which in this case is 2 mV. The resulting voltage gain,

obtained through this process, is 100.0123 V/V. This value is fairly accurate as we can know the gain of an non inverting amplifier is $(R_2+R_1)/R_1$. In our case, R_2 is $50k\Omega$ while R_1 is 500Ω which give us a gain of 101 V/V .

- E) For this part, I have increased the input signal of the 1 KHz signal and observed the output. As we can see from the graph and the values obtained that the output is linear till about 100 mV, after which it become non linear.



- F) i) A test voltage source was put into the positive terminal of the input while keeping the same configuration as D and V_{test}/I_{test} was plotted and the value for R_{in} was obtained at 1KHz. The value for R_{in} is $2.5190 M\Omega$.
- ii) A test voltage source was put into the output terminal of the input while keeping the same configuration as D and V_{test}/I_{test} was plotted and the value for R_{out} was obtained at 1KHz. The value for R_{out} is 3.5513284Ω .

Discussion: The R_{out} values for the amplifier in part B and F makes sense as I have consulted the textbook in and understood how to calculate R_{out} . From the textbook, I have learned that $R_o = R_6 \parallel [r_{e8} + R5/(\beta+1)]$ which comes out to be 152 ohms and in the calculations, I have acquired 152.4705Ω which seems fairly close. Similarly, the measured gain was found to be 11814 V/V where in class, we have measure the gain to be 8600 V/V. Despite having an error of 27% in the gain, I would say, this is pretty accurate a lot of internal factors work when you simulate a circuit in Ltpice. As mentioned above the voltage gain achieved in part D also seemed fairly accurate. As seen from part B and F, I input resistance have increased a lot in part F. This is because in part D we have created a non-inverting amplifier which usually have a pretty big input resistance. The maximum input signal for which the output is linear comes out to be 100 mv.

Part 4

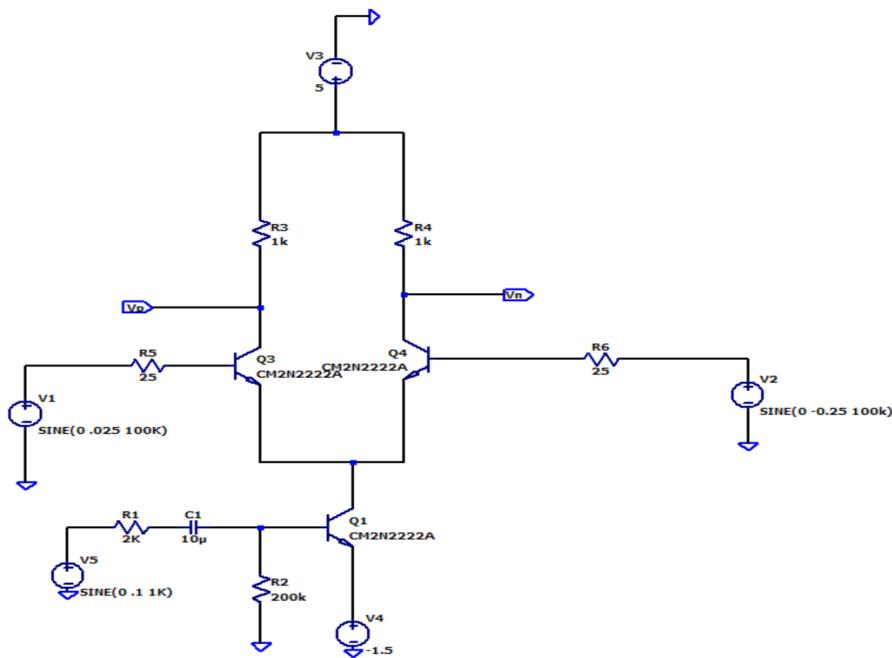


Figure 4.1: AM modulator circuit

- A) For this part, I have applied a 50mV_p, 1kHz sine wave to the input of the modulation and observed the differential output. The circuit in figure 4.1 was simulated in order to do the the mentioned task.

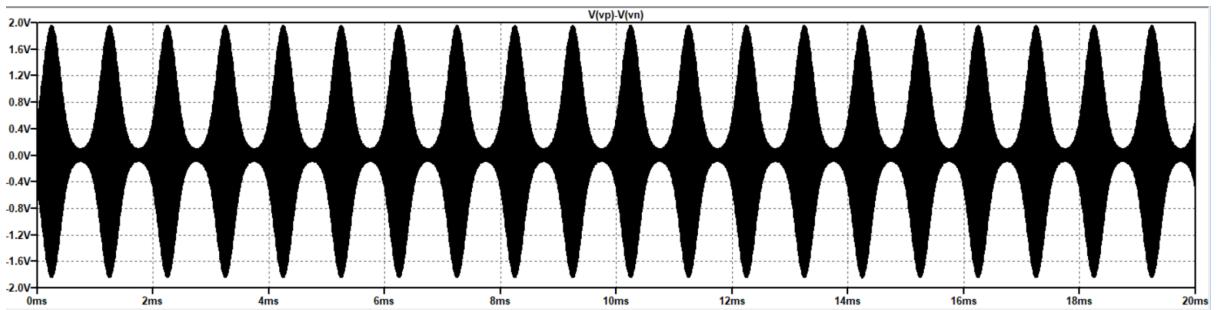


Figure 4.2: Output signal with 50mV Vpk input signal

- B) In this part, we have modulated the amplitude of the input signal within the range of 10mV_p to 100mV_p and documented the corresponding changes in the differential output signal. Examination of the graphs in the Appendix A reveals that distortion becomes perceptible when the input amplitude reaches a mV_p of 40mV, signifying the threshold beyond which further increase results in a distortion of the sinusoidal output. Thus, the least distorted envelope is seen to be around that value.
- C) This part of the project is exactly like part B but employs a square wave input instead of a sine wave. A similar trend as part B is observed and it is found that the greater the amplitude, the greater the distortion at the peak.

Discussion:

An AM modulator operates by combining a high-frequency carrier signal with a lower-frequency input signal, such as an audio waveform. This modulation process

involves applying the input signal to a component, often a transistor, which functions as a constant current source when properly biased. Concurrently, two transistors receive sine wave carrier signals(Q3 and Q3 in figure 4.1) at their bases, phased 180 degrees apart. The sinusoidal nature of these carrier signals induces variations in the output voltage. The varying current from the modulating signal then modulates the carrier signals, convoluting them to produce an output signal with amplitude variations reflective of the modulating input. The resulting AM signal carries the frequencies of both the carrier and input signals. When transmitted, a receiver can reconstruct the original input signal by filtering for the specific frequency associated with the modulation. Careful consideration of the input signal's amplitude is essential to prevent overmodulation and the introduction of distortions to the output signal.

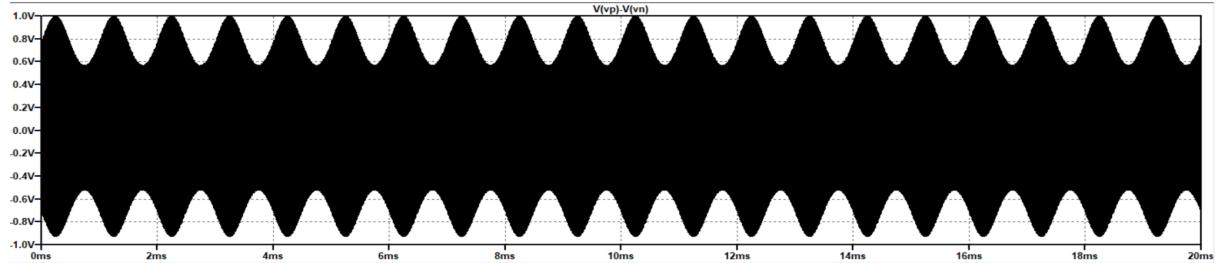
References:

- [1] Miniproject 3 handout
- [2] Miniproject 2 report
- [3] ELEC 301 course notes

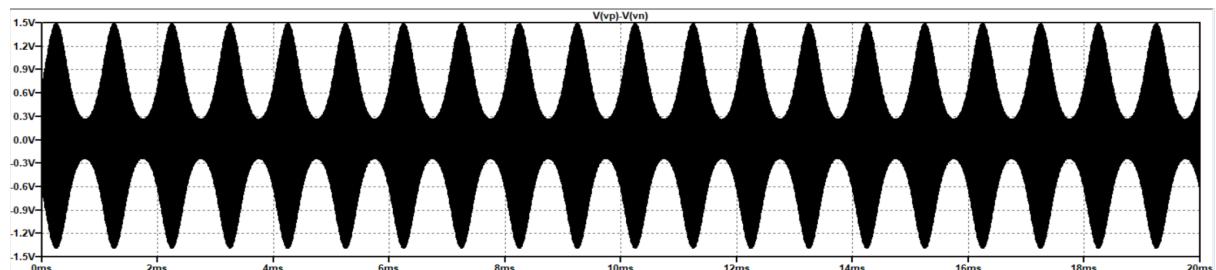
Appendix A

Part 4-B: Varying Sine Input

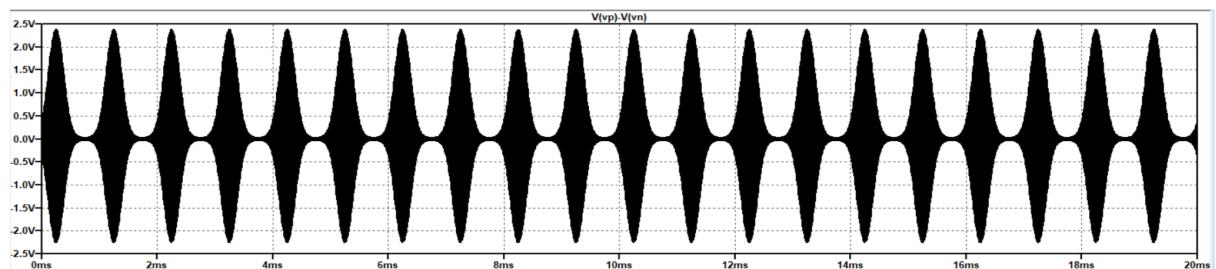
10 mVp



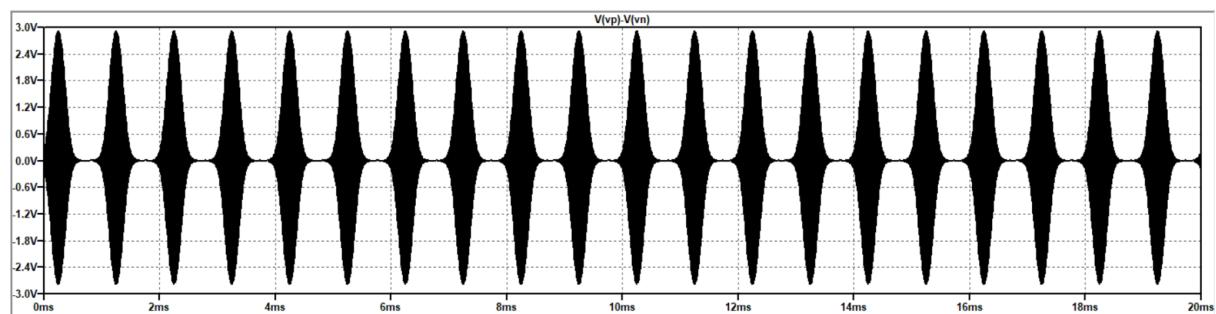
30 mVp



70 mVp



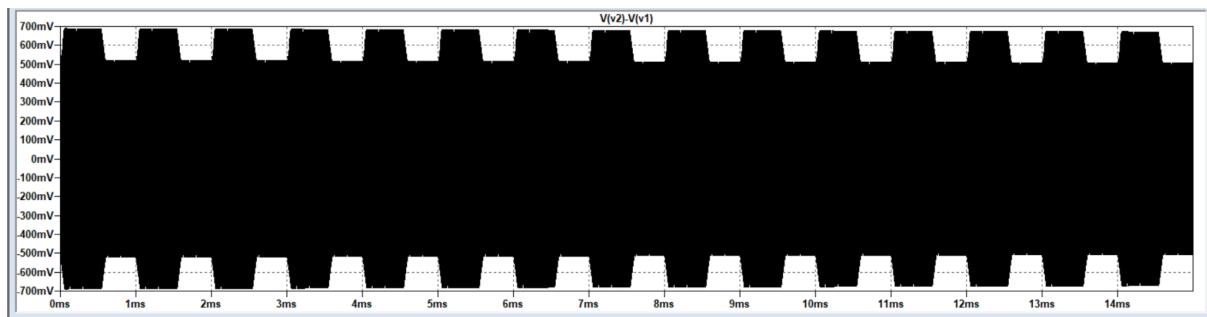
100 mVp



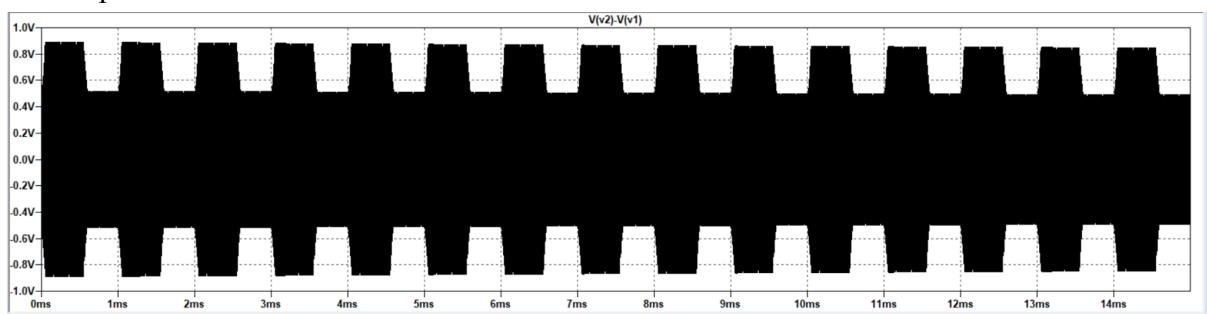
Appendix B

Part 4-C: Varying Square Wave Input

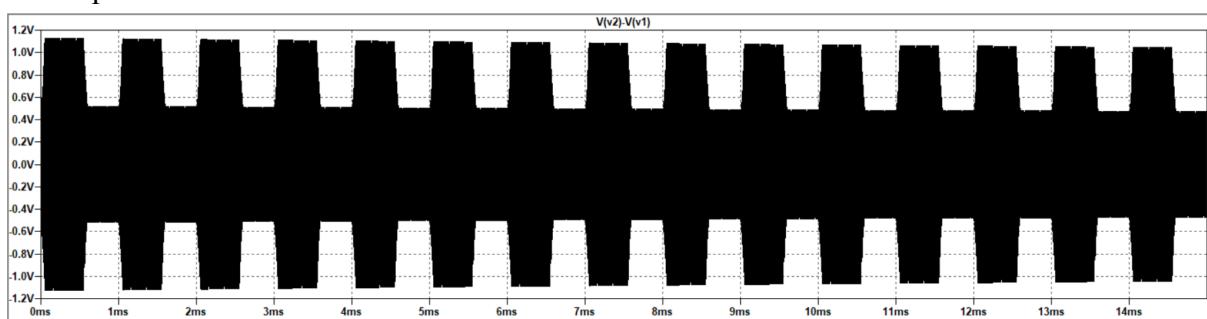
10 mVp



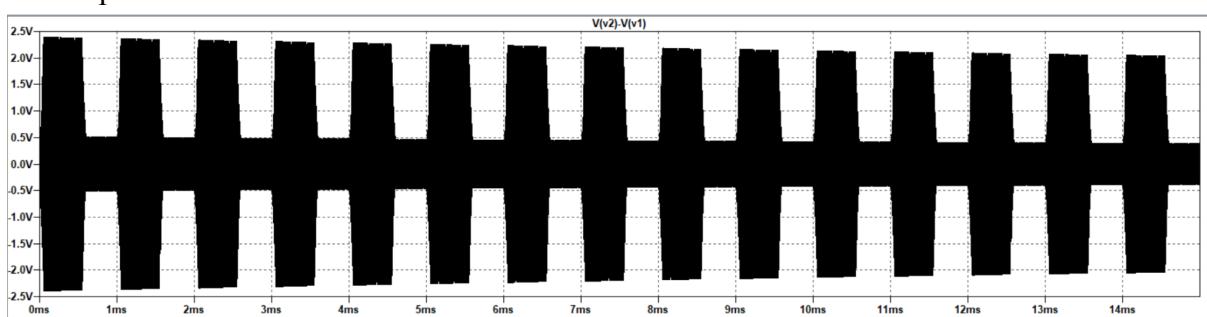
20 m Vp



30 m vp



70 m Vp



100 mVp

