ELEC 301 - Mini Project 1

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Question 1- Part 1

Midband Gain: In order to find the miband gain we open C2 and C3, short C1 and C4 and doing so we acquire the following circuit.

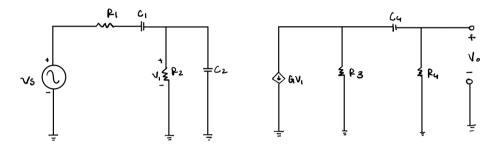


Figure 1.1: Midband gain circuit

Now, we can get the following equation from the above circuit and calculate the value for midband gain.

$$V_{o} = \frac{\left(-\frac{G_{1}}{G_{1}}\right)\left(V_{1}\right)\left(R_{3}P_{4}\right)}{R_{3} + P_{4}}$$

$$V_{5} = V_{1}\left(\frac{P_{1}}{P_{2}} + 1\right)$$

$$A_{m} = \frac{V_{0}}{V_{5}}$$

$$A_{m} = \frac{\left(-G_{1}\right)\left(R_{3}P_{4}\right)}{\left(P_{3} + P_{4}\right)\left(\frac{P_{1}}{P_{2}} + 1\right)}$$

$$A_{m} = -195\cdot12195122 \frac{V}{V}$$

Location of poles at low frequency: At low frequency, C2 and C3 are open circuit which gives rise to the following circuit.

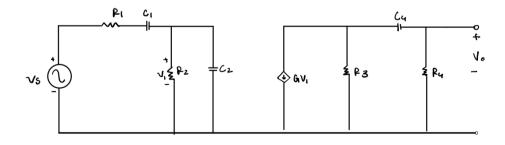


Figure 1.2: Transconductance Amplifier at low frequency

$$W_{LP1} = \frac{1}{(R_1 + R_2)C_1}$$

$$= 121.9512195 \text{ rad/5}$$

$$W_{LP2} = \frac{1}{(R_3 + R_4)C_4}$$

$$= 125 \text{ rad/5}$$

$$W_{L3dB} = \sqrt{\omega_{LP_1}^2 + \omega_{LP_2}^2}$$

$$= 174.63418892 \text{ rad/5}$$

Location of poles at high frequency: At high frequency C1 and C4 are short circuits

which gives rise to the circuit below.

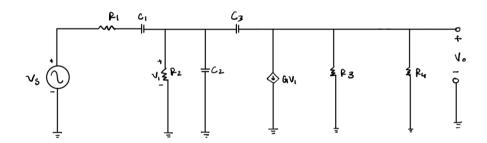


Figure 1.3: Transconductance amplifier at high frequency

From the above circuit in 1.4, we can find the miller gain k which gives rise to the circuit in figure 1.5.

$$k = \frac{V_o}{V_l} = (-G_l)(R_3 || R_4)$$

$$= -200$$

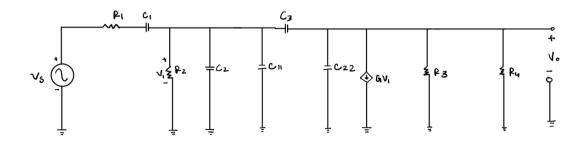


Figure 1.4: Transconductance Amplifier at High frequency

= 0.000000000402 F

$$C_{22} = C_3 \left(\frac{k}{1-k} \right)$$

= 2.01005025126 X 10⁻¹²

$$C_{22} = C_3 \left(\frac{k}{1-k} \right)$$

= 2.01005025126 X 10⁻¹²

$$T_2 = (C_{22}) (F_3 || F_4)$$

= 4.02010050251X10-95
= 248750000 mad/s

$$W_{H3dB} = \frac{1}{\left(2.0098 \times 10^{-8}\right)^2 + \left(4.0201 \times 10^{-9}\right)^2}$$

$$= 48790754.0884 \text{ mad/s}$$

Question 1 - Part 2

Here we simulate the original circuit and probe it around V_0 in order to plot the bode plot.

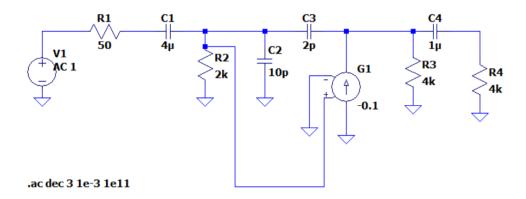
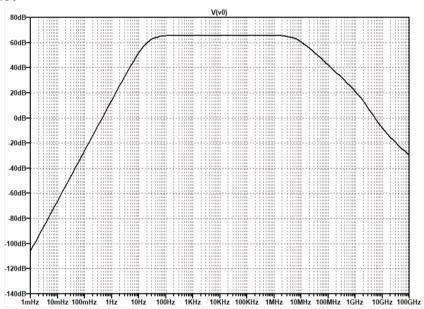
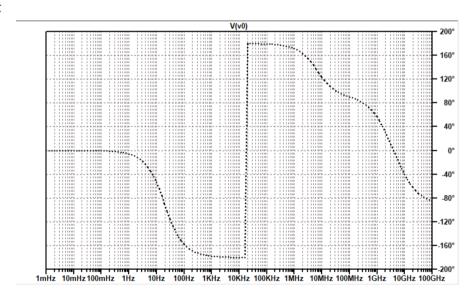


Figure 1.5: Simulated circuit for bode plot

Magnitude Plot



Phase plot



To determine the locations of our poles, we employ a variety of slopes, with their intersections indicating pole positions. Notably, this time, our plot reveals the presence of a

high-frequency zero. I sketched lines on the plot at the highest dB level, a slope of 40dB per decade, a slope of 20dB per decade, a slope of -40dB per decade, and two slopes of -20dB per decade. These lines were aligned on my bode plot, with the points of intersection indicating the positions of both poles and zeros.

Table 1.1: Comparing Graphically Simulated Pole-Zero Values to Calculated Poles

	$\mathbf{W}_{\mathrm{lp1}}$	$\mathbf{W}_{\mathrm{lp2}}$	$\mathbf{W}_{\mathtt{h1}}$	W _{h2}	W_{z1}
Calculated rad/s	121.9512	125	49.7573*10 ⁶	25.1250*10 ⁸	N/A
Simulated rad/s	123.9327	121.8812	45.8675*10 ⁶	12.7651*10 ⁶	5.2131*10 ¹⁰

We notice that low-frequency poles exhibit values that closely resemble each other. However, as we move to higher frequencies, we observe greater deviations among these values. Additionally, the high zero is no longer present when Miller's theorem is applied.

Table 1.2: Determining Percent Error between Graphically Simulated and Calculated 3 dB Values

	Calculated (rad/s)	Simulated (rad/s)	% error
\mathbf{W}_{L3dB}	174.6342	192.9120	9.4747%
$\mathbf{W}_{ ext{H3dB}}$	48790754.0884	41698188.3885	17.0093%

We use the following equation to carry out the above percentage calculations:

Discussion:

As it can be seen from the above table, we notice that the error is relatively low at the lower 3 dB point, but it significantly escalates at the higher 3 dB point. The same trend is seen in the simulated values of poles versus the calculated values of poles. Therefore, it is safe to assume that any calculated pole values in higher frequency would have a higher percentage error and would not produce the most accurate result.

Question 2

Question 2 - part 1

Magnitude Plot

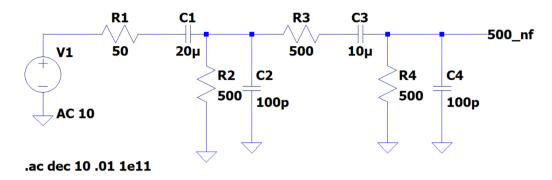
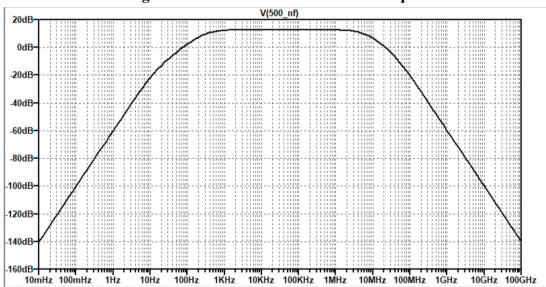
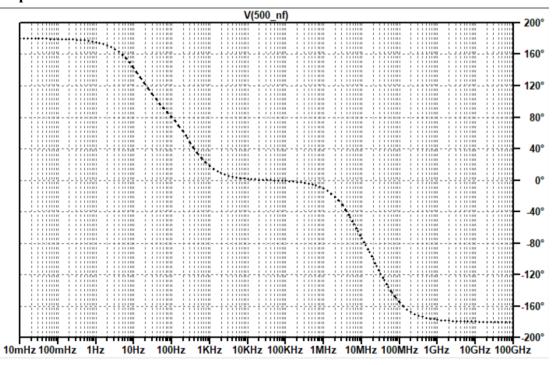


Figure: 2.1: Simulated circuit for bode plot



Phase plot



Location of poles

I visually determined the pole positions by sketching lines that traversed the highest dB value, as well as lines with slopes of -20 dB/dec, -40 dB/dec, 20 dB/dec, and 40 dB/dec, aligning them with the magnitude plot. The initial pole was identified at the point where the -40 dB/dec and -20 dB/dec slopes intersected. The second pole was pinpointed at the intersection of the -20 dB/dec slope and the line representing the maximum value. A similar process was employed on the right side of the plot to ascertain the locations of the third and fourth poles.

Table	2	1.	Location	of Poles
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Poles	Frequency (Hz)
$\mathbf{W_{lp1}}$	15.1135 Hz
$\mathbf{W_{lp2}}$	320.5673 Hz
$\mathbf{W}_{\mathrm{lp3}}$	5.10 MHz
$\mathbf{W_{lp4}}$	41.7225 MHz

From graphically, it is also determined that the f_{13dB} point is at 313.11365 Hz and the f_{h3dB} point is at 5.97729 MHz.

Question 2 - Part 2

We solve for W_{Lp1} by open circuit C_2 , C_3 and C_4 and calculating the resistance seen by C_1 .

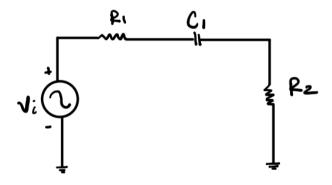


Figure 2.1: Circuit for finding W_{LP1}

$$W_{LP1} = \frac{1}{(P_1 + P_2) C_1}$$

$$= 90.9091 \text{ rod/s}$$

We solve for W_{lp2} by short circuit C_1 and open circuiting C_2 and C_4 and find the resistance seen by C_3 . Then we find the W_{L3dB} value using the formula in [1].

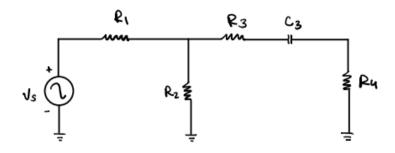


Figure 2.2: Circuit for finding W_{LP2}

$$W_{LP2} = \frac{1}{(C_3)(\frac{1}{R_1} + \frac{1}{R_2} + R_3 + R_4)}$$

$$= 1913.0435 \quad \text{rad/s}$$

$$W_{L3dB} = \sqrt{W_{LP_1}^2 + W_{LP_2}^2}$$

$$= 1915.2023 \quad \text{rad/s}$$

We follow the same process for the other capacitor values and acquire the following result:

Capacitor values	1 μF	2 μF	5 μF	10 μF
Calculated W _{Lp1} values	90.901 rad/s	90.901 rad/s	90.901 rad/s	90.901 rad/s
Calculated W _{Lp2} values	956.5218 rad/s	478.2609 rad/s	191.3043 rad/s	95.6522 rad/s
Simulated W _{Lp1} values	84.6513 rad/s	68.1657 rad/s	51.2523 rad/s	36.1471 rad/s
Simulated W _{Lp2} values	1102.4729 rad/s	607.9885 rad/s	607.8763 rad/s	227.8746 rad/s
W _{L3dB} Values	960.8321 rad/s	486.8243 rad/s	211.8061 rad/s	131.9614 rad/s

Table 2.2: Calculated and simulated poles for different values for C₃

We use the following equation to calculate error:

Capacitor Values	Calculated W _{L3dB} rad/s	Simulated W _{L3dB} rad/s	Error %
500 nF	1915.2023	1967.3232	2.6493
1uf	960.8321	1010.6146	4.9260
2 uf	486.8243	543.0436	10.3526
5 uf	211.8061	272.4714	22.2648
10 uf	131.9614	189.5995	30.39910

Table 2.3: Percentage error for calculated and simulated W_{L3dB} values for different C₃ values

Discussion:

From the above calculation and simulation of plots, we can see that the circuit is a bandpass filter and the percentage of error increases as the values values of C_3 increases.

Question 3

Question 3 - Part 1

In order to solve this problem, we first need to find the values of the resistor. We know that four of the resistors have a value of 750 Ω and two of the 1.5 k Ω values. We can achieve this by leveraging the provided mid-band gain of 0.125. Given that there are three nodes in the circuit, we can conclude that each node or voltage ratio will exhibit a gain of $(0.125)^{\frac{1}{13}} = 0.5$. Therefore we can split the midband gain as the following:

$$A_{m} = \frac{V_{o}}{V_{2}} \times \frac{V_{2}}{V_{i}} \times \frac{V_{i}}{V_{s}}$$

Since each voltage ratio have a gain of 0.5 and we are working in the midband all the high-frequency capacitors would have to be open circuit and all the low-frequency capacitors would have to be short circuits. Since this problem only has high-frequency capacitors, opening them would give rise to the following circuit:

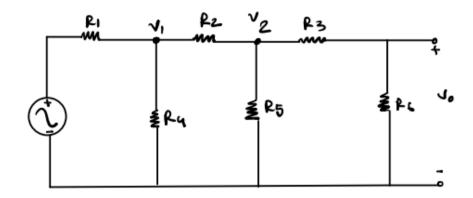


Figure 3.1: Midband Gain Circuit

$$\frac{V_0}{V_2} = \frac{P_0}{P_3 + P_0} = \frac{1}{2} \implies P_3 = P_0$$

$$\frac{V_{2}}{V_{1}} = \frac{P_{5} || (P_{3} + P_{6})}{P_{2} + P_{5} || (P_{3} + P_{6})} = \frac{1}{2} , \implies P_{2} = \frac{2P_{5}P_{6}}{P_{5} + 2P_{6}}$$

$$\frac{V_{1}}{V_{5}} = \frac{P_{4} \| \left(P_{2} + P_{5} \| P_{3} + P_{6} \right) \right)}{P_{1} + P_{4} \| \left(P_{2} + P_{5} \| P_{3} + P_{6} \right) \right)} = \frac{1}{2} \implies P_{1} = \frac{2P_{2} R_{4}}{2P_{2} + P_{4}}$$

With our resistor values identified, we can proceed to ascertain the capacitor values using the OC and SC time constant method. Given the hierarchy of capacitor values, where $C_1 > C_2 > C_3$, we apply short-circuiting to capacitors with higher values than the one for which we are determining the OC time constant. Conversely, for capacitors with lower values (OC time constant, as these pertain to high-frequency capacitors), we open circuit them.

For finding C_1 , we open circuit C_2 and C_{3a} and find the equivalent resistance seen by C_1 .

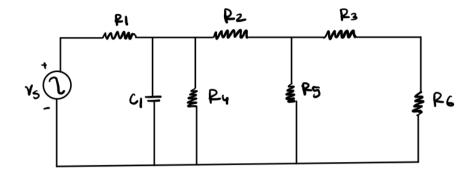


Figure 3.2: Circuit for finding C₁

$$\omega_{P1} = \frac{1}{(C_1)(Req)} = \frac{1}{(C_1)(R_1 || (R_2 + R_5 || (R_3 + R_4)))}$$

$$C_1 = \frac{1}{(\omega_{P1})(Req)}$$

$$= 26.6667 nf$$

For finding C_2 , we short circuit C_1 and open circuit C_3 and find equivalent resistance seen by C_2 .

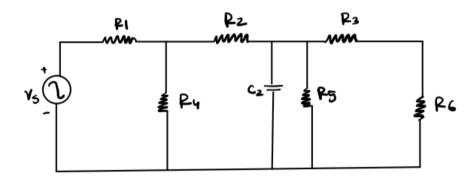


Figure 3.3: Circuit for finding C₂

$$W_{P2} = \frac{1}{(C_2)(R_{eq})} = \frac{1}{(C_2)(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_{eq})(R_{eq})(R_{eq})(R_{eq})(R_{eq})(R_{eq})(R_{eq})(R_{eq})} = \frac{1}{(C_2)(R_{eq})(R_$$

For C_3 , we short circuit C_1 and C_2 and find equivalent resistance seen by C_2 .

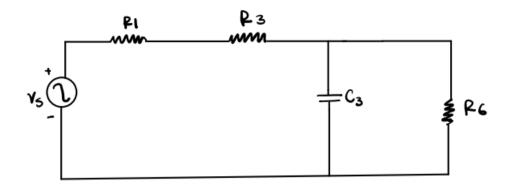


Figure 3.4: Circuit for finding C₃

$$W_{P3} = \frac{1}{(C_3)(Peq)} = \frac{1}{(C_3)(Peq)}$$

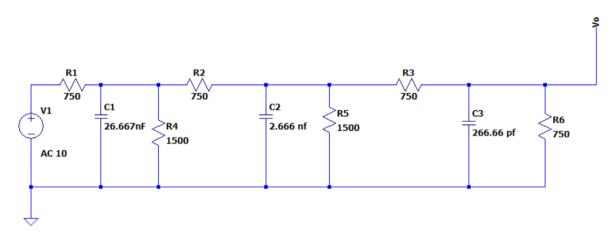
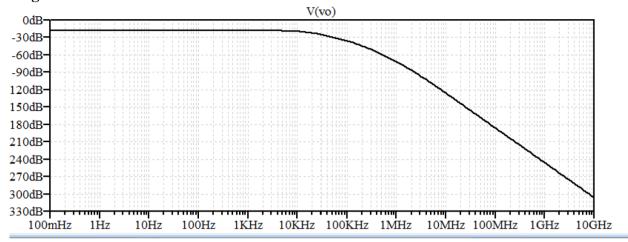
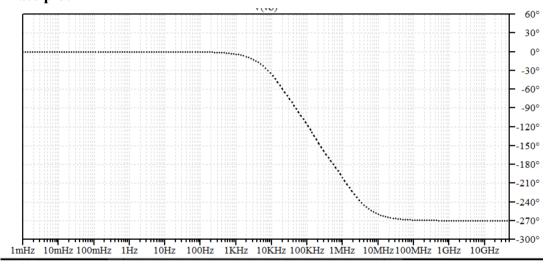


Figure 3.5: Simulated Circuit for plots

Magnitude Plot



Phase plot



Question 3 - Part 2

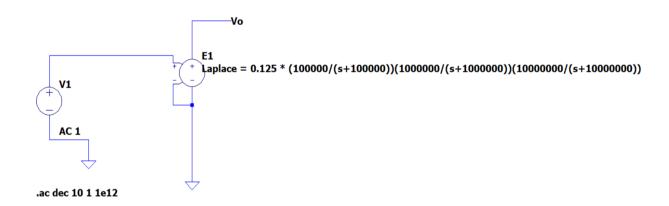
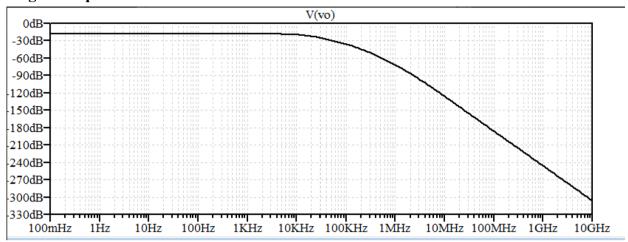
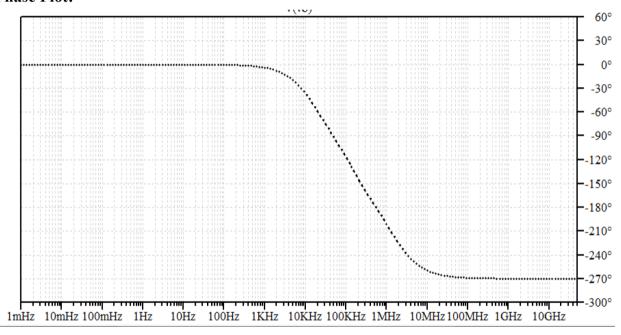


Figure 3.6: Simulated Laplace circuit

Magnitude plot



Phase Plot:



Discussion:

Upon analyzing the Bode plots of the circuit in both part 1 and part 2, it becomes evident that the magnitude and phase plots exhibit an exceptionally close resemblance. This serves as compelling evidence that the transfer function serves as an exceptionally accurate mathematical approximation and model for the system.

References

- [1] ELEC 301 Course Notes.
- [2] A. Sedra and K. Smith, "Microelectronic Circuits," 5th (or higher) Ed., Oxford University Press, New York.
- [3] LTSPICe™ User's Manual