Archi

Opcodes

Opcode	Opcode(binary)	Instruction Id	Instruction Type	Instruction
0	0000	L	Memory	lw
1	0001	A	Arithmetic	add
2	0010	B	Arithmetic	addi
3	0011	K	Logic	nor
4	0100	O	Control	bneq
5	0101	D	Arithmetic	subi
6	0110	C	Arithmetic	sub
7	0111	H	Logic	ori
8	1000	N	Control	beq
9	1001	I	Logic	sll
10	1010	J	Logic	srl
11	1011	E	Logic	and
12	1100	P	Control	jump
13	1101	F	Logic	andi
14	1110	G	Logic	or
15	1111	M	Memory	sw

Instructions

Type	`Field_1` bit(12-15)	`Field_2` bit(8-11)	`Field_3` bit(4-7)	`Field_4` bit(0-3)	operations
R	Opcode	Src Reg 1	Src Reg 2	Dst reg	add, nor, sub, and, or
S	Opcode	Src Reg 1	Dst Reg	Shamt	sll, srl
I	Opcode	Src Reg 1	Dst Reg	Immdt.	addi, subi, ori, andi

Type	`Field_1` bit(12-15)	`Field_2` bit(8-11)	`Field_3` bit(4-7)	`Field_4` bit(0-3)	operations
I	Opcode	Src Reg 1	Src Reg 2	Addr.	bneq, beq
I	Opcode	Src Reg 1	Dst Reg	Immdt	lw
I	Opcode	Src Reg 1	Src Reg 2	Immdt	sw
J	Opcode	Jump Address	Jump Address	0	jump

Mappings

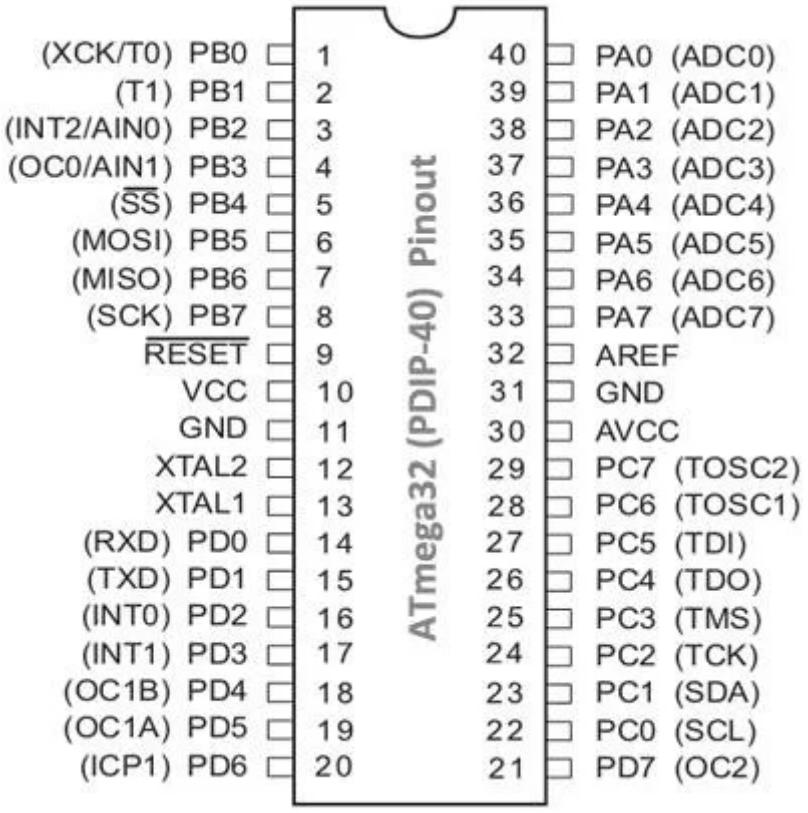
Control Bit	0	1	Opcode for 0	Opcode for 1
RegDst	`Field_4` as Register for write	`Field_3` as Register for write	R type	
Jump	Instruction is not Jump	Instruction is jump		jump
Branch	Instruction is not branch	Instruction is branch		beq
Branch not equal	Instruction is not bneq	Instruction is bneq		bneq
Mem Read	Data not read from memory	Data read from memory		lw
Mem to reg	Data for writing to memory comes from ALU	Data for writing to memory comes from memory		lw
Mem Write	Data not written to memory	Data Written to memory		sw
Alu Src	ALU input 2 comes from register output	ALU input 2 comes from sign extension of immdt(`Field_4`)	R type	
Reg Write	Register writing enabled	Register Writing Disabled	bneq, beq, jump, sw	

ALU operands mapping

ALU operation	control	control(binary)	operations
add	0	000	lw, add, addi, jmp, sw
sub	1	001	bneq, subi, sub, beq
and	2	010	and, andi
or	3	011	ori, or
nor	4	100	nor
sll	5	101	sll
srl	6	110	srl

EPROM codes

Atmega diagram



PC rom ATMEGA

PIN	NO	ROLE	Maps To	Bit no	Comment
PB	0-3	Input	PC	7-4	
PD	3-6	Input	PC	3-0	

PIN	NO	ROLE	Maps To	Bit no	Comment
PA	0-7	Output	MC	15-8	
PC	7-0	Output	MC	7-0	
PD	2	Interupt	Clock Pulse		

Register File AtMega

PIN	NO	ROLE	Maps To	Bit no	Comment
PB	0-3	Input	src reg 1	0-3	
PB	4-7	Input	src reg 2	0-3	
PD	3-6	Input	dest reg 1	0-3	
PC	3-0	Input	data	3-0	
PD	2	Input	Clock Pulse		
PD	0	Input	regWrite		
PA	0-3	Output	register value 1	0-3	
PA	4-7	Output	register value 2	0-3	

ALU

PIN	NO	ROLE	Maps To	Bit no	Comment
PB	0-3	Input	operand 1	0-3	
PD	3-6	Input	operand 2	0-3	
PA	0-2	Input	control	0-3	
PA	3	Output	zero flag		
PA	4-7	Output	Result	0-3	

Memory

PIN	NO	ROLE	Maps To	Bit no	Comment
PB	0-3	Input	Address	0-3	
PD	3-6	Input	write data	0-3	
PD	0	Input	MemWrite		

PIN	NO	ROLE	Maps To	Bit no	Comment
PD	1	Input	MemRead		
PD	2	Input	Clock pulse		
PA	0-3	Output	Read Data	0-3	

Control

PIN	NO	ROLE	Maps To	Bit no	Comment
PD	3-6	Input	opcode	0-3	
PA	0-7	Output	Flag		
PC	7-4	Output	Flag		