

Exp no: 1

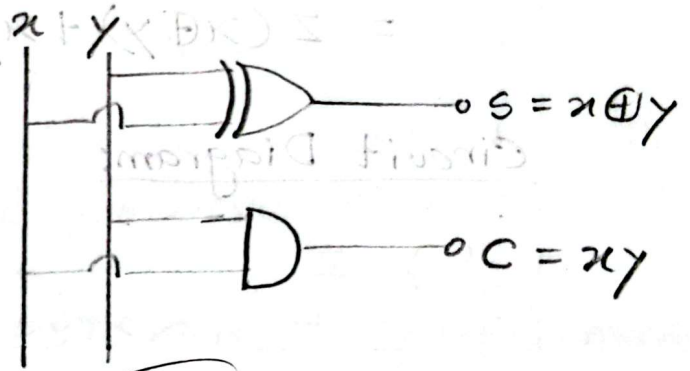
Exp name: Implementing Full-Adder by using Half-Adder and basic logic gates.

Half-Adder: (Truth Table)

x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$s = xy' + x'y = x \oplus y$$

$$c = xy$$



Circuit diagram

Full-Adder: (Truth Table)

x	y	z	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$s = x'y'z + x'yz' + xy'z' + xyz$$

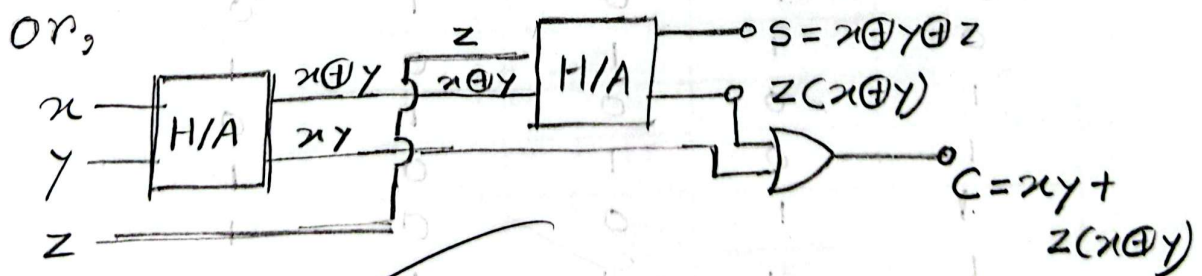
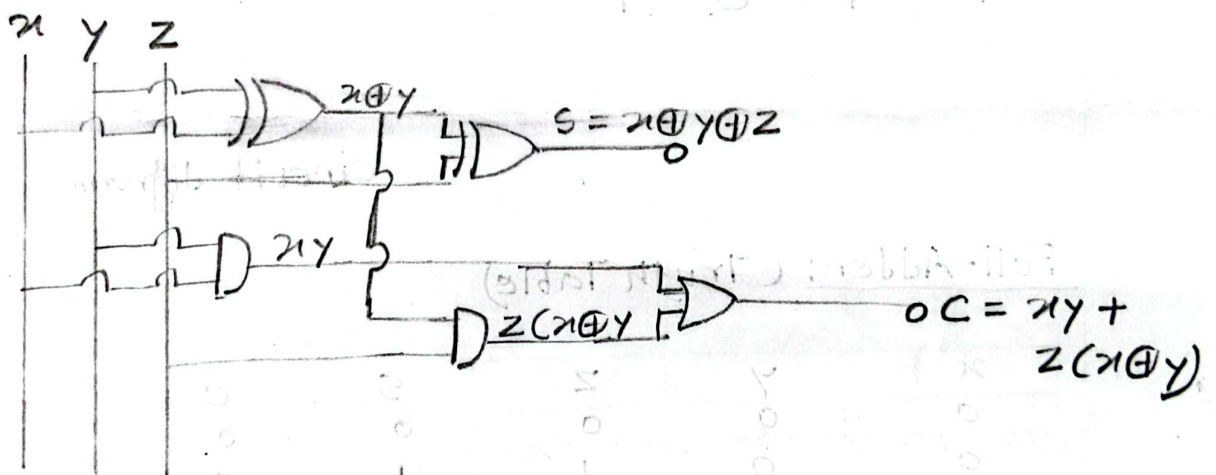
$$c = x'yz + xy'z + x\bar{y}z' + xyz$$

## Implementation of Full-Adder by using Half-Adder

$$\begin{aligned}
 S &= x'y'z + x'yz' + xy'z' + xyz \\
 &= z'(x'y + xy') + z(xy + x'y) \\
 &= z'(x \oplus y) + z(x \oplus y)' \\
 &= x \oplus y \oplus z
 \end{aligned}$$

$$\begin{aligned}
 C &= x'yz + xy'z + xyz' + xyz \\
 &= z(x'y + xy') + xy(z + z') \\
 &= z(x \oplus y) + xy
 \end{aligned}$$

Circuit Diagram:



Rolls: 089

115

116

118

306

250

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20/10/2024

Experiment Name: Implementation of half adder circuit using 2 to 4 line decoder with enable input.

Half adder: (Truth Table)

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = \bar{x}\bar{y} + xy \quad (1, 2) \rightarrow \text{min term}$$

$$C = xy \quad (3) \rightarrow \text{min term.}$$

2 to 4 line decoder:

E	$I_1 I_0$	$Y_3$	$Y_2$	$Y_1$	$Y_0$
0	xx	0	0	0	0
1	00	0	0	0	1
1	01	0	0	1	0
1	10	0	1	0	0
1	11	1	0	0	0

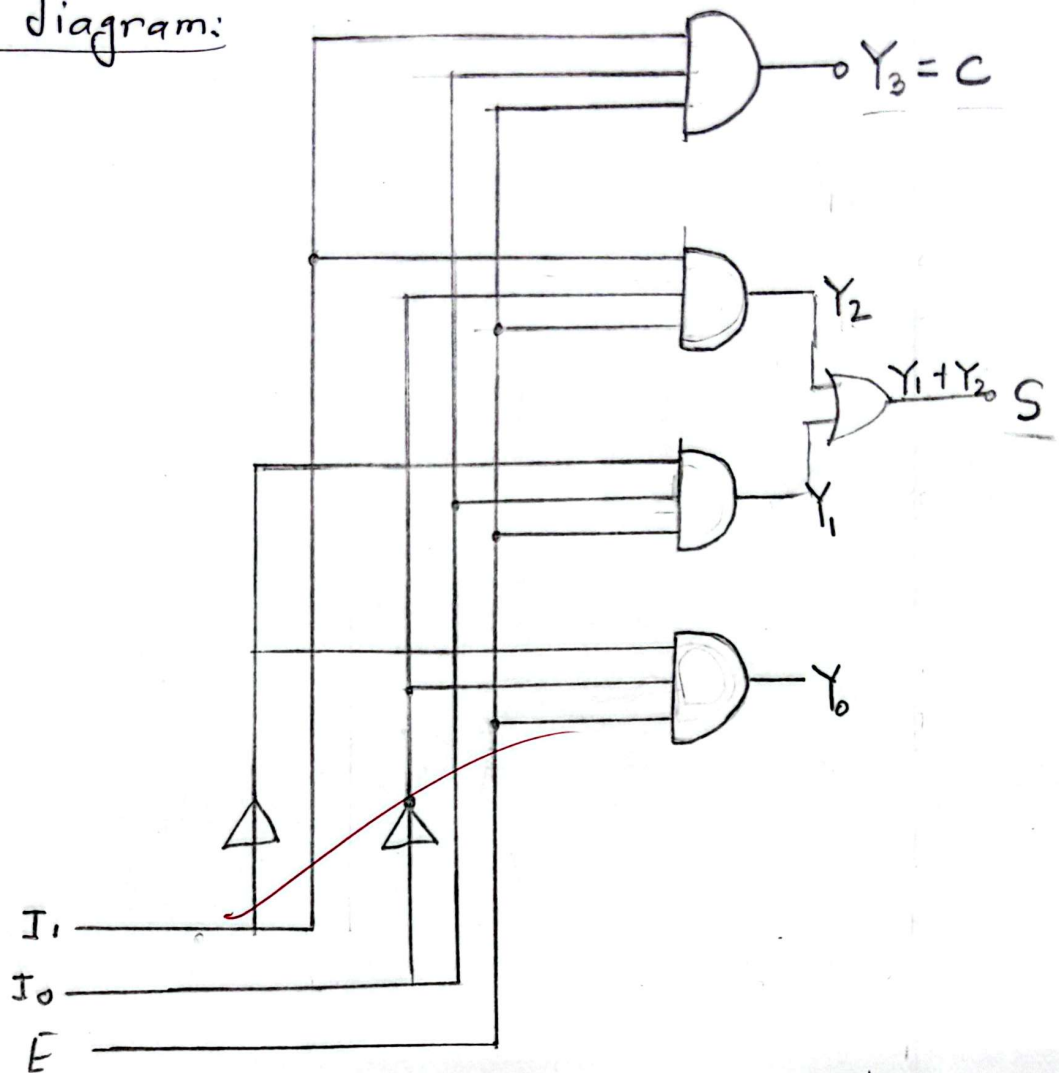
$$\left. \begin{aligned} Y_0 &= I_1 I_0 \\ Y_1 &= \bar{I}_1 I_0 \\ Y_2 &= I_1 \bar{I}_0 \\ Y_3 &= I_1 I_0 \end{aligned} \right\} \begin{array}{l} E \text{ is} \\ \text{always} \\ 1 \end{array}$$

$$\therefore S = Y_1 + Y_2$$

$$C = Y_3$$



Circuit diagram:



~~ID: 306, 118, 250, 089~~

*Amr*  
21/11/2024

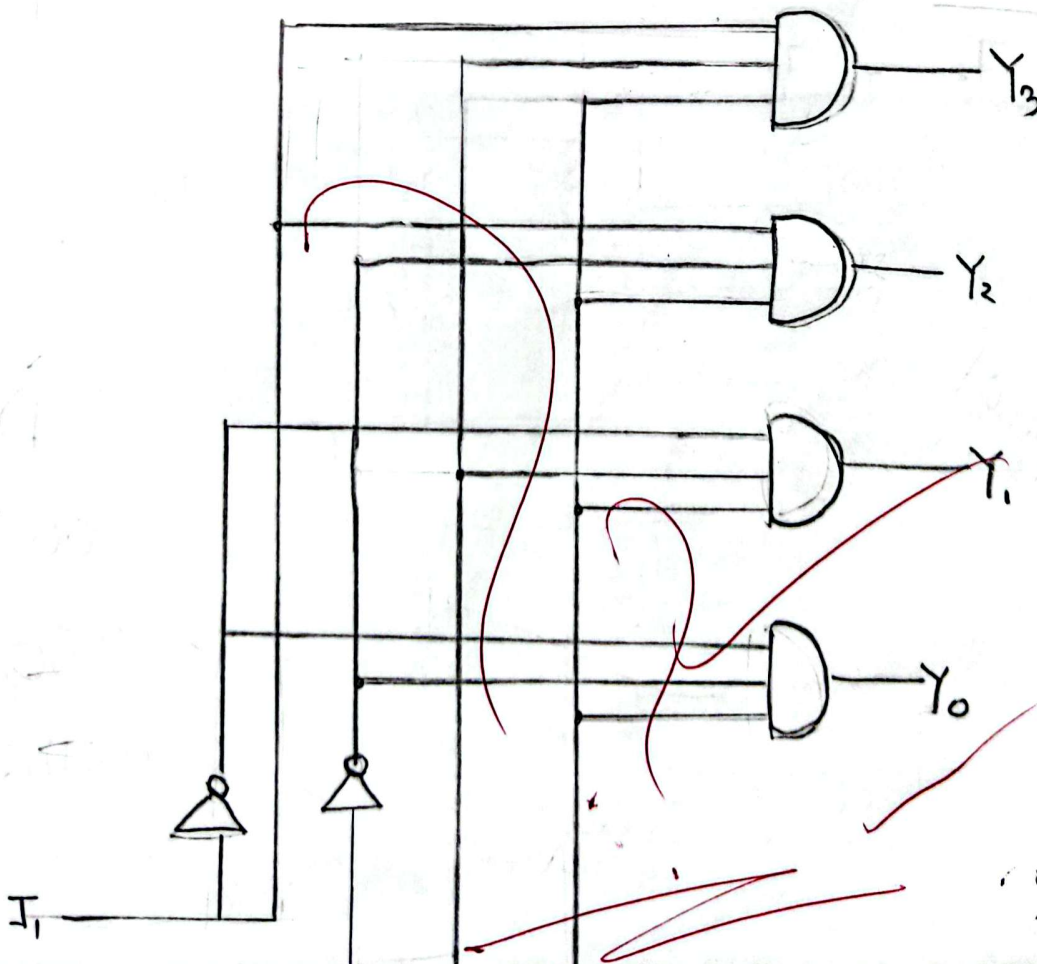
## Experiment No:4

Experiment name: Design a 3 to 8 line decoder by using 2 to 4 line decoder.

$E$	$I, I_0$	$\gamma_3$	$\gamma_2$	$\gamma_1$	$\gamma_0$
0	x x	0	0	0	0
1	0 0	0	0	0	1
1	0 1	0	0	1	0
1	1 0	0	1	0	0
1	1 1	1	0	0	0

→ 2 to 4 line decoder

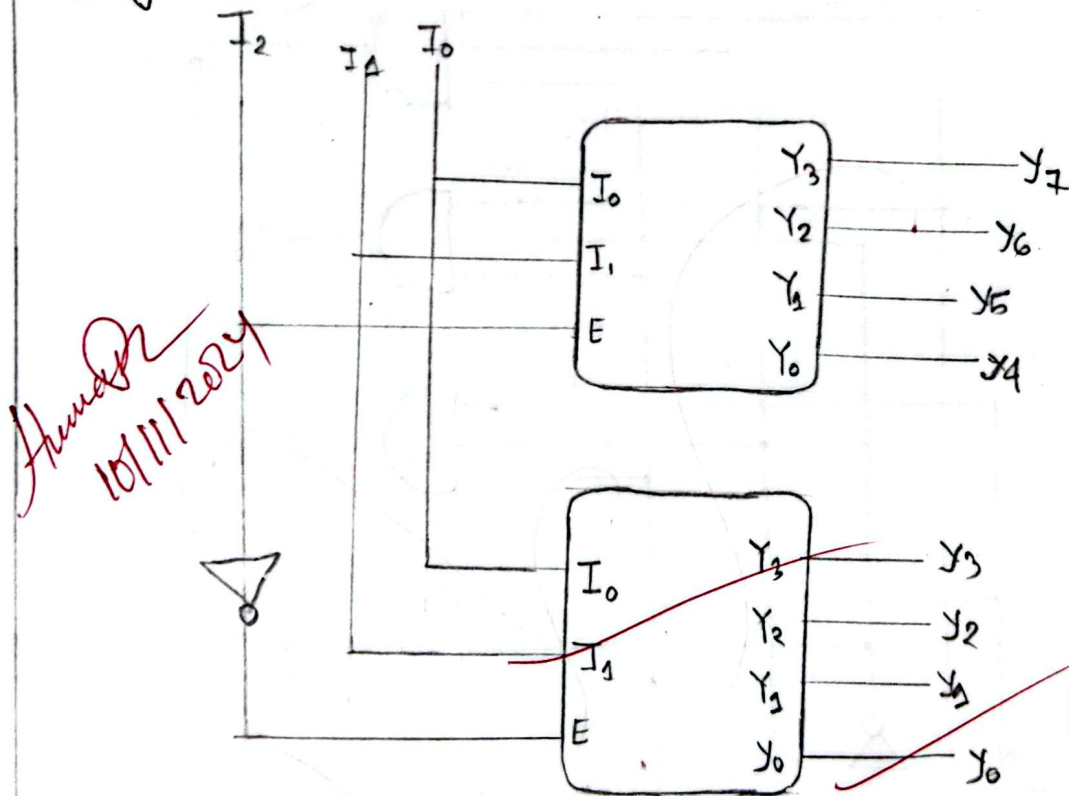
Circuit Diagram:



## 3 to 8 line decoder

$I_2, I_1, I_0$	$Y_7$	$Y_6$	$Y_5$	$Y_4$	$Y_3$	$Y_2$	$Y_1$	$Y_0$
000	0	0	0	0	0	0	0	1
001	0	0	0	0	0	0	1	0
010	0	0	0	0	0	1	0	0
011	0	0	0	0	1	0	0	0
100	0	0	0	1	0	0	0	0
101	0	0	1	0	0	0	0	0
110	0	1	0	0	0	0	0	0
111	1	0	0	0	0	0	0	0

## Diagram



ID

306, 118,

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115, 116,



Exp no: 2

Experiment name: Design a combinational circuit which will convert BCD code to Excess 3 code.

BCD to Excess-3 →

Input				output			
a	b	c	d	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

$c$

$a$

$b$

$d$

0	1	3	2
4	5	7	6
X	X	X	X
12	13	15	14
8	9	11	10

$$w = a + bc + bd$$

0	1	3	2
4	5	7	6
X	X	X	X
12	13	15	14
8	9	11	10

$$y = c'd' + cd$$



					c
	1	1	1		
0	1	3	2		
1					
4	5	7	6		b
X	X	X	X		
12	13	15	14		
	1	X	X		
8	9	11	10		
					d
a					

$$x = b'C + b'D + bc'd'$$

					c
1		1	1		
0	1	3	2		
1			1		
4	5	7	6		b
X	X	X	X		
12	13	15	14		
1		X	X		
8	9	11	10		
					d
a					

$$z = d'$$

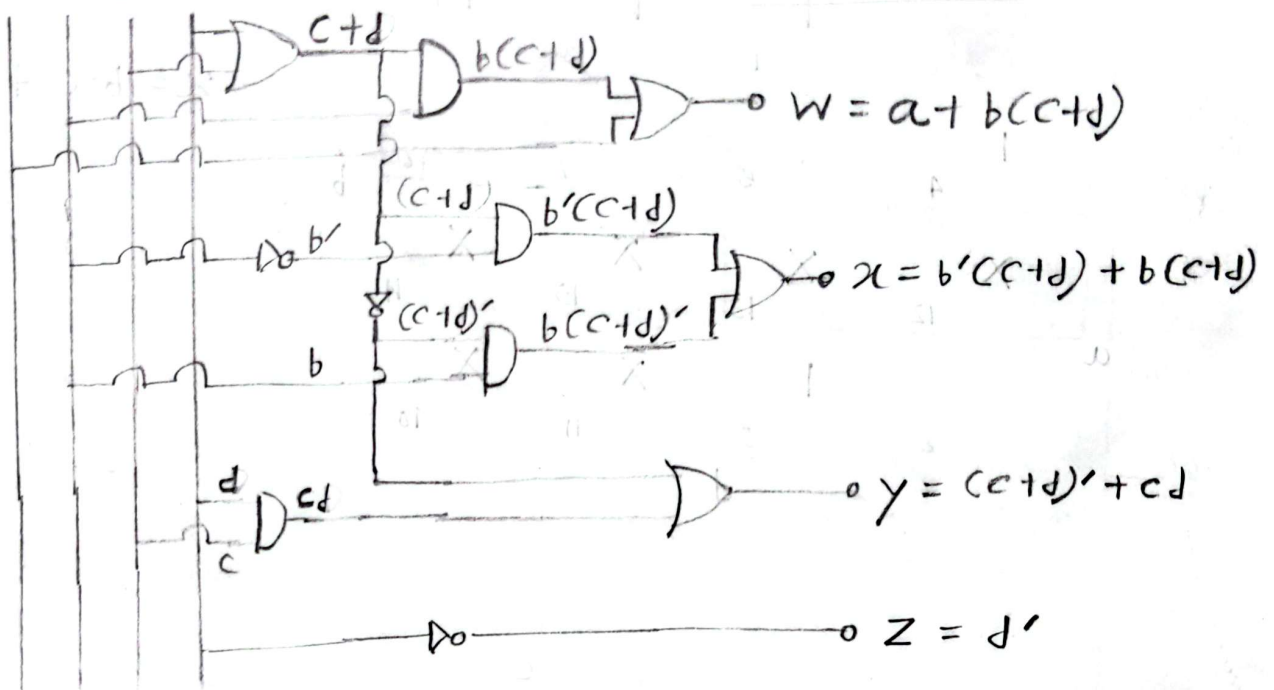
$$\therefore w = A + a + b(c + d)$$

$$x = b'(c + d) + b(c + d)'$$

$$y = (c + d)' + cd$$

$$z = d'$$

a b c d



ID: 118, 89, 250, 306,  
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Humay  
27/10/2024